AURIX™ TC39x variants

About this document

Scope and purpose

This document is an addendum to the TC39x Product Data Sheet and User's Manual, listing all planned product variants, key parameters such as memory size and optional features.

The User's Manual lists functions implemented on the Silicon, but this document counts functions that are pinning dependent; i.e. functions are counted that are connected to at least one package pin. As pins are overlaid with several functions the pinning needs to be checked (see Product Data Sheet) to determine the number of usable functions in an application.

Naming conventions

Prefix:

- SAK: $T_{ambient}$ Temperature Range from -40 °C up to +125 °C.
- SAL: $T_{ambient}$ Temperature Range from -40 °C up to +150 °C (packaged device).

Feature package:

- P: Standard feature.
- E: Emulation device with all features of the emulated standard type, additionally full MCDS, overlay functionality for calibration, AGBT as trace interface for development (depending on the package). Refer to the Emulation devices Data Sheet for further details.
- C,V,Z: Customer Specific.
- A: ADAS ext. Memory.
- T: ADAS + emulation.
- X: Extended Feature device. These products contain the extended memory (EMEM) of the ADAS subsystem. The ADAS peripherals SPU and RIF are not available.
- M: MotionWise software.
- F: Extended Flash.
- G: Additional Connectivity.
- H: ADAS Standard feature.
- N: Standard feature with AMU.

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1 TC39x BD step variants

1.1 TC39x BD step (part 1)

A table listing the TC39x BD step variants.

Table 1 TC39x_BD step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
Step						
BD	BD	BD	BD	BD	BD	BD
Production Status						
Standard	Standard	Standard	Standard	Standard	Standard	Standard
Package Type						
PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-292
Pinout						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	ADAS
Reference Silicon						
TC39x	TC39x	TC39x	TC39x	TC39x	TC39x	TC39x
Temperature Range (Ambient)						
SAL	SAL	SAL	SAK	SAK	SAK	SAK
Chip ID ***Attention*: *The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***						
0xAF019993	0x8F019993	0x8F019793	0x8F019993	0xAF019993	0x8F019793	0xBF019793
Cores / Checker Cores						
6/4	6/4	6/4	6/4	6/4	6/4	6/4
Max. Freq. (MHz)						
300	300	300	300	300	300	300
Program Flash (MB)						
16	16	16	16	16	16	16
Data Flash0 (single-ended) (KB)						
1024	1024	1024	1024	1024	1024	1024
Total SRAM (without EMEM and Cache) (KB)						
2528	2528	2528	2528	2528	2528	2528
EMEM Size (KB)						
4096	0	0	0	4096	0	4096
DSPR (KB)						

(table continues...)

1 TC39x BD step variants

Table 1 (continued) TC39x_BD step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
DLMU (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
PSPR (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)						
768	768	768	768	768	768	768
DAM (KB)						
128	128	128	128	128	128	128
AMU[1)]						
No	No	No	No	No	No	No
ADC (Primary Groups/Channels)						
8/64	8/64	5/40	8/64	8/64	5/40	4/26
ADC (Secondary Groups/Channels)						
4/60	4/60	4/60	4/60	4/60	4/60	4/42
ADC (Fast Compare Channels)						
8	8	8	8	8	8	8
ADC (EDSADC Channels)						
14	14	6	14	14	6	6
CAN (Modules/Nodes)						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules						
2	2	2	2	2	2	2
ASCLIN Modules / with ASC & LIN / with 3-wire SPI						
12/12/12	12/12/12	12/12/11	12/12/12	12/12/12	12/12/11	12/12/9
QSPI Modules / with LVDS						
6/2	6/2	6/2	6/2	6/2	6/2	6/1

(table continues...)

1 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

1 TC39x BD step variants

Table 1 (continued) TC39x_BD step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
SENT Channels						
25	25	20	25	25	20	17
MSC Modules						
4	4	2	4	4	2	1
PSI5 Channels						
4	4	4	4	4	4	4
PSI5-S Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDMMC Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
Max. Ethernet Availability: 1GBit/100Mbit/No						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability[2)]						
MCDS	MCDS	MCDS	MCDS	MCDS	MCDS	MCDS
ADAS Cluster Available						
No	No	No	No	No	No	Yes
CIF						
No	No	No	No	No	No	No
HSM Available						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

2 Refer to the ***MCDS availability*** section of this document for additional details.

1.2 TC39x BD step (part 2)

A continuation table listing the TC39x BD step variants.

Table 2 TC39x_BD step (part 2)

SAK-TC397QA-160 F300S	SAK-TC397XX-256 F300S	SAK-TC397QP-192 F300S	SAK-TC397QP-256 F300S	SAK-TC397XZ-256 F300S	SAK-TC397XM-256 F300S	SAL-TC397QP-192 F300S
Step						
BD	BD	BD	BD	BD	BD	BD
Production Status						
Standard	Standard	Customer Specific	Customer Specific	Customer Specific	Standard	Customer Specific
Package Type						
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout						
ADAS	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
Reference Silicon						
TC39x	TC39x	TC39x	TC39x	TC39x	TC39x	TC39x
Temperature Range (Ambient)						
SAK	SAK	SAK	SAK	SAK	SAK	SAL
Chip ID						
Attention: The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.						
0xCC019793	0xAF019793	0xCD019793	0xCF019793	0xFF019793	0x8F019793	0xCD019793
Cores / Checker Cores						
4/3	6/4	4/4	4/4	6/4	6/4	4/4
Max. Freq. (MHz)						
300	300	300	300	300	300	300
Program Flash (MB)						
10	16	12	16	16	16	12
Data Flash0 (single-ended) (KB)						
1024	1024	1024	1024	1024	1024	1024
Total SRAM (without EMEM and Cache) (KB)						
1696	2528	1184	2080	1632	2528	1184
EMEM Size (KB)						
4096	4096	0	0	0	0	0
DSPR (KB)						

(table continues...)

1 TC39x BD step variants

Table 2 (continued) TC39x_BD step (part 2)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S	SAK-TC397XM-256F300S	SAL-TC397QP-192F300S
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
DLMU (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
PSPR (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)						
512	768	0	768	0	768	0
DAM (KB)						
0	128	0	128	0	128	0
AMU[3)]						
No	No	No	No	No	No	No
ADC (Primary Groups/Channels)						
4/26	5/40	5/40	5/40	5/40	5/40	5/40
ADC (Secondary Groups/Channels)						
4/42	4/60	4/60	4/60	4/60	4/60	4/60
ADC (Fast Compare Channels)						
8	8	8	8	8	8	8
ADC (EDSADC Channels)						
6	6	6	6	6	6	6
CAN (Modules/Nodes)						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules						
2	2	2	2	2	2	2
ASCLIN Modules / with ASC & LIN / with 3-wire SPI						
12/12/9	12/12/11	12/12/11	12/12/11	12/12/11	12/12/11	12/12/11
QSPI Modules / with LVDS						
6/1	6/2	6/2	6/2	6/2	6/2	6/2

(table continues...)

3 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

1 TC39x BD step variants

Table 2 (continued) TC39x_BD step (part 2)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S	SAK-TC397XM-256F300S	SAL-TC397QP-192F300S
SENT Channels						
17	20	20	20	20	20	20
MSC Modules						
1	2	2	2	2	2	2
PSI5 Channels						
4	4	4	4	4	4	4
PSI5-S Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDMMC Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
Max. Ethernet Availability: 1GBit/100Mbit/No						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability[4)]						
MCDS	MCDS	MCDS	MCDS	MCDS	MCDS	MCDS
ADAS Cluster Available						
Yes	No	No	No	No	No	No
CIF						
No	No	No	No	No	No	No
HSM Available						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

4 Refer to the ***MCDS availability*** section of this document for additional details.

1.3 TC39x BD step (part 3)

A continuation table listing the TC39x BD step variants.

Table 3 TC39x BD step (part 3)

SAL-TC397QP-256F300S	SAL-TC397XZ-256F300S	SAL-TC397XX-256F300S	SAK-TC399QP-192F300S
Step			
BD	BD	BD	BD
Production Status			
Customer Specific	Customer Specific	Standard	Customer Specific
Package Type			
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-516
Pinout			
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
Reference Silicon			
TC39x	TC39x	TC39x	TC39x
Temperature Range (Ambient)			
SAL	SAL	SAL	SAK
Chip ID ***Attention**: **The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***			
0xCF019793	0xFF019793	0xAF019793	0xCD019993
Cores / Checker Cores			
4/4	6/4	6/4	4/4
Max. Freq. (MHz)			
300	300	300	300
Program Flash (MB)			
16	16	16	12
Data Flash0 (single-ended) (KB)			
1024	1024	1024	1024
Total SRAM (without EMEM and Cache) (KB)			
2080	1632	2528	2080
EMEM Size (KB)			
0	0	4096	0
DSPR (KB)			
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
DLMU (KB)			
64 per CPU	64 per CPU	64 per CPU	64 per CPU

(table continues...)

1 TC39x BD step variants

Table 3 (continued) TC39x BD step (part 3)

SAL-TC397QP-256F300S	SAL-TC397XZ-256F300S	SAL-TC397XX-256F300S	SAK-TC399QP-192F300S
PSPR (KB)			
64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)			
768	0	768	768
DAM (KB)			
128	0	128	128
AMU[5)]			
No	No	No	No
ADC (Primary Groups/Channels)			
5/40	5/40	5/40	8/64
ADC (Secondary Groups/Channels)			
4/60	4/60	4/60	4/60
ADC (Fast Compare Channels)			
8	8	8	8
ADC (EDSADC Channels)			
6	6	6	14
CAN (Modules/Nodes)			
3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)			
2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules			
2	2	2	2
ASCLIN Modules / with ASC & LIN / with 3-wire SPI			
12/12/11	12/12/11	12/12/11	12/12/12
QSPI Modules / with LVDS			
6/2	6/2	6/2	6/2
SENT Channels			
20	20	20	25
MSC Modules			
2	2	2	4
PSI5 Channels			
4	4	4	4

(table continues...)

5 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

1 TC39x BD step variants

Table 3 (continued) TC39x BD step (part 3)

SAL-TC397QP-256F300S	SAL-TC397XZ-256F300S	SAL-TC397XX-256F300S	SAK-TC399QP-192F300S
PSI5-S Module			
Yes	Yes	Yes	Yes
SDMMC Module			
Yes	Yes	Yes	Yes
Max. Ethernet Availability: 1GBit/100Mbit/No			
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability[6)]			
MCDS	MCDS	MCDS	MCDS
ADAS Cluster Available			
No	No	No	No
CIF			
No	No	No	No
HSM Available			
Yes	Yes	Yes	Yes

6 Refer to the ***MCDS availability*** section of this document for additional details.

2 TC39x BC step variants

2.1 TC39x BC step (part 1)

A table listing the TC39x BC step variants.

Table 4 TC39x_BC step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
Step						
BC	BC	BC	BC	BC	BC	BC
Production Status						
Standard	Standard	Standard	Standard	Standard	Standard	Standard
Package Type						
PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-292
Pinout						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	ADAS
Reference Silicon						
TC39x	TC39x	TC39x	TC39x	TC39x	TC39x	TC39x
Temperature Range (Ambient)						
SAL	SAL	SAL	SAK	SAK	SAK	SAK
Chip ID ***Attention*: *The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***						
0xAF019992	0x8F019992	0x8F019792	0x8F019992	0xAF019992	0x8F019792	0xBF019792
Cores / Checker Cores						
6/4	6/4	6/4	6/4	6/4	6/4	6/4
Max. Freq. (MHz)						
300	300	300	300	300	300	300
Program Flash (MB)						
16	16	16	16	16	16	16
Data Flash0 (single-ended) (KB)						
1024	1024	1024	1024	1024	1024	1024
Total SRAM (without EMEM and Cache) (KB)						
2528	2528	2528	2528	2528	2528	2528
EMEM Size (KB)						
4096	0	0	0	4096	0	4096
DSPR (KB)						

(table continues...)

2 TC39x BC step variants

Table 4 (continued) TC39x_BC step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
DLMU (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
PSPR (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)						
768	768	768	768	768	768	768
DAM (KB)						
128	128	128	128	128	128	128
AMU[7)]						
No	No	No	No	No	No	No
ADC (Primary Groups/Channels)						
8/64	8/64	5/40	8/64	8/64	5/40	4/26
ADC (Secondary Groups/Channels)						
4/60	4/60	4/60	4/60	4/60	4/60	4/42
ADC (Fast Compare Channels)						
8	8	8	8	8	8	8
ADC (EDSADC Channels)						
14	14	6	14	14	6	6
CAN (Modules/Nodes)						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules						
2	2	2	2	2	2	2
ASCLIN Modules / with ASC & LIN / with 3-wire SPI						
12/12/12	12/12/12	12/12/11	12/12/12	12/12/12	12/12/11	12/12/9
QSPI Modules / with LVDS						
6/2	6/2	6/2	6/2	6/2	6/2	6/1

(table continues...)

7 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

2 TC39x BC step variants

Table 4 (continued) TC39x_BC step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
SENT Channels						
25	25	20	25	25	20	17
MSC Modules						
4	4	2	4	4	2	1
PSI5 Channels						
4	4	4	4	4	4	4
PSI5-S Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDMMC Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
Max. Ethernet Availability: 1GBit/100Mbit/No						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability[8]						
MCDS	MCDS	MCDS	MCDS	MCDS	MCDS	MCDS
ADAS Cluster Available						
No	No	No	No	No	No	Yes
CIF						
No	No	No	No	No	No	No
HSM Available						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

8 Refer to the ***MCDS availability*** section of this document for additional details.

2.2 TC39x BC step (part 2)

A continuation table listing the TC39x BC step variants.

Table 5 TC39x_BC step (part 2)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S
Step				
BC	BC	BC	BC	BC
Production Status				
Standard	Standard	Customer Specific	Customer Specific	Customer Specific
Package Type				
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout				
ADAS	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
Reference Silicon				
TC39x	TC39x	TC39x	TC39x	TC39x
Temperature Range (Ambient)				
SAK	SAK	SAK	SAK	SAK
Chip ID ***Attention*: *The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***				
0xCC019792	0xAF019792	0xCD019792	0xCF019792	0xFF019792
Cores / Checker Cores				
4/3	6/4	4/4	4/4	6/4
Max. Freq. (MHz)				
300	300	300	300	300
Program Flash (MB)				
10	16	12	16	16
Data Flash0 (single-ended) (KB)				
1024	1024	1024	1024	1024
Total SRAM (without EMEM and Cache) (KB)				
1696	2528	1184	2080	1632
EMEM Size (KB)				
4096	4096	0	0	0
DSPR (KB)				
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
DLMU (KB)				

(table continues...)

2 TC39x BC step variants

Table 5 (continued) TC39x_BC step (part 2)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
PSPR (KB)				
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)				
512	768	0	768	0
DAM (KB)				
0	128	0	128	0
AMU[9)]				
No	No	No	No	No
ADC (Primary Groups/Channels)				
4/26	5/40	5/40	5/40	5/40
ADC (Secondary Groups/Channels)				
4/42	4/60	4/60	4/60	4/60
ADC (Fast Compare Channels)				
8	8	8	8	8
ADC (EDSADC Channels)				
6	6	6	6	6
CAN (Modules/Nodes)				
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)				
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules				
2	2	2	2	2
ASCLIN Modules / with ASC & LIN / with 3-wire SPI				
12/12/9	12/12/11	12/12/11	12/12/11	12/12/11
QSPI Modules / with LVDS				
6/1	6/2	6/2	6/2	6/2
SENT Channels				
17	20	20	20	20
MSC Modules				
1	2	2	2	2

(table continues...)

9 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

2 TC39x BC step variants

Table 5 (continued) TC39x_BC step (part 2)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S
PSI5 Channels				
4	4	4	4	4
PSI5-S Module				
Yes	Yes	Yes	Yes	Yes
SDMMC Module				
Yes	Yes	Yes	Yes	Yes
Max. Ethernet Availability: 1GBit/100Mbit/No				
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability[10)]				
MCDS	MCDS	MCDS	MCDS	MCDS
ADAS Cluster Available				
Yes	No	No	No	No
CIF				
No	No	No	No	No
HSM Available				
Yes	Yes	Yes	Yes	Yes

10 Refer to the ***MCDS availability*** section of this document for additional details.

3 Memory maps of TC39x variants

This section describes the influence of the available feature variants on the memory map.

Program Flash

Variants:

- 16 MB: umbrella (5 x 3 MB, 1 x 1 MB), see User's Manual.
- 12 MB: 4 x 3 MB (see Figure below).
- 10 MB: 3 + 2 + 3 + 2 MB (see Figure below).

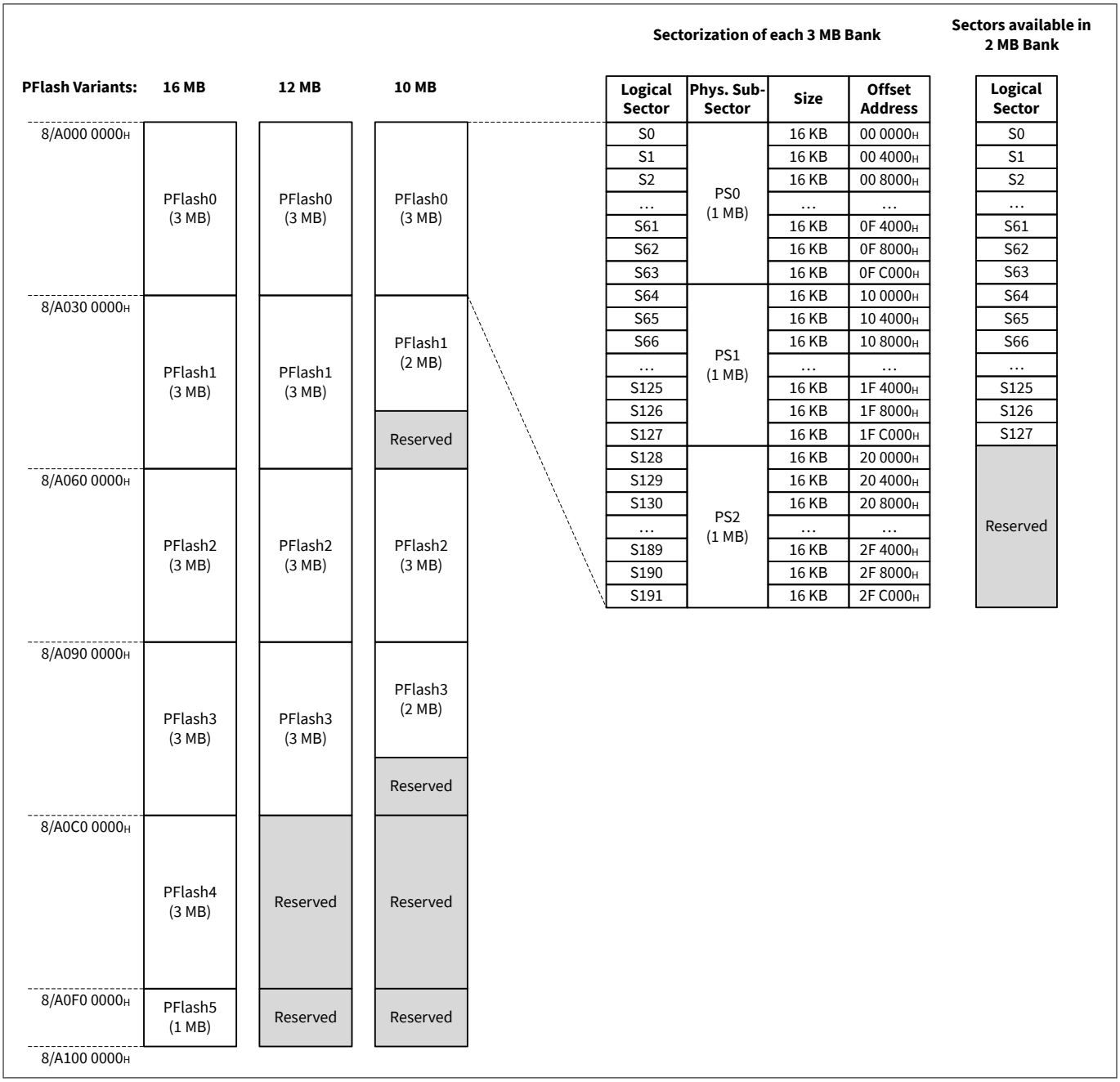

Figure 1 TC39x PFlash variants

Cores / checker cores

Variants:

- 6/4: umbrella, see User's Manual
- 4/4: not available are CPU4 and CPU5 including their RAMs (DSPR, DCACHE, DTAG, PSPR, PCACHE, PTAG, DLMU)
- 4/3: not available are CPU4 and CPU5 including their RAMs (DSPR, DCACHE, DTAG, PSPR, PCACHE, PTAG, DLMU) and CPU3 lockstep is not available (LCLCON1.LSEN3 must stay 0_B).

LMU

Variants:

- 768 KB: umbrella, see User's Manual.
- 512 KB: only LMU0 and LMU1 LMU RAM are available (see Figure below).
- 0 KB: no LMURAM is available (see Figure below)

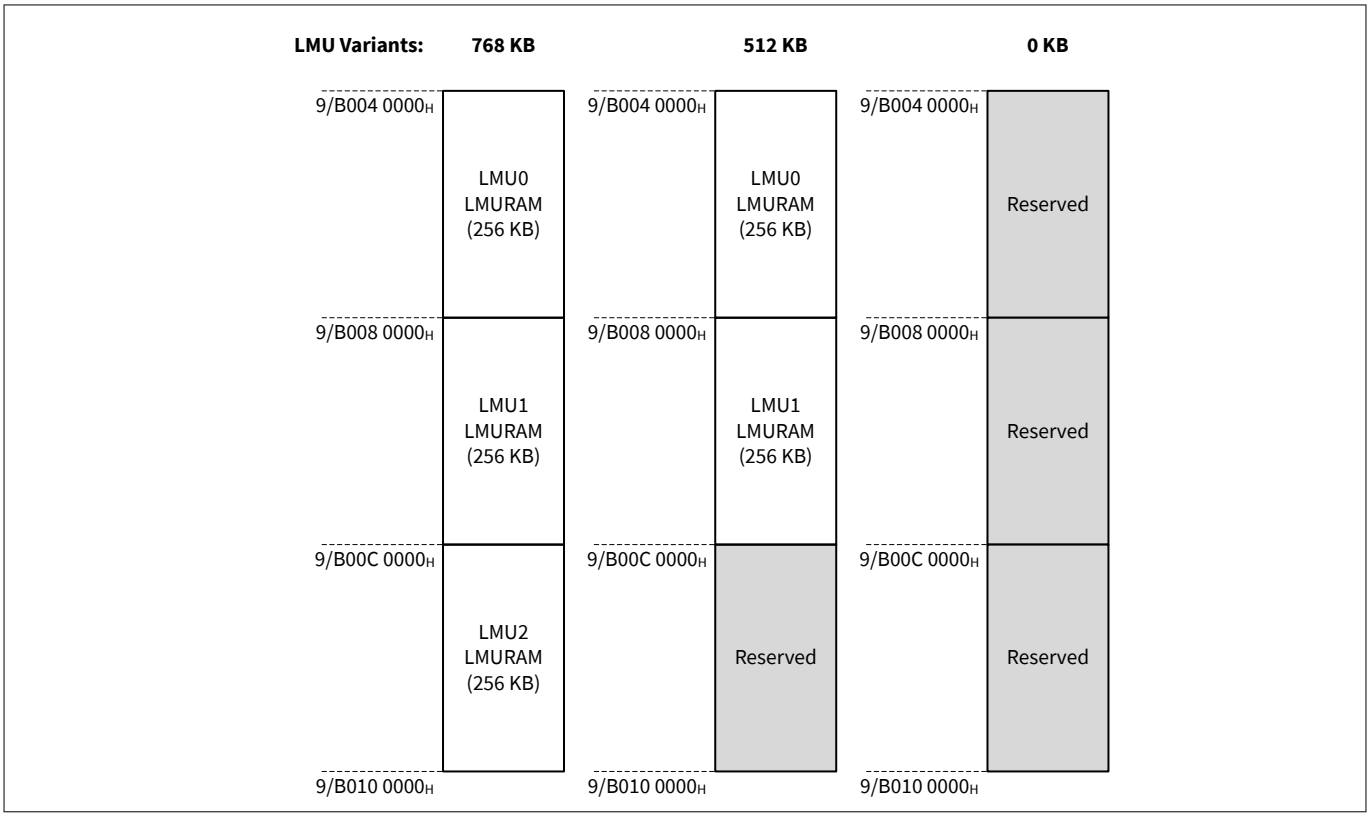

Figure 2 TC39x LMU Variants

DAM

Variants:

- 128 KB: umbrella, see User's Manual
- 0 KB: none of the DAM RAMs are available

ADAS cluster available

Variants:

- Yes: umbrella, see User's Manual
- No: the following instances are not available: HSPDM, RIF0, RIF1, SPU0, SPU1, SPUCFG0, SPUCFG1, SPU Lockstep SFR.

EMEM availability

Variants:

3 Memory maps of TC39x variants

- 4096 KB: umbrella, see User's Manual.
- 0 KB: no EMEM available.

ADC availability

- Limitation on availability of ADC channels are caused by pin limitations. See Data Sheet for the pinning table of the package.

MCDS availability

- MCDS is not intended for use in productive devices. It may not be tested and is not covered by the safety case. For this functionality, please refer to the Aurix 2G Emulation device Data Sheet.

Revision history

Document version	Date of release	Description of changes
V1.0	2018-06-08	• First release.
V1.1	2018-08-06	• Added row "Reference Silicon" (needed e.g. for TC37x) to refer user to User's Manual Appx.
V1.2	2019-03-01	• In "About this document": Corrected "overloaded" to "overlaid". • In "About this document": Added Feature Package "M" and "E" and remove "R". • In "About this document": Added clarification concerning AGBT in E, A and T. • In "About this document": Removed feature packages B, C, H. • In "Variant Tables of TC39x": added device "SAK-TC397XM-256F300S" • In "Variant Tables of TC39x": added Feature Package "E" devices (Emulation Devices).
V1.3	2019-06-12	• Added the TC39x "BD" step Variants to Chapter 1 • Removed the following Variants SAK-TC397XT-25 6F300S, SAK-TC397TT-25 6F300S for "BC" Step, Chapter 2 • Chapter 1 and 2: TC39x Bx step variants table format changed to fit all the contents. • Chapter 1 and 2:Added new row in the variant tables called "AMU" with the footnote for additional details. • Chapter: About this document: Feature package definitions are updated to consistent with the product naming nomenclature definition.
V1.4	2020-01-09	• Added the new TC39x "BD" step Variants SAL-TC397QP-192F300S,SAL-TC397QP-256F300S,SAL-TC397XZ-256F300S,SAL-TC397XX-256F300S to Chapter 1 • Page 1: About the document:Feature Package 'X' definition is updated to remove CIF. • Chapter 1 and 2:Added new row in the variant tables called "CIF" indicating the Camera Interface availability.
V1.5	2020-04-29	• Chapter 3: Added a note on the MCDS availability in productive devices. • About this document section: Added an additional note for the Feature package 'E'.
V1.6	2020-11-19	• Chapter 1, 2: Added a Foot note for the 'MCDS Availability' to explain its usage. • Chapter 3: Updated 'MCDS Availability' section to describe its usage.
V1.7	2021-06-17	• Chapter 1: Added a new TC39x BD variant: SAK-TC399QP-192F300S.

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