# Customer Training Workshop

# Traveo™ II Local Interconnect Network (LIN)

Q4 2020

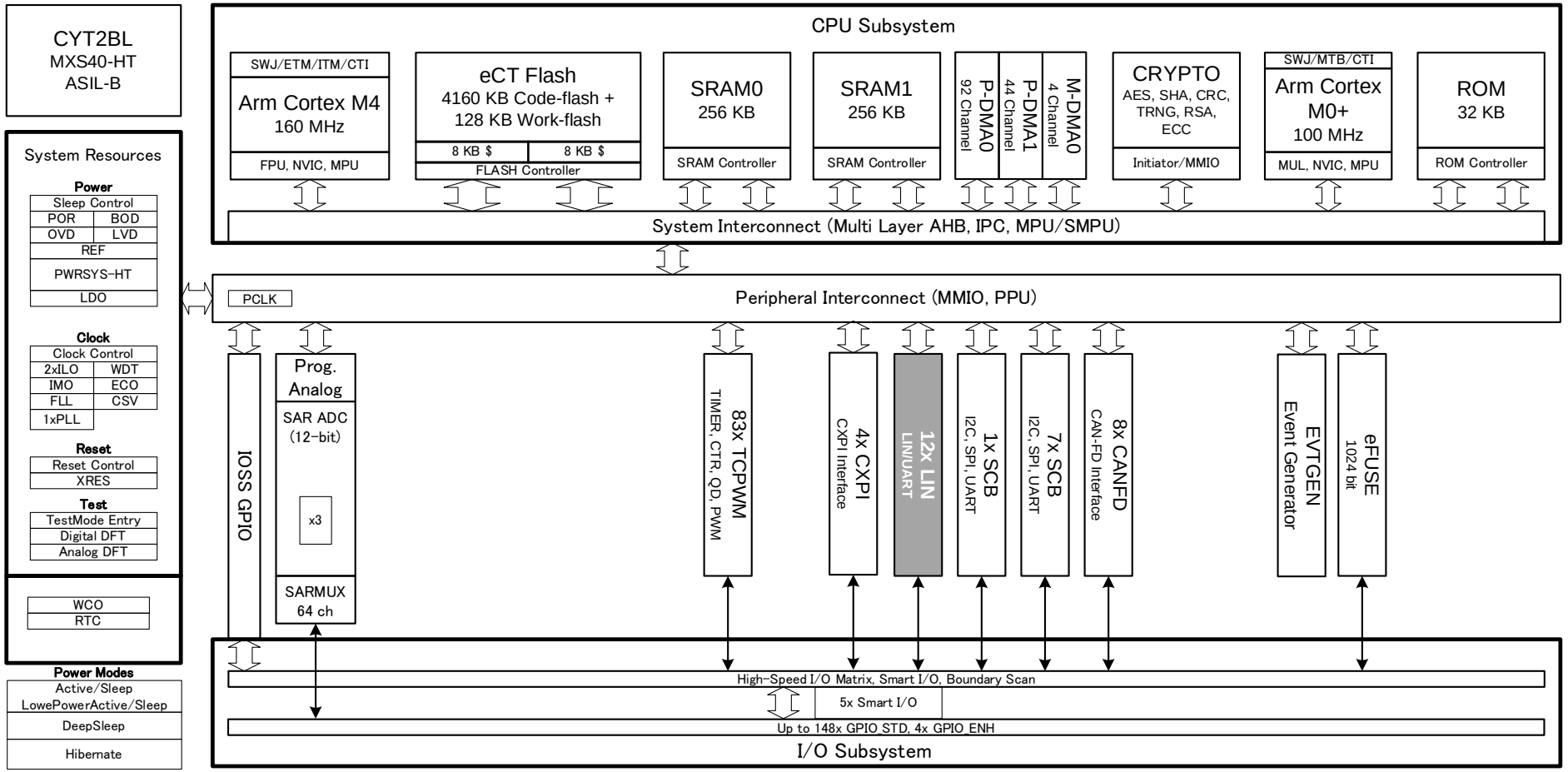
# Target Products

› Target product list for this training material:

| Family Category | Series | Code Flash Memory Size |
|---|---|---|
| Traveo™ II Automotive Body Controller Entry | CYT2B6 | Up to 576 KB |
| Traveo II Automotive Body Controller Entry | CYT2B7 | Up to 1088 KB |
| Traveo II Automotive Body Controller Entry | CYT2B9 | Up to 2112 KB |
| Traveo II Automotive Body Controller Entry | CYT2BL | Up to 4160 KB |
| Traveo II Automotive Body Controller High | CYT3BB/4BB | Up to 4160 KB |
| Traveo II Automotive Body Controller High | CYT4BF | Up to 8384 KB |
| Traveo II Automotive Cluster | CYT3DL | Up to 4160 KB |
| Traveo II Automotive Cluster | CYT4DN | Up to 6336 KB |

# Introduction for Traveo II Body Controller Entry

› LIN is part of peripheral blocks.

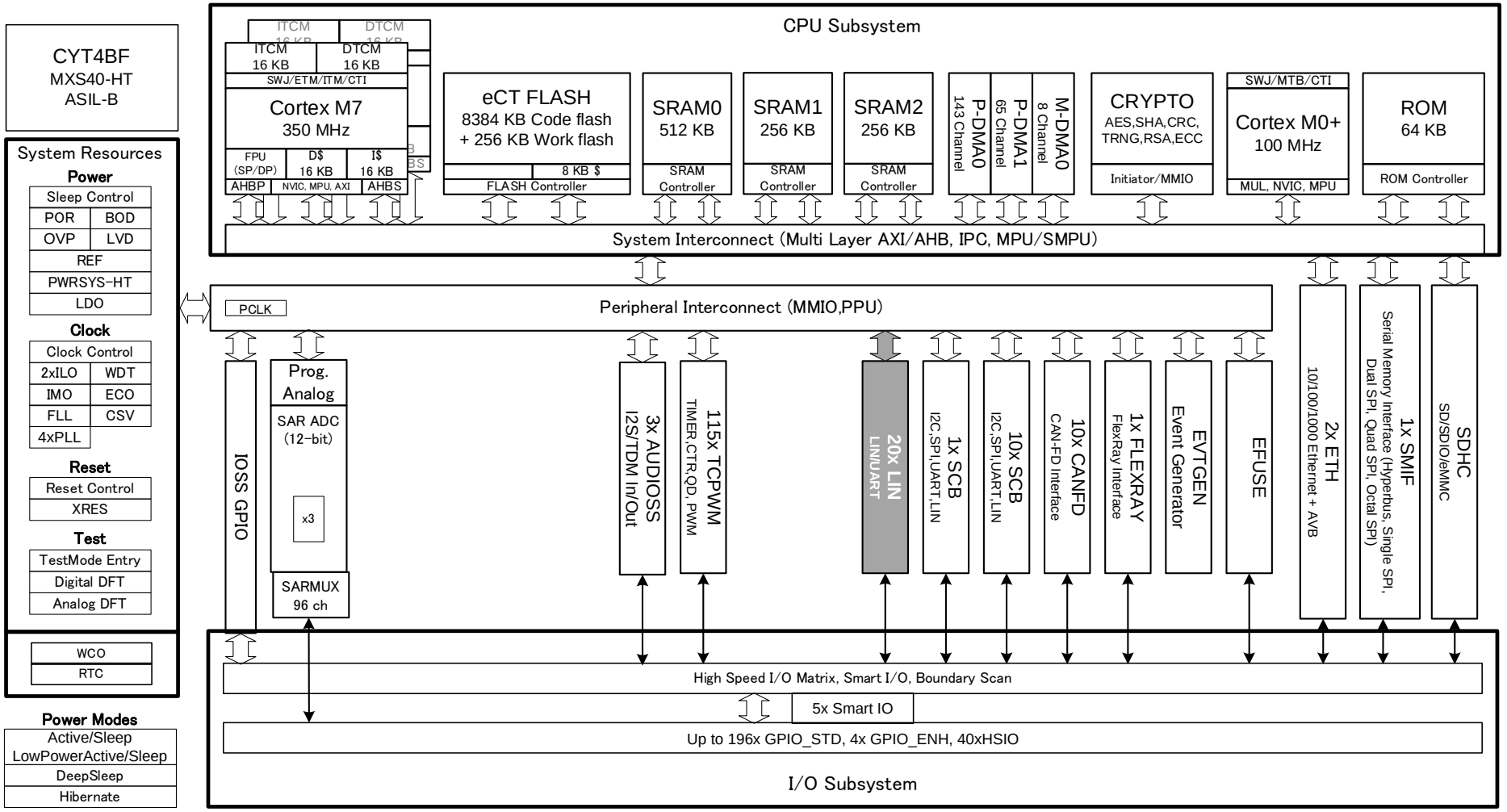



## Hint Bar

**Review TRM chapter 26 for additional details**

# Introduction for Traveo II Body Controller High

› LIN is part of peripheral blocks.

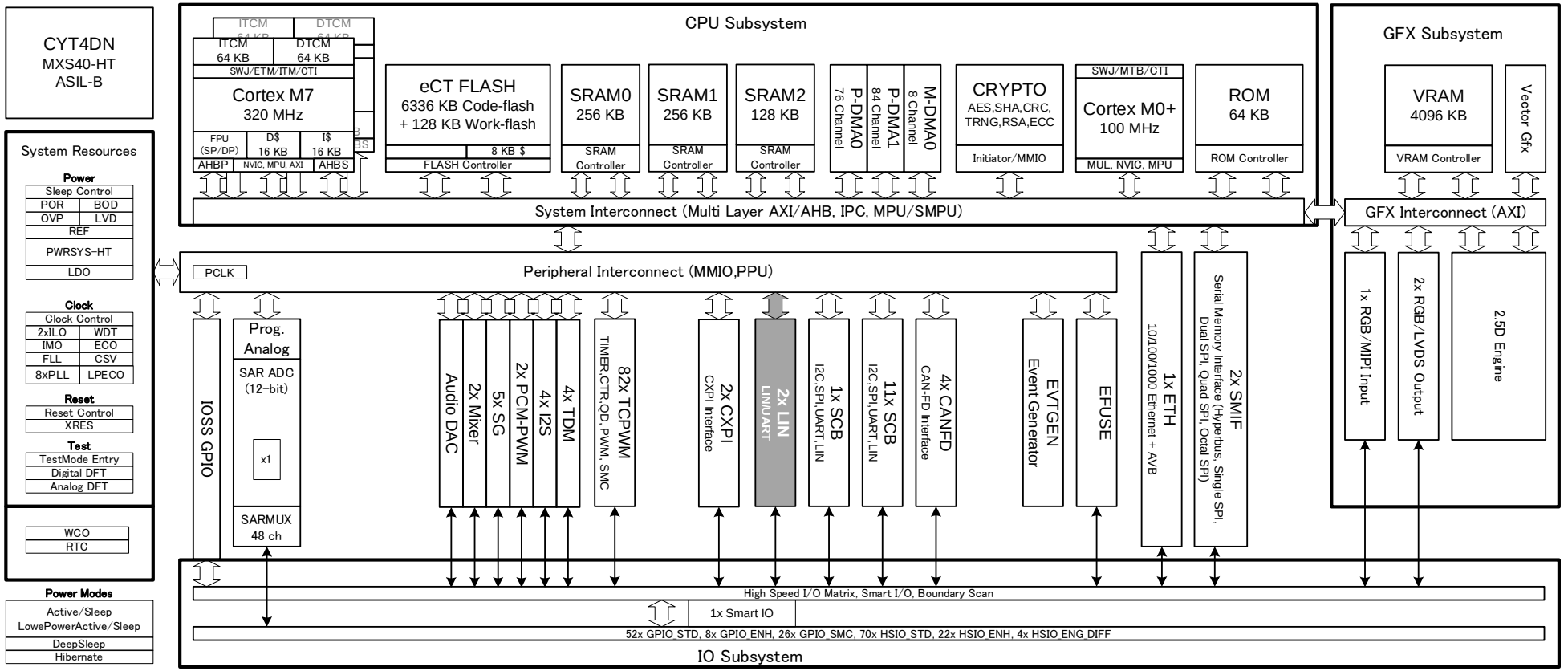



**Hint Bar**

**Review TRM chapter 26 for additional details**

# Introduction for Traveo II Cluster

› LIN is part of peripheral blocks.




**Hint Bar**

**Review TRM chapter 26 for additional details**

# Local Interconnect Network Overview

- The LIN block supports the LIN and UART serial interface protocols
- Features (LIN)
  - ISO 17987 standard
  - Master node functionality
    - Autonomous header transmission
    - Autonomous response transmission and reception
  - Slave node functionality
    - Autonomous header reception
    - Autonomous response transmission and reception
    - Baud rate detection
  - Autonomous Error Handling
    - PID error
    - Checksum error
    - Bit error (leads to transmission stop)

**Hint Bar**

**Review Chapter 26 in the TRM for additional details**

# Features

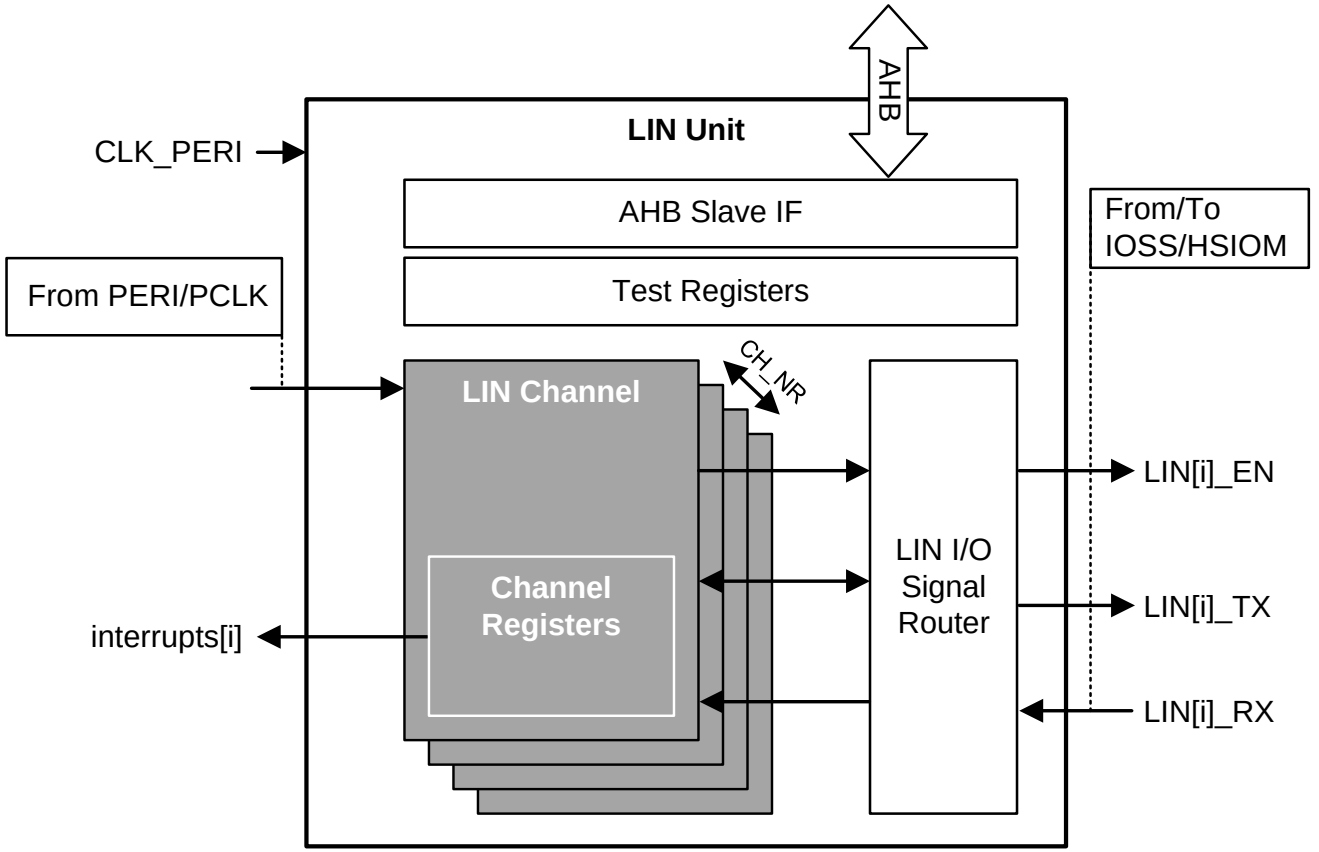
- LIN
  - Wakeup transmission and detection
  - Timeout detection
  - Data buffer (up to 8 bytes)
  - Test modes
- UART
  - Programmable 5/6/7/8-bit data fields
  - Programmable number of STOP bits: ½, 1, 1½, or 2 bits
  - Optional parity functionality with odd and even parity
- LIN/UART
  - Oversampling
  - Noise filter

**Hint Bar**

**Review Chapter 26 in the TRM for additional details**

# LIN Block Diagram

- LIN Unit components
  - LIN channel
  - LIN mode
  - Master operation
  - Slave operation
  - Wakeup
  - Timeout
  - UART mode
  - Test mode
  - Oversampling
  - Noise filter




**Hint Bar**

**Review Chapter 26 in the TRM for additional details**

# Master and Slave Operation Commands

- These commands are set in the CMD register

| Command | Description | Node |
|---|---|---|
| TX_HEADER | Transmit a header | Master |
| RX_HEADER | Receive a header | Slave |
| TX_RESPONSE | Transmit a response | Master, Slave |
| RX_RESPONSE | Receive a response | Master, Slave |
| TX_WAKEUP | Transmit a wakeup signal | Master, Slave |

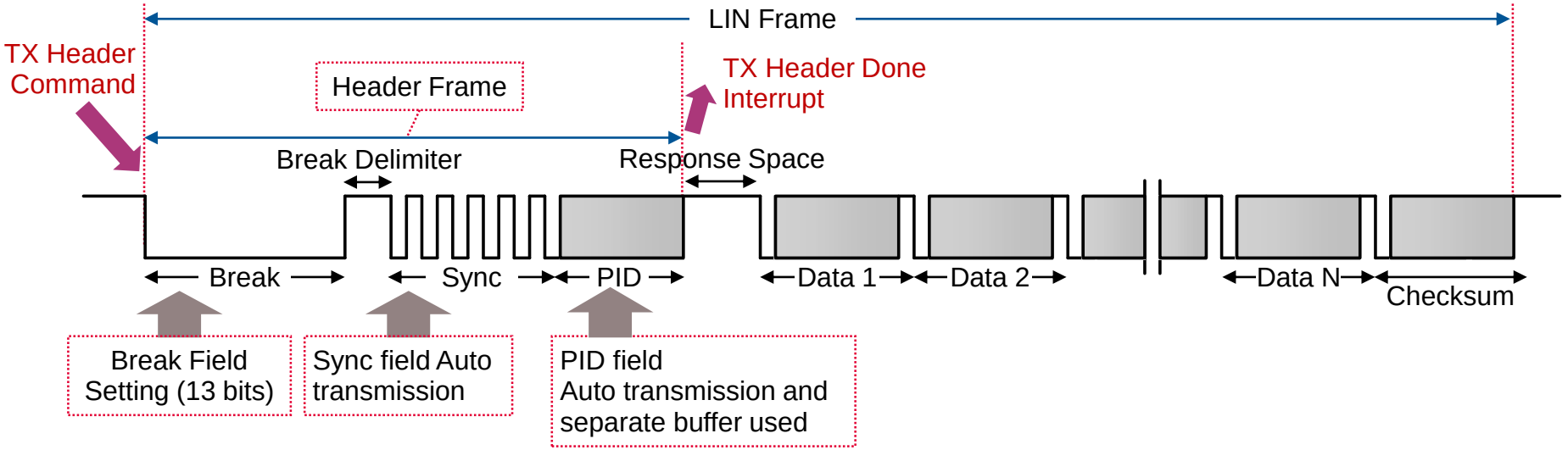
- Advantage
  - Reduces CPU load

**Hint Bar**

**Review TRM section 26.9.1 for additional details.**

# LIN Mode (Master Operation)

- Header transmission
  - Operated by command
  - Only in master mode




| Field | Field Description | Data Length | Buffer Available | Autonomous Field |
|---|---|---|---|---|
| Break | LIN start frame | 13–31 bits | No | Yes |
| Sync | Baud rate synchronization | 10 bits | No | Yes |
| PID | Frame identifier and parity bit | 8 bits | Yes | Yes |

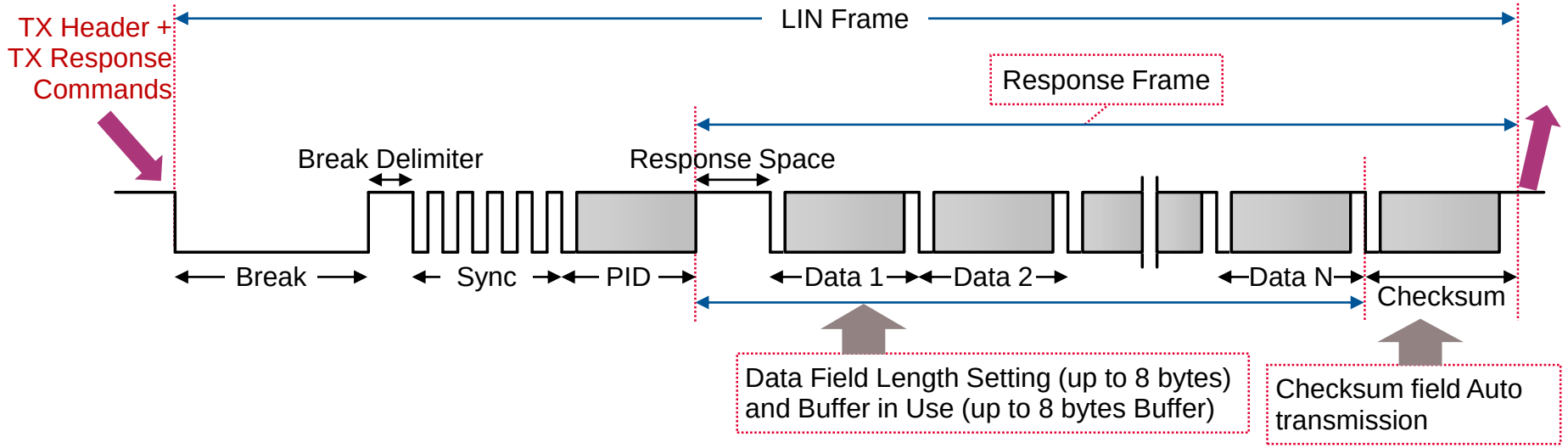
**Hint Bar**

**Review TRM section 26.9.1.1 for additional details about commands**

**Review Register TRM for additional details about the PID field buffer**

# LIN Mode (Master Operation)

- Response transmission
  - Operated by command




| Field | Field Description | Data Length | Buffer Available | Autonomous Field |
|---|---|---|---|---|
| Data | Transmission/Reception data | 1–8 Bytes | Yes | Yes |
| Checksum | Checksum for Data field or PID and Data field (Selectable) | 10 bits | Yes | Yes |

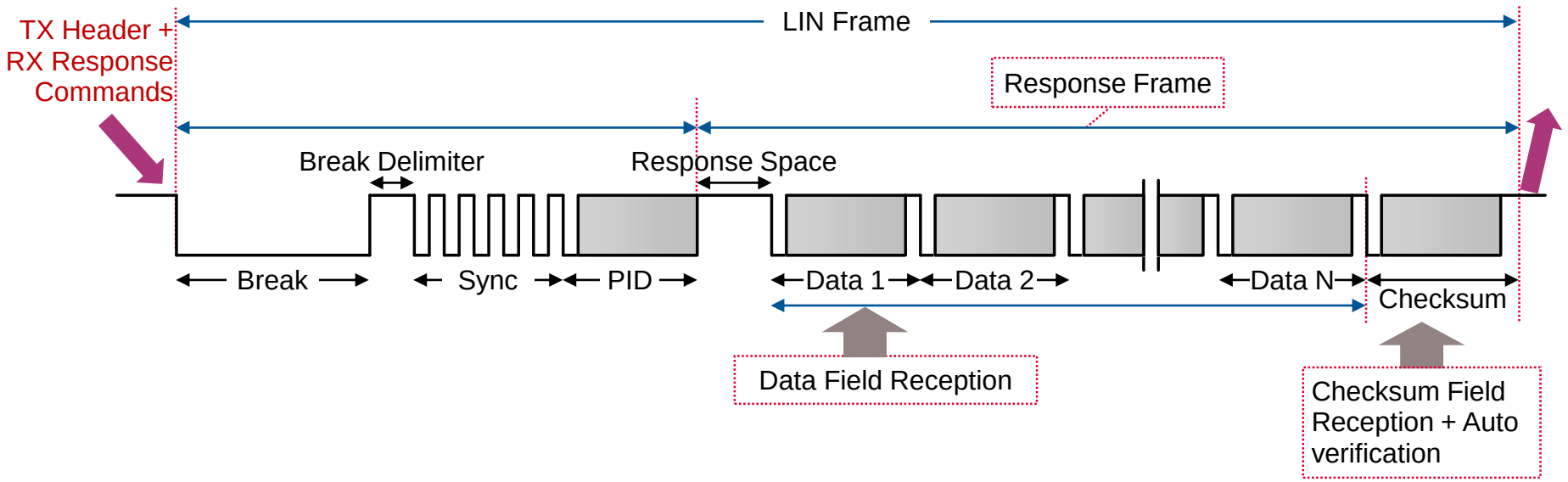
**Hint Bar**

**Review TRM chapter 26 for additional details**

**Review Register TRM for additional details about Data and Checksum**

# LIN Mode (Master Operation)

- Response reception
  - Operated by command



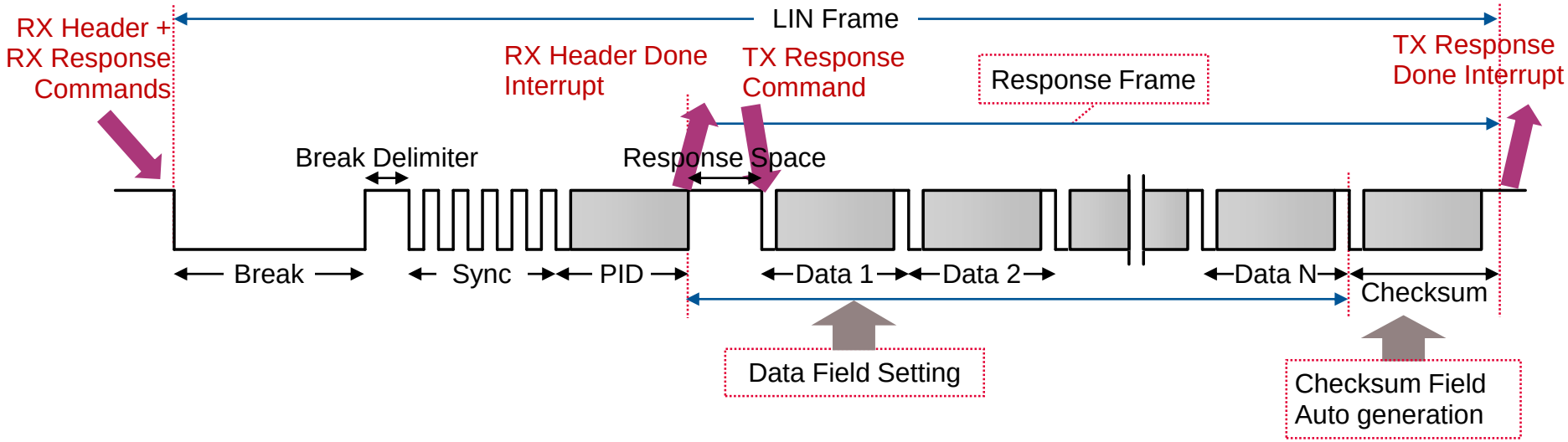

**Hint Bar**

**Review TRM chapter 26 for additional details**

**Review Register TRM for additional details about the Data and Checksum field buffers**

# LIN Mode (Slave Operation)

- Response transmission
  - Operated by command



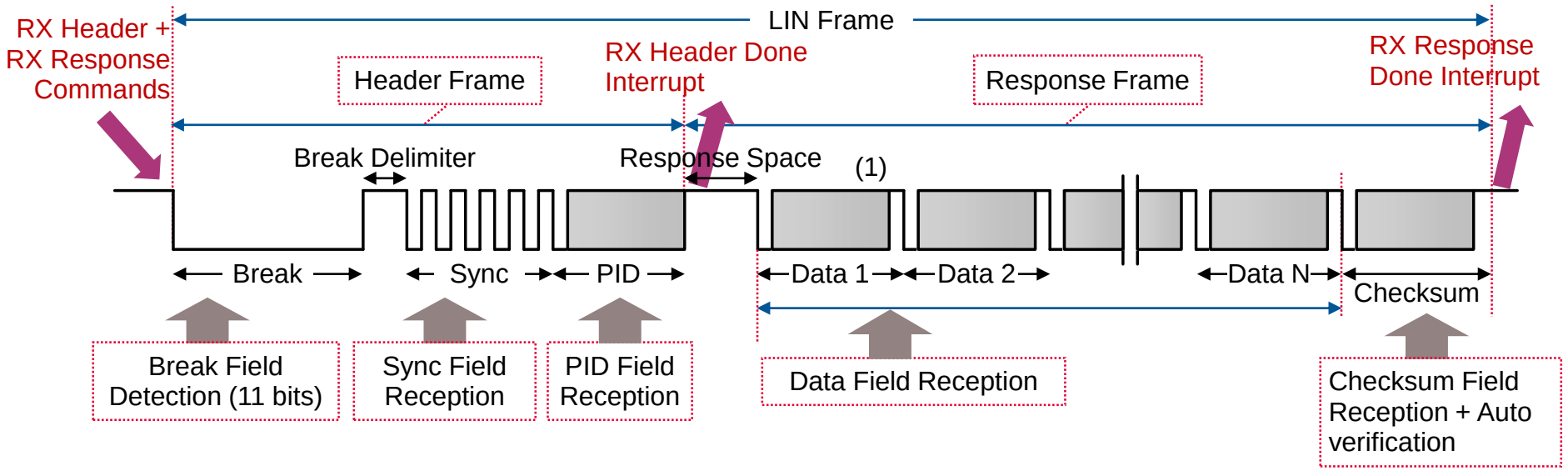

**Hint Bar**

**Review TRM chapter 26 for additional details**

**RX RESPONSE is enabled before LIN frame, to avoid Response data loss due to delayed header reception processing.**

# LIN Mode (Slave Operation)

- Header and Response reception
  - Header and Response reception are operated by command
  - Header reception is only in slave mode




[1] Data length and checksum type must be set before receiving the latest Stop bit of Data1 in the Response as slave.

**Hint Bar**

**Review TRM chapter 26 for additional details**

# Wakeup

- When a LIN node is in sleep state, a wakeup signal can initiate a transfer to an operational state
- Both wakeup signal generation and detection are supported in hardware
  - Wakeup signal transmission
    - Wakeup signal length is set in the register[1]
  - Wakeup signal reception
    - Minimum low pulse length must be configured for detection[2]
    - Wakeup is detected by the rising edge

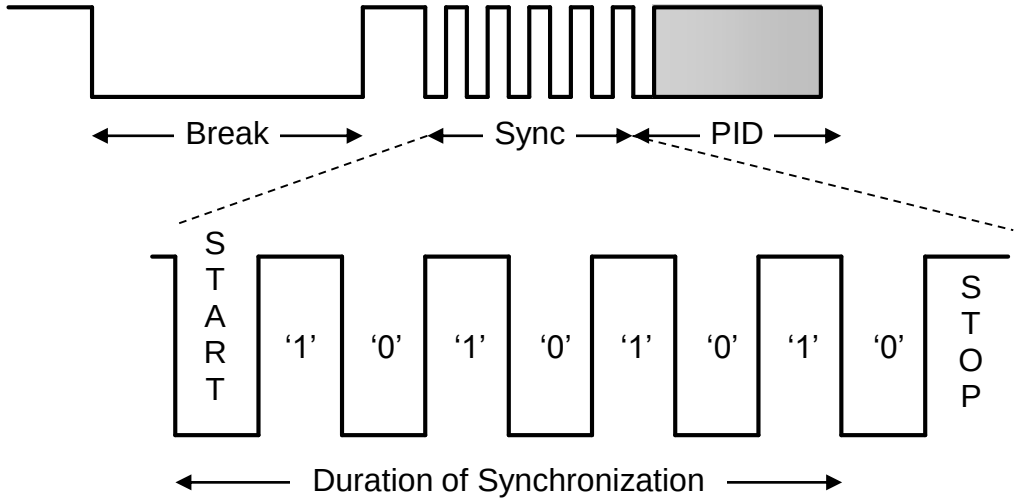
**Hint Bar**

**Review TRM section 26.6 and Register TRM for additional details**

[1] Wakeup signal setting length range: 1–31 bit periods
[2] Wakeup pulse length: 250 µs–5 ms

# Baud Rate Detection

- The sync field synchronizes slave clocks to the master clock in a slave operation
- Baud rate is adjusted by software and a detected correction factor
  - Synchronization procedure
    - (1) HW measures the sync field (8-bit duration from the START bit in the figure) and sets it to SYNC_COUNTER
    - (2) SW calculates PERI clock divider value using the SYNC_COUNTER value
    - (3) SW sets PERI clock divider value to PERI clock divider register

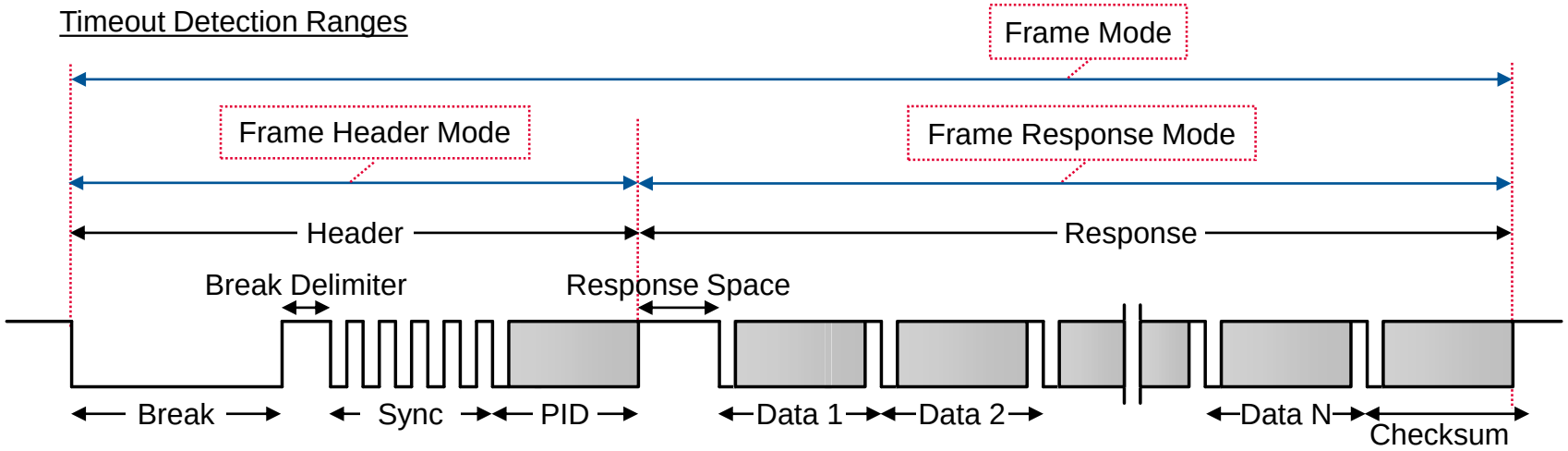



**Hint Bar**

**Review TRM chapter 26 and Register TRM for additional details**

# Timeout Detection

- Timeout detections are of three types
  - Frame mode
  - Frame header mode
  - Frame response mode
- Timeout length must be configured in bit periods[1]




- Advantage
  - Can set timeout value and initiate interrupt

[1] Timeout length range: Frame mode: 54–75 bit periods; Frame header mode: 34–47 bit periods; Frame response mode: 20–28 bit periods.

**Hint Bar**

**Review TRM section 26.5 and Register TRM for additional details**

# Interrupt Events in LIN Master Mode

| Event Type | Event | Event Detection Condition |
|---|---|---|
| TX | Header Transmission Done | Header transmission succeeded |
| TX | Response Transmission Done | Response transmission succeeded |
| RX | Response Reception Done | Response reception succeeded |
| Error | Timeout | A frame, header, or response does not finish within a specified time |
| TX Error | Transmitter Response Bit Error | During the response transmission, the received bus value does not match the transmitted value |
| RX Error | Receiver Response Frame Error | An invalid start bit or stop bit occurs during response reception (data field, checksum) |
| RX Error | Receiver Response Checksum Error | The calculated checksum over the data bytes, and optionally the PID field, does not match the received checksum |

**Hint Bar**

**Review TRM section 26.11 for additional details**

**Bit error detection leads to automatic transmission stop**

# Interrupt Events in LIN Slave Mode

| Event Type | Event | Event Detection Condition |
|---|---|---|
| TX | Response Transmission Done | Response transmission succeeded |
| RX | Header Reception Done | Header reception succeeded |
| RX | Response Reception Done | Response reception succeeded |
| RX | Synchronization Field Reception Done | Synchronization field successfully received |
| Error | Timeout | A frame, header, or response does not finish within a specified time |
| RX Error | Receiver Header Frame Error | An invalid start bit occurs during PID field<br>An invalid stop bit occurs during SYNC or PID field |
| RX Error | Receiver Synchronization Error | An invalid data field pattern is detected during the reception of the SYNC field |
| RX Error | Receiver PID Parity Error | The received PID field has a parity error |
| RX Error | Receiver Response Frame Error | An invalid stop bit occurs during response reception (data field, checksum) |
| RX Error | Receiver Response Checksum Error | The calculated checksum over the data bytes, and optionally the PID field, does not match the received checksum |

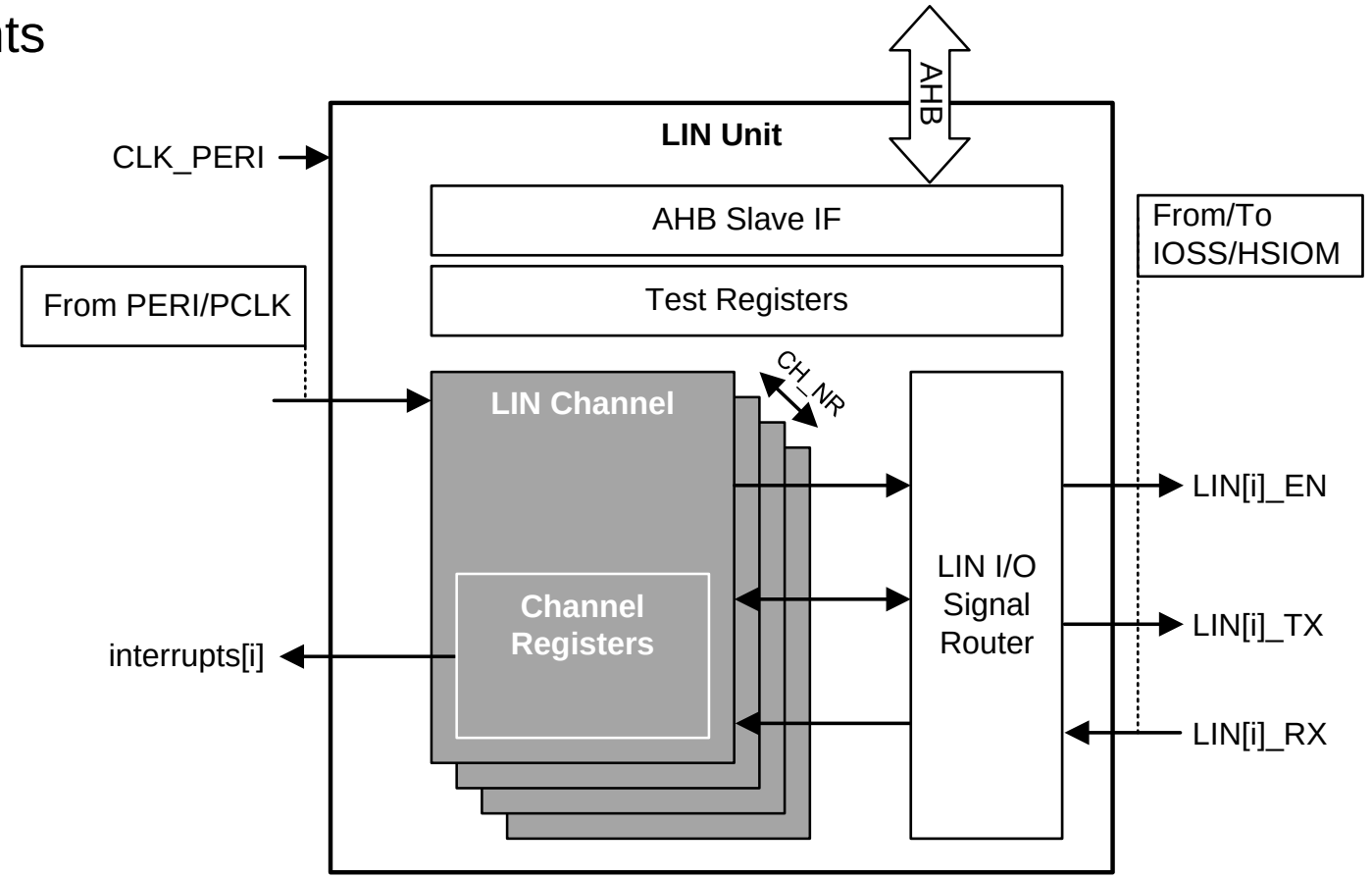
**Hint Bar**

**Review TRM section 26.11 for additional details**

**Bit error detection leads to automatic transmission stop**

# LIN Channel Block Diagram

- LIN Unit components
  - LIN channel
  - UART mode

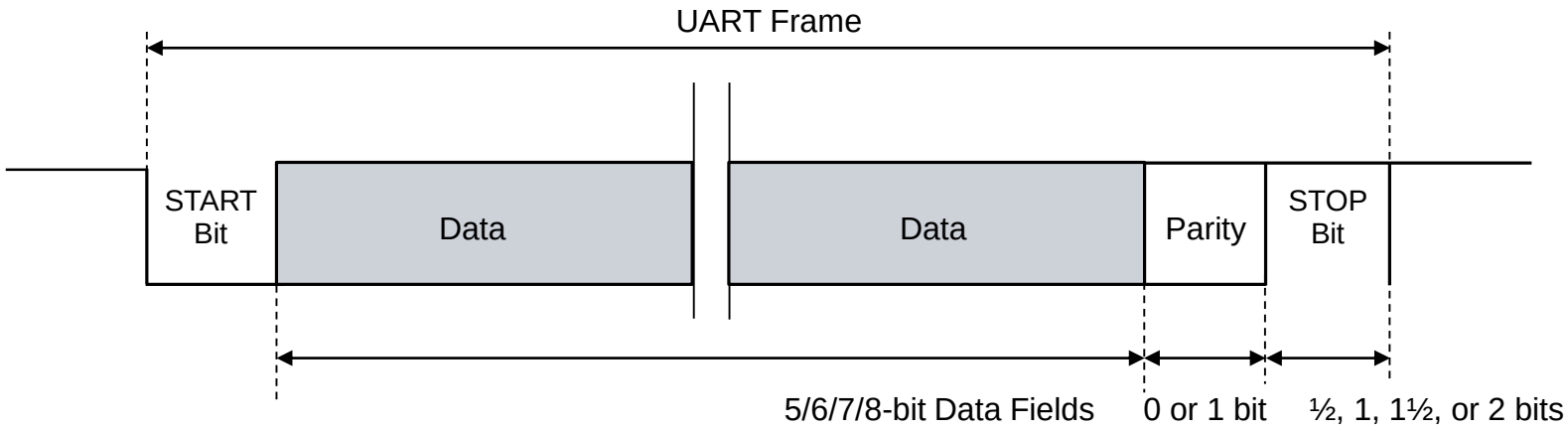



**Hint Bar**

**Review TRM chapter 26 for additional details**

# UART Mode (1/2)

- Operation
  - The UART frame is transmitted in
    - START bit (single bit)
    - Data field (programmable 5/6/7/8-bit data fields, single data buffer)
    - Parity bit (optional functionality with odd and even parity)
    - STOP bits (programmable ½, 1, 1½, or 2 bits)




**Hint Bar**

**Review TRM chapter 26 for additional details**

# UART Mode (2/2)

## Interrupt Events in UART Mode

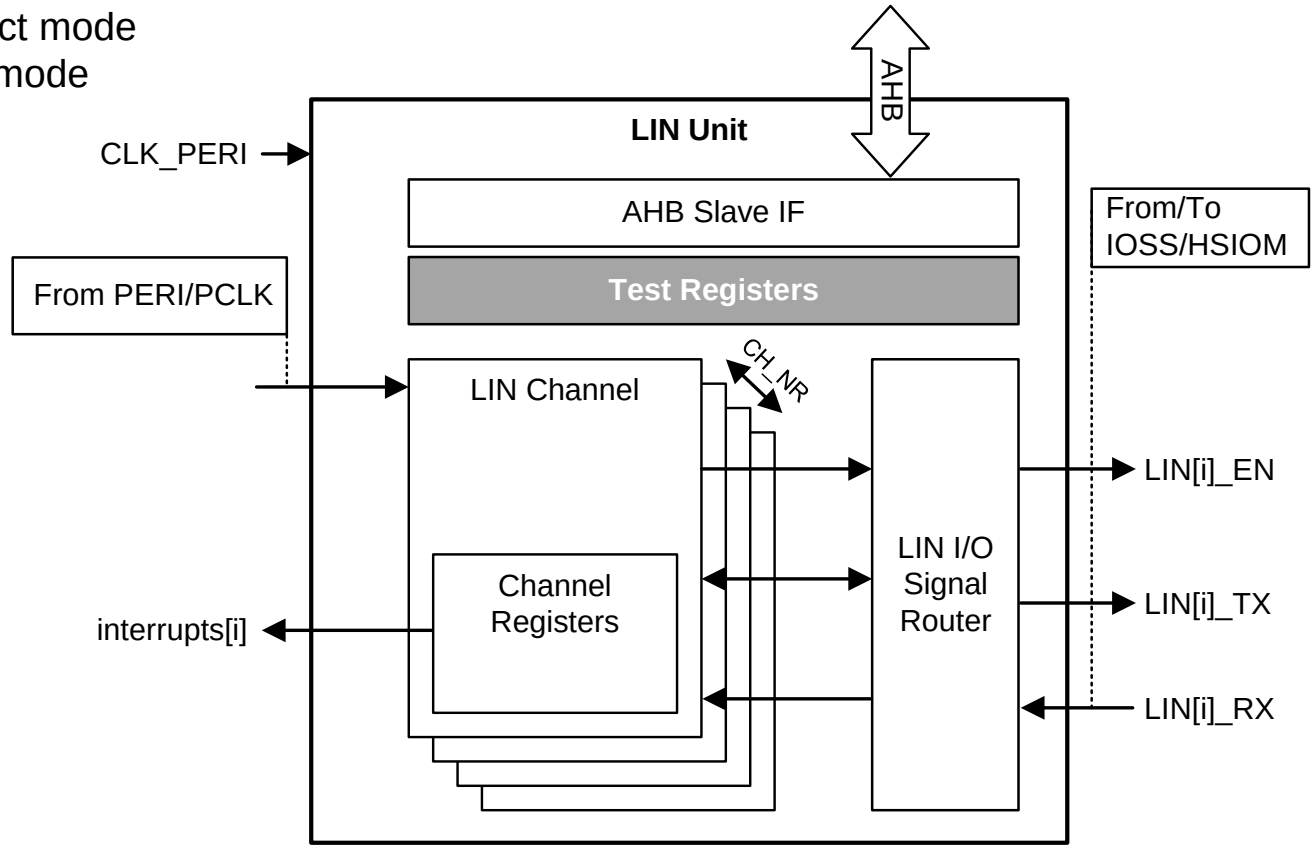
| Event Type | Event | Event Detection Condition |
|---|---|---|
| TX | Transmission Done | Transmission succeeded |
| RX | Reception Done | Reception succeeded |
| Error | Transmitter Bit Error | The incoming bus level does not match the transmitted value during transmission |
| Error | Receiver Frame Error | An invalid start bit or stop bit occurs during reception |
| Error | Receiver Parity Error | The received field has a parity error |

**Hint Bar**

**Review TRM section 26.11 for additional details**

# LIN Registers Block Diagram

- LIN Unit components
  - Test registers
    - Test mode
      - Partial Disconnect mode
      - Full Disconnect mode

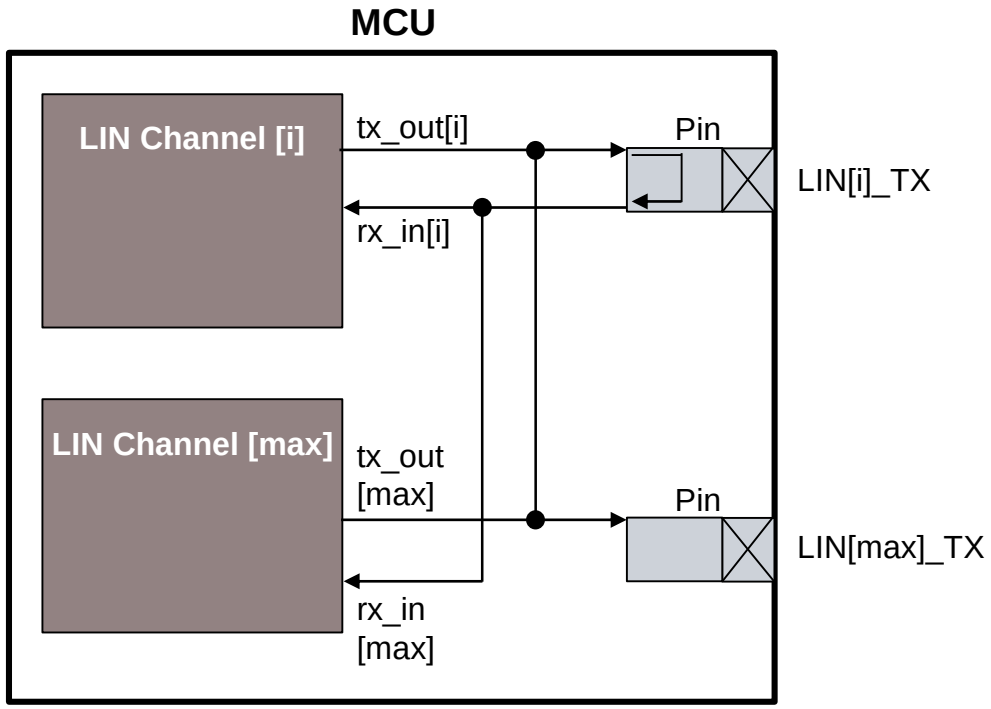



**Hint Bar**

**Review TRM chapter 26 for additional details.**

# Test Modes (1/2)

- Partial Disconnect mode
  - Loopback mode via the IOSS port pin structure
  - Connection between LIN ch.[i] and LIN ch.[max]




- Advantage
  - The LIN frame can be monitored on the TX port pins

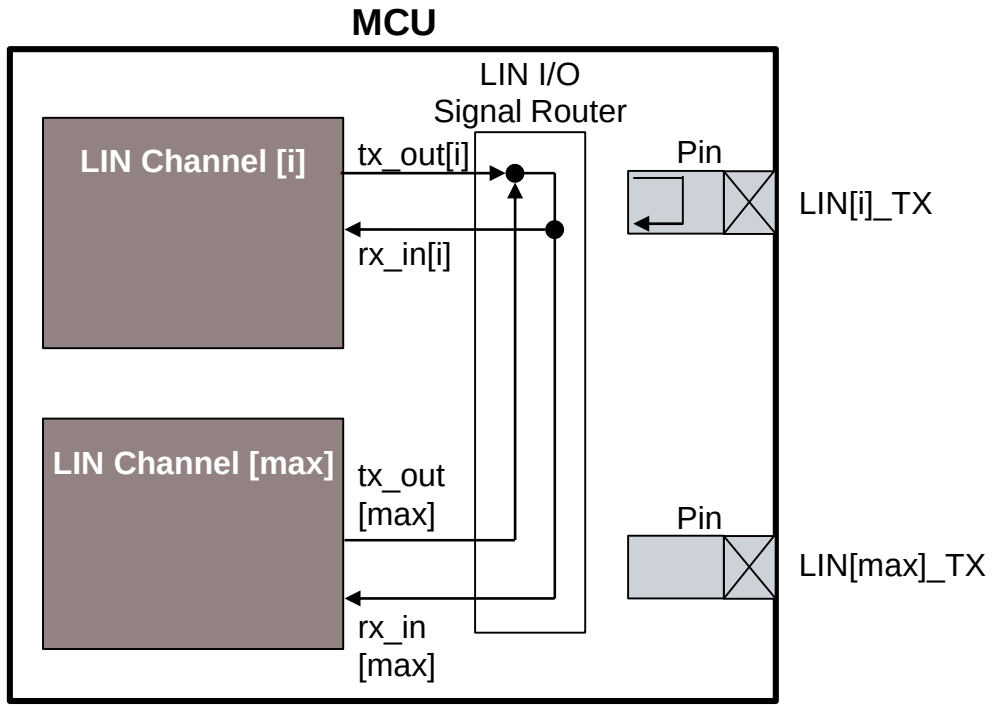
**Hint Bar**

**Review TRM section 26.8.2 for additional details**

**TVII-B-E-1M is available in the following LIN channels:**
**LIN ch.[i] = 0-6**
**LIN ch.[max] = 7**

# Test Modes (2/2)

- Full Disconnect mode
  - Full Loopback mode between LIN ch.[i] and LIN ch.[max]
  - There is no connection to port pins




- Advantage
  - Full LIN operation possible without external LIN bus

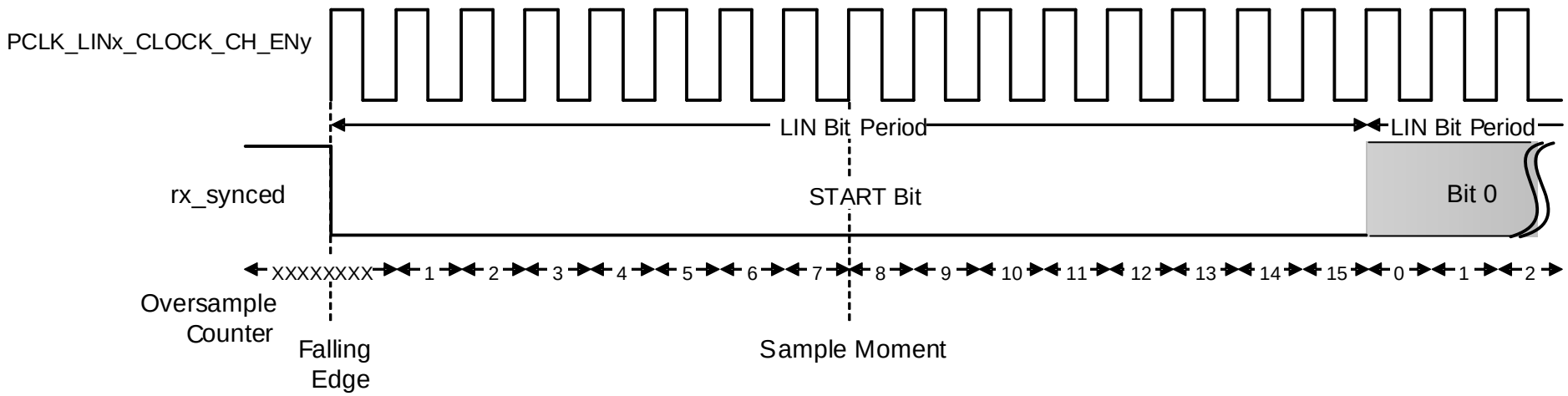
**Hint Bar**

**Review TRM section 26.8.2 for additional details**

**TVII-B-E-1M is available in the following LIN channels:**
**LIN ch.[i] = 0-6**
**LIN ch.[max] = 7**

# Oversampling

- One LIN bit length corresponds to 16 PCLK_LINx_CLOCK_CH_ENy[1] cycles
- A bit value is sampled when the oversample counter changes from ‘7’ to ‘8’



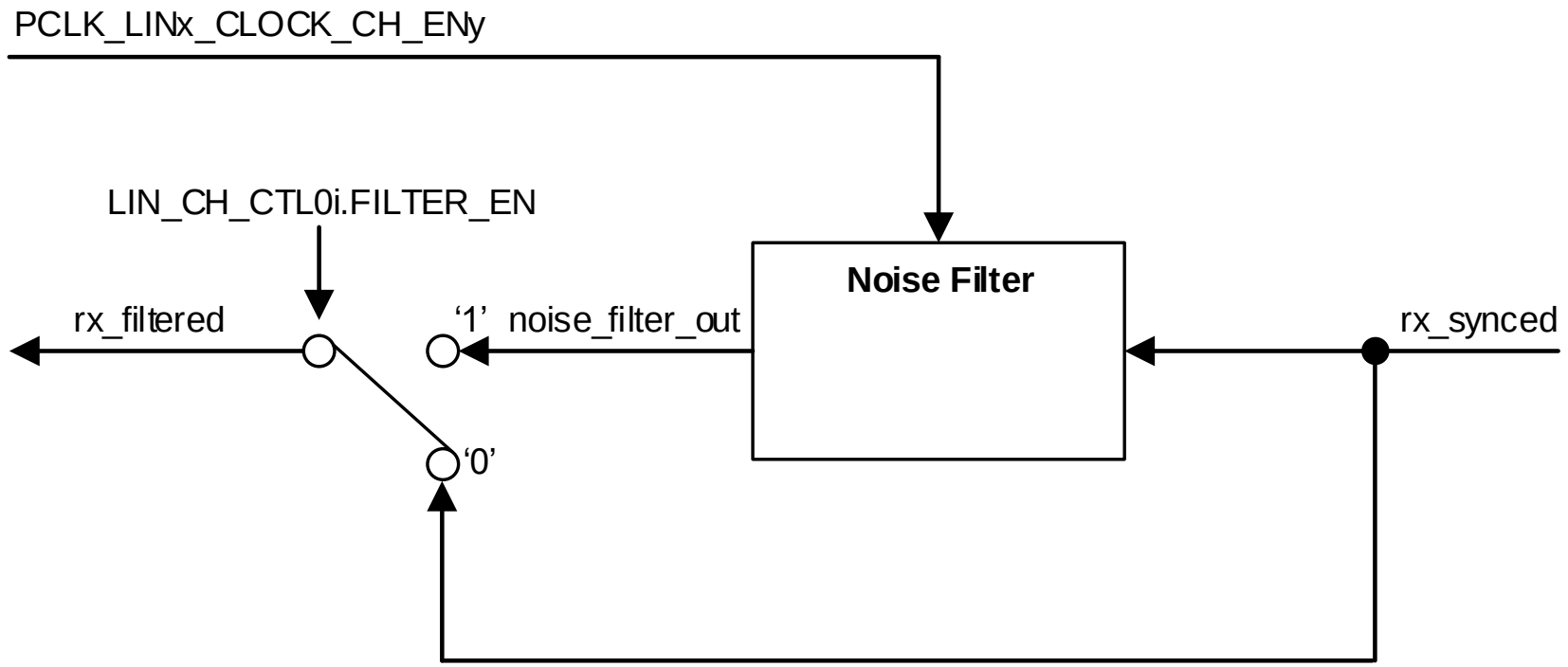

**Hint Bar**

**Review TRM section 26.3.1 and Register TRM for additional details**

[1] PCLK_LINx_CLOCK_CH_ENy is used for each LIN channel clock. This clock is derived from the peripheral interconnect (PERI) clock.

# Noise Filter

- The noise filter suppresses glitches on the RX input (rx_in) signal




**Hint Bar**

**Review TRM section 26.10 and Register TRM for additional details**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002-22212 *C, 2020-12-16

# Revision History

| Revision | ECN | Submission Date | Description of Change |
|---|---|---|---|
| ** | 6183154 | 05/24/2018 | Initial release |
| *A | 6406686 | 12/10/2018 | Added pages 2, 4, and 5, and the note descriptions for all pages<br>Updated page 3 |
| *B | 6677193 | 09/13/2019 | Updated page 2, 3, 4, 6, 7, 8, 14, 16, 20, 22, 23, 26 and 27.<br>Added page 5 |
| *C | 7062547 | 01/08/2021 | Updated page 2, 3, 8, 17, 20, 23, 24 and 25. |