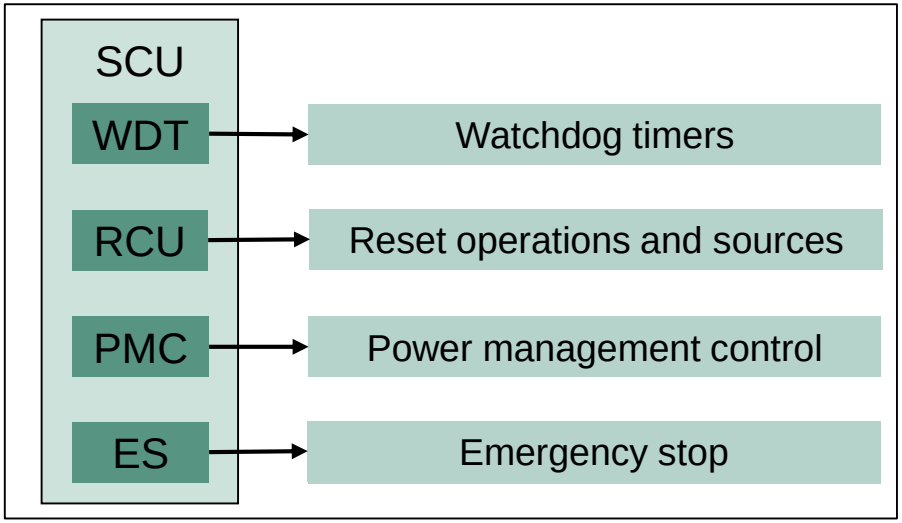
SCU

System Control Units

AURIX™ TC3xx Microcontroller Training
V1.0 2020-09

SCU
System Control Units



Highlights

› The SCU comprises various units, which handle reset operations (incl. effects and triggers), power management control (e.g. reducing power consumption) and many other miscellaneous submodules such as watchdogs.

Key Features

Watchdog timers

Reset operations and sources

Power management control

Emergency stop

Customer Benefits

› Robust failure detection and recovery

› Scalable reset concept based on different triggers

› Minimize power use during operation

› Fast reaction to emergency events without the SW intervention

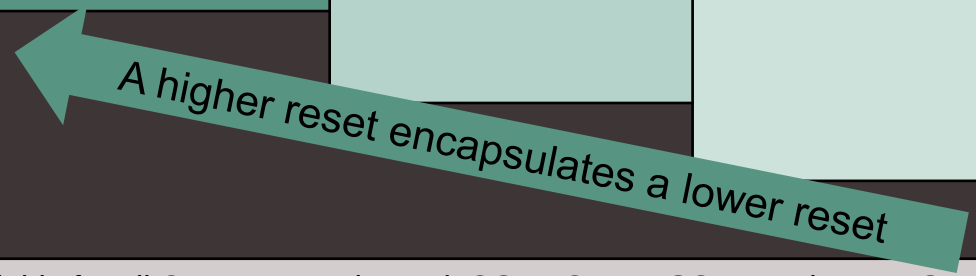
SCU
WDT - Watchdog Timers

- The WatchDog Timers (WDTs) provide a highly reliable and secure way of detecting and recovering from software or hardware failure
- They can be used to abort any accidental malfunction of a CPU or internal module within a user-specified time period
- Additionally, each of the WDTs incorporates an End-of-Initialization (ENDINIT) feature which protects the critical registers from unintended writes
- To protect these functions a sophisticated scheme is implemented that requires a password and guard bits during the accesses to the WDT control registers. Any write access that does not provide the correct values for the password and guard bits is regarded as malfunction and results in an alarm
- On top of the general WDTs, a Safety Watchdog Timer is provided. It is independent from the CPU watchdogs and it also provides temporal protection against unintended writes to critical system registers which could impact the safety-critical systems
- These feature ensures that the system runs in a robust and safe manner (e.g. Trigger an alarm, a reset or stopping the CPU in case of malfunction)

SCU
RCU – Reset types and effects

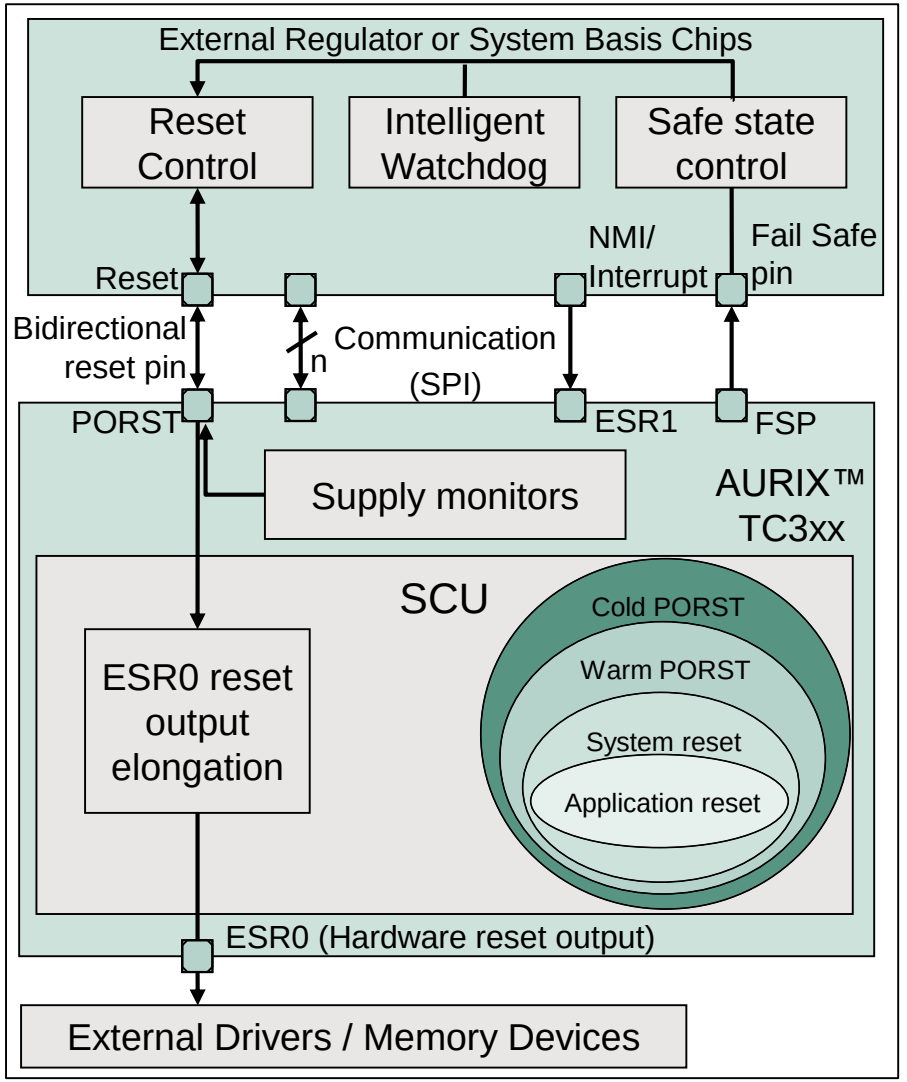
- AURIX™ TC3xx has a scalable reset concept, where different types of reset are encapsulated one into the other. The **Cold Power-On Reset** is the highest reset type, where the Embedded Voltage Regulator (EVR), internal clocks and RAMs are reset, additionally to the modules affected by the **Application Reset**, **System Reset** and **Warm Power-On Reset**
- SW Module Reset and Debug Reset enable the user to directly trigger a reset of the connected modules

Reset Type	Additional Modules affected by **Cold Power-On Reset**	Additional Modules affected by **Warm Power-On Reset**	Additional Modules affected by **System Reset**	Modules affected by **Application Reset**
Cold Power-On Reset	› Embedded Voltage Regulator › Internal clocks › RAMs: - DSPRs/PSPRs - LMU/BMU	› JTAG interface › OCDS › MCDS › SMU – Fault Signaling Protocol Pin	› Flash memory › Clock source › PLL › External Service Requests pins	› All CPUs › All Peripherals › SCU › Port pins in reset › RAMs: - Dcache invalid - Pcache invalid
Warm Power-On Reset				
System Reset				
Application Reset				
SW Module Reset	Available for all CPUs, DMA channel, QSPI, CAN, ASCLIN, Ethernet, GTM, SENT, ADC, HSSL, CCU6...			
Debug Reset	OCDS and MCDS reset, all CPUs and peripherals (except SCU) are put into reset			



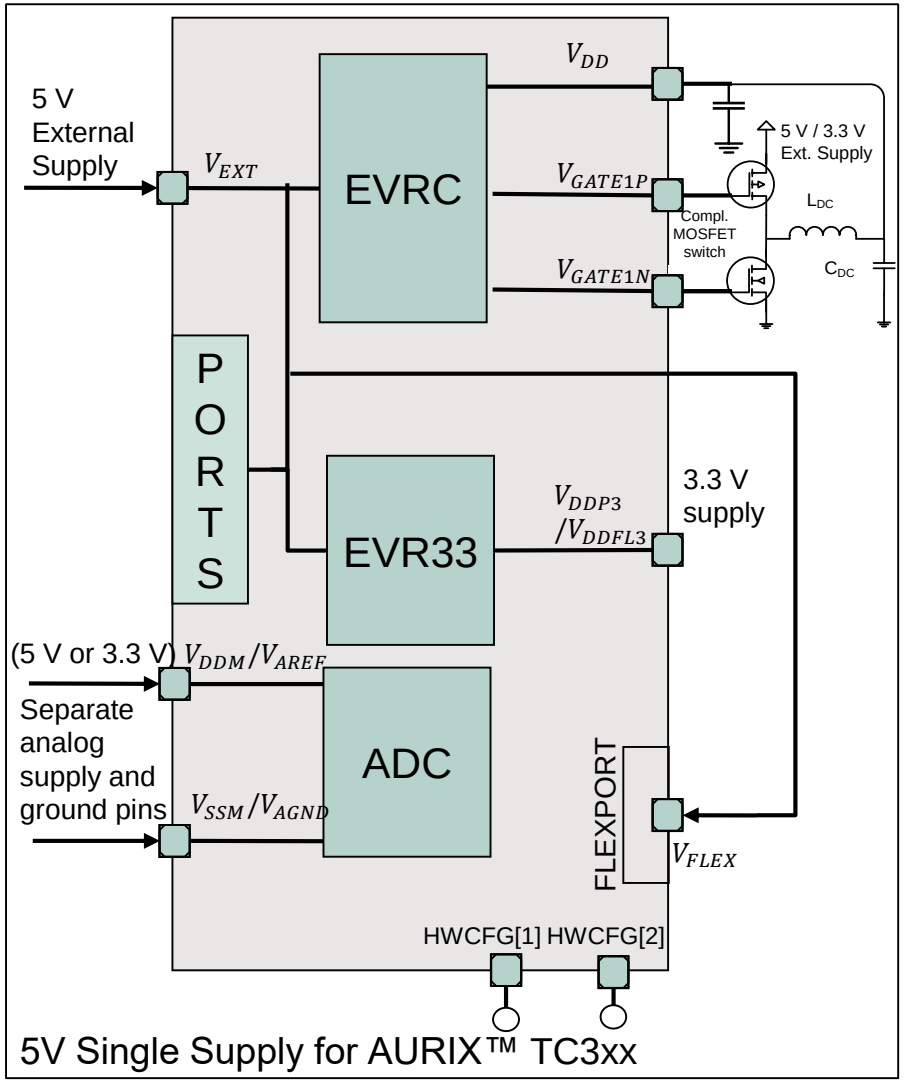
SCU
RCU – Reset types and sources

Reset Type	Source of reset
Cold Power-on Reset	› Startup › Temporary power fail on any of the 3 supplies (VEXT< 3.0 V; VDDP3 <3.0V; VDD < 1.125 V)
Warm Power-on Reset	› PORST pad asserted
System Reset	› ESR0/ESR1 › SMU › STMx › Watchdog (SMU) › Software reset
Application Reset	› ESR0/ESR1 › SMU › STMx › Software reset › Tuning protection
SW Module Reset	› Configurable by registers
Debug Reset	› OCDS request trigger › JTAG reset



SCU
PMC – Single source power supply concept

- AURIX™ devices support different supply modes:
  - Single 5 V source supply
  - Single 3.3 V source supply
  - Dual supply modes
- AURIX™ contains 2 separate parallel Embedded Voltage Regulators (EVR33 and EVRC) generating 3.3 V and 1.3 V supply voltages from the external supply
- All supply and generated voltages are monitored internally against overshoot and brownout conditions based on programmable thresholds
- The reaction to these situations is triggering either a cold Power-On Reset or an alarm
- This approach reduces the complexity of the system, since additional regulators are not needed to obtain the 3.3 V or 1.3 V voltages



5V Single Supply for AURIX™ TC3xx

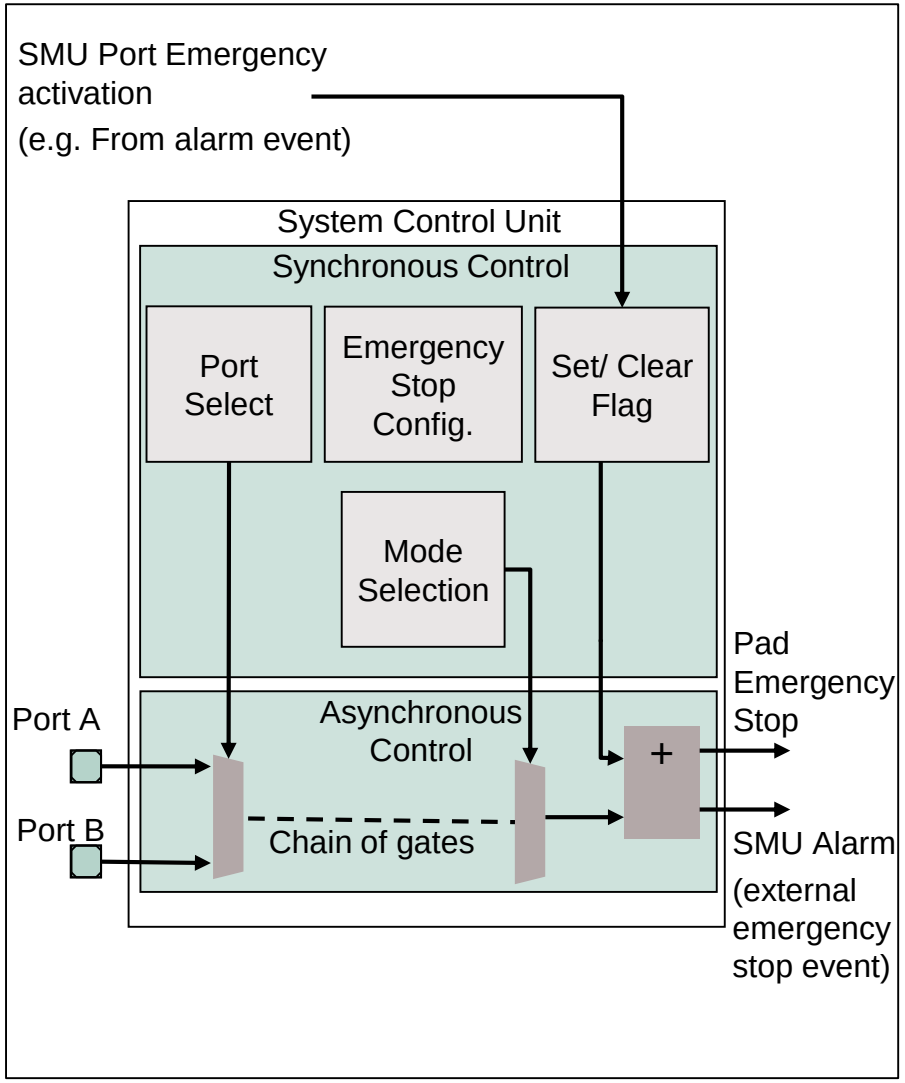
SCU
PMC – Idle, Sleep & Standby modes

- The power management scheme allows activation of power down modes so that the system operates with the minimum required power for the corresponding application state
- A progressive reduction in power consumption is achieved by invoking Idle, Sleep or Standby modes
- The Idle mode is specific to each individual CPU, while the Sleep and Standby modes influence the complete system

Mode/Current	Description	Entry/Exit
CPUx Run	Normal operation	-
CPUx Idle	The CPU clock is disabled. All peripherals remain active.	Entry: via Software, SMU Exit: on CPUx Interrupt, Trap, Reset
System Sleep	Peripheral clocks are gated if configured by control registers. All CPUs are set to IDLE	Entry: via Software Exit: on CPUx Interrupt, Trap, Reset
System Standby	Main domain is powered off. Standby RAM may be active	Entry: via Software, NMI Exit: on edge detection on NMI/pins, PORST assertion In case of separate standby supply pin: entry & exit are done on the VEXT supply ramp-down, respectively ramp-up

SCU
Emergency Stop

- The emergency stop feature provides a fast reaction to an emergency event without the intervention of the software. As reaction to the emergency event, selected output ports can be immediately placed into a defined state (e.g. bring the actuators in a known state)
- An emergency stop can be triggered by the following:
  - A transition on the port which is configured as the Emergency Stop input
  - An alarm event or command from the Safety Management Unit that is configured to generate a port emergency stop
- The emergency stop control logic for the ports operates in two modes:
  - Synchronous mode (default): the emergency case is activated by hardware and released by software
  - Asynchronous mode: both the activation and releasing of the emergency case are done by hardware



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