Customer Training Workshop
Traveo™ II Device Power Modes

Q4 2020

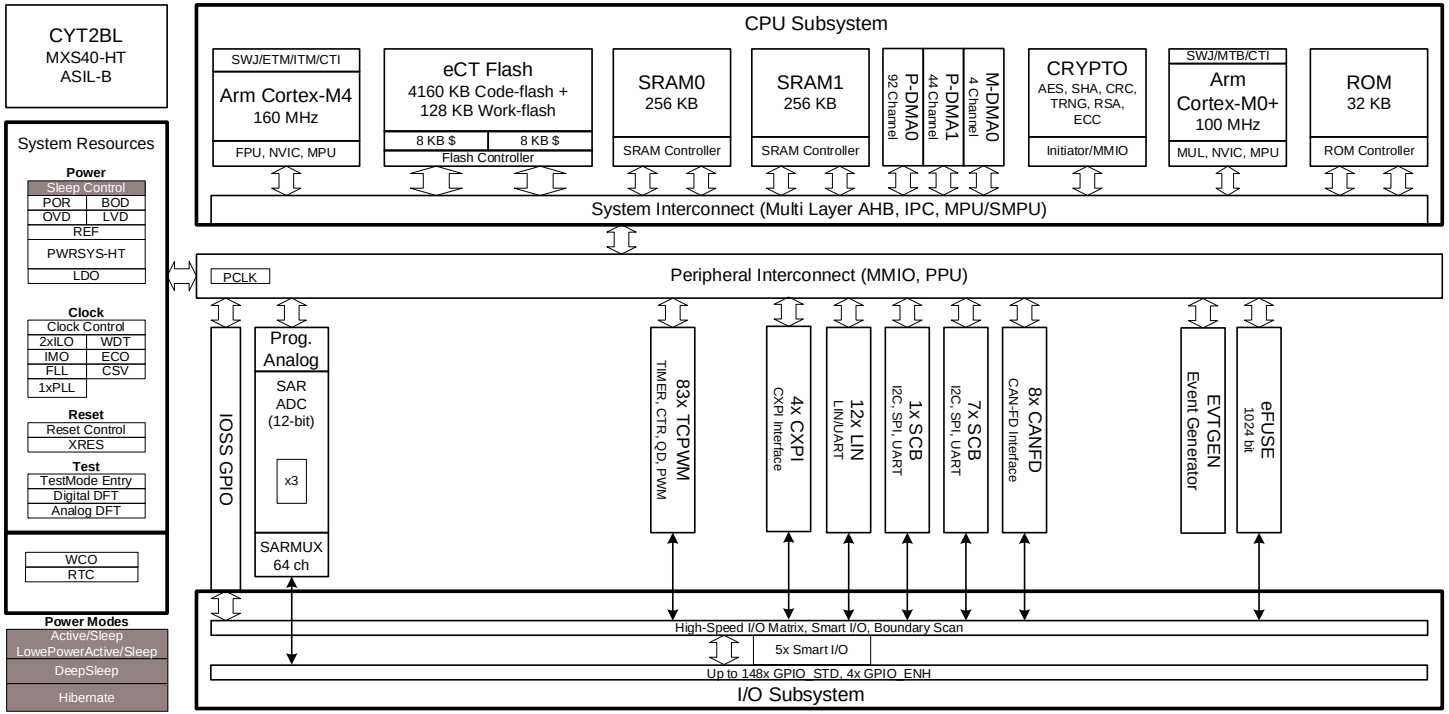
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160KB
Traveo II Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Body Controller Entry

› Device power modes are controlled by sleep control in System Resources

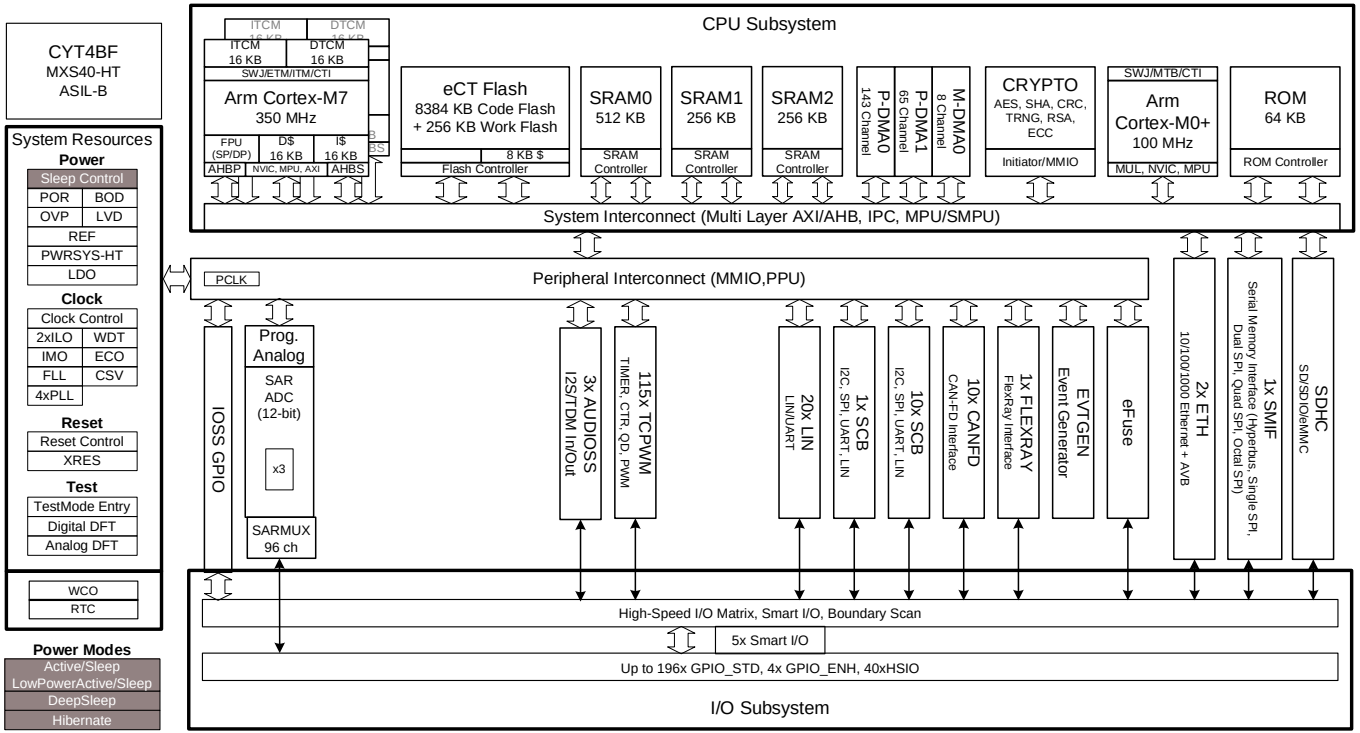


Hint Bar

Review TRM chapter 17 for additional details

Introduction to Traveo II Body Controller High

› Device power modes are controlled by sleep control in System Resources



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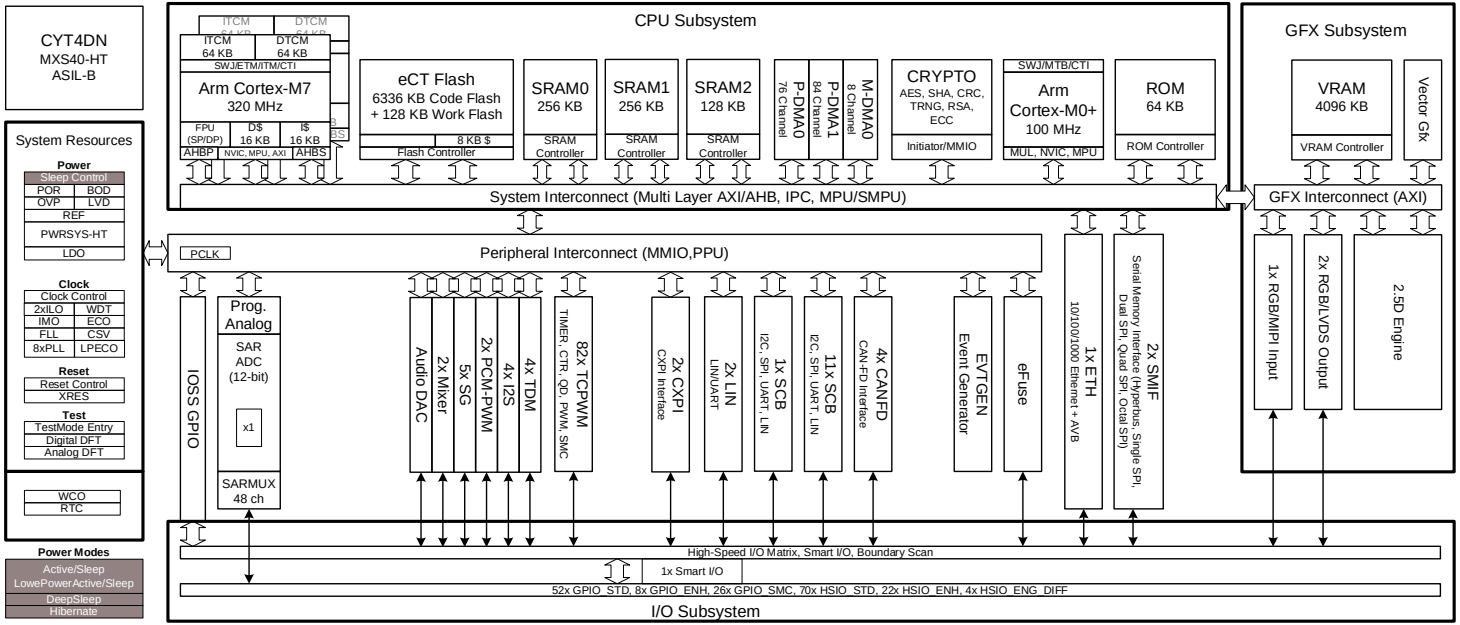
Review TRM chapter 17 for additional details

Introduction to Traveo II Cluster

› Device power modes are controlled by sleep control in System Resources



Hint Bar

Review TRM chapter 17 for additional details

Device Power Modes

- Overview
  - Traveo II supports the following power modes:
    - Active mode (high power consumption)
    - Sleep mode (medium/high power consumption)
    - DeepSleep mode (medium/low power consumption)
    - Hibernate mode (low power consumption)
- Advantage
  - Supported device power modes optimize power consumption for user applications

Hint Bar

Review TRM chapter 17 for additional details

Power Modes

Active mode

- The device enters Active mode upon any device reset
- All the logic, memory, and peripherals are available
- The software can decide to enable or disable specific peripherals and power domains

	Component	State	Component	State
Core Function	CPU	On	High-speed clock (IMO/ECO/PLL)	On
	P-DMA/M-DMA	On	ILO/WCO/LPECO[1]	On
	SRAM	On	Power-on-Reset (POR)	On
	Flash	On	LVD/BOD/OVD/OCD	On
	CSV	On	-	-
Peripherals	ADC	On	RTC	On
	TCPWM	On	SCB	On
	GPIO	On	LIN	On
	EVTGEN	On	M_TTCAN	On
	WDT/MCWDT	On	Others	On

Hint Bar

Review the Device Power Modes TRM chapter for additional details

In Active mode, power consumption can be reduced using software control (such as clock settings and power on/off). The software setting is available in the low-power profiles (LPACTIVE)

Refer to the datasheet for the current consumption details

[1] See the device-specific datasheet to check if LPECO is supported.

Power Modes

Sleep mode

- The CPU clock is turned off and the CPU enters Sleep mode
- All other peripherals are available
- Any peripheral interrupt can wake up the CPU in Active mode

	Component	State	Component	State
Core Function	CPU	Sleep	High-speed clock (IMO/ECO/PLL)	On
	P-DMA/M-DMA	On	ILO/WCO/LPECO[1]	On
	SRAM	On	Power-on-Reset (POR)	On
	Flash	On	LVD/BOD/OVD/OCD	On
	CSV	On	-	-
Peripherals	ADC	On	RTC	On
	TCPWM	On	SCB	On
	GPIO	On	LIN	On
	EVTGEN	On	M_TTCAN	On
	WDT/MCWDT[2]	On	Others	On

Hint Bar

Review the Device Power Modes TRM chapter for additional details

In Sleep mode, power consumption can be reduced using software control (such as clock settings and power on/off). The software setting is available in the low-power profiles (LPSLEEP)

Refer to the datasheet for the current consumption details

[1] See the device-specific datasheet to check if LPECO is supported.
[2] WDT/MCWDT operation can be disabled before switching to low-power mode. If WDT/MCWDT is used in low-power mode, CPU must wake up to clear the WDT/MCWDT

Power Modes

DeepSleep mode

- Only low-frequency peripherals are available
- SRAM data is retained[1]
- LVD/BOD/OVD/OCD monitors power lines in low-power mode

	Component	State	Component	State
Core Function	CPU	Retention[3]	High-speed clock (IMO/ECO/PLL)	Off
	P-DMA/M-DMA	Retention[3]	ILO/WCO/LPECO[2]	On
	SRAM	Retention[3]	Power-on-Reset (POR)	On
	Flash	Off	LVD/BOD/OVD/OCD	On
	CSV	On	-	-
Peripherals	ADC	Retention[3]	RTC	On
	TCPWM	Off	SCB	On (only 0ch)
	GPIO	On/Freeze	LIN	Retention[3]
	EVTGEN	On	M_TTCAN	Retention[3]
	WDT/MCWDT[4]	On	Others	Retention[3]

Hint Bar

Review the Device Power Modes TRM chapter for additional details

Specific peripheral (WDT, RTC, EVTGEN, SCB#0, and GPIO) interrupts can wake up the CPU to Active mode

In Debug mode, an attempt to enter DeepSleep results in a transition to Sleep mode instead, with all power and clocks active. Upon terminating the debug session, the device will automatically transition to DeepSleep mode

Refer to the datasheet for the current consumption details

[1] This is not retained by default. It must be configured by software
[2] See the device-specific datasheet to check if LPECO is supported.
[3] Specific registers of CPU, DMA, and peripherals are retained while other parts are powered off
[4] WDT/MCWDT operation can be disabled before switching to low-power mode. If WDT/MCWDT is used in low-power mode, CPU must wake up to clear WDT/MCWDT

Power Modes

Hibernate mode

- I/O states, RTC, WDT, and POR are retained; everything else is off
- Device resets on wakeup
- Wakeup event: RTC or GPIO (up to 4 pins[1]) or WDT

	Component	State	Component	State
Core Function	CPU	Off	High-speed clock (IMO/ECO/PLL)	Off
	P-DMA/M-DMA	Off	ILO/WCO/LPECO[2]	On
	SRAM	Off	Power-on-Reset (POR)	On
	Flash	Off	LVD/BOD/OVD/OCD	Off
	CSV[3]	On	-	-
Peripherals	ADC	Off	RTC	On
	TCPWM	Off	SCB	Off
	GPIO	Freeze[4]	LIN	Off
	EVTGEN	Off	M_TTCAN	Off
	WDT/MCWDT[5]	On (only WDT)	Others	Off

[1] In the Traveo II device, only two pins support this wakeup functionality. The datasheet contains additional details
[2] See the device-specific datasheet to check if LPECO is supported.
[3] See the device-specific datasheet to check if CSV function is available in Hibernate mode.
[4] The I/O state must be frozen before going into Hibernate mode and unfrozen after Reset, to complete the transition to Active mode
[5] WDT/MCWDT operation can be disabled before switching to low-power mode. If WDT/MCWDT is used in low-power mode, CPU must wake up to clear WDT/MCWDT

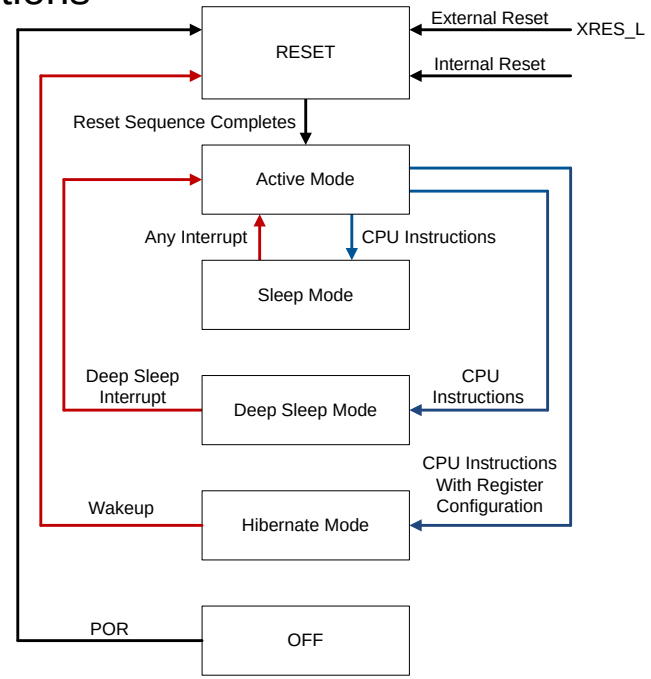
Hint Bar

Review the Device Power Modes TRM chapter for additional details

Refer to the datasheet for the current consumption details

Power Mode Transitions

- Device state and low-power mode transitions
  - RESET/OFF state transitions
  - Low-power mode transitions
    - Sleep mode
    - DeepSleep mode
    - Hibernate mode



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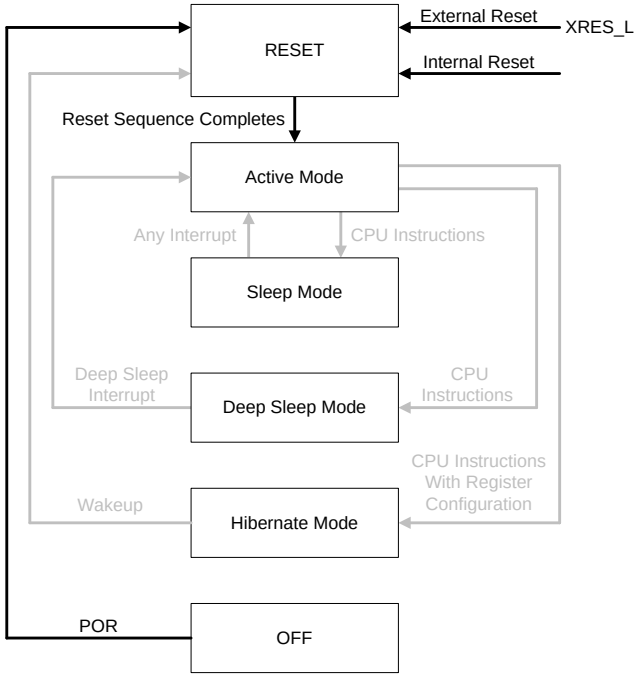
Review the Device Power Modes TRM chapter for additional details

Power Mode Transitions

- RESET/OFF state transitions
  - OFF state:
    - Represents the state with no power applied
    - Goes to RESET when power-up is above POR level (POR event)
  - RESET state:
    - Detects reset event − POR, external reset, internal reset[1]
    - Goes to Active mode after reset sequence completion
    - Starts IMO
  - Assertion of XRES_L during any of the power modes will transition device to RESET



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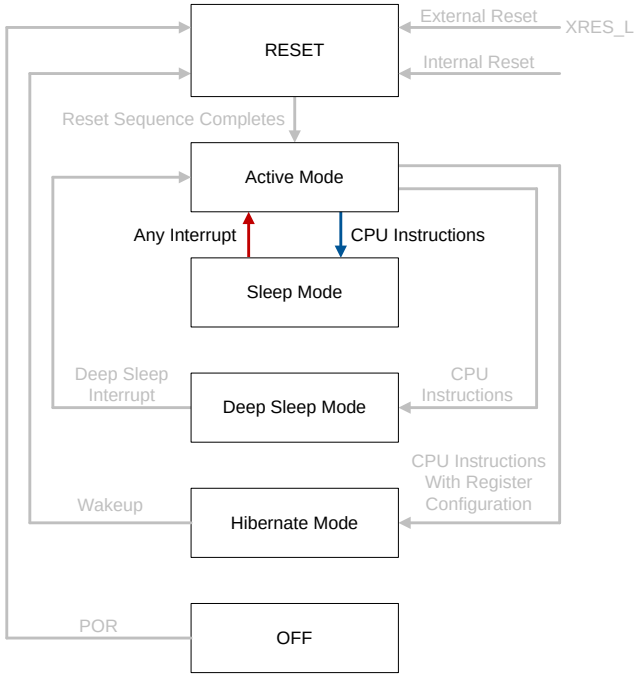
Review the Device Power Modes TRM chapter for additional details

Review the Reset Sources training section for additional details

[1] Internal reset refers to reset by all factors except external reset (XRES_L)

Power Mode Transitions

- Sleep mode transitions
  - Enter Sleep mode[1]
    - Set the interrupt controller for application-specific wakeup interrupt
    - Clear the SLEEPDEEP in SCR[2] register of both CPUs
    - Execute WFI[3] instruction on both CPUs
  - Wakeup
    - Wakeup of application-specific interrupt occurs
    - CPU goes from Sleep mode to Active mode and executes interrupt handler



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Review the Device Power Modes TRM chapter for additional details

Arm® provides additional supporting material on their webpage: infocenter.arm.com

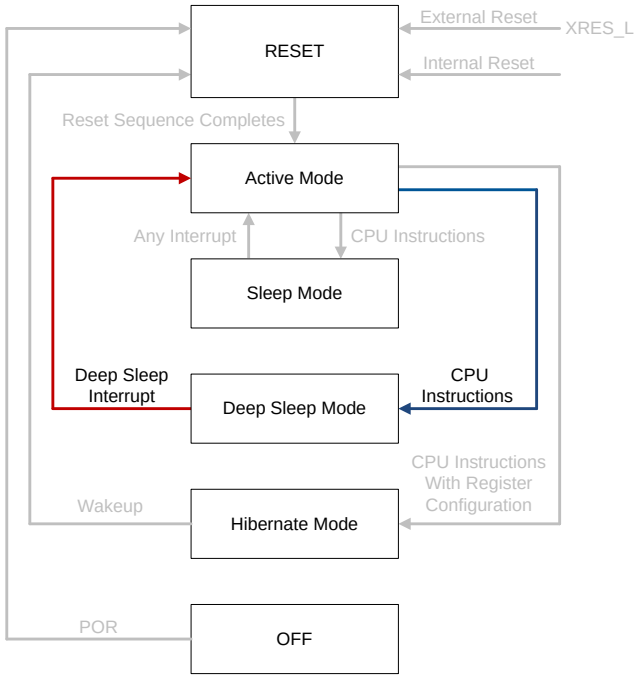
When transitioning from Active mode to Sleep mode, the LPACTIVE profile is inherited

When transitioning from Sleep mode to Active mode, the LPSLEEP profile is inherited

[1] Device will enter Sleep mode only when both cores are in sleep state
[2] The SCR register is CPU-specific
[3] Wait for interrupt. Forces processor to suspend execution until Interrupt events

Power Mode Transitions

- DeepSleep mode transitions
  - Enter DeepSleep mode
    - Check if low-power functions are ready[1]
    - Set the wakeup interrupt controller (WIC)
      for application-specific wakeup interrupt
    - Set the SLEEPDEEP in the SCR register of both CPUs
    - Execute WFI instructions on both CPUs
  - Wakeup
    - Wakeup interrupt from DeepSleep peripherals or GPIOs
    - Device transitions to Active mode
    - CPU exits DeepSleep mode and executes interrupt handler



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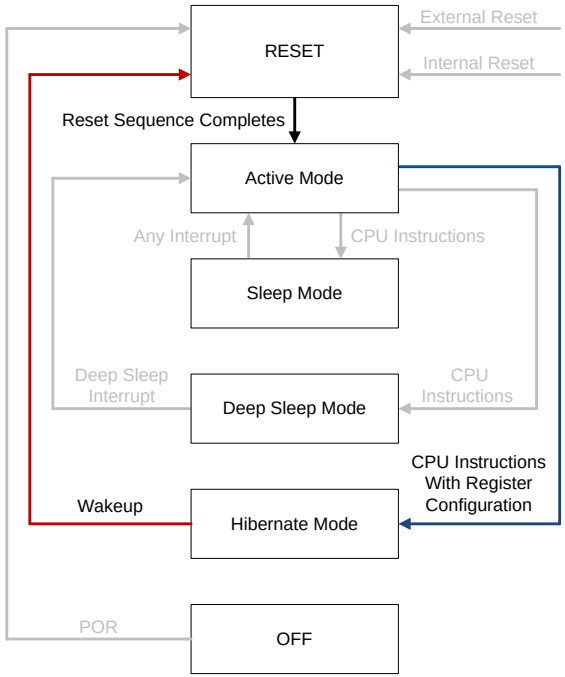
Review the Device Power Modes TRM chapter for additional details

If an attempt is made to transition to DeepSleep mode while low-power circuits are not ready or the debugger is connected, the device will enter Sleep mode temporarily and automatically transition to DeepSleep mode when both conditions are satisfied

[1] Review the Register TRM for additional PWR_CTL.LPM_READY details

Power Mode Transitions

- Hibernate mode transitions
  - Enter Hibernate mode
    - Set the PWR_HIBERNATE[1] and PWR_HIB_DATA[1] registers based on the wakeup requirement
    - Set the FREEZE bit [17] of PWR_HIBERNATE register to freeze the I/O pins
    - Set the HIBERNATE bit [31] of PWR_HIBERNATE register to enter Hibernate mode
    - Read the PWR_HIBERNATE register to make sure that the write has taken effect
    - Execute WFI instruction on both CPUs
  - Wakeup
    - Wakeup event from RTC, designated GPIOs, or WDT
    - Goes to RESET state
    - Transitions to Active mode after reset sequence completion[2]



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Review the Device Power Modes TRM chapter for additional details

Traveo II offers four 32-bit registers in the backup domain to hold the data during Hibernate mode

[1] The Register TRM provides additional details of PWR_HIBERNATE and PWR_HIB_DATA
[2] Unfreeze the I/Os after reaching Active state to complete transition

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6141414	04/25/2018	Initial release
*A	6360852	10/23/2018	Added page 2 Updated pages 3, 4, 5, 6, 7, 8, 10, 13, and 15
*B	6678067	09/24/2019	Added page 5 Updated page 2 to 4, 6, 7, 9, 10, 12, 13, 14, 15, and 16 - Deleted CYT2B5 series - Changed from “Deep Sleep” to “DeepSleep” - Changed from “XRES” to “XRES_L” - Changed “Execute WFI instructions on all CPUs” to “Execute WFI instructions on both CPUs
*C	6825785	03/06/2020	Updated pages: 6 to 15 - Change to SRAM from System SRAM: 7 to 10 - Change to M_TTCAN from CAN: 7 to 10 - Updated the Hint Bar comments: 6 to 15 - Updated figures for better view: 11 to 15
*D	7041467	12/10/2020	Page 2: Added the new products Page 3 to 5: Changed to new block diagram. Page t to 10: Added the LPECO and CSV to table. Page 10 and 15: Added the WDT to wakeup event factors.