

I2C

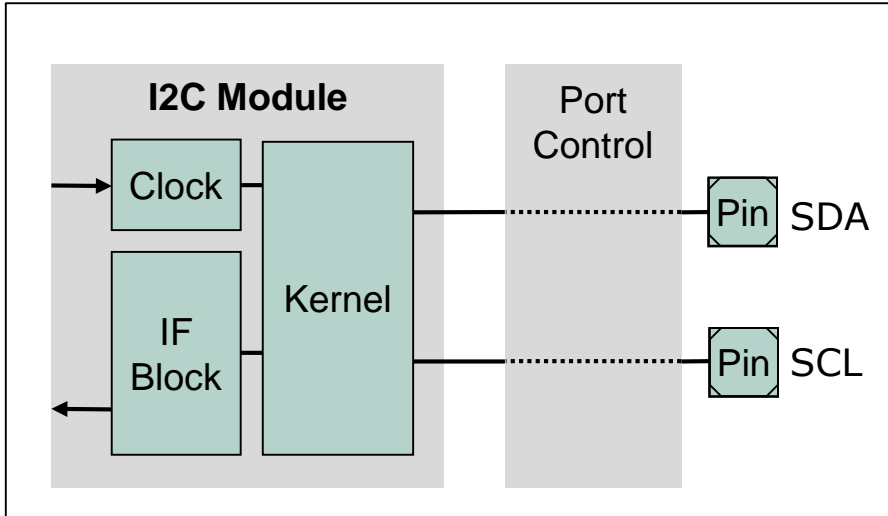
Inter-Integrated Circuit Module

AURIX™ TC3xx Microcontroller Training
V1.0 2020-06



I2C

Inter-Integrated Circuit Module



Highlights

- > 2-wire communication in multi-master mode, master mode and slave mode
- > Supporting all speed grades including High-speed mode with up to 3.4 Mbit/s
- > Fully compatible with I2C-bus specification version 2.1.

Key Features

Automatic execution of low-level tasks

FIFO operation

Customer Benefits

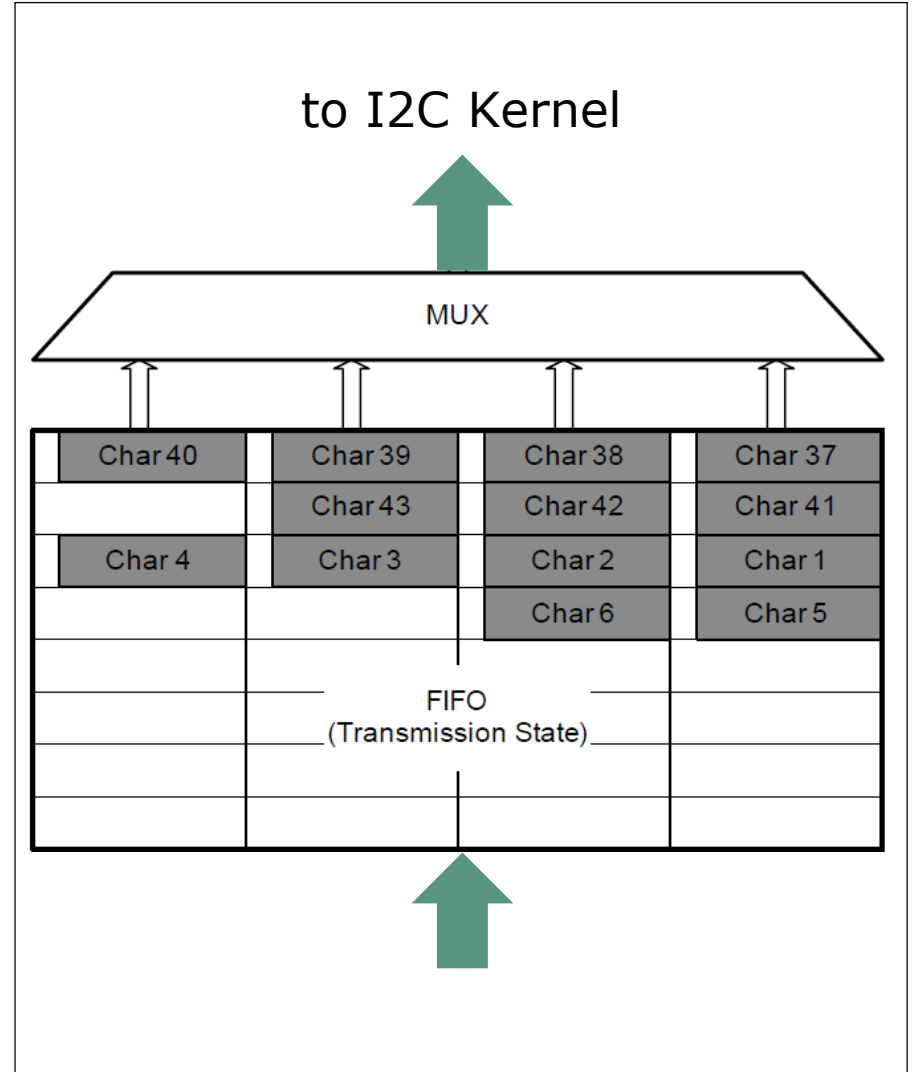
- > Off-loading CPU from I2C specific tasks
- > Allows reading and writing of multiple bytes without software intervention

Automatic execution of low-level tasks

- › Serialization/de-serialization of the I2C bus data
- › Generation/detection of start and stop signal
- › Generation/detection of acknowledge signal
- › Bus state detection
- › Bus access arbitration in multi-master mode
- › Recognition of device address in slave mode
- › Configurable detection of general call address
- › Configurable repeated start in master mode

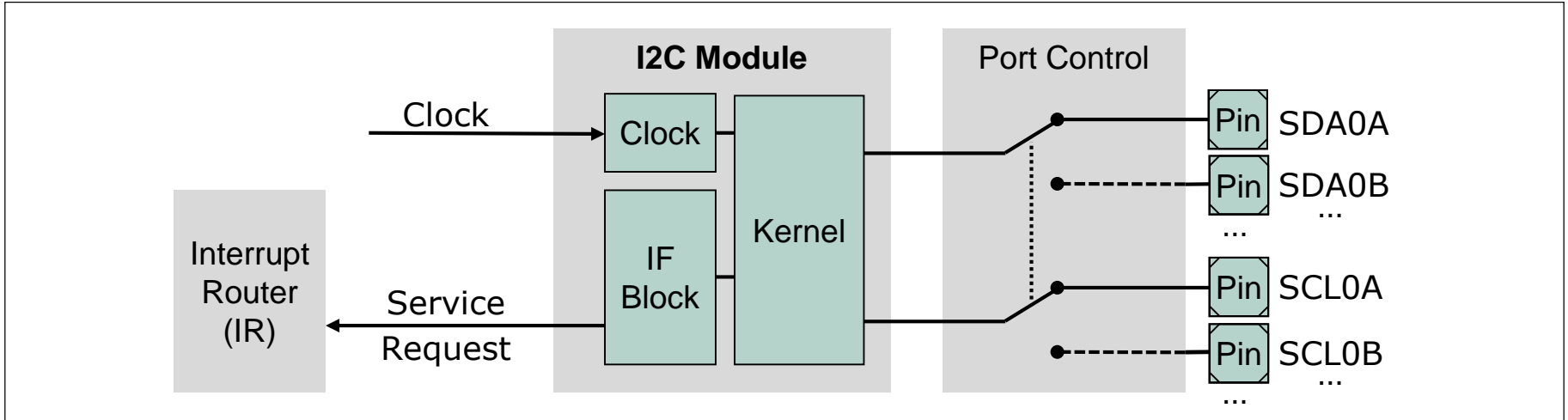
I2C FIFO Operation

- > The picture on the right shows a byte aligned FIFO, keeping two transmit packets
- > The 1st packet is currently being transmitted by the I2C kernel. Characters 37-40 will be transmitted next. Char43 is the last character
- > The 2nd packet consist of 6 characters, waiting to be transmitted
- > FIFO can be filled by continuous write access to a 32-bit register via software or DMA
- > FIFO also supports half-word (16-bit) or word aligned (32-bit) characters



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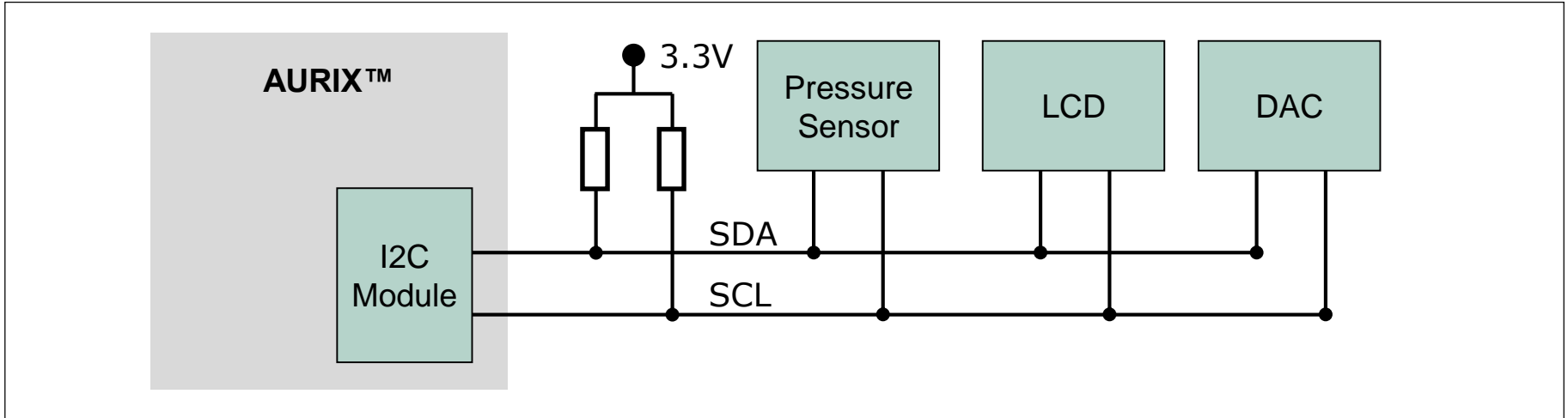
System integration



- › Several I2C service requests can be routed to the Interrupt Router (IR)
 - Service requests for FIFO handling
 - I2C protocol specific requests e.g. “Transmission End Request”
 - Error service requests e.g. FIFO full or empty
- › The external I2C lines SDA and SCL can be connected to one out of several port pin pairs

Application example

AURIX™ with 3 slave devices



Overview

- › AURIX is the I2C bus master, the other devices acting as I2C bus slaves
- › The master always provides the clock signal at SCL and starts the transmission by addressing a slave
- › Each slave has an unique slave address

Advantages

- › Communication (read/write) with many different external devices consumes only 2 pins for the data line (SDA) and clock line (SCL)

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Document reference

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