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AN2011-05 Industrial IGBT Modules
Explanation of Technical Information

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AN 2011-05

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- Update of Paragraph 3.7
- Update of Paragraph 6.3
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1 Abstract

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This Application Note is intended to provide an explanation of the parameters and diagrams given in the datasheet of industrial IGBT modules. With the Application Note, the designer of power electronic systems, requiring an IGBT module, is able to use the datasheet in a proper way and will be provided with background information.

2 Introduction

The parameters listed in the datasheet are values that describe the characteristics of the module as detailed as possible.

With this information, the designer should be able to compare devices from different suppliers to each other. Furthermore, the information should be sufficient to figure out the limits of the device.

This document explains the interaction between the parameters and the influence of conditions like temperature. Datasheet values that refer to dynamical characterization tests, e.g. switching losses, are related to a specific test setup with its individual characteristics. Therefore, these values can deviate from a user's application.

The attached diagrams, tables and explanations are referring to the datasheet of a FS200R07N3E4R_B11 rev.2.0 from 2011-04-06 as an example. The values and characteristics shown are not necessarily feasible to be used for design-in activities. For the latest version of datasheets please refer to our website.

Infineon's datasheets of IGBT power modules are structured as listed below:

- Summarized device description on the front page as shown in Figure 1
- Maximum rated electrical values of IGBT-chips
- Recommended electrical operating conditions of IGBT-chips
- Maximum rated electrical values of diode-chips
- Recommended electrical operating conditions of diode-chips
- NTC-Thermistor if applicable
- Parameters concerning the overall module
- Operating characteristics
- Circuit diagram
- Package outline
- Terms and conditions of usage

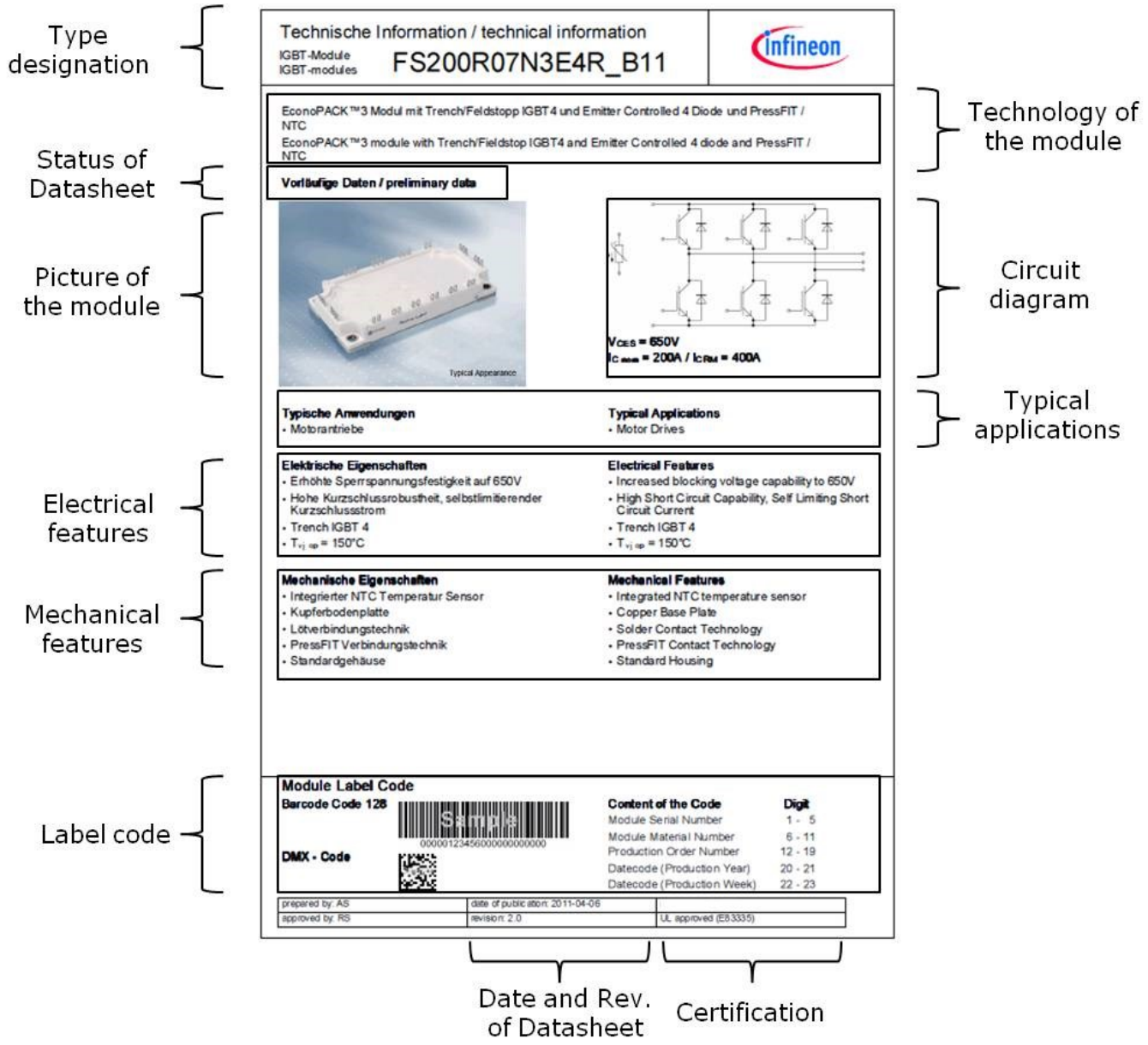


Figure 1: Front page of the datasheet

There are also datasheets for older IGBT modules i.e. BSM100GAL120DLCK, where the front page as shown in Figure 1 does not exist.

2.1 Status of datasheets

Depending on the status of the product development, the relating technical information contains:

- **Target data**

The numbers in these datasheets are target values, which are expected to be achieved. Values from these target datasheets are useful for the initial calculations and approximations. The information and values of a target datasheet cannot be guaranteed for the final product. The dimensioning of an inverter should only be done with values based on a preliminary or final datasheet.

During the development phase, the modules are labeled with their type designation and carry the suffix ENG. Modules with the ENG designation are supplied with a Sample Release Document. Important information can be taken from this additional Sample Release Document, e.g. which values of the module are already fixed and which values can still change during the development phase. ENG module samples are used for preliminary and functional tests during the early stages of a product development phase. Samples marked as ENG are not liable to Product Change Notification (PCN).

- **Preliminary data**

The difference between a preliminary and a final datasheet is, that certain values are still missing, for example the maximum values. These missing values in the preliminary datasheet are marked *to be defined* (t.b.d.).

Modules without ENG on the label reached series production status. All quality requirements are completely fulfilled. If any major change to a module with series production status is necessary, customers must be informed by means of a PCN containing information about the type and extent as well as the time of the changes.

This also applies to modules that have preliminary datasheets.

- **Final data**

The final datasheet is completed with the values which were missing in the preliminary datasheet. Major changes of module characteristics or changes in datasheet values in the series status are accompanied by a PCN.

2.2 Type designation

The first section of the datasheet begins with the type designation of the module as shown in Figure 2.

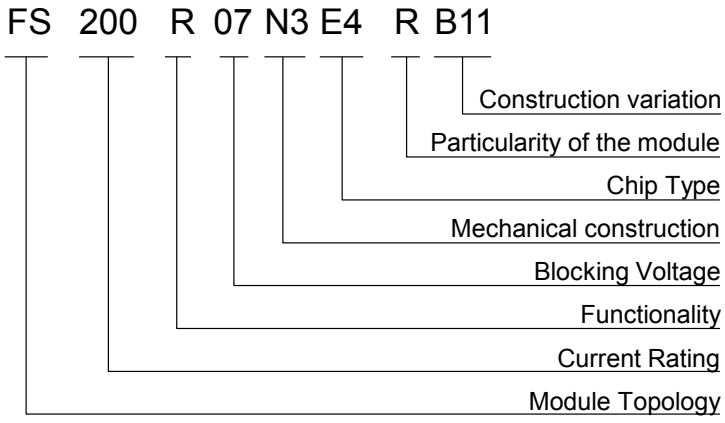


Figure 2: Structure of the type designation

The following tables give a detailed insight to the type designation of Infineon's industrial IGBT Modules.
As an example the FS200R07N3E4R_B11 is chosen.

FS	200	R	07	N	E	4	R	B11	Explanations
FF									Dual switch
FZ									Single switch
FS									3 phase full bridge
FP									Power integrated module
FB									Power integrated module with single phase input rectifier
FM									Matrix converter module
FR									Switched reluctance module
F4									H bridge
F5									Module with 5 switches
FD/ DF									Chopper configuration
DD									Dual diode (for circuit see outline)
F3L									3-Level one leg IGBT module
FS3L									3-level 3 phase bridge
FT									Tripack
	200								Max. DC-collector current
		R							Reverse conducting
		S							Fast diode
		T							Reverse blocking
			06 07 12 17 33 45 65						Collector-emitter-voltage in 100 V 07 denotes 650V
				K					Mechanical construction: module
				H					Package: IHM / IHV B-Series
				I					Package: PrimePACK™
				M					Econo DUAL™
				N1..3					EconoPACK™1..3
				O					EconoPACK™+
				P					EconoPACK™4
				U1..3					Package: Smart 1..3
				V					Easy 750
				W1.. 3					EasyPACK , EasyPIM™ 1..3
					F				Fast switching IGBT chip
					H				High speed IGBT chip
					J				SiC JFET chip
					L				Low Loss IGBT chip
					S				Fast Short tail IGBT chip
					E				Low Sat & fast IGBT chip
					T				Fast trench IGBT
					P				Soft switching trench IGBT
						1..n			Internal reference numbers
							C		With Emitter Controlled-Diode
							D		Higher diode current
							F		With very fast switching diode
							G		Module in big housing
							I		Integrated cooling
							P		Pre-applied thermal interface material
							R		Reduced numbers of pins
							T		Low temperature type
							-K		Design with common cathode
								B1..n	Construction variation
								S1..n	Electrical selection

BSM100GB120DLx as an Example for the old designation

BSM	100	GB	120	DLx	Explanations
BSM					Switch with IGBT and FWD
BYM					Diode module
	100				Max. DC-collector current (A)
		GA			Single switch with one IGBT and FWD
		GB			Half bridge
		GD			3 phase full bridge
		GT			3 single switches and FWD
		GP			Power integrated module B6 / Break / Inverter
		GAL			Chopper module (diode on collector side)
		GAR			Chopper module (diode on emitter side)
		A			Single diode
			120		Collector-emitter-voltage in 10V
				DL	Typ with low V_{CEsat}
				DN2	Fast switching type
				DLC	Low loss type with Emitter Controlled-diode
				S	With collector sense
				G	Design variation
				Exx	Special type

Example for MIPAQ module IFS150B12N3T4

Designation of MIPAQ (Module Integrating Power, Application and Quality)									
I	**FS**	**150**	**B**	**12**	**N3**	**T**	**4**		**Explanations**
I									MIPAQ family
	FF								Dual switch
	FZ								Single switch
	FS								3 phase full bridge
	FT								Tripack
	FP								Power Integrated Module
		150							Max. DC-collector current in A
			B						With current sensor
			S						With digital current measurement
			V						With gate driver and temperature measurement
				12					Collector-emitter-voltage in 100 V
					N1..3				Package: EconoPACK™1..3
					P				Package: EconoPACK™4
					U1..3				Package: Smart1..3
						S			Fast Short tail IGBT chip
						E			Low Sat & fast IGBT chip
						T			Thin IGBT
						P			Soft switching IGBT chip
							1..n		Internal reference numbers
								B1..n	Construction variation
								S1..n	Electrical selection

2.3 Module Label Code

To facilitate the handling of the module from logistic's and traceability point of view, all Infineon IGBT modules are considered as unique and labeled as represented in Figure 3. Each module can be identified with its material number, serial number, date code and lot number. All IGBT modules follow similar rules for labeling and identification. Bar code or DMX codes are given on the modules for automated identification. Test data are stored for eleven years.

Figure 3: Example of Module Label Code

3 Datasheet parameters IGBT

This section explains the electrical properties of the IGBT chip inside the given IGBT module.

If one of these maximum ratings presented in the datasheet is exceeded, it may result in a breakdown of the semiconductor, even if the other ratings are not stressed to their limits. Unless specified to the contrary, the values apply at a temperature of 25°C.

3.1 Collector - emitter voltage V_{CES}

The permissible peak collector - emitter voltage is specified at a junction temperature of 25°C as seen in Figure 4. This value decreases for lower temperatures with a factor of approximately $B_{V_{CES}} \approx 0.1\frac{\%}{K}$.

Kollektor-Emitter-Sperrspannung collector-emitter voltage	T_{vj} = 25°C	V_{CES}	650	V

Figure 4: Collector - emitter voltage of the IGBT

3.2 Total power dissipation P_{tot}

This parameter as shown in Figure 5 describes the maximum feasible power dissipation through the thermal resistance junction to module case R_{thJC}.

Gesamt-Verlustleistung total power dissipation	T_C = 25°C, T_{vj} = 175°C	P_{tot}	600	W

Figure 5: Maximum rating for P_{tot}

The total power dissipation can be calculated in general to be:

$$P_{tot} = \frac{\Delta T}{R_{th}} \quad (1)$$

The considered IGBT module is an EconoPACK™ 3 with a base plate structure. The power dissipation is related to ΔT between junction and case and the thermal resistance R_{thJC} between junction and case as hinted out in equation (2).

$$P_{tot} = \frac{T_{vj} - T_C}{R_{thjc}} \tag{2}$$

At a case temperature of 25°C, the power dissipation is specified as a maximum value of:

$$P_{tot} = \frac{(175 - 25)\,K}{0.25\,\frac{K}{W}} = 600W \tag{3}$$

The power dissipation of the diode chips can be calculated the same way as for the IGBTs, in accordance to equation(2).

3.3 DC Collector Current I_C

Based on the total power dissipation, the maximum permissible collector current rating of a module can be calculated with equation (4). Thus, in order to give a current rating of a module, the corresponding junction and case temperature has to be specified, as shown for example in Figure 6. Please note that current ratings without defined temperature conditions have no technical meaning at all.

$$I_C = \frac{T_{vj} - T_C}{R_{thjc} \cdot V_{CEsat}(I_C, T_{vj})} \tag{4}$$

Since I_C is not known in equation (4), V_{CEsat} @ I_C is also not known, but can be found within a few iterations. The ratings of continuous DC-collector current are calculated using maximum values for V_{CEsat} to ensure the specified current rating, taking component tolerances into account.

Kollektor-Dauergleichstrom DC-collector current	T_C = 60°C, T_{vj} = 175°C	$I_{C\ nom}$	200	A

Figure 6: DC collector current

3.4 Repetitive peak collector current I_{CRM}

The nominal current rating can be exceeded in an application for a short time. This is defined as repetitive peak collector current in the datasheet as can be seen in Figure 7 for the specified pulse duration. In theory, this value can be derived from the feasible power dissipation and the transient thermal impedance Z_{th}, if the duration of the over current condition is defined. However, this theoretical value is not taking any limitations of bond wires, bus-bars or power connectors into account.

Therefore, the datasheet value is quite low compared to a calculated value based on theory, but it specifies a safe operation considering all practical limitations of the power module.

Periodischer Kollektor Spitzenstrom repetitive peak collector current	t_P = 1 ms	I_{CRM}	400	A

Figure 7: Repetitive peak collector current

3.5 Reverse bias safe operating area RBSOA

This parameter describes safe operating conditions at turn-off for the IGBT. The chip can be driven within its specified blocking voltage up to twice its nominal current rating, if the maximum temperature under switching conditions is not exceeded. The safe operating area of the power module is limited due to the module's internal stray inductances and specified at the maximum temperature under switching conditions as shown in Figure 8. With increasing currents, the allowed DC-Link voltage is decreased. Furthermore, this derating strongly depends on system related parameters, like stray inductance of the DC-Link and the current commutation slope during the switching transitions. The DC-Link capacitor is assumed to be ideal for this operating area. The current commutation slope is defined via a specified gate resistance and gate driving voltage. In no event the voltage spike must not exceed the specified voltage of the module at the terminals or at chip level to keep the RBSOA limits.

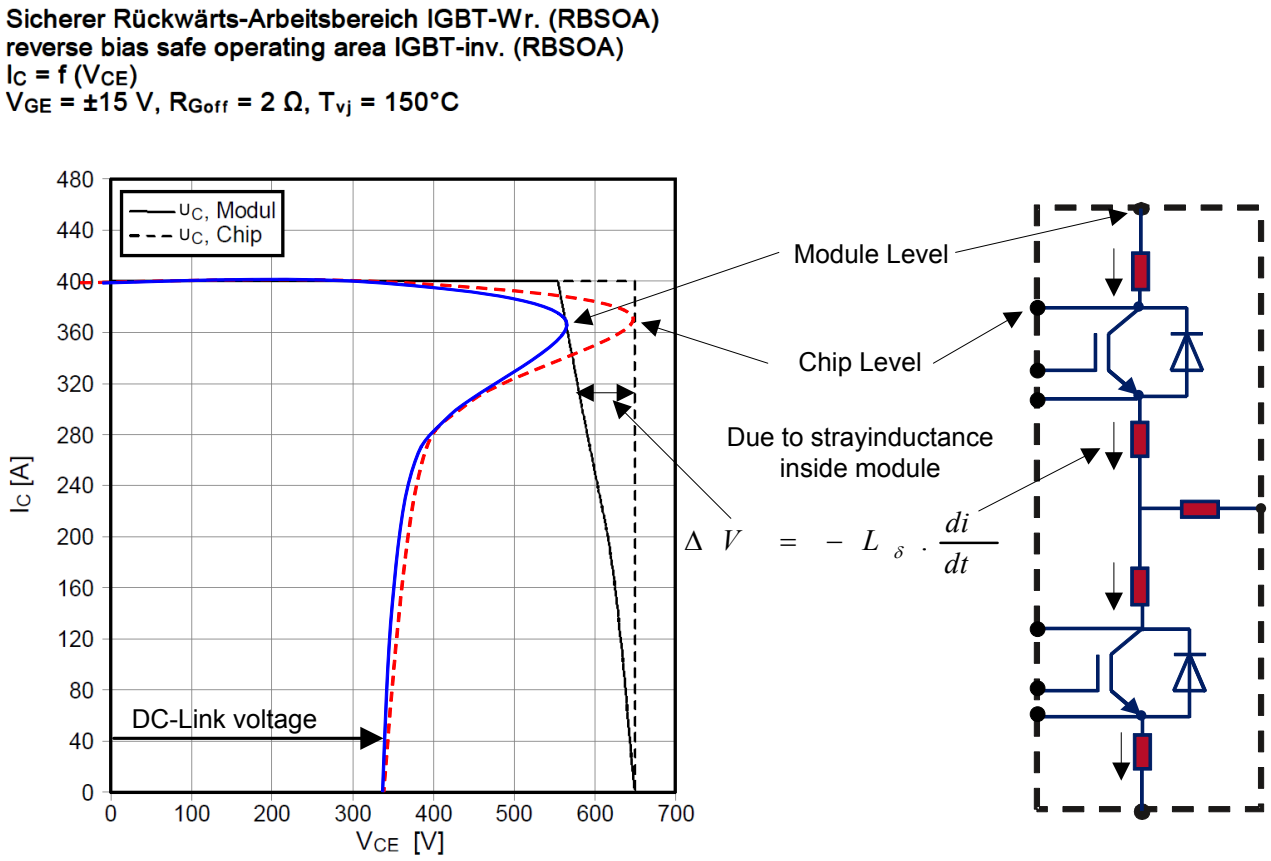


Figure 8: Reverse bias safe operating area

3.6 Typical output and transfer characteristics

This data can be used to calculate conduction losses of the IGBT. In order to contribute to a much better understanding of these parameters, the IGBT device structure as well as it's difference in output characteristic compared to a power MOSFET is discussed briefly. After this, the datasheet parameters of the IGBT module are explained.

Figure 9a shows in detail the structure of a trench-field-stop IGBT with a simplified two-transistor equivalent circuit. The emitter-sided pn-junction of the pnp-transistor resembles the IGBT's collector side. Like a diode it leads to a characteristic voltage drop when the IGBT is conducting current. The intrinsic bipolar transistor of the IGBT is driven by a MOSFET. Therefore, the gate driving characteristic is quite similar to a power MOSFET. The output characteristic is different, which is illustrated in Figure 9b schematically. It shows the characteristic of turned-on devices at two different junction temperatures.

The MOSFET as shown in Figure 9b is reverse conducting for negative drain-source voltages due to its intrinsic body diode. The IGBT has no body diode and thus an anti-parallel diode has to be used, when this

operating mode is required. The advantage is, that the external diode can be optimized independently to suit the IGBT's switching characteristics.

In contrast to the MOSFET, that has an on resistance as a dominant parameter, the IGBT has a forward voltage drop. As a result, at very low load, indicated with 1 in Figure 9b, the MOSFET always has lower conduction losses than an IGBT.

Both output characteristics depend on the junction temperature. The $R_{ds(on)}$ of a MOSFET typically increases by a factor of about two, when the junction temperature increases from 25°C to 150°C. The temperature coefficient of an IGBT's forward voltage is much lower. At low load, the conduction losses even decrease with increasing temperature, due to the lower voltage drop at the pn-junction as represented in Figure 9b. At higher currents, the increase of the ohmic resistance is dominant. Due to this, a parallel connection of several IGBTs is possible and is commonly required for high current IGBT power modules.

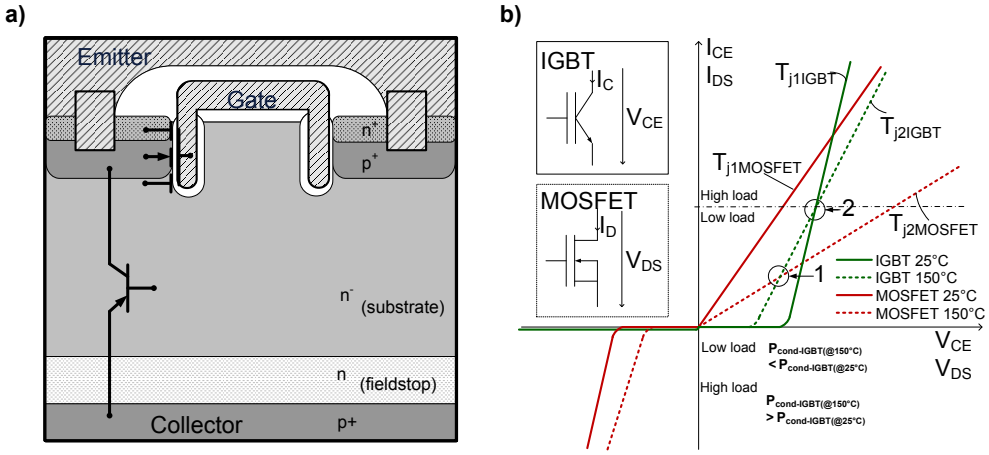


Figure 9: Structure of a Trench-Field-Stop IGBT and two-transistor equivalent circuit (a). Comparison of the output characteristics of power MOSFET and IGBT (b)

The transfer characteristic shows, that the turn-on threshold voltage decreases with increasing junction temperature as seen in Figure 10.

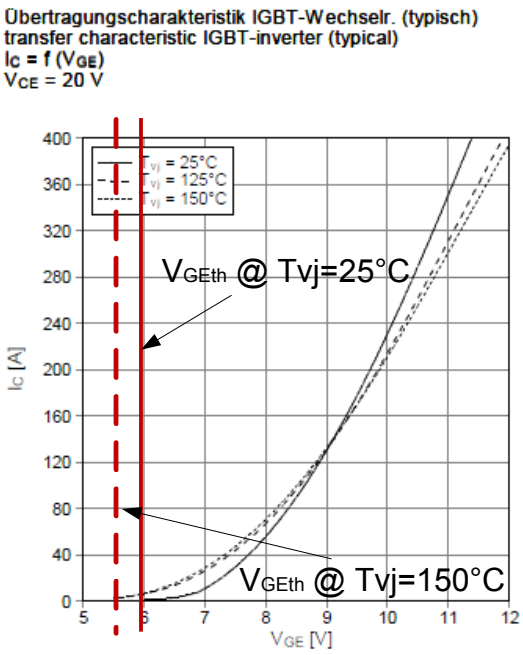


Figure 10: Typical transfer characteristic

As discussed in chapter 3.6, the output characteristic of the IGBT depends on the temperature of the junction. Figure 11a shows the collector current in conducting state as a function of the collector-emitter

voltage at different junction temperatures. For currents lower than about 80A, the conduction losses decrease with increasing temperature. For higher currents, the conduction losses increase slightly. In the case considered, an increase in conduction losses of about 6% at nominal current 200A and a temperature increase from 25°C to 150°C can be observed.

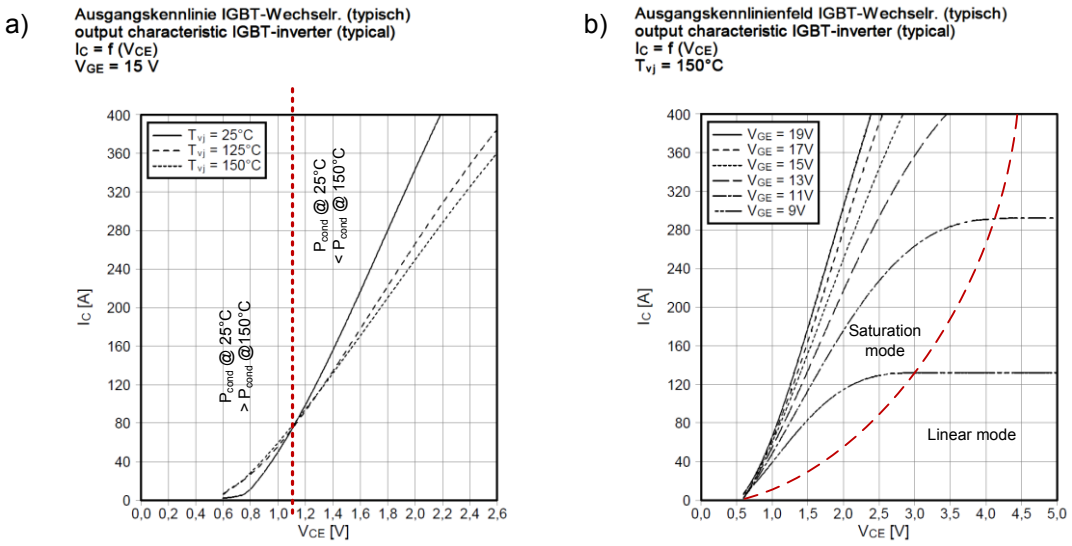


Figure 11: Typical output characteristic as a function of the temperature (a) and gate-emitter voltage variation (b)

Figure 11b shows the typical output characteristic for different gate-emitter voltages. The IGBT should not be operated in linear mode, as this causes excessive conduction losses. If the power dissipation is not limited in magnitude and time, the device might be destroyed. Using 15V as typical gate drive voltage, this linear mode only occurs for short periods at the switching transitions, which is a normal operating condition for the IGBT.

3.7 Parasitic Capacitances

The dynamic characteristics of an IGBT are influenced by several parasitic capacitances. These are inherent parts of the die's internal structure as represented in Figure 12a. A simplified schematic is shown in Figure 12b. The input capacitance C_{ies} and the reverse transfer capacitance C_{res} are the basis for an adequate dimensioning of the gate driver circuit. The output capacitance C_{oss} limits the dV/dt at switching transitions. Losses related to C_{oss} can usually be neglected.

The major parasitic capacitances inside the IGBT die are:

- Input capacitance $C_{ies} = C_{GE} + C_{res}$. C_{GE} includes C_1,C_3,C_4 and C_6.
- Reverse transfer capacitance C_{res} including C_2 and C_5. $C_{res} = C_{CG}$
- Output capacitance C_{ce} represented by C_7. $C_{oss} = C_{CE} + C_{res}$

a) b)

Figure 12: Parasitic capacitances of an IGBT, internal structure a), schematic b)

The values of the parasitic capacitances strongly depend on the operating point of the IGBT. To measure these capacitances with gate- or collector-emitter voltages applied, dedicated measurement circuits according to IEC60747-8 have to be utilized.

Input capacitance C_{ies}

This parameter is determined using the setup in Figure 13. C_{ies} is measured across the gate and emitter connections with collector-emitter connection shorted for AC voltage. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. Capacitors C_1 and C_2 must form an adequate bypass at the test frequency. The inductor L decouples the DC supply.

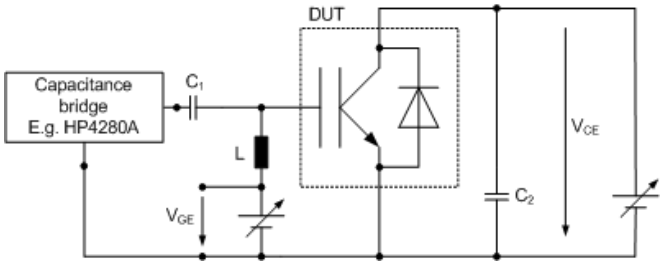


Figure 13: Basic circuit diagram for measuring the input capacitance C_{ies}

Output capacitance C_{oss}

C_{oss} is measured according to the setup in Figure 14. This value is measured across the collector and emitter connections with gate-emitter connections shorted for AC voltage. The values of the DC voltage across the gate-emitter and collector-emitter connections are specified with the test frequency. The capacitors C_1, C_2 and C_3 must form an adequate bypass at the test frequency. The inductor L decouples the DC supply.

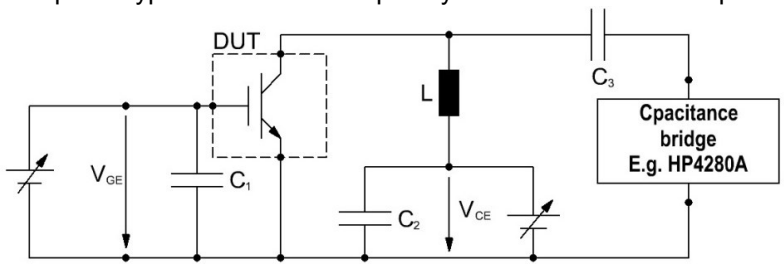


Figure 14: Basic circuit diagram for measuring the output capacitance C_{oss}

Reverse transfer capacitance C_{res}

Figure 15 gives details about the measurement setup for the reverse transfer capacitance. C_{res} is measured across the collector and gate connections, the emitter connection being connected to the protective screen of the bridge. The values of the DC voltage across the gate-emitter connection are specified with the test frequency. Capacitors C_1 and C_2 must form an adequate bypass at the test frequency. The inductors L_1 and L_2 decouple the DC supply.

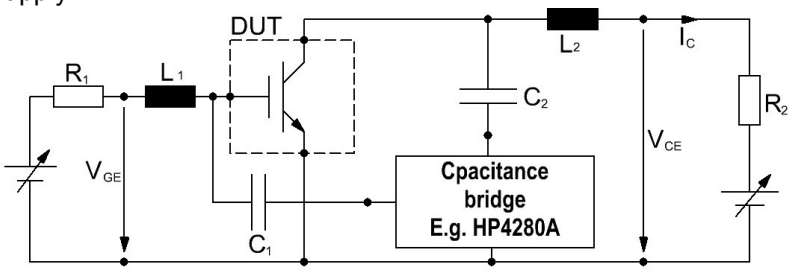


Figure 15: Basic circuit diagram for measuring the reverse transfer capacitance C_{res}

The capacitance meter used for the measurements of C_{ies}, C_{oss} and C_{res} has to be a high resolution capacitance bridge with a sufficient measurement range.

3.8 Gate charge Q_G, gate current, internal and external gate resistor

The value of the gate charge can be used to optimize the design of the gate driver circuit. The average output power that the gate driving circuit has to deliver can be calculated with data of the gate charge, gate driver voltages and switching frequency as given in equation (5).

$$P_{Gdr} = Q_G \cdot \left(V_{GE(on)} - V_{GE(off)}\right) \cdot f_{sw} \qquad (5)$$

Within this formula, Q_G refers to the part of the gate charge that is truly active in the given design. What part is used is depending on the gate driver output voltage; an accurate approximation can be done using the gate charge curve.

The real gate charge Q'_G that has to be taken into account results from the diagram in Figure 16, by choosing the values that correspond to the gate driver's output voltage:

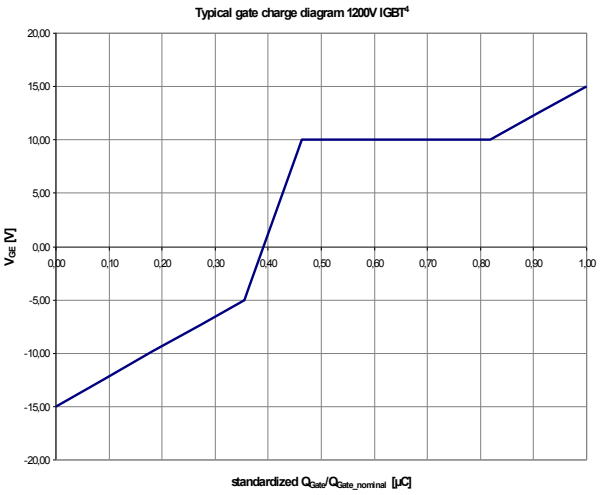


Figure 16: Typical gate charge curve of an 1200V IGBT

Typical values used in industrial applications include designs with a turn-off voltage V_{GE}=0V as well as designs featuring negative supply like V_{GE}=-8V

$Q'_G = 0.62 \cdot Q_G$ for 0V/15V

$Q'_G = 0.75 \cdot Q_G$ for -8V/15V

At a switching frequency of f_{sw}=10 kHz and a driver output voltage of +15/ -8V, the required output power of the gate driving circuit P_{Gdr} can be calculated using the adapted gate charge from Figure 16 and the gate charge as seen in the datasheet Figure 17.

$$P_{Gdr} = 2.15\mu C \cdot 0.75 \cdot (15V + 8V) \cdot 10kHz = 0.37W$$

Gateladung gate charge	V_{GE} = -15 V ... +15 V	Q_G		2,15		µC
Interner Gatewiderstand internal gate resistor	T_{vj} = 25°C	R_{Gint}		2,0		Ω

Figure 17: Gate charge and internal gate resistor

The theoretical gate drive peak current can be calculated according to equation (6), knowing the gate drive voltages and gate resistances. The gate resistor is the sum of external and internal gate drive resistance. Figure 17 shows the value for the internal resistance to be considered.

$$I_{Gdr,peak} = \frac{V_{GE(on)} - V_{GE(off)}}{R_{Gext} + R_{Gint}} \quad (6)$$

In practice, this peak current will not be reached, because it is limited by stray inductances and non-ideal switching transitions of a real gate driving circuit.
The datasheet value given for the internal gate resistor has to be understood as a single resistance and may result from paralleled resistors inside the IGBT module as illustrated in Figure 18. This usually counts for larger modules only, especially medium- and high-power types. These internal resistors lead to improved internal current sharing.
The internal resistance should be considered as one part of total gate resistor to calculate the peak current capability of a driver.

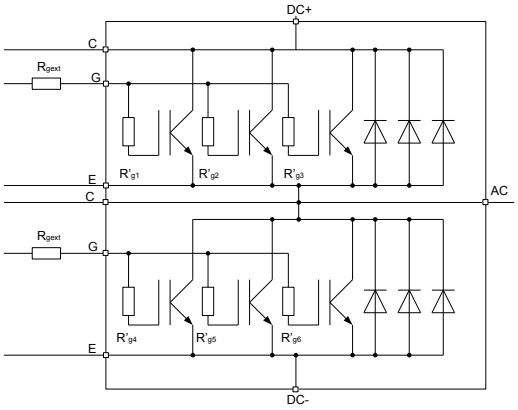


Figure 18: internal gate resistor of the IGBT

The designer can use the external gate resistor to influence the switching performance of the IGBT. Minimum R_{Gon} is limited by turn-on di/dt, minimum R_{Goff} is limited by turn-off dV/dt. Too small gate resistors can cause oscillations and may lead to damage the IGBT or diode. The minimum recommended external gate resistor R_{Gext} is given in the switching losses test conditions as mentioned in Figure 19. The allowed external gate resistor values are shown in the switching loss diagram of Figure 24b.

Einschaltverlustenergie pro Puls turn-on energy loss per pulse	I_C = 200 A, V_{CE} = 300 V, L_S = 30 nH V_{GE} = ±15 V, di/dt = 5700 A/µs (T_{vj}=150°C) R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}	1,10 1,70 2,00		mJ mJ mJ
Abschaltverlustenergie pro Puls turn-off energy loss per pulse	I_C = 200 A, V_{CE} = 300 V, L_S = 30 nH V_{GE} = ±15 V, du/dt = 4000 V/µs (T_{vj}=150°C) R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}	7,90 9,40 9,65		mJ mJ mJ

Figure 19: External gate resistors

3.9 Parasitic turn-on

With the parasitic capacitances of the IGBT, noted in the datasheet as stated in Figure 20, dV/dt induced parasitic turn-on phenomena can occur. The cause of a possible parasitic turn-on is based on the intrinsic capacitive voltage divider between collector-gate and gate-emitter.

In consideration of high voltage transients across collector-emitter, this intrinsic capacitive voltage divider is much faster than an external gate driving circuit that is limited by parasitic inductances. Therefore, even if the gate driver turns off the IGBT with zero gate-emitter voltage, transients of collector-emitter voltage lead to an increase of the gate-emitter voltage. If the gate emitter voltage exceeds the gate threshold voltage V_{GEth}, the

IGBT will turn on. Neglecting the influence of the gate driving circuit, the gate-emitter voltage can be calculated by

$$V_{GE} = \frac{C_{GC}}{C_{GC} + C_{GE}} \cdot \Delta V_{CE} = \frac{C_{res}}{C_{ies}} \cdot \Delta V_{CE} \qquad (7)$$

The quotient C_{res}/C_{ies} should be as low as possible. To avoid a parasitic dV/dt induced turn-on, the quotient C_{ies}/C_{res} for the FS200R07N3E4_B11 is about 35. Furthermore, the input capacitance should be as low as possible to avoid gate driving losses; therefore the use of additional gate-emitter capacitance C_{GE} has to be evaluated carefully.

Eingangskapazität input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V	C_{ies}		13,0		nF
Rückwirkungskapazität reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V	C_{res}		0,38		nF

Figure 20: Parasitic capacitances of the IGBT

The parasitic capacitances are determined under the conditions given in Figure 20. The gate-emitter capacitance C_{GE} as shown in Figure 21 can be approximated to be constant over the collector-emitter voltage as shown in equation (8).

$$C_{GE} \approx C_{ies}(25V) - C_{res}(25V) \qquad (8)$$

The reverse transfer capacitance C_{res} strongly depends on the collector-emitter voltage and can be estimated according to equation (9).

$$C_{res}(V_{CE}) \approx \frac{C_{res}(25V) \cdot \sqrt{25V}}{\sqrt{V_{CE}}} \qquad (9)$$

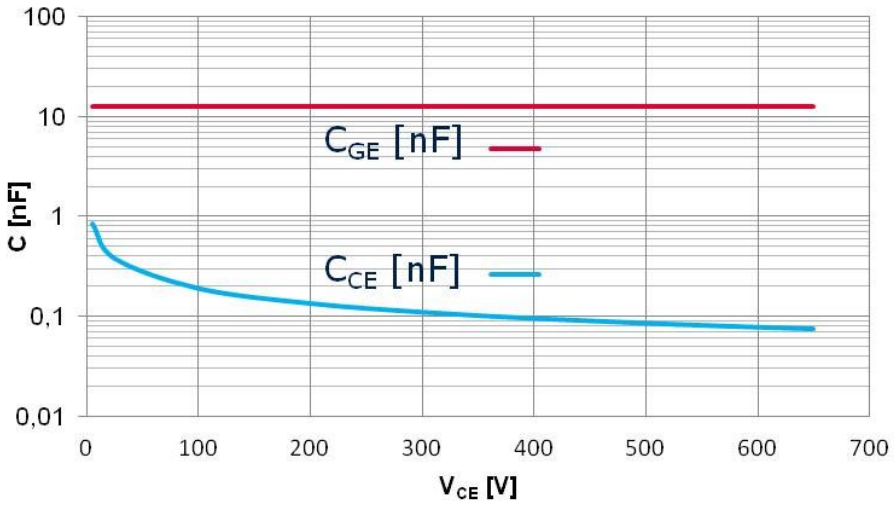


Figure 21: Approximation of C_{GE} and C_{CE} as function of the collector-emitter voltage according to equations (8) and (9)

Consequently, the robustness against dV/dt induced parasitic turn-on increases with the collector-emitter voltage as seen in equation (7).

3.10 Dynamic behavior

The switching characteristic described in the datasheet provides useful information to determine an appropriate dead time between turn-on and turn-off of the complementary devices in a half bridge configuration. For further information about dead time calculation please refer to AN2007-04[1] available at Infineon's website.

- Turn-on delay time t_d on:
  Time it takes from getting the gate-emitter voltage to 10% of the rated value to the moment the collector current reaches 10% of its nominal size
- Rise time t_r:
  Time which the collector current takes to rise from 10% to 90% of its nominal value
- Turn-off delay time $t_{d\,off}$:
  Time necessary from getting the gate-emitter voltage to 90% of the rated value to the moment the collector current reaches 90% of its nominal size
- Fall time t_f:
  Time which the collector current takes to fall from 90% to 10% of his nominal value

The times in the datasheet are defined as detailed in Figure 22:

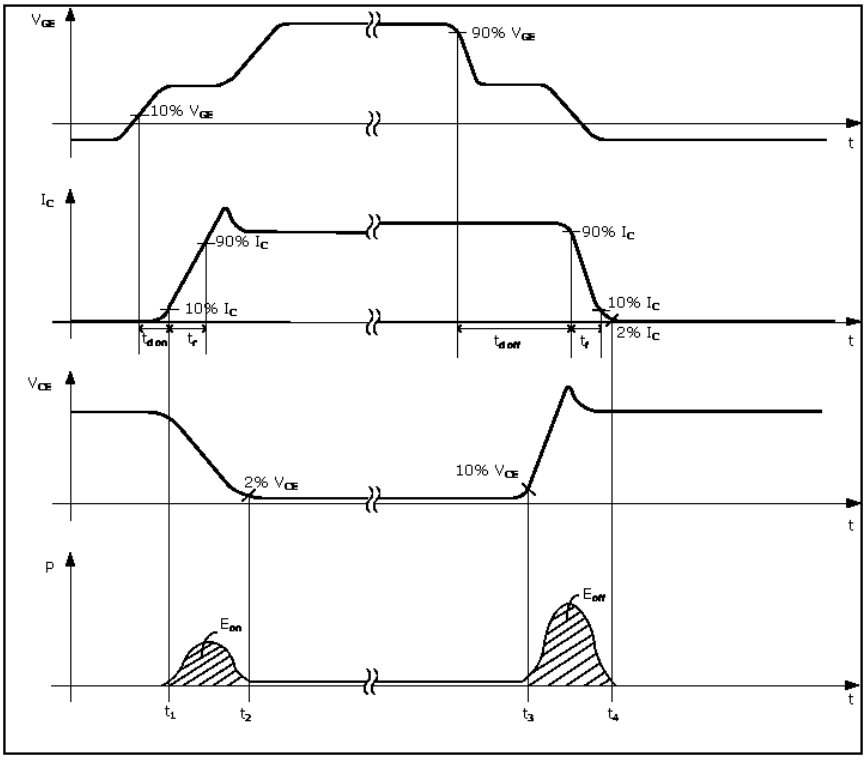


Figure 22: Specification of rise and fall times and conditions to calculate switching losses

[1] Application note 2007-04: How to calculate and minimize the dead time requirement for IGBTs properly.

These times alone will not give reliable information about switching losses, because voltage rise and fall times as well as current tail shape are not specified. Therefore, switching losses per pulse are given separately.

The switching losses per pulse are defined using the integrals:

$$E_{on} = \int_{t_1}^{t_2} U_{CE} \cdot I_C \cdot dt \qquad E_{off} = \int_{t_3}^{t_4} U_{CE} \cdot I_C \cdot dt \tag{10}$$

The integration limits for the switching losses are given in Figure 22:

- E_{on} as turn-on energy per pulse from t_1 to t_2
- E_{off} as turn-off energy per pulse from t_3 to t_4

Dynamic behavior and thus energy per pulse strongly depend on a variety of application specific operating conditions like gate driving circuit, layout, gate resistance, magnitude of voltages and currents to be switched as well as the junction temperature. Therefore, datasheet values can only give an indication for the switching performance of the power module. For more accurate values, detailed simulations taking application specific parameters into account or experimental investigations are necessary.
Typically, switching transition duration and energy per pulse are characterized at nominal operating conditions for different temperatures as noted in Figure 23.

Einschaltverzögerungszeit (ind. Last) turn-on delay time (inductive load)	I_C = 200 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\ on}$	0,15 0,16 0,17	µs µs µs
Anstiegszeit (induktive Last) rise time (inductive load)	I_C = 200 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r	0,03 0,04 0,04	µs µs µs
Abschaltverzögerungszeit (ind. Last) turn-off delay time (inductive load)	I_C = 200 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\ off}$	0,34 0,37 0,38	µs µs µs
Fallzeit (induktive Last) fall time (inductive load)	I_C = 200 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_f	0,06 0,07 0,07	µs µs µs
Einschaltverlustenergie pro Puls turn-on energy loss per pulse	I_C = 200 A, V_{CE} = 300 V, L_S = 30 nH V_{GE} = ±15 V, di/dt = 5700 A/µs (T_{vj}=150°C) R_{Gon} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}	1,10 1,70 2,00	mJ mJ mJ
Abschaltverlustenergie pro Puls turn-off energy loss per pulse	I_C = 200 A, V_{CE} = 300 V, L_S = 30 nH V_{GE} = ±15 V, du/dt = 4000 V/µs (T_{vj}=150°C) R_{Goff} = 2,0 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}	7,90 9,40 9,65	mJ mJ mJ

Figure 23: Switching times and energies

A first estimation of dynamical losses can be done utilizing Figure 24. The diagram hints out typical losses depending on R_G, I_C and junction temperature T_{vj}. The switching loss diagram Figure 24b and Figure 35b shows also the allowed external gate resistor values. The left end of the curves in Fig 24b and Fig 35b specifies the minimum allowed external gate resistor value. The gate resistors must not be lower because this may lead to a destruction of the device.

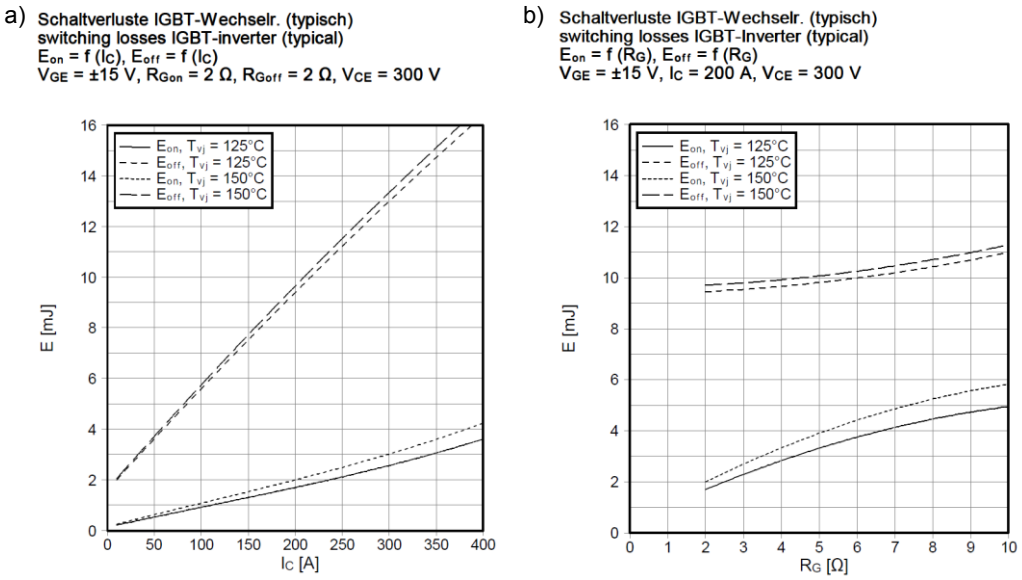


Figure 24: Switching losses per pulse as a function of the collector current and the gate resistance

3.11 Short circuit

The short circuit characteristic strongly depends on application specific parameters like temperature, stray inductances, gate driving circuits and the resistance of the short circuit path. For device characterization, a test setup as drawn in Figure 25a is used. One IGBT is short circuited while the other IGBT is driven with a single pulse. The corresponding typical voltage and current waveforms are illustrated in Figure 25b. The current in the conducting IGBT increases rapidly with a current slope that is depending on parasitic inductances and the DC-Link voltage. Due to desaturation of the IGBT, the current is limited to about 5 times the nominal current in case of IGBT3 and the collector-emitter voltage remains on the high level. The chip temperature increases during this short circuit due to high currents and thus high losses. Because of the increasing chip temperature the current decreases slightly while operating in short circuit condition.
Within a defined short-circuit-withstand time t_{sc} the IGBT has to be switched off to avoid a device failure.

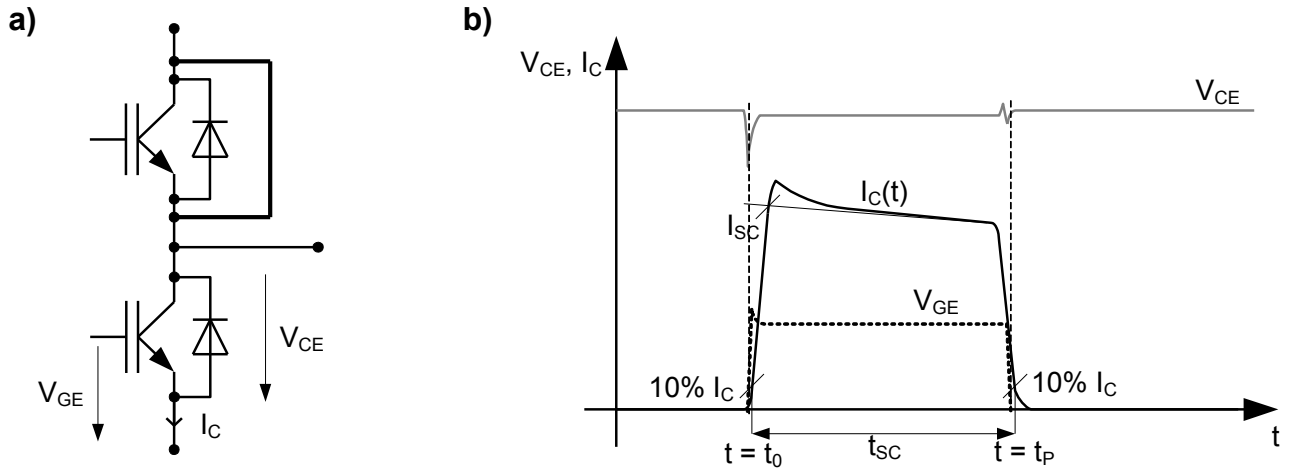


Figure 25: Short circuit test setup (a) and typical voltage/current waveforms during short circuit test (b)

The data of the measured short circuit and the applied parameters are noted in the datasheet as depicted in Figure 26. All of Infineon's IGBT modules are designed to achieve a short circuit-withstand-time of up to 10µs. The IGBT3 600V is an exception as it features a short circuit withstands time of t_p = 6µs

Kurzschlussverhalten SC data	$V_{GE} \le 15$ V, V_{CC} = 360 V $V_{CEmax} = V_{CES} - L_{sCE} \cdot di/dt$	$t_P \le 10$ µs, T_{vj} = 25°C $t_P \le 10$ µs, T_{vj} = 150°C	I_{SC}		960 760		A A

Figure 26: Short circuit data

3.12 Leakage currents I_{CES} and I_{GES}

Two major types of leakage currents as given in Figure 27 have to be considered:

- The maximum collector-emitter cut-off current describes the leakage current between the collector and emitter, when the IGBT is in blocking mode
- The gate-emitter leakage current gives a hint about the maximum leakage current between gate and emitter, with collector-emitter short circuited and maximum gate-emitter voltage applied.

Kollektor-Emitter Reststrom collector-emitter cut-off current	V_{CE} = 650 V, V_{GE} = 0 V, T_{vj} = 25°C	I_{CES}			1,0	mA
Gate-Emitter Reststrom gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C	I_{GES}			400	nA

Figure 27: Leakage currents

3.13 Thermal characteristics

The values of power dissipation and current ratings as discussed in chapters 3.2 and 3.3 have no meaning without specification of temperatures as well as thermal resistances. Therefore, in order to compare different devices, it is also necessary to compare thermal characteristics. More information about the thermal equivalent circuit can be found in AN2008-03[2].

When power modules with a base plate or discrete devices are characterized, junction-, case-, and heat sink temperatures are observed. The thermal resistances of junction to case and case to heat sink are specified in the datasheet as given in Figure 28. The datasheet value of the R_{thCH} with a referenced thermal resistance of the thermal interface material is a typical value under the specified conditions.

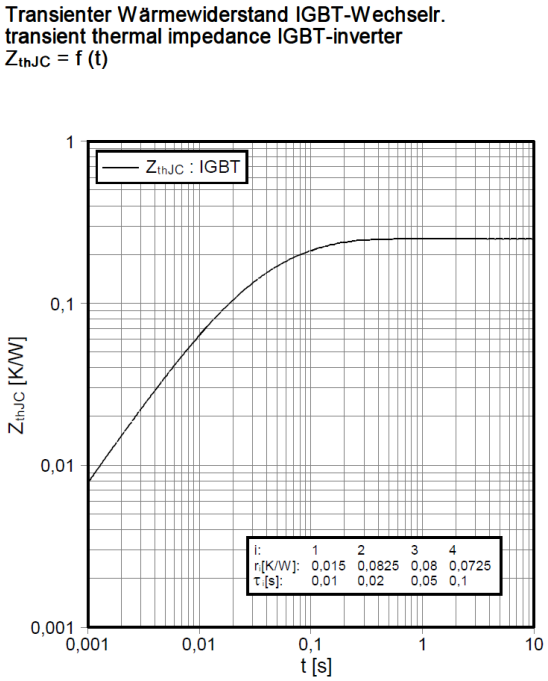
Innerer Wärmewiderstand thermal resistance, junction to case	pro IGBT / per IGBT	R_{thJC}			0,25	K/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,085		K/W

Figure 28: Thermal resistance IGBT, junction to case and case to heat sink

The thermal resistance characterizes the thermal behavior of the IGBT module at steady state, whereas the thermal impedance characterizes the thermal behavior of the IGBT module at transient conditions like short current pulses. Figure 29a shows the transient thermal impedance Z_{thJC} as a function of the time.

[2]Application note 2008-03: Thermal equivalent circuit model

a)



b)

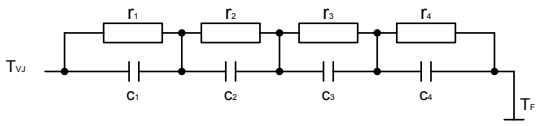


Figure 29: a) Transient thermal impedance junction to case and b) transient thermal model

The main power losses of the IGBT module are dissipated from the silicon die to the heat sink through different materials. Each material within the dissipation path has its own thermal characteristics. As a result, the thermal impedance behavior can be modeled with the appropriate coefficients of the IGBT module and is given as diagram $Z_{thJC}(t)$ as shown in Figure 29a. The separate RC-elements from Figure 29b have no physical meaning. Their values are extracted from the measured heating-up curve of the module by a corresponding analysis tool. The datasheet includes the partial fraction coefficients in tabular form as shown in Figure 29a. The values of the capacitances can be calculated by:

$$c_i = \frac{\tau_i}{r_i} \tag{11}$$

4 Datasheet parameters Diode

This section explains the electrical properties of the diode-chip inside the given IGBT module

4.1 Diode forward characteristic

The maximum permissible diode forward current rating can be calculated with equation (12). To give a current rating of a module, the corresponding junction and case temperature have to be specified, for example in Figure 30. Please note that current ratings without defined temperature conditions have no technical meaning at all. Since I_F is not known in equation (12), V_F @ I_F is also not known, but can be found within a few iterations. The ratings of continuous collector current are calculated with maximum values for V_F to ensure the specified current rating, taking component tolerances into account.

$$I_F = \frac{(T_{vj} - T_C)}{R_{thJC} \cdot V_F(I_F, T_{vj})} \tag{12}$$

Figure 30 depicts the typical forward characteristic of the implemented diode at different junction temperatures. A negative temperature coefficient of the diode's forward voltage drop can be observed, which is typical for minority-carrier devices. Therefore, the conduction losses of the diode decrease with increasing temperatures.

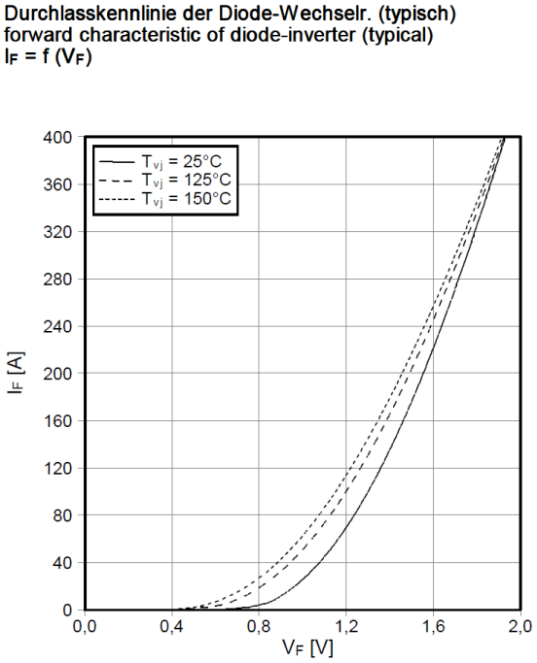


Figure 30: Forward characteristic of diode datasheet

4.2 Repetitive peak forward current

The nominal diode current rating can be exceeded in an application for a short time. This is defined as repetitive peak forward current in the datasheet for the specified pulse duration, for example 1ms as noted in Figure 31. In theory, this value can be derived from the feasible power dissipation and the transient thermal impedance Z_{th}, if the duration of the over current condition is defined. However, this theoretical value is not taking any limitations of bond wires, bus-bars or power connectors into account.

Periodischer Spitzenstrom repetitive peak forward current	t_P = 1 ms	I_{FRM}	400	A

Figure 31: Repetitive peak forward current

4.3 I^2t value

This value defines the surge current capability of the diode. The I^2t value applied should be lower than the specified I^2t value and t_p should not exceed 10ms as mentioned in Figure 32.

Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C V_R = 0 V, t_P = 10 ms, T_{vj} = 150°C	I²t	2850 2700	A²s A²s

Figure 32: Values of the surge capability

4.4 Reverse recovery

To investigate the transient behavior of a diode, the surrounding circuitry as already shown in Figure 8 on page 11 has to be taken into account. To simplify the circuitry, the output current of the half bridge can be assumed to be constant during commutation. The remaining stray inductances formed by the current loop

can now be replaced by just one stray inductance between high-side and low-side switch/freewheeling diode.

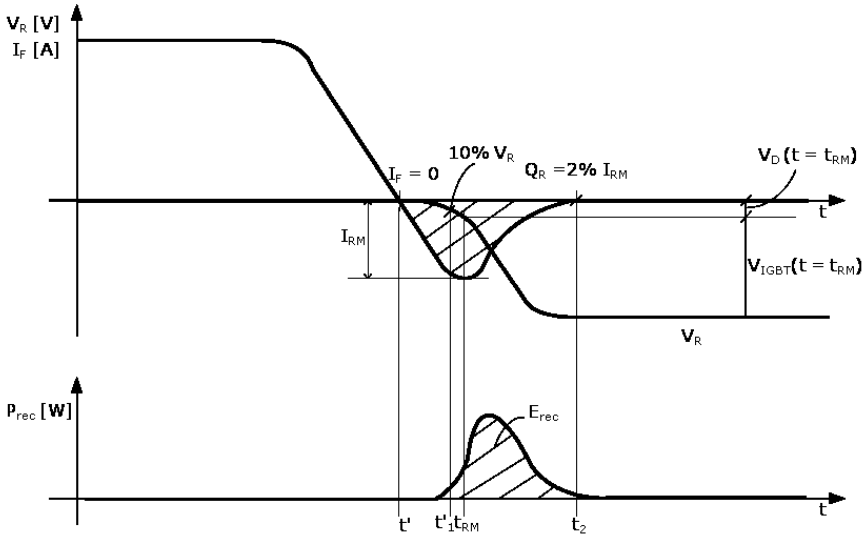


Figure 33: Schematic voltage and current waveform of a soft-recovery diode during turn-off transition

Figure 33 describes the current commutation from a high-side (HS) freewheeling diode to a low-side (LS) IGBT.

The commutation is triggered by turning-on the LS-IGBT which will not reduce the blocking voltage to roughly zero immediately. It will keep a portion of blocking voltage during the commutation. Due to the fact that the HS-diode is still on, the difference $V_L = V_R - V_{IGBT}$ will drop across the stray inductance causing a linear change of current. The diode current will reduce in the same way as the IGBT current increases. As soon as the diode current at t = t' crosses zero, a space charge region within the diode can be formed. Hence the voltage drop across the diode increases as can be seen in Figure 33.

The voltage drop across the stray inductance will be zero if the sum of diode and IGBT voltage is equal to the blocking voltage V_R

$$V_R = V_{IGBT} - V_D \text{ if } di/dt = 0 \tag{13}$$

As a result, the peak reverse recovery current I_{RM} is reached. The current commutation is finished and the reverse recovery current has to be reduced to zero. Any kind of oscillation has to be avoided.

After t > t_{RM}, the LS-IGBT which is still not fully turned on will reduce its voltage further and the blocking voltage of the HS-diode will increase to the final V_R. During this last step, the current change from I_{RM} to zero will result in an overvoltage across the diode; however in this case it will be masked by the increasing blocking voltage.

The reverse recovery of the diode will lead to additional turn-off losses as well as additional turn-on losses in the complementary switch. A current and voltage waveform of a soft-recovery emitter controlled diode during turn-off transition can be seen in Figure 33

The characterized peak reverse recovery current I_{RM} given in the datasheet section on Figure 34, is defined as the difference between the maximum negative current peak and zero current. The recovered charge results from:

$$Q_r = \int_{t'_1}^{t'_2} I_F \cdot dt \tag{14}$$

The integration limits are defined as t = t'$_1$ @ I_F =0 and t = t'$_2$ @ $|I_F| \leq 0.02 \cdot I_{RM}$ as marked in Figure 33.
The losses due to reverse recovery can be calculated with the recovered energy per pulse. The energy is determined as defined in equation (15):

$$E_{rec} = \int_{t_1'}^{t_2} V_R \cdot I_F \cdot dt \qquad (15)$$

The integration limits are chosen for the time t'$_1$ corresponding to 10% of the diode reverse voltage V_R and the time t_2 when the reverse recovery current I_{RM} peak attains 2%.
The recovered charge and thus switching losses caused by the reverse recovery of the diode strongly depend on junction temperature as well as current slope.

Rückstromspitze peak reverse recovery current	I_F = 200 A, - di$_F$/dt = 5700 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}	160 230 240		A A A
Sperrverzögerungsladung recovered charge	I_F = 200 A, - di$_F$/dt = 5700 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r	10,0 17,0 20,0		µC µC µC
Abschaltenergie pro Puls reverse recovery energy	I_F = 200 A, - di$_F$/dt = 5700 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}	3,00 5,20 5,80		mJ mJ mJ

Figure 34: Reverse recovery current, charge and reverse recovery energy

To give an indication of application specific switching losses, the losses per diode turn-off pulse as noted in the datasheet are a function of diode forward current and gate resistance of the switching IGBT as represented in Figure 35. The variation in gate resistance is an equivalent to a variation in commutation current slopes.

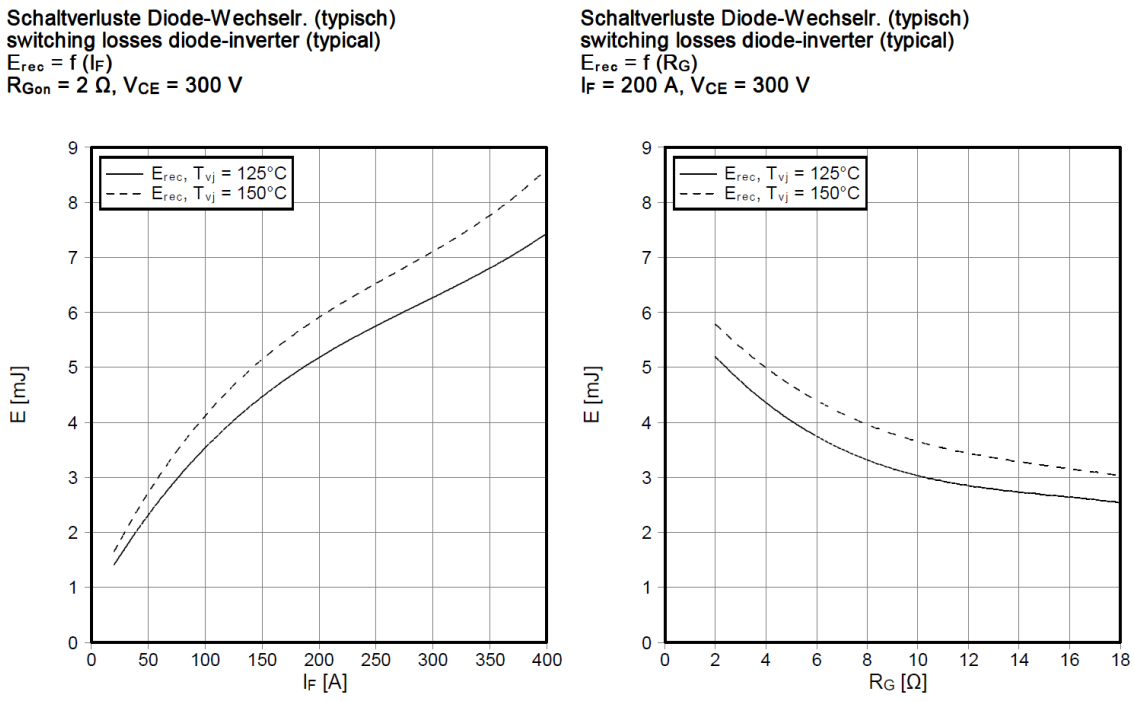


Figure 35: Reverse recovery energy per pulse as a function of
a) diode conducting current and b) gate resistance

5 Datasheet parameters NTC-thermistor

One of the most important parameters in power electronic devices is the chip temperature. The measurement of this temperature during operation is very difficult. One approach to estimate the real chip temperature in steady state is to use the NTC inside the IGBT module. This method is not adequate for measurement of fast variation of the chip temperature.
The temperature of the chips can be calculated using a thermal model and measuring the temperature at the NTC. The resistance of the NTC can be calculated as a function of the NTC temperature T2

$$R_2 = R_{25} \cdot e^{B \cdot \left(\frac{1}{T_2} - \frac{1}{T_1}\right)} \tag{16}$$

The resistance R25 at temperature $T_1 = 298.15K$ is specified in the datas eet as shown in Figure 36.
With measurement of the actual NTC-resistance R2, the temperature T_2 can be calculated with equation (17).

$$T_2 = \frac{1}{\frac{\ln\left(\frac{R_2}{R_{25}}\right)}{B} + \frac{1}{T1}} \tag{17}$$

The maximum relative deviation of the resistance is defined at a temperature of 100°C by $\Delta R/R$ from Figure 36. To avoid self heating of the NTC, the power dissipation inside the NTC has to be limited.

To limit the self heating of the NTC up to a maximum value of 1K, the current through the NTC can be calculated according to equation (18). More detailed information how to use the NTC inside the IGBT module is provided in AN2009-10[3]

$$I_{max} = \sqrt{\frac{P_{25}}{R_2}} \tag{18}$$

NTC-Widerstand / NTC-thermistor

Charakteristische Werte / characteristic values			min.	typ.	max.	
Nennwiderstand rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R_{100} deviation of R_{100}	T_C = 100°C, R_{100} = 493 Ω	$\Delta R/R$	-5		5	%
Verlustleistung power dissipation	T_C = 25°C	P_{25}			20,0	mW

Figure 36: Characteristic values of the NTC-thermistor

To calculate the NTC resistance as well as temperature more accurately, B-values are required. The B-value stated in Figure 37 depends on the temperature range considered. Typically a range of 25 to 100°C is of interest and thus $B_{25/100}$ has to be used. In case a lower temperature range is in focus, the B-values $B_{25/80}$ or $B_{25/50}$ can be used, which leads to more accurate calculation of the resistance in these lower ranges.

[3] Application note 2009-10: Using the NTC inside a power electronic module

B-Wert B-value	$R_2 = R_{25} \exp [B_{25/50}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/80}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/80}$		3411		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/100}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/100}$		3433		K

Figure 37: B-values of the NTC-thermistor

The use of the NTC for temperature measurement is not suitable for short circuit detection or short term overload, but may be used to protect the module from long term overload conditions or malfunction of the cooling system.

6 Datasheet parameters Module

This part covers electrical topics related to the mechanical construction of the IGBT module.

6.1 Insulation voltage

To verify the rated insulation voltage of the IGBT module, all terminals are connected to the high side of a high voltage source. The base plate is connected to the low side of the high voltage source. This high voltage source with high impedance must be able to supply the required voltage V_{iso}. A test voltage is slowly raised to the specified value determined by equation (19) and maintained at that value for the specified time t.

$$U_p = 2 \cdot \frac{U_m}{\sqrt{2}} + 1000V \quad (19)$$

The voltage is then reduced to zero. Infineon's IGBT modules are designed to achieve at least the basic insulation class 1 according to IEC 61140. For IGBT modules with an internal NTC, the functional insulation requirement is fulfilled between the grounded NTC terminals and the remaining control and power terminals connected and powered by the high voltage source.
The appropriate insulation voltage depends on the maximum rated collector-emitter voltage of the IGBT. Most drive applications require an insulation voltage of 2.5kV for IGBT modules up to 1700V blocking voltage. For traction applications, the required insulation voltage is defined to be 4kV for the same IGBT blocking voltage of 1700V. Therefore it is important to focus on the application field during the choice of the IGBT module.

Isolations-Prüfspannung insulation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}	2,5	kV

Figure 38: Insulation test voltage

The insulation test voltage in the datasheet as mentioned in Figure 38 is measured before and after reliability tests of the power module and is furthermore part of failure criteria of such stress tests.
The insulation voltage of the NTC inside the IGBT fulfills a functional isolation requirement only. In case of failures, for example of the gate driving circuit, a conducting path can be formed by moving bond wires that change their position during the failure event or by a plasma path forming as a consequence of arcing during failure. Therefore, if insulation requirements higher than a functional insulation have to be achieved, additional insulating barriers have to be added externally.

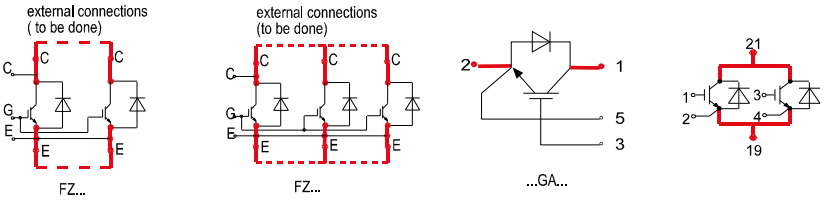
6.2 Stray inductance L_δ

Stray inductances lead to transient over voltages at the switching transients and are a major source of EMI. Furthermore, in combination with parasitic capacitances of the components, they can lead to resonant circuits, which can cause voltage and current ringing at switching transients. The transient voltage due to stray inductances can be calculated with:

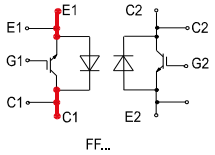
$$\Delta V = -L_\delta \cdot \frac{di_{L_\delta}}{dt} \quad (20)$$

Consequently, the stray inductances have to be minimized in order to reduce voltage overshoot at turn-off transitions. The value of the stray inductance as given in Figure 39, depends on the IGBT topology and would be understood as:

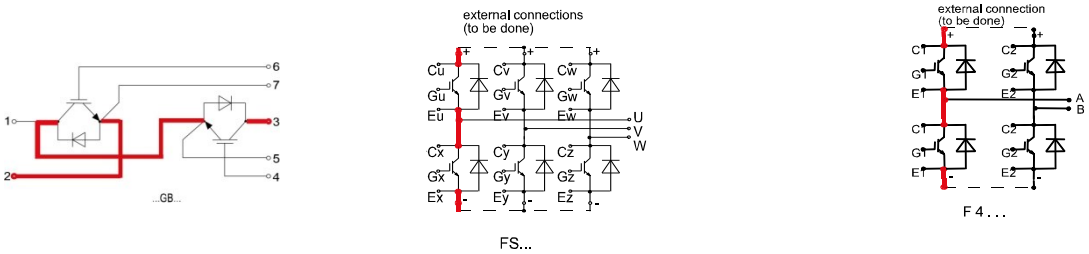
- The inductance of single switch modules



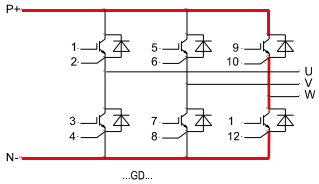
- The inductance of one switch for modules with two switches



- The loop with the highest inductance for half bridge, four- and sixpack modules specifies the inductance of one bridge



- The largest loop from P to N specifies the inductance for PIM modules



Modulinduktivität stray inductance module		L_{sCE}		21		nH

Figure 39: Module stray inductance

6.3 Module resistance $R_{CC'+EE'}$

The lead resistance of the module is a further contributor to voltage drop and power losses. The specified value in the datasheet characterizes the lead resistance between the power terminals of one switch as mentioned in Figure 40. According to the equivalent circuit shown in Figure 41, the module's lead resistance is defined as:

$$R_{CC'+EE'} = R_{CC'} + R_{EE'} + R_{E''E'} \tag{21}$$

Modulleitungswiderstand, Anschlüsse - Chip module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		1,80		mΩ

Figure 40: Module lead resistance

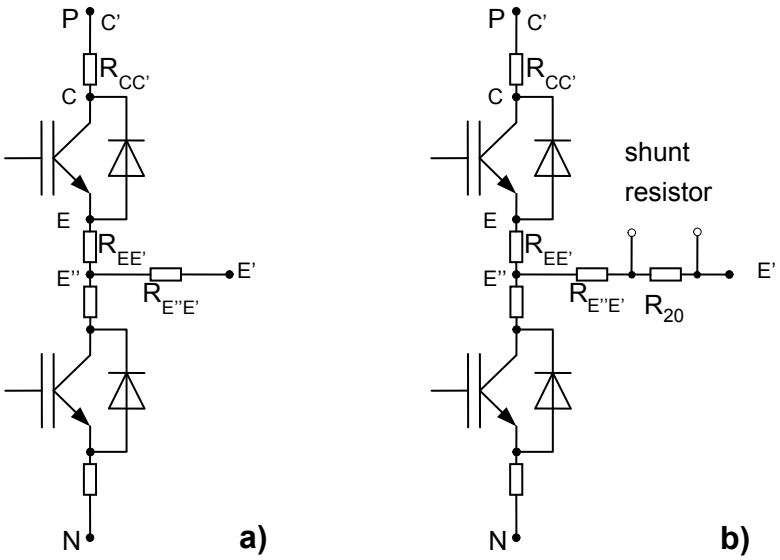


Figure 41: Equivalent circuit of module lead resistance a) without integrated shunt resistor, b) with integrated shunt resistor

If the module is equipped with a shunt resistor at the output terminal, as displayed in Figure 41 b), the resistance of the shunt resistor R_{20} is not included in the module lead resistance $R_{CC'+EE'}$.

6.4 Mounting torque M

The torque for the mechanical mounting of the module is specified in the datasheet as noted in Figure 42. These values are important to ensure the proper clamping force of the module to the heat sink. For modules with screwable power terminals, an additional mounting torque for terminal connection is given in the datasheet to ensure a reliable mechanical and electrical connection of bus-bars.

Anzugsdrehmoment f. mech. Befestigung mounting torque	Schraube M5 - Montage gem. gültiger Applikation Note screw M5 - mounting according to valid application note	M	3,00	-	6,00	Nm

Figure 42: Module mounting torque requirements

7 Symbols and Terms

Symbols and terms used in this document are part of the standards specification as listed below:

Symbols	Terms
A	Anode
C	Capacitance, collector
$C_{o(er)}$	Effective output capacitance, energy related
$C_{o(tr)}$	Effective output capacitance, time related
C_{ies}	Input capacitance
C_{oes}	Output capacitance
C_{res}	Reverse transfer capacitance
C_{th}	Thermal capacitance
C_{DS}	Drain-Source capacitance
C_{GD}	Gate-Drain capacitance
C_{GS}	Gate-Source capacitance
C_{Mi}	Miller capacitance
C_{σ}	Stray capacity
D	Pulse duty factor/duty cycle D = tp/T
di_F/dt	Rate of diode current rise
di/dt	Rate of current rise general
di_{rr}/dt	Peak rate fall of reverse recovery current
dv/dt	Rate of diode voltage rise
E	Energy
E_A	Avalanche energy
E_{AR}	Avalanche energy, repetitive
E_{AS}	Avalanche energy, single pulse
E_{off}	Turn-off loss energy
E_{on}	Turn-on loss energy
F	Frequency
G	Gate
G_{fs}	Transconductance
I	Current
I	Current, instantaneous value
I_{AR}	Avalanche current, repetitive
I_D	DC drain current
I_{Dpuls}	DC drain current, pulsed
I_{DSS}	Drain cutoff current
I_{DSV}	Drain cutoff current with gate voltage applied
I_C	Collector current
I_{CM}	Peak collector current
I_{CES}	Collector cut-off current, gate-emitter short-circuited
I_{CRM}	Repetitive peak collector current
I_{Cpuls}	Collector current, pulsed
I_G	Gate current

Symbols	Terms
I_F	General diode forward current
I_{FSM}	Diode current surge crest value 50 Hz sinusoidal
$I_{c\,nom}$, I_c	Continuous DC collector current
I_{GSS}	Gate-Source leakage current
I_{RM}	Diode peak reverse recovery current
I_{SM}	Inverse diode direct current, pulsed
I_{GES}	Gate leakage current, collector-emitter short-circuited
I_L	Current through inductance
I_{RRM}	Maximum reverse recovery current
K	Cathode
L	Inductance
L_L	Load inductance
L_p	Parasitic inductance (e.g. lines)
L_σ	Leakage inductance
P_{AV}	Avalanche power losses
P_{sw}	Switching power losses
P_{tot}	Total power dissipation
P_{con}	Conducting state power dissipation
Q_G	Gate charge
Q_{GS}	Charge of Gate-Source capacitance
Q_{GD}	Charge of Gate-Drain capacitance
Q_{Gtot}	Total Gate charge
Q_{rr}	Reverse recovery charge
$R_{DS(on)}$	Drain-Source on state resistance
R_G	Gate resistance
R_{Gint}, r_g	Internal gate resistance
R_{GE}	Gate-emitter resistance
R_{Gon}	Gate-turn on resistance
R_{Goff}	Gate-turn off resistance
R_{GS}	Gate-Source resistance
R_i	Internal resistance (pulse generator)
R_L	Load resistance
R_{thCH}	Thermal resistance, case to heat sink
R_{thHA}	Thermal resistance, heat sink to ambient
R_{thJA}	Thermal resistance, junction to ambient
R_{thJC}	Thermal resistance, junction to case
R_{thJS}	Thermal resistance, junction to soldering point
S	Source
T	Cycle time; temperature
T_A	Ambient temperature
T_C	Case temperature

Symbols	Terms
t	Time, general
t_1	Instant time
$t_{d\ off}$	Turn-off delay time
$t_{d\ on}$	Turn-on delay time
t_f	Fall time
T_j	Chip or operating temperature
t_p	Pulse duration time
$T_{vj\ max}$	Maximum junction temperature
$T_{vj\ op}$	Temperature under switching condition
t_{off}	Turn-off time
t_{on}	Turn-on time
t_r	Rise time
t_{rr}	Reverse recovery time
T_{stg}	Storage temperature
T_{sold}	Soldering temperature
V	Voltage, instantaneous value
V_{IN}	Drive voltage
$V_{(BR)CES}$	Collector-emitter breakdown voltage
$V_{(BR)DSS}$	Drain-Source Avalanche breakdown voltage
V_{CC}	Supply voltage
V_{CE}	Collector-emitter voltage
V_{CES}	Collector-emitter voltage, gate-emitter short-circuited
V_{CEsat}	Collector-emitter saturation voltage
V_{CGR}	Collector-Gate voltage
V_{DD}	Supply voltage
V_{DGR}	Drain-Gate voltage
V_{DS}	Drain-Source voltage
V_F	Diode forward voltage
V_{GE}	Gate-emitter voltage
V_{GES}	Gate-emitter voltage, collector-emitter short-circuited
$V_{GE(th)}$	Gate-emitter threshold voltage (IGBT)
V_{GS}	Gate-Source voltage
V_{GSth}	Gate threshold voltage
V_{SD}	Inverse diode forward voltage
$V_{plateau}$	Gate plateau voltage
Z_{thJA}	Transient thermal resistance, chip to ambient
Z_{thJS}	Transient thermal resistance, chip to solder point
Z_{thJC}	Transient thermal resistance, chip to case

8 References

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