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Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CYUSB3015
CYUSB3016
CYUSB3017

EZ-USB SX3: Configurable SuperSpeed USB Controller

Features

- Universal Serial Bus (USB) integration
  - USB 3.2, Gen 1 and USB 2.0 peripherals compliant with USB 3.2 Specification Revision 1.0
  - 5-Gbps SuperSpeed PHY compliant with USB 3.2 Gen 1
  - Three physical endpoints
  - Supports UVC, UAC, and USB vendor class protocol
- General Configurable Interface
  - Support up to 100 MHz
  - 8-, 16-, 24-, and 32-bit data bus
  - Supports Slave FIFO, parallel camera interface
- 32-bit CPU
  - ARM926EJ core with 200-MHz operation
  - 512-KB embedded SRAM
- Additional connectivity to the following peripherals
  - SPI boot flash
  - I^2C slaves at 100 kHz / 400 kHz / 1 MHz
- Selectable clock input frequencies
  - 19.2, 26, 38.4, and 52 MHz
  - 19.2-MHz crystal input support
- Ultra low-power in core power-down mode
  - Less than 60 µA with VBATT on and 20 µA with VBATT off
- Independent power domains for core and I/O
  - Core operation at 1.2 V
  - SPI operation at 1.8 V to 3.3 V
  - I^2C operation at 1.2 V to 3.3 V
- Package options
  - 121-ball, 10-mm × 10-mm, 0.8-mm pitch Pb-free ball grid array (BGA)
  - See Table 16 for details on SX3 variants
- EZ-USB™ SX3 configuration utility for configuration of SX3
  - Works on Windows, macOS, Linux
  - Example configurations for image sensor, HDMI receiver, and data applications
  - Supports programming of SX3 and configure the FPGA
  - Supports merging of FPGA configuration with SX3 configuration and store in a single SPI flash
- SX3 Development Kit available for rapid prototyping
  - Third party HDMI to USB3 capture card kit available from Cypress design partner

Applications

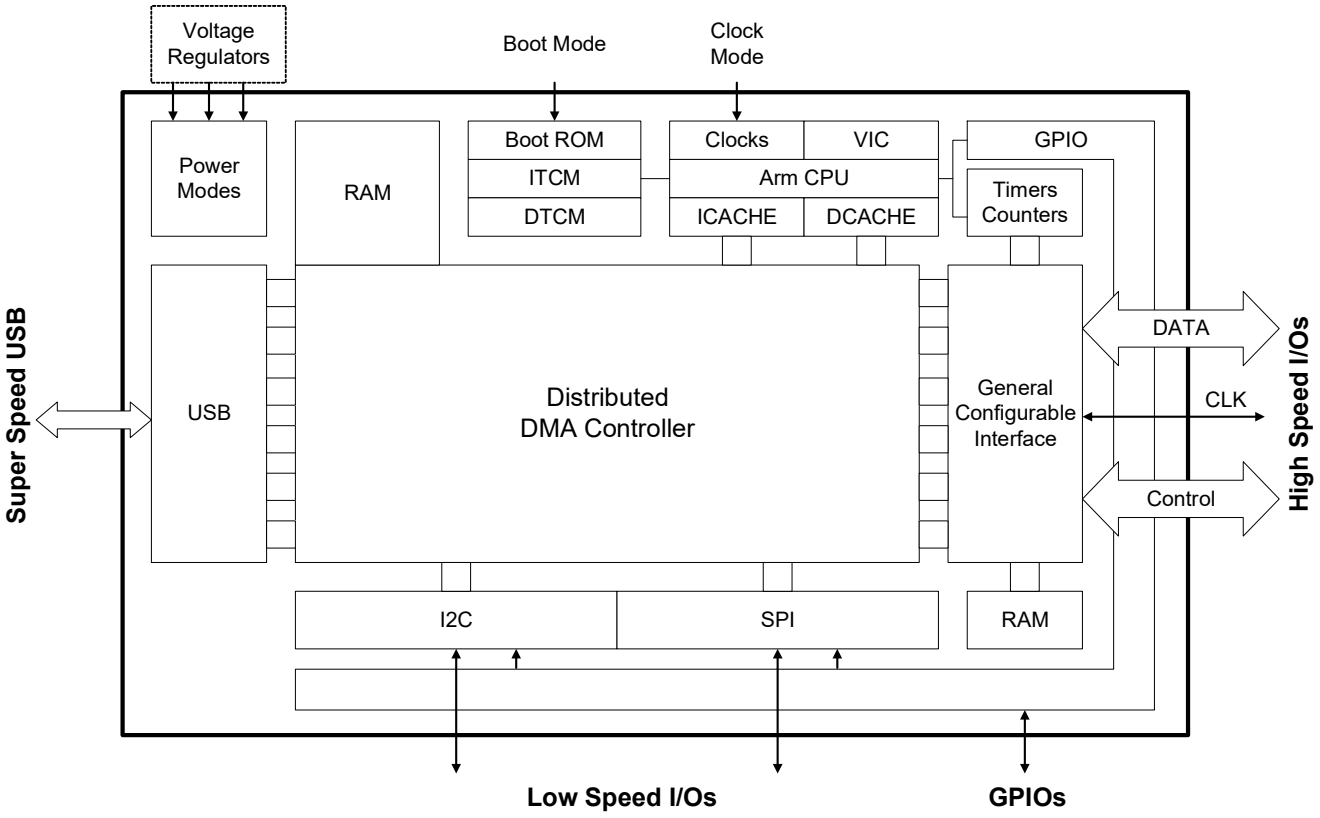
- USB WebCAMs
- Document cameras
- Video conference systems
- USB to Low-voltage Differential Signaling (LVDS) camera interface boards
- HDMI USB video capture cards
- SDI USB video capture cards
- Test and measurement equipment
- Surveillance cameras
- Medical imaging devices
- Industrial cameras
- USB logic analyzers
- USB oscilloscopes
- USB data loggers
- USB data acquisition systems
- USB Time-of-Flight (TOF) Cameras

Functional Description

For a complete list of related documentation, click here.

Errata: For information on silicon errata, see "Errata" on page 35. Details include trigger conditions, devices affected, and proposed workaround.

SX3 Block Diagram



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right <product> device for your design, and to help you to quickly and effectively integrate the device into your design.

- Overview: USB Portfolio, USB Roadmap
- USB 3.0 Product Selectors: SX3, FX3, FX3S, CX3, GX3, HX3
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application note for getting started with SX3 is:
  - AN231295 - Getting started with EZ-USB SX3

The following Application notes can be used for reference only.

- AN75705 - Getting Started with EZ-USB FX3
- AN76405 - EZ-USB FX3 Boot Options
- AN70707 - EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist
- AN65974 - Designing with the EZ-USB FX3 Slave FIFO Interface
- AN75779 - How to Implement an Image Sensor Interface with EZ-USB FX3 in a USB Video Class (UVC) Framework
- AN86947 - Optimizing USB 3.0 Throughput with EZ-USB FX3
- AN84868 - Configuring an FPGA over USB Using Cypress EZ-USB FX3
- AN73609 - EZ-USB FX2LP/ FX3 Developing Bulk-Loop Example on Linux

- Development Kits:
  - CYUSB3KIT-004, EZ-USB SX3 SuperSpeed Explorer Kit
- Models: IBIS

EZ-USB SX3 Configuration Utility

EZ-USB SX3 Configuration Utility is a graphical user application that allows users to configure the EZ-USB SX3 USB 3.0 Device controller variants.

The user can completely configure the EZ-USB SX3 based on the system requirements. The tool supports configuration of SX3-UVC and SX3-Data variants.

Users can configure the following using EZ-USB Configuration Utility for each variant:

- SX3-UVC (CYUSB3017 - variant supporting UVC and UAC)
  - USB descriptor settings
    - Vendor ID
    - Product ID
    - String descriptors (Product, Manufacturer, Serial Number)
    - Remote wakeup configuration
  - GPIO configuration
  - Debug interface
  - FPGA, HDMI receiver, or ISP configuration
  - DMA buffer configuration
  - UVC video formats and resolutions
  - Camera terminal controls
  - Processing unit controls
  - Extension unit controls
  - Image sensor / HDMI RX configuration
  - Audio interface configuration
- SX3-Data (CYUSB3015, CYUSB3016 - variant supporting USB vendor class)
  - USB descriptor settings
    - Vendor ID
    - Product ID
    - String descriptors (Product, Manufacturer, Serial Number)
    - Remote wakeup configuration
  - GPIO configuration
  - Debug interface
  - FPGA configuration
  - Buffer configuration

Users can also program the created configuration into the EX-USB SX3 using the programming tool integrated into the utility. This utility allows the user to save the created configuration. It also allows users to load the selected configuration. The utility is supported across Windows, Linux and Mac OSX platforms.

Contents

Functional Overview

Cypress' EZ-USB™ SX3 is a Configurable SuperSpeed peripheral controller, providing integrated and flexible features.

SX3 has a fully configurable, parallel interface called General Configurable Interface, which can connect to any ASIC, ISP, image sensor or FPGA that supports Slave FIFO or Video interface.

SX3 has integrated the USB 3.2 Gen 1 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from General Configurable Interface to the USB interface.

SX3 contains 512 KB of on-chip SRAM (see Ordering Information on page 33) for code and data. EZ-USB SX3 also provides interfaces to connect to serial peripherals such as SPI and I2C.

SX3 comes with "SX3 Configuration Utility", that will help customers to configure the SX3 for various applications. This tool can also merges the FPGA configuration or ISP firmware along with SX3 configuration and stores it in a single SPI Flash.

SX3 complies with the USB 3.2, Gen 1.0 specification and is also backward compatible with USB 2.0.

Application Examples

In a typical application (see Figure 1), the SX3 functions as the main processor running the application software that connects external hardware to the SuperSpeed USB connection.

Figure 1. Application Example Block Diagram for CYUSB3015 / CYUSB3016

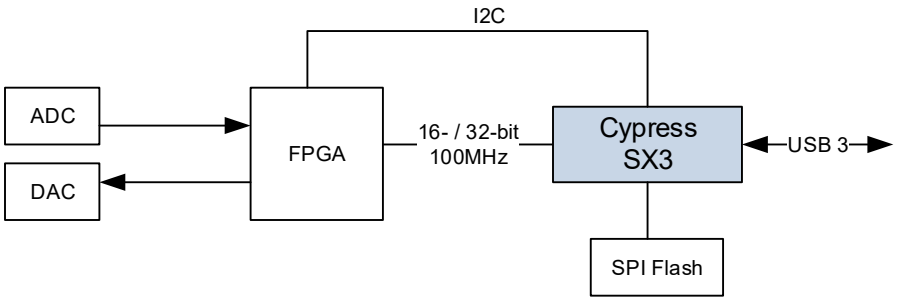
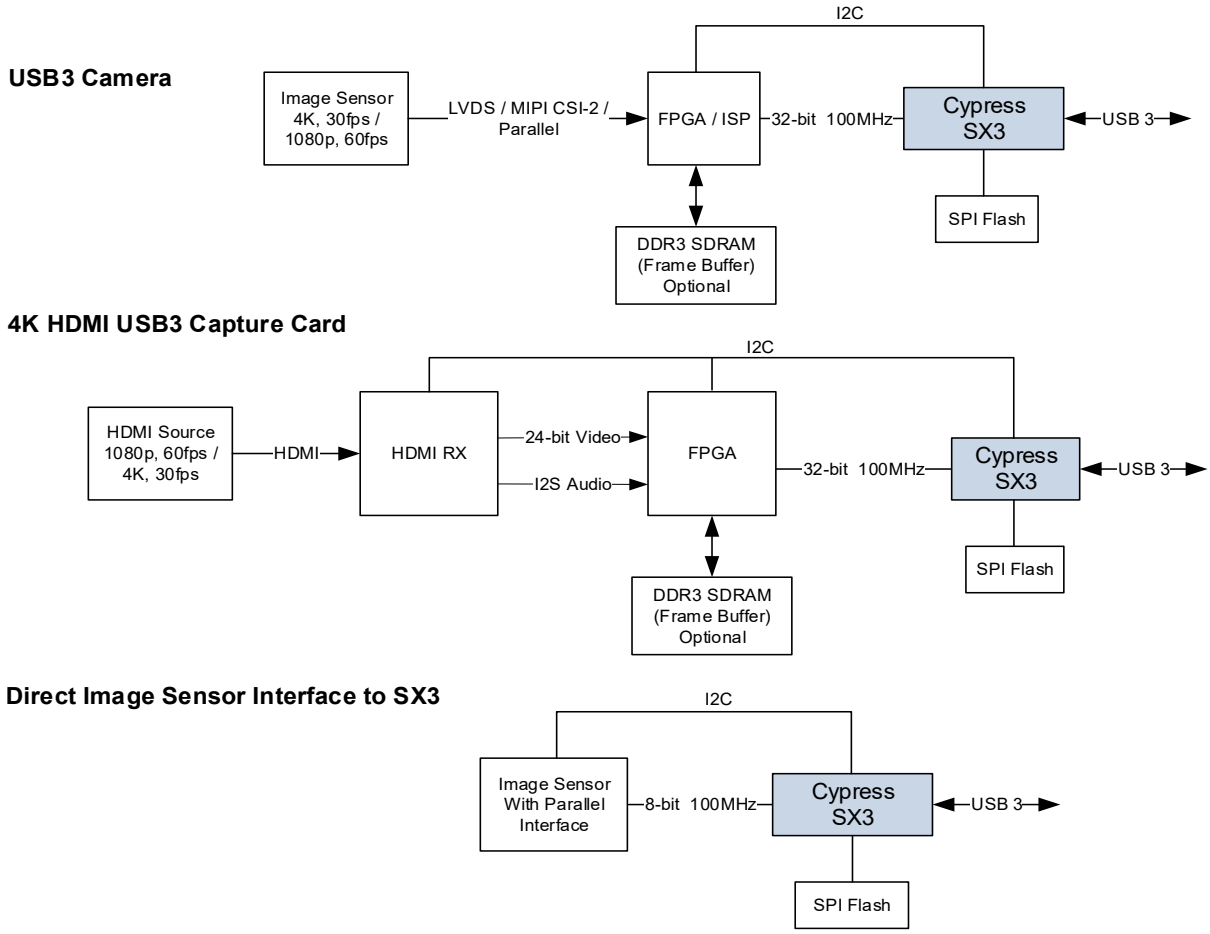


Figure 2. Application Example Block Diagram for CYUSB3017 (SX3 – UVC)



USB Interface

SX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality complaint with USB 3.2 Gen.1 specification revision 1.0 and is also backward compatible with the USB 2.0 specification.
- SX3 is capable of SuperSpeed, HighSpeed and FullSpeed.
- Supports USB video class (UVC) and USB vendor class.

Re-enumeration

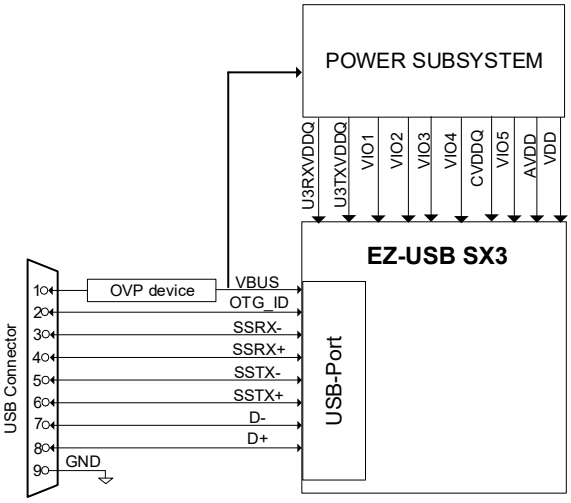
Because of SX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, SX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. SX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called Re-enumeration, happens instantly when the device is plugged in.

VBUS Overvoltage Protection

The maximum input voltage on SX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect SX3 from damage on VBUS. Figure 3 shows the system application diagram with an OVP device connected on VBUS. Refer to Table 6 for the operating range of VBUS and VBATT.

Figure 3. System Diagram with OVP Device For VBUS



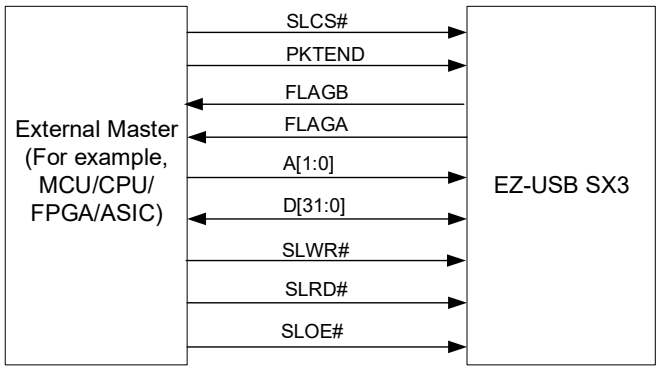
General Configurable Interface

The high-performance general configurable interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces. The general configurable interface is a configurable state machine that enables a flexible interface that may function as slave FIFO or parallel video interface, and supports 8-bit, 16-bit, 24-bit and 32-bit parallel data bus. Enables interface frequencies up to 100 MHz.

Slave FIFO Interface

The Slave FIFO interface signals are shown in Figure 4. This interface allows an external processor to directly access up to four buffers internal to SX3. For more information, see Slave FIFO Interface.

Figure 4. Slave FIFO Interface

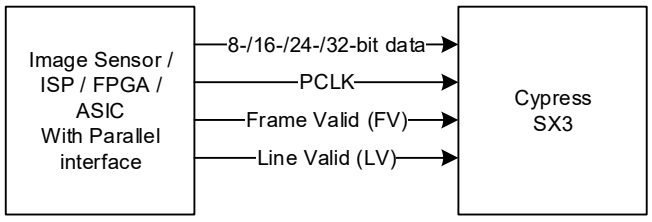


Note: Multiple Flags may be configured.

Image Sensor Parallel Interface

The Image sensor parallel interface will allow to interface the image sensors / ISPs with parallel interface directly with SX3. Refer to Section 3 of AN75779 - How to Implement an Image Sensor Interface Using EZ-USB FX3 in a USB Video Class (UVC) Framework for more details.

Figure 5. Camera Parallel Interface



CPU

SX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. SX3 offers the following advantages: Integrates 512 KB of embedded SRAM for code and data

SX3 offers the following advantages:

- Integrates 512 KB of embedded SRAM for code and data.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, General Configurable Interface, SPI, I^2C), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy configuration using SX3 Configuration utility.

Examples of the SX3 configurations available with SX3 Configuration utility.

Other Interfaces

SX3 supports the following serial peripherals: SPI and I^2C. The CYUSB3015, CYUSB3016, and CYUSB3017 Pin List shows the pin details.

SPI Interface

SX3 supports an SPI Master interface that can be used only for interfacing a SPI Flash that can store the SX3 firmware, configuration data, FPGA configuration / ISP firmware and Image sensor / HDMI RX configuration data. The maximum operation frequency is 33 MHz. The SPI controller supports four modes of SPI communication (see SPI Timing Specifications for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from four bits to 32 bits.

I^2C Interface

SX3's I^2C interface is compatible with the I^2C Bus Specification Revision 3. This I^2C interface is capable of operating only as I^2C master; therefore, it may be used to communicate with other I^2C slave devices.

SX3's I^2C Master Controller also supports multi-master mode functionality.

The power supply for the I^2C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I^2C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I^2C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I^2C controller supports clock-stretching to enable slower devices to exercise flow control.

The I^2C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

Boot Options

SX3 can load boot images from various sources, selected by the configuration of the PMODE pins.

Following are the SX3 boot options:

- Boot from USB
- Boot from SPI
  - Cypress SPI Flash parts supported are S25FS064S (64-Mbit), S25FS128S (128-Mbit), and S25FL064L (64-Mbit).

Table 1. SX3 Booting Options

PMODE[2:0][1]	Boot From
F11	USB boot
0F1	SPI, On Failure, USB Boot is Enabled

Note
1. 'F' indicates Floating.

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on SX3. The specific reset sequence and timing requirements are detailed in Figure 15 and Table 15. All I/Os are tristated during a hard reset. Note however, that the on-chip bootloader has control after a hard reset and it will configure I/O signals depending on the selected boot mode; see AN76405 - EZ-USB FX3/FX3S Boot Options for more details.

Clocking

SX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

SX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in Table 2.

Clock inputs to SX3 must meet the phase noise and jitter requirements specified in Table 3.

The input clock frequency is independent of the clock and data rate of the SX3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 2. Crystal/Clock Frequency Selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 3. SX3 Input Clock Specifications

Parameter	Description	Specification		Unit
		Min	Max	
Phase noise	100-Hz offset	–	-75	dB
	1-kHz offset	–	-104	
	10-kHz offset	–	-120	
	100-kHz offset	–	-128	
	1-MHz offset	–	-130	
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	
Undershoot	–	–	-3	
Rise time/fall time	–	–	3	ns

Power

SX3 has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os. The voltage level on these supplies is 1.8 V to 3.3 V. SX3 provides six independent supply domains for digital I/Os listed as follows (see Table 5 for details on each of the power domain signals):
  - **VIO1**: General configurable interface I/Os
  - **VIO2**: IO2
  - **VIO3**: IO3
  - **VIO4**: SPI
  - **VIO5**: I^2C
  - **CVDDQ**: This is the supply voltage for clock and reset I/O. It should be either 1.8 V or 3.3 V based on the voltage level of the CLKIN signal.
  - **V_{DD}**: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
    - **AVDD**: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits
    - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS**: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through SX3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Note: No specific power-up sequence for SX3 power domains. Minimum power-on reset (POR) time of 1 ms should be met and the power domains must be stable for SX3 operation.

Power Modes

SX3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
  - Normal operating power consumption does not exceed the sum of I_{CC} Core max and I_{CC} USB max (see Table 6 for current consumption specifications).
  - The I/O power supplies VIO2, VIO3, VIO4, and VIO5 can be turned off when the corresponding interface is not in use. VIO1 cannot be turned off at any time if the general configurable interface is used in the application.
- Low-power modes (see Table 4):
  - Suspend mode with USB 3.0 PHY enabled (L1)
  - Suspend mode with USB 3.0 PHY disabled (L2)
  - Standby mode (L3)
  - Core power-down mode (L4)

Table 4. Entry and Exit Methods for Low-Power Modes

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Enabled (L1)	■ The power consumption in this mode does not exceed I_{SB1} ■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone is operational with its internal clock while all other clocks are shut down ■ All I/Os maintain their previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory, and all internal RAM are maintained ■ All transactions must be completed before SX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put SX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SX3 into suspend mode ■ External Processor, through the use of mailbox registers, can put SX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ General configurable interface assertion of CTL[0] ■ Assertion of RESET#

Table 4. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Disabled (L2)	■ The power consumption in this mode does not exceed I_{SB2} ■ USB 3.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before SX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put SX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SX3 into suspend mode ■ External Processor, through the use of mailbox registers can put SX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Detection of VBUS ■ General configurable interface assertion of CTL[0] ■ Assertion of RESET#
Standby Mode (L3)	■ The power consumption in this mode does not exceed I_{SB3} ■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting SX3 into this Standby Mode ■ The program counter is reset after waking up from Standby ■ GPIO pins maintain their configuration ■ Crystal oscillator is turned off ■ Internal PLL is turned off ■ USB transceiver is turned off ■ ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	■ Firmware executing on ARM926EJ-S core or external processor configures the appropriate register	■ Detection of VBUS ■ General configurable interface assertion of CTL[0] ■ Assertion of RESET#
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed I_{SB4} ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply V_{DD} ■ Assertion of RESET#

Digital I/Os

SX3 has internal firmware-controlled pull-up and pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

SX3 supports seven GPIOs. They can be configured to one of the pre-defined Input or Output function using the SX3 Configuration utility. All general configurable interface pins and GPIO pins support an external load of up to 16 pF for every pin.

EMI

SX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. SX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

SX3 has built-in electrostatic discharge (ESD) protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification.
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A.
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

Pin Configurations

Figure 6. SX3 CYUSB3015-16bit - 121-BGA Ball Map (Top View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
U3VSSQ	U3RXVDDQ	SSRX-	SSRX+	SSTX+	SSTX-	AVDD	VSS	D+	D-	DNU
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**	**B11**
VIO4	FSLC[0]	R_usb3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	DNU
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**C11**
SPI_SSN	SPI_MISO	VDD	FIFOM_SS / GPIO_6	RESET#	XTALIN	XTALOUT	R_usb2	OTG_ID	DNU	VIO5
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**	**D11**
GPIO_3	GPIO_4	GPIO_5	SPI_SCK	SPI_MOSI	DNU	CLKIN	VSS	I2C_SCL	I2C_SDA	SUSPEND OUT
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**	**E11**
DNU	VSS	VIO3	DNU	DNU	FSLC[2]	DNU	DNU	VDD	VBATT	VBUS
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**	**F11**
VIO2	GPIO_2	DNU	DNU	DNU	DNU	DQ[2]	DQ[5]	DQ[1]	DQ[0]	VDD
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**	**G11**
VSS	DNU	DNU	PMODE[0]	GPIO_1	DMA_READY	DMA_PARTIAL	DQ[15] [4]	DQ[4]	DQ[3]	VSS
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**	**H11**
VDD	DNU	DNU	PMODE[1]	A0	INIT# / RESET	SLRD#	PKTEND#	DQ[7]	DQ[6]	VIO1
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**	**J11**
DNU	DNU	DNU	DNU	A1	PCLK	SLOE#	DQ[14] [4]	DQ[9]/A1 [3]	DQ[8]/A0 [3]	VDD
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**	**K11**
DNU	DNU	VSS	VSS	PROGRAM#	GPIO_0	SLWR#	SLCS#	DQ[13]	DQ[12]	DQ[10]
L1	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**	**L8**	**L9**	**L10**	**L11**
VSS	VSS	VSS	PMODE[2]	VDD	VSS	VDD	DNU	VIO1	DQ[11]	VSS

Figure 7. SX3 CYUSB3016-32bit - 121-BGA Ball Map (Top View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
U3VSSQ	U3RXVDDQ	SSRX-	SSRX+	SSTX+	SSTX-	AVDD	VSS	D+	D-	DNU
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**	**B11**
VIO4	FSLC[0]	R_usb3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	DNU
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**C11**
SPI_SSN	SPI_MISO	VDD	FIFOM_SS / GPIO_6	RESET#	XTALIN	XTALOUT	R_usb2	OTG_ID	DNU	VIO5
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**	**D11**
GPIO_3	GPIO_4	GPIO_5	SPI_SCK	SPI_MOSI	DNU	CLKIN	VSS	I2C_SCL	I2C_SDA	SUSPEND OUT
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**	**E11**
DQ[29]	VSS	VIO3	DQ[31]	DQ[30]	FSLC[2]	DNU	DNU	VDD	VBATT	VBUS
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**	**F11**
VIO2	GPIO_2	DQ[27]	DQ[24]/A0[5]	DQ[28]	DNU	DQ[2]	DQ[5]	DQ[1]	DQ[0]	VDD
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**	**G11**
VSS	DQ[25]/A1[5]	DQ[26]	PMODE[0]	GPIO_1	DMA_READY	DMA_PARTIAL	DQ[15] [4]	DQ[4]	DQ[3]	VSS
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**	**H11**
VDD	DQ[22]	DQ[23]	PMODE[1]	A0	INIT# / RESET	SLRD#	PKTEND#	DQ[7]	DQ[6]	VIO1
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**	**J11**
DQ[21]	DQ[19]	DQ[20]	DQ[17]	A1	PCLK	SLOE#	DQ[14] [4]	DQ[9]/A1 [3]	DQ[8]/A0 [3]	VDD
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**	**K11**
DQ[18]	DQ[16]	VSS	VSS	PROGRAM#	GPIO_0	SLWR#	SLCS#	DQ[13]	DQ[12]	DQ[10]
L1	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**	**L8**	**L9**	**L10**	**L11**
VSS	VSS	VSS	PMODE[2]	VDD	VSS	VDD	DNU	VIO1	DQ[11]	VSS

Figure 8. SX3 CYUSB3017-UVC - 121-BGA Ball Map (Top View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
U3VSSQ	U3RXVDDQ	SSRX-	SSRX+	SSTX+	SSTX-	AVDD	VSS	D+	D-	DNU
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**	**B11**
VIO4	FSLC[0]	R_usb3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	DNU
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**	**C11**
SPI_SSN	SPI_MISO	VDD	FIFOM_SS / GPIO_6	RESET#	XTALIN	XTALOUT	R_usb2	OTG_ID	DNU	VIO5
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**	**D11**
GPIO_3	GPIO_4	GPIO_5	SPI_SCK	SPI_MOSI	DNU	CLKIN	VSS	I2C_SCL	I2C_SDA	SUSPEND OUT
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**	**E11**
DQ[29]	VSS	VIO3	DQ[31]	DQ[30]	FSLC[2]	DNU	DNU	VDD	VBATT	VBUS
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**	**F11**
VIO2	GPIO_2	DQ[27]	DQ[24]/A0[5]	DQ[28]	DNU	DQ[2]	DQ[5]	DQ[1]	DQ[0]	VDD
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**	**G11**
VSS	DQ[25]/A1[5]	DQ[26]	PMODE[0]	GPIO_1	DMA_READY	DMA_PARTIAL	DQ[15] [4]	DQ[4]	DQ[3]	VSS
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**	**H11**
VDD	DQ[22]	DQ[23]	PMODE[1]	A0	INIT# / RESET	SLRD# / LV	PKTEND#	DQ[7]	DQ[6]	VIO1
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**	**J11**
DQ[21]	DQ[19]	DQ[20]	DQ[17]	A1	PCLK	SLOE# / FV	DQ[14] [4]	DQ[9]/A1 [3]	DQ[8]/A0 [3]	VDD
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**	**K11**
DQ[18]	DQ[16]	VSS	VSS	PROGRAM#	GPIO_0	SLWR#	SLCS#	DQ[13]	DQ[12]	DQ[10]
L1	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**	**L8**	**L9**	**L10**	**L11**
VSS	VSS	VSS	PMODE[2]	VDD	VSS	VDD	DNU	VIO1	DQ[11]	VSS

Pin Description

Table 5. CYUSB3015, CYUSB3016, and CYUSB3017 Pin List

SI#	Pin#	Power Domain	I/O / Power	SX3 Pin Name			Remarks
				CYUSB3015 - 16bit	CYUSB3016 - 32bit	CYUSB3017 - UVC	
1	F10	VIO1	I/O	DQ[0]	DQ[0]	DQ[0]	–
2	F9	VIO1	I/O	DQ[1]	DQ[1]	DQ[1]	–
3	F7	VIO1	I/O	DQ[2]	DQ[2]	DQ[2]	–
4	G10	VIO1	I/O	DQ[3]	DQ[3]	DQ[3]	–
5	G9	VIO1	I/O	DQ[4]	DQ[4]	DQ[4]	–
6	F8	VIO1	I/O	DQ[5]	DQ[5]	DQ[5]	–
7	H10	VIO1	I/O	DQ[6]	DQ[6]	DQ[6]	–
8	H9	VIO1	I/O	DQ[7]	DQ[7]	DQ[7]	–
9	J10	VIO1	I/O	DQ[8]/A0 [3]	DQ[8]/A0 [3]	DQ[8]/A0 [3]	[3] - Address bit 0 for 8-bit mode
10	J9	VIO1	I/O	DQ[9]/A1 [3]	DQ[9]/A1 [3]	DQ[9]/A1 [3]	[3] - Address bit 1 for 8-bit mode
11	K11	VIO1	I/O	DQ[10]	DQ[10]	DQ[10]	–
12	L10	VIO1	I/O	DQ[11]	DQ[11]	DQ[11]	–
13	K10	VIO1	I/O	DQ[12]	DQ[12]	DQ[12]	–
14	K9	VIO1	I/O	DQ[13]	DQ[13]	DQ[13]	–
15	J8	VIO1	I/O	DQ[14]	DQ[14]	DQ[14]	–
16	G8	VIO1	I/O	DQ[15]	DQ[15]	DQ[15]	–
17	J6	VIO1	I	PCLK	PCLK	PCLK	–
18	K8	VIO1	I	SLCS#	SLCS#	SLCS#	–
19	K7	VIO1	I	SLWR#	SLWR#	SLWR#	–
20	J7	VIO1	I	SLOE#	SLOE#	SLOE# / FV	–
21	H7	VIO1	I	SLRD#	SLRD#	SLRD# / LV	–
22	G7	VIO1	O	DMA_PARTIAL	DMA_PARTIAL	DMA_PARTIAL	–
23	G6	VIO1	O	DMA_READY	DMA_READY	DMA_READY	–
24	K6	VIO1	I/O	GPIO_0	GPIO_0	GPIO_0	–
25	H8	VIO1	I	PKTEND#	PKTEND#	PKTEND#	–
26	G5	VIO1	I/O	GPIO_1	GPIO_1	GPIO_1	–
27	H6	VIO1	O	INIT# / RESET	INIT# / RESET	INIT# / RESET	FIFO MASTER signal
28	K5	VIO1	O	PROGRAM#	PROGRAM#	PROGRAM#	
29	J5	VIO1	I	A1	A1	A1	Address bit 1 for 16-, 32-bit mode
30	H5	VIO1	I	A0	A0	A0	Address bit 0 for 16-, 32-bit mode
31	G4	VIO1	I	PMODE[0]	PMODE[0]	PMODE[0]	–
32	H4	VIO1	I	PMODE[1]	PMODE[1]	PMODE[1]	–
33	L4	VIO1	I	PMODE[2]	PMODE[2]	PMODE[2]	–
34	L8	VIO1	I	DNU	DNU	DNU	–
35	K2	VIO2	I/O	DNU	DQ[16]	DQ[16]	–

Table 5. CYUSB3015, CYUSB3016, and CYUSB3017 Pin List (continued)

SI#	Pin#	Power Domain	I/O / Power	SX3 Pin Name			Remarks
				CYUSB3015 - 16bit	CYUSB3016 - 32bit	CYUSB3017 - UVC	
36	J4	VIO2	I/O	DNU	DQ[17]	DQ[17]	–
37	K1	VIO2	I/O	DNU	DQ[18]	DQ[18]	–
38	J2	VIO2	I/O	DNU	DQ[19]	DQ[19]	–
39	J3	VIO2	I/O	DNU	DQ[20]	DQ[20]	–
40	J1	VIO2	I/O	DNU	DQ[21]	DQ[21]	–
41	H2	VIO2	I/O	DNU	DQ[22]	DQ[22]	–
42	H3	VIO2	I/O	DNU	DQ[23]	DQ[23]	–
43	F4	VIO2	I/O	DNU	DQ[24]/A0[5]	DQ[24]/A0[5]	[5] - Address bit 0 for 24-bit mode
44	G2	VIO2	I/O	DNU	DQ[25]/A1[5]	DQ[25]/A1[5]	[5] - Address bit 1 for 24-bit mode
45	G3	VIO2	I/O	DNU	DQ[26]	DQ[26]	–
46	F3	VIO2	I/O	DNU	DQ[27]	DQ[27]	–
47	F2	VIO2	I/O	GPIO_2	GPIO_2	GPIO_2	–
48	F5	VIO3	I/O	DNU	DQ[28]	DQ[28]	–
49	E1	VIO3	I/O	DNU	DQ[29]	DQ[29]	–
50	E5	VIO3	I/O	DNU	DQ[30]	DQ[30]	–
51	E4	VIO3	I/O	DNU	DQ[31]	DQ[31]	–
52	D1	VIO3	I/O	GPIO_3	GPIO_3	GPIO_3	–
53	D2	VIO3	I/O	GPIO_4	GPIO_4	GPIO_4	–
54	D3	VIO3	I/O	GPIO_5	GPIO_5	GPIO_5	–
55	D4	VIO4	O	SPI_SCK	SPI_SCK	SPI_SCK	–
56	C1	VIO4	O	SPI_SSN	SPI_SSN	SPI_SSN	–
57	C2	VIO4	I	SPI_MISO	SPI_MISO	SPI_MISO	–
58	D5	VIO4	O	SPI_MOSI	SPI_MOSI	SPI_MOSI	–
59	C4	VIO4	I/O	FIFOM_SS / GPIO_6	FIFOM_SS / GPIO_6	FIFOM_SS / GPIO_6	–
USB Port							
60	A3	U3RXVDDQ	I	SSRX-	SSRX-	SSRX-	–
61	A4	U3RXVDDQ	I	SSRX+	SSRX+	SSRX+	–
62	A6	U3TXVDDQ	O	SSTX-	SSTX-	SSTX-	–
63	A5	U3TXVDDQ	O	SSTX+	SSTX+	SSTX+	–
64	B3	U3TXVDDQ	I/O	R_usb3	R_usb3	R_usb3	Precision resistor for USB 3.0 (Connect a 200±1% resistor between this pin and GND)
65	C9	VBUS/VBATT	I	OTG_ID	OTG_ID	OTG_ID	–
66	A9	VBUS/VBATT	I/O	D+	D+	D+	–
67	A10	VBUS/VBATT	I/O	D-	D-	D-	–

Table 5. CYUSB3015, CYUSB3016, and CYUSB3017 Pin List (continued)

SI#	Pin#	Power Domain	I/O / Power	SX3 Pin Name			Remarks
				CYUSB3015 - 16bit	CYUSB3016 - 32bit	CYUSB3017 - UVC	
68	C8	VBUS/VBATT	I/O	R_usb2	R_usb2	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND)
Clock and Reset							
69	B2	CVDDQ	I	FSLC[0]	FSLC[0]	FSLC[0]	–
70	C6	AVDD	I/O	XTALIN	XTALIN	XTALIN	–
71	C7	AVDD	I/O	XTALOUT	XTALOUT	XTALOUT	–
72	B4	CVDDQ	I	FSLC[1]	FSLC[1]	FSLC[1]	–
73	E6	CVDDQ	I	FSLC[2]	FSLC[2]	FSLC[2]	–
74	D7	CVDDQ	I	CLKIN	CLKIN	CLKIN	–
75	D6	CVDDQ	I	DNU	DNU	DNU	DNU - Do not use
76	C5	CVDDQ	I	RESET#	RESET#	RESET#	–
I2C							
77	D9	VIO5	I/O	I2C_SCL	I2C_SCL	I2C_SCL	–
78	D10	VIO5	I/O	I2C_SDA	I2C_SDA	I2C_SDA	–
79	E7	VIO5	I	DNU	DNU	DNU	DNU - Do not use
80	C10	VIO5	O	DNU	DNU	DNU	
81	B11	VIO5	I	DNU	DNU	DNU	
82	E8	VIO5	I	DNU	DNU	DNU	
83	F6	VIO5	I	DNU	DNU	DNU	
84	D11	VIO5	O	SUSPEND OUT	SUSPEND OUT	SUSPEND OUT	–
Power							
85	E10		PWR	VBATT	VBATT	VBATT	–
86	B10		PWR	VDD	VDD	VDD	–
87	A1		PWR	U3VSSQ	U3VSSQ	U3VSSQ	–
88	E11		PWR	VBUS	VBUS	VBUS	–
89	D8		PWR	VSS	VSS	VSS	–
90	H11		PWR	VIO1	VIO1	VIO1	–
91	E2		PWR	VSS	VSS	VSS	–
92	L9		PWR	VIO1	VIO1	VIO1	–
93	G1		PWR	VSS	VSS	VSS	–
94	F1		PWR	VIO2	VIO2	VIO2	–
95	G11		PWR	VSS	VSS	VSS	–
96	E3		PWR	VIO3	VIO3	VIO3	–
97	L1		PWR	VSS	VSS	VSS	–
98	B1		PWR	VIO4	VIO4	VIO4	–
99	L6		PWR	VSS	VSS	VSS	–
100	B6		PWR	CVDDQ	CVDDQ	CVDDQ	–
101	B5		PWR	U3TXVDDQ	U3TXVDDQ	U3TXVDDQ	–

Table 5. CYUSB3015, CYUSB3016, and CYUSB3017 Pin List (continued)

Sl#	Pin#	Power Domain	I/O / Power	SX3 Pin Name			Remarks
				CYUSB3015 - 16bit	CYUSB3016 - 32bit	CYUSB3017 - UVC	
102	A2		PWR	U3RXVDDQ	U3RXVDDQ	U3RXVDDQ	–
103	C11		PWR	VIO5	VIO5	VIO5	–
Power Domain							
104	L11		PWR	VSS	VSS	VSS	–
105	A7		PWR	AVDD	AVDD	AVDD	–
106	B7		PWR	AVSS	AVSS	AVSS	–
107	C3		PWR	VDD	VDD	VDD	–
108	B8		PWR	VSS	VSS	VSS	–
109	E9		PWR	VDD	VDD	VDD	–
110	B9		PWR	VSS	VSS	VSS	–
111	F11		PWR	VDD	VDD	VDD	–
112	H1		PWR	VDD	VDD	VDD	–
113	L7		PWR	VDD	VDD	VDD	–
114	J11		PWR	VDD	VDD	VDD	–
115	L5		PWR	VDD	VDD	VDD	–
116	K4		PWR	VSS	VSS	VSS	–
117	L3		PWR	VSS	VSS	VSS	–
118	K3		PWR	VSS	VSS	VSS	–
119	L2		PWR	VSS	VSS	VSS	–
120	A8		PWR	VSS	VSS	VSS	–
121	A11			DNU	DNU	DNU	Do not use

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... -40 °C to +85 °C

Ambient temperature with power supplied (Commercial) ..... 0 °C to +70 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} ..... 1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} ....3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ....1.25 V

DC input voltage to any input pin ..... .V_{CC} + 0.3 V

DC voltage applied to outputs in high-Z state ..... V_{CC} + 0.3 V

(V_{CC} is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-kV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D-, and GND pins, and serial peripheral pins
- ± 6-kV contact discharge, ± 8-kV air gap discharge based on IEC61000-4-2 level 3A, ± 8-kV contact discharge, and ± 15-kV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ..... .> 200 mA

Maximum output short-circuit current for all I/Os (cumulative) ..... -100 mA

Maximum output current per I/O (source or sink) ..... 20 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... -40 °C to +85 °C

Commercial ..... 0 °C to +70 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage ..... 1.15 V to 1.25 V

V_{BATT} supply voltage ....3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage ..... 1.7 V to 3.6 V

V_{IO5} supply voltage .... 1.15 V to 3.6 V

DC Specifications

Table 6. DC Specifications

Parameter	Description	Min	Max	Unit	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	General Configurable Interface I/O power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
V_{IO4}	SPI power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C voltage supply	1.15	3.6	V	1.2-V, 1.8-V, 2.5-V, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × V_{CC}	V_{CC} + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port). V_{CC} is the corresponding I/O voltage supply.

Table 6. DC Specifications (continued)

Parameter	Description	Min	Max	Unit	Notes
V_{IH2}	Input HIGH voltage 2	V_{CC} – 0.4	V_{CC} + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × V_{CC}	V	VCC is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	0.9 × V_{CC}	–	V	I_{OH} (max) = -100 µA tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply. See Table 7 for values of I_{OH} at various drive strength and V_{CC}.
V_{OL}	Output LOW voltage	–	0.1 × V_{CC}	V	I_{OL} (min) = +100 µA tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply. See Table 7 for values of I_{OL} measured at various drive strength and V_{CC}.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD})
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB	USB voltage supply operating current	–	60	mA	–
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

Table 7. I_{OH}/I_{OL} values for different drive strength and V_{DDIO} Values

V_{DDIO} (V)	V_{OH} (V)	V_{OL} (V)	Drive Strength	$I_{OH\ max}$ (mA)	$I_{OL\ min}$ (mA)
1.7	1.53	0.17	Quarter	1.02	2.21
			Half	1.51	3.28
			Three-Quarters	1.83	3.85
			Full	2.28	4.73
2.5	2.25	0.25	Quarter	5.03	3.96
			Half	7.38	5.84
			Three-Quarters	8.89	6.89
			Full	11.07	8.61
3.6	3.24	0.36	Quarter	7.80	5.74
			Half	11.36	8.64
			Three-Quarters	13.64	10.15
			Full	16.92	12.67

Thermal Characteristics

Table 8. Thermal Characteristics

Parameter	Description	Value	Unit
$T_{J\ MAX}$	Maximum junction temperature	125	°C
Θ_{JA}	Thermal resistance (junction to ambient)	34.66	°C/W
Θ_{JB}	Thermal resistance (junction to board)	27.03	°C/W
Θ_{JC}	Thermal resistance (junction to case)	13.57	°C/W

AC Timing Parameters

General Configurable Interface Lines AC Characteristics at 100 MHz

Table 9. General Configurable Interface Lines AC Characteristics at 100 MHz

Symbol	Parameter	Min	Typ	Max	Unit
Tr	Rise time	–	–	2.5	ns
Tf	Fall time	–	–	2.5	ns
Tov	Overshoot	–	–	3	%
Tun	Undershoot	–	–	3	%

General Configurable Interface PCLK Jitter Characteristics

Table 10. General Configurable Interface PCLK Jitter Characteristics

Clk Freq (MHz)	Period Jitter (ps)[2]	C-C Min (ps)	C-C Max (ps)
10.08	354.44	-187.92	204.55
25.2	205.97	-153.54	126.53
50.4	144.62	-100.16	85.769
100.8	171.43	-155.13	157.14

Note
2. The clock jitter is measured using internally generated PCLK. i.e., PCLK is configured as an output from general configurable interface. The data is measured over 10,000 clock cycles.

General Configurable Interface Timing

Figure 9. General Configurable Interface Timing in Synchronous Mode

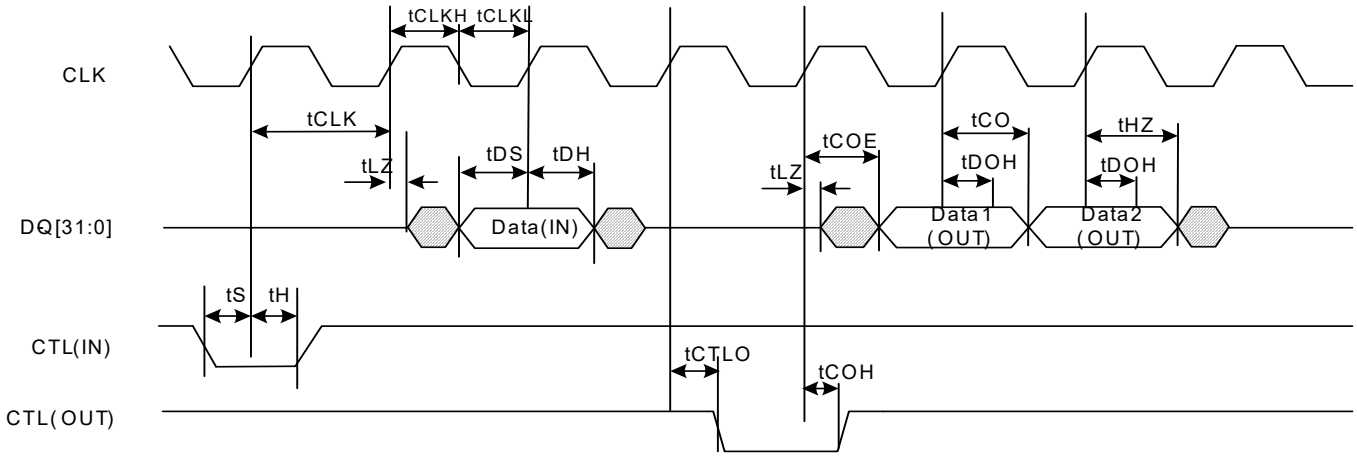


Table 11. General Configurable Interface Timing Parameters in Synchronous Mode[3]

Parameter	Description	Min	Max	Unit
Frequency	Interface clock frequency	–	100	MHz
t_{CLK}	Interface clock period	10	–	ns
t_{CLKH}	Clock high time	4	–	ns
t_{CLKL}	Clock low time	4	–	ns
t_S	CTL input to clock setup time	2	–	ns
t_H	CTL input to clock hold time	0.5	–	ns
t_{DS}	Data in to clock setup time	2	–	ns
t_{DH}	Data in to clock hold time	0.5	–	ns
t_{CO}	Clock to data out propagation delay when DQ bus is already in output direction	–	7	ns
t_{COE}	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus	–	9	ns
t_{CTLO}	Clock to CTL out propagation delay	–	8	ns
t_{DOH}	Clock to data out hold	2	–	ns
t_{COH}	Clock to CTL out hold	0	–	ns
t_{HZ}	Clock to high-Z	–	8	ns
t_{LZ}	Clock to low-Z	0	–	ns

Note
3. All parameters guaranteed by design and validated through characterization.

Slave FIFO Interface

Synchronous Slave FIFO Read Sequence Description

- FIFO address is stable and SLCS is asserted
- FLAG indicates FIFO not empty status
- SLOE is asserted. SLOE is an output-enable only, whose sole function is to drive the data bus.
- SLRD is asserted

The FIFO pointer is updated on the rising edge of the PCLK, while the SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of t_{CO} (measured from the rising edge of PCLK), the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE must also be asserted.

The same sequence of events is applicable for a burst read.

FLAG Usage

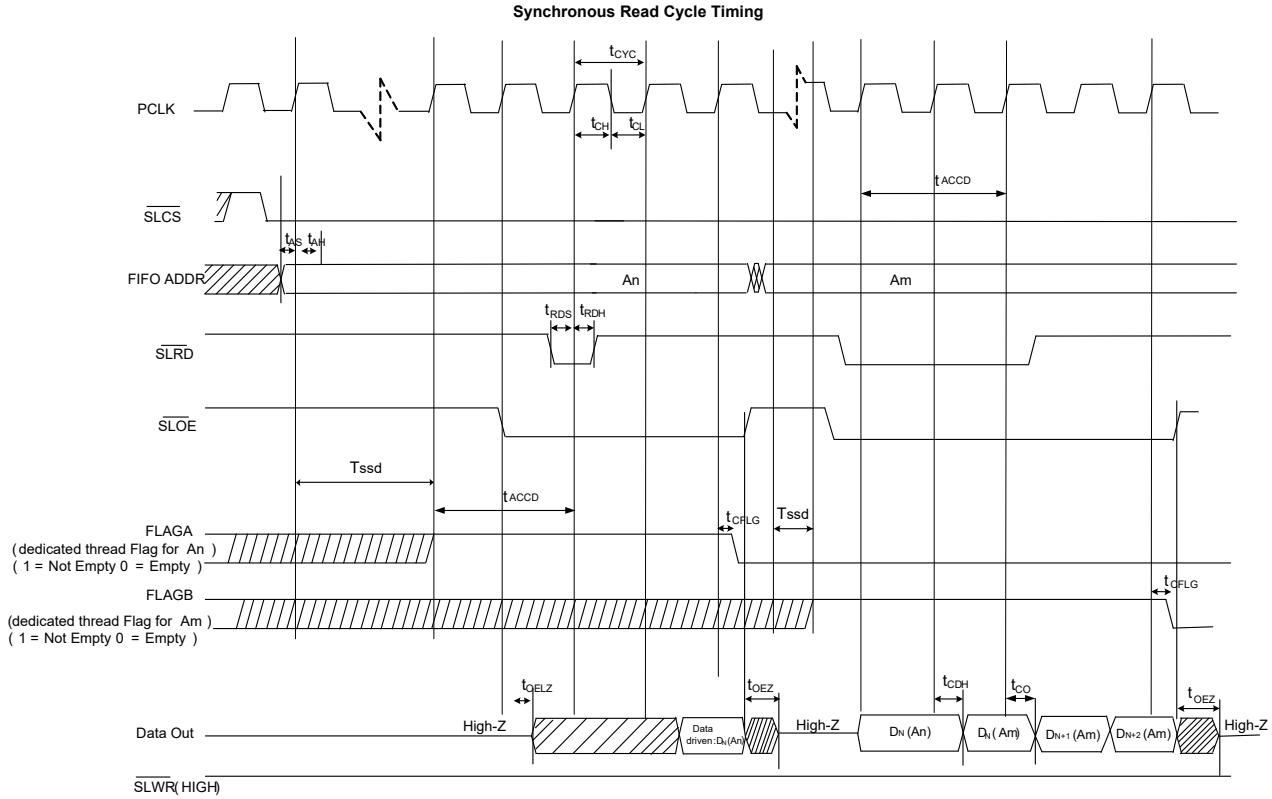
The FLAG signals are monitored for flow control by the external processor. FLAG signals are outputs from SX3 that may be configured to show empty, full, or partial status for a dedicated thread or the current thread that is addressed.

Socket Switching Delay (Tssd)

The socket-switching delay is measured from the time EPSWITCH# is asserted by the master, with the new socket address on the address bus, to the time the Current_Thread_DMA_Ready flag is asserted. For the Producer socket, the flag is asserted when it is ready to receive data in the DMA buffer. For the Consumer socket, the flag is asserted when it is ready to drive data out of the DMA buffer. For a synchronous slave FIFO interface, the switching delay is measured in the number of general configurable interface clock cycles; for an asynchronous slave FIFO interface, in PIB clock cycles. This is applicable only for the 5-bit Slave FIFO interface; there is no socket-switching delay in SX3's 2-bit Slave FIFO interface, which makes use of thread switching in the General Configurable Interface state machine.

Note: For burst mode, the SLRD# and SLOE# are asserted during the entire duration of the read. When SLOE# is asserted, the data bus is driven (with data from the previously addressed FIFO). For each subsequent rising edge of PCLK, while the SLRD# is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

Figure 10. Synchronous Slave FIFO Read Mode



Synchronous Slave FIFO Write Sequence Description

- FIFO address is stable and the signal SLCS# is asserted
- External master or peripheral outputs the data to the data bus
- SLWR# is asserted
- While the SLWR# is asserted, data is written to the FIFO and on the rising edge of the PCLK, the FIFO pointer is incremented
- The FIFO flag is updated after a delay of t_{WFLG} from the rising edge of the clock

The same sequence of events is also applicable for burst write

Note: For the burst mode, SLWR# and SLCS# are asserted for the entire duration, during which all the required data values are written. In this burst write mode, after the SLWR# is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of PCLK. The FIFO pointer is updated on each rising edge of PCLK.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a Zero-Length Packet (ZLP) to SX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and address must be driven as shown in Figure 11.

Figure 11. Synchronous Slave FIFO Write Mode

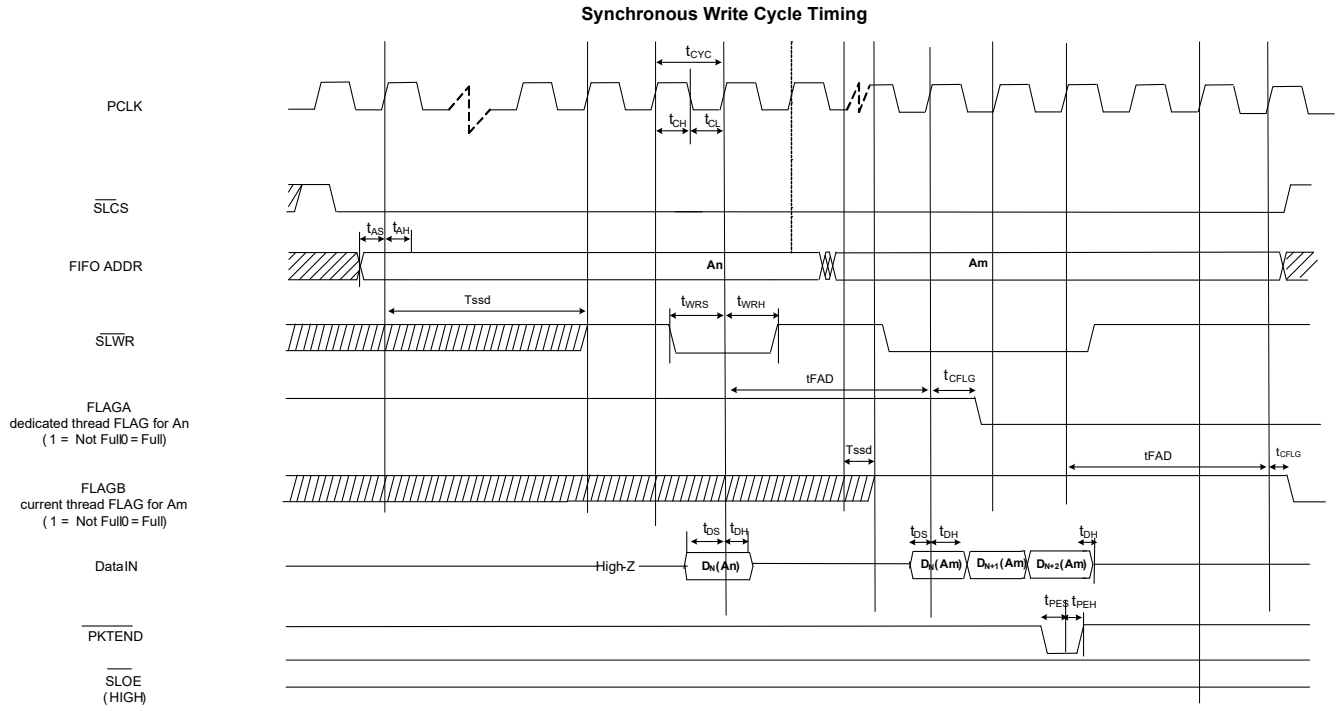


Figure 12. Synchronous Slave FIFO ZLP Write Cycle Timing

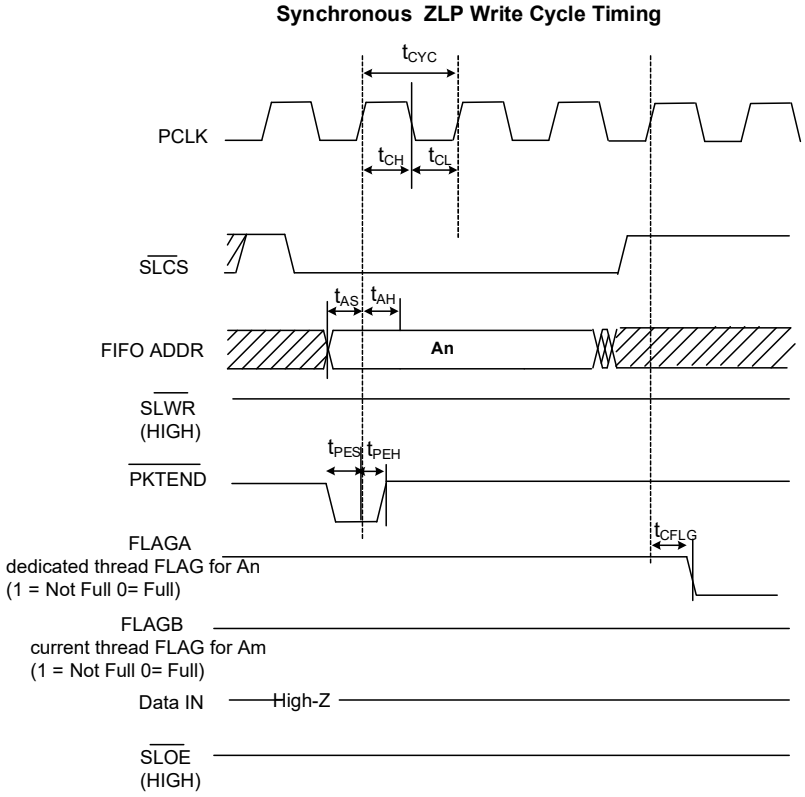


Table 12. Synchronous Slave FIFO Parameters[4]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
t_{CYC}	Clock period	10	–	ns
t_{CH}	Clock high time	4	–	ns
t_{CL}	Clock low time	4	–	ns
t_{RDS}	SLRD# to CLK setup time	2	–	ns
t_{RDH}	SLRD# to CLK hold time	0.5	–	ns
t_{WRS}	SLWR# to CLK setup time	2	–	ns
t_{WRH}	SLWR# to CLK hold time	0.5	–	ns
t_{CO}	Clock to valid data	–	7	ns
t_{DS}	Data input setup time	2	–	ns
t_{DH}	CLK to data input hold	0.5	–	ns
t_{AS}	Address to CLK setup time	2	–	ns
t_{AH}	CLK to address hold time	0.5	–	ns
t_{OELZ}	SLOE# to data low-Z	0	–	ns
t_{CFLG}	CLK to flag output propagation delay	–	8	ns
t_{OEZ}	SLOE# deassert to Data Hi Z	–	8	ns
t_{PES}	PKTEND# to CLK setup	2	–	ns
t_{PEH}	CLK to PKTEND# hold	0.5	–	ns
t_{CDH}	CLK to data output hold	2	–	ns
t_{SSD}	Socket switching delay	2	68	Clock cycles
t_{ACCD}	Latency from SLRD# to Data	2	2	Clock cycles
t_{FAD}	Latency from SLWR# to FLAG	3	3	Clock cycles

Note
4. Three-cycle latency from ADDR to DATA/FLAGS.

Serial Peripherals Timing

I^2C Timing

Figure 13. I^2C Timing Definition

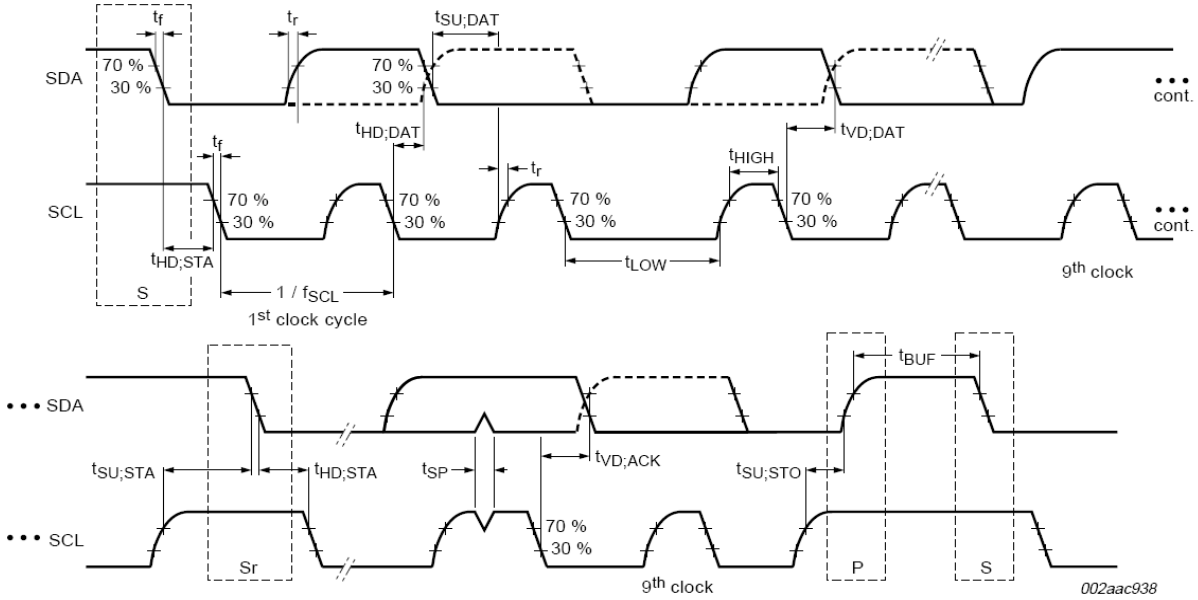


Table 13. I^2C Timing Parameters

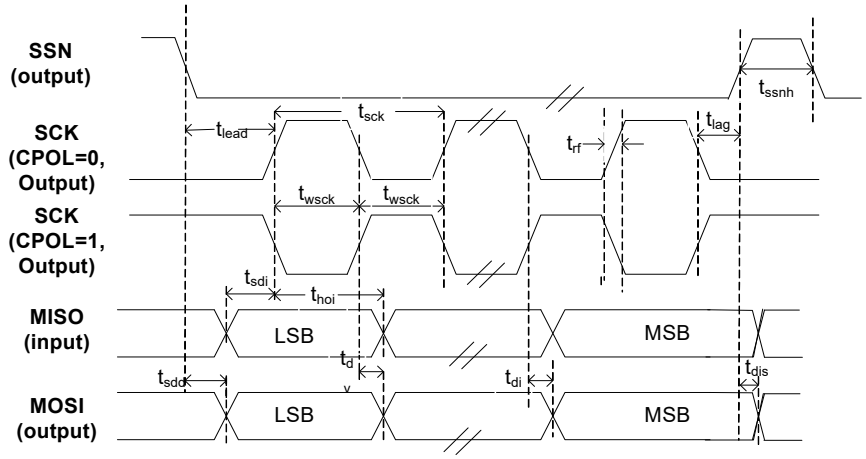
Parameter	Description	Min	Max	Unit
I^2C Standard Mode Parameters				
f_{SCL}	SCL clock frequency	0	100	kHz
t_{HD}:STA	Hold time START condition	4	–	µs
t_{LOW}	LOW period of the SCL	4.7	–	µs
t_{HIGH}	HIGH period of the SCL	4	–	µs
t_{SU}:STA	Setup time for a repeated START condition	4.7	–	µs
t_{HD}:DAT	Data hold time	0	–	µs
t_{SU}:DAT	Data setup time	250	–	ns
t_r	Rise time of both SDA and SCL signals	–	1000	ns
t_f	Fall time of both SDA and SCL signals	–	300	ns
t_{SU}:STO	Setup time for STOP condition	4	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	µs
t_{VD}:DAT	Data valid time	–	3.45	µs
t_{VD}:ACK	Data valid ACK	–	3.45	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I^2C Fast Mode Parameters				
f_{SCL}	SCL clock frequency	0	400	kHz
t_{HD}:STA	Hold time START condition	0.6	–	µs
t_{LOW}	LOW period of the SCL	1.3	–	µs
t_{HIGH}	HIGH period of the SCL	0.6	–	µs

Table 13. I²C Timing Parameters (continued)

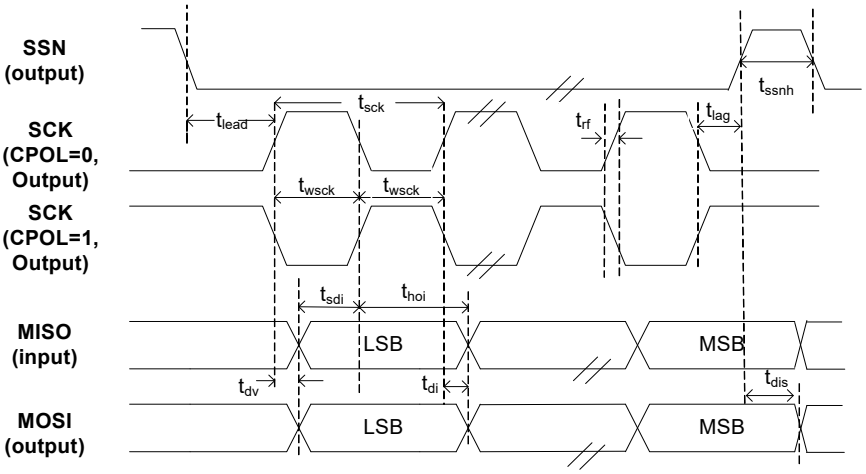
Parameter	Description	Min	Max	Unit
t_{SU}:ST_A	Setup time for a repeated START condition	0.6	–	µs
t_{HD}:DAT	Data hold time	0	–	µs
t_{SU}:DAT	Data setup time	100	–	ns
t_r	Rise time of both SDA and SCL signals	–	300	ns
t_f	Fall time of both SDA and SCL signals	–	300	ns
t_{SU}:STO	Setup time for STOP condition	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	1.3	–	µs
t_{VD}:DAT	Data valid time	–	0.9	µs
t_{VD}:ACK	Data valid ACK	–	0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter	0	50	ns
I²C Fast Mode Plus Parameters (Not supported at I2C_VDDQ = 1.2 V)				
f_{SCL}	SCL clock frequency	0	1000	kHz
t_{HD}:STA	Hold time START condition	0.26	–	µs
t_{LOW}	LOW period of the SCL	0.5	–	µs
t_{HIGH}	HIGH period of the SCL	0.26	–	µs
t_{SU}:STA	Setup time for a repeated START condition	0.26	–	µs
t_{HD}:DAT	Data hold time	0	–	µs
t_{SU}:DAT	Data setup time	50	–	ns
t_r	Rise time of both SDA and SCL signals	–	120	ns
t_f	Fall time of both SDA and SCL signals	–	120	ns
t_{SU}:STO	Setup time for STOP condition	0.26	–	µs
t_{BUF}	Bus-free time between a STOP and START condition	0.5	–	µs
t_{VD}:DAT	Data valid time	–	0.45	µs
t_{VD}:ACK	Data valid ACK	–	0.55	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter	0	50	ns

SPI Timing Specifications

Figure 14. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Table 14. SPI Timing Parameters

Parameter	Description	Min	Max	Unit
f_{op}	Operating frequency	0	33	MHz
t_{sck}	Cycle time	30	–	ns
t_{wsck}	Clock high/low time	13.5	–	ns
t_{lead}	SSN-SCK lead time	1/2 t_{sck}[5]-5	1.5 t_{sck}[5]+ 5	ns
t_{lag}	Enable lag time	0.5	1.5 t_{sck}[5]+5	ns
t_{rf}	Rise/fall time	–	8	ns
t_{sdd}	Output SSN to valid data delay time	–	5	ns
t_{dv}	Output data valid time	–	5	ns
t_{di}	Output data invalid	0	–	ns
t_{ssnh}	Minimum SSN high time	10	–	ns
t_{sdi}	Data setup time input	8	–	ns
t_{hoi}	Data hold time input	0	–	ns
t_{dis}	Disable data output on SSN high	0	–	ns

Note
5. Depends on LAG and LEAD setting in the SPI_CONFIG register.

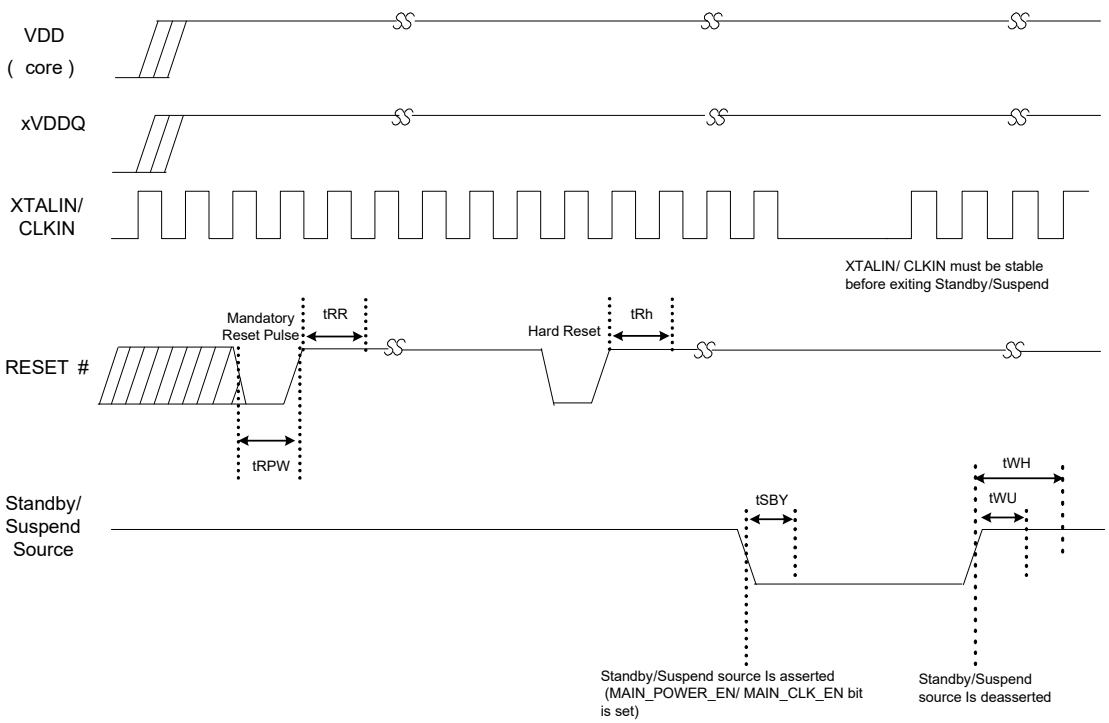
Reset Sequence

SX3's hard reset sequence requirements are specified in this section.

Table 15. Reset and Standby Timing Parameters

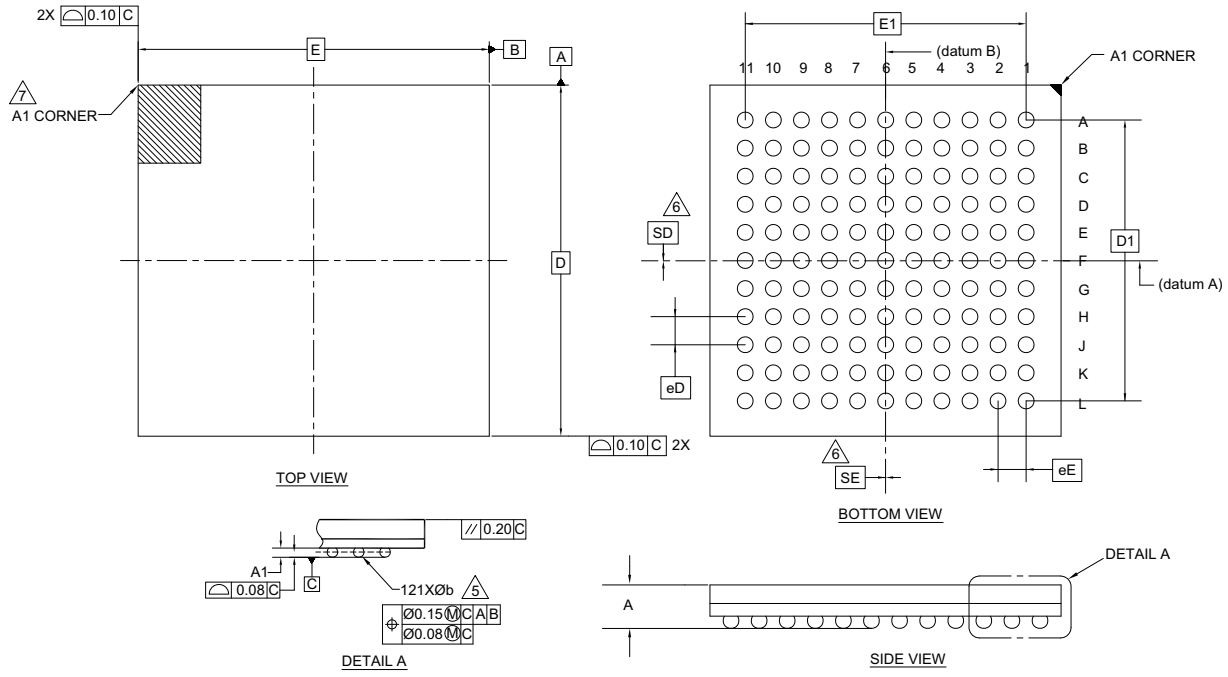
Parameter	Definition	Conditions	Min (ms)	Max (ms)
t_{RPW}	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
t_{RH}	Minimum high on RESET#	–	5	–
t_{RR}	Reset recovery time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
t_{SBY}	Time to enter standby/suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
t_{WU}	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
t_{WH}	Minimum time before Standby/Suspend source may be reasserted	–	5	–

Figure 15. Reset Sequence



Package Diagram

Figure 16. 121-ball BGA Package Diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.15	-	-
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		
E1	8.00 BSC		
MD	11		
ME	11		
N	121		
∅ b	0.25	0.30	0.35
eD	0.80 BSC		
eE	0.80 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

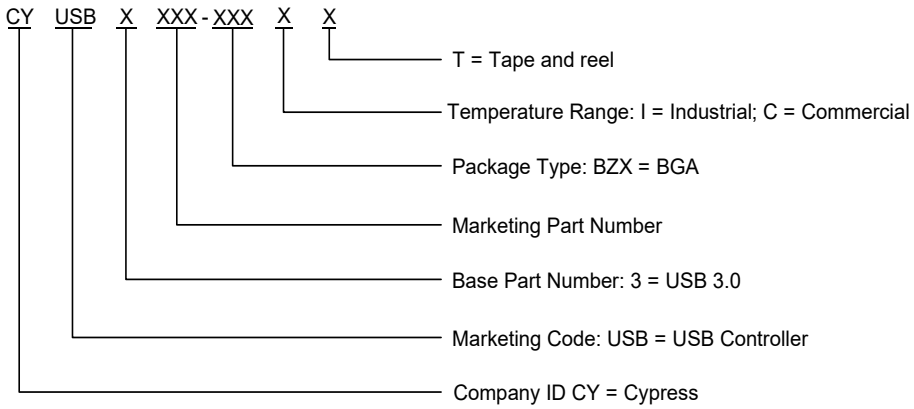
001-54471 *F

Ordering Information

Table 16. Ordering Information

Ordering Code	USB	SRAM	Data Bus Width	USB Protocol Support	Operating Temperature	Package Type
CYUSB3015-BZXC	USB 3.0	512KB	16-bit	USB Vendor Class	0 °C to +70 °C	121-ball BGA
CYUSB3015-BZXI	USB 3.0	512KB	16-bit	USB Vendor Class	-40°C to +85°C	121-ball BGA
CYUSB3016-BZXC	USB 3.0	512KB	32-bit	USB Vendor Class	0 °C to +70 °C	121-ball BGA
CYUSB3016-BZXI	USB 3.0	512KB	32-bit	USB Vendor Class	-40°C to +85°C	121-ball BGA
CYUSB3017-BZXC	USB 3.0	512KB	32-bit	USB Video Class (UVC)	0 °C to +70 °C	121-ball BGA
CYUSB3017-BZXI	USB 3.0	512KB	32-bit	USB Video Class (UVC)	-40°C to +85°C	121-ball BGA

Ordering Code Definitions



Acronyms

Table 17. Acronyms Used in this Document

Acronym	Description
DMA	direct memory access
ESD	electrostatic discharge
FIFO	first in, first out
GPIF™	general programmable interface
HBM	human body model
HNP	host negotiation protocol
I^2C	inter-integrated circuit
ISP	image signal processor
MISO	master in, slave out
MOSI	master out, slave in
MMC	multimedia card
MSC	mass storage class
MTP	media transfer protocol
OTG	on-the-go
OVP	overvoltage protection
PHY	physical layer
PLL	phase locked loop
PMIC	power management IC
PVT	process voltage temperature
RTOS	real-time operating system
SCL	serial clock line
SCLK	serial clock
SD	secure digital
SD	secure digital
SDA	serial data clock
SDI	serial data interface
SDIO	secure digital input / output
SLC	single-level cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	serial peripheral interface
SRP	session request protocol
SSN	SPI slave select (Active low)
TOF	time-of-flight
UAC	USB audio class
UVC	USB video class

Table 17. Acronyms Used in this Document

Acronym	Description
USB	universal serial bus
ZLP	zero-length packet

Document Conventions

Units of Measure

Table 18. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabits per second
MBps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Errata

This section describes the errata for Revision D of the SX3. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CYUSB301x-xxxx	All Variants

Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available Rev. D EZ-USB SX3 Configurable SuperSpeed USB Controller family devices.

Items	Part Number	Silicon Revision	Fix Status
1. Turning off VIO1 during Normal, Suspend, and Standby modes causes the SX3 to stop working.	CYUSB301x-xxxx	Rev. D	Workaround provided
2. USB enumeration failure in USB boot mode when SX3 is self-powered.	CYUSB301x-xxxx	Rev. D	Workaround provided
3. Bus collision is seen when the I2C block is used as a master in the I2C Multi-master configuration.	CYUSB301x-xxxx	Rev. D	Use SX3 in single-master configuration
4. I2C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle.	CYUSB301x-xxxx	Rev. D	No workaround needed

1. Turning off VIO1 during Normal, Suspend, and Standby modes causes the SX3 to stop working.	
Problem Definition	Turning off the VIO1 during Normal, Suspend, and Standby modes will cause the SX3 to stop working.
Parameters Affected	NA
Trigger Condition(s)	This condition is triggered when the VIO1 is turned off during Normal, Suspend, and Standby modes.
Scope of Impact	SX3 stops working.
Workaround	VIO1 must stay on during Normal, Suspend, and Standby modes.
Fix Status	No fix. Workaround is required.

2. USB enumeration failure in USB boot mode when SX3 is self-powered.	
Problem Definition	When SX3 is self-powered and not connected to the USB host, it enters low-power mode and does not wake up when connected to USB host afterwards. This is because the bootloader does not check the VBUS pin on the connector to detect USB connection. It expects that the USB bus is connected to the host when it is powered on.
Parameters Affected	NA
Trigger Condition(s)	This condition is triggered when SX3 is self-powered in USB boot mode.
Scope of Impact	Device does not enumerate
Workaround	Reset the device after connecting to USB host.
Fix Status	No fix. Workaround is required.

3. Bus collision is seen when the I^2C block is used as a master in the I^2C Multi-master configuration.	
Problem Definition	When SX3 is used as a master in the I^2C multi-master configuration, there can be occasional bus collisions.
Parameters Affected	NA
Trigger Condition(s)	This condition is triggered only when the SX3 I^2C block operates in Multi-master configuration.
Scope of Impact	The SX3 I^2C block can transmit data when the I^2C bus is not idle leading to bus collision.
Workaround	Use SX3 as a single master.
Fix Status	No fix.

4. I^2C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle.	
Problem Definition	I^2C Data Valid (tVD:DAT) parameter at 400 kHz with a 40/60 duty cycle is 1.0625 µs, which exceeds the I^2C specification limit of 0.9 µs.
Parameters Affected	NA
Trigger Condition(s)	This violation occurs only at 400 kHz with a 40/60 duty cycle of the I^2C clock.
Scope of Impact	Setup time (t_{SUDAT}) is met with a huge margin for the transmitted data for 400 kHz and so $t_{vd:DAT}$ violation will not cause any data integrity issues.
Workaround	No workaround needed.
Fix Status	No fix needed.

Document History Page

Document Title: CYUSB3015 / CYUSB3016 / CYUSB3017, EZ-USB SX3: Configurable SuperSpeed USB Controller Document Number: 002-30704			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6897108	06/24/2020	Initial release.
*A	6970371	09/23/2020	Updated Document Status from “ADVANCE” to “PRELIMINARY”. Updated Figure 6. Updated Table 5.
*B	7076787	01/28/2021	Removed “PRELIMINARY” document status. Updated Features: Updated USB 3.1 to USB 3.2. Removed text (TID # XXXXXXXXX). Updated More Information: Added reference to “AN231295”. Updated Functional Overview: Updated USB 3.1 to USB 3.2. Updated Pin Configurations: Updated “INIT#” to “INIT# / RESET”. Updated "PROGRAM# / RESET” to “PROGRAM#”.
*C	7146147	06/14/2021	Updated G6 and G7 in Table 5 and Figure 6 through Figure 8. Updated Copyright information.

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