TLE4997A8D Grade1

Programmable Linear Dual Hall Sensor

Technical Product Description

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Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2014-05-21	

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1 Overview

Characteristic	Supply Voltage	Supply Current	Sensitivity Range	Interface	Temperature
Programmable Linear Hall Sensor	4.5~5.5 V	7.5 mA	±50mT ±100mT ±200mT	Analog Ratiometric Output	-40°C to 125°C

Figure 1-1 SMD package PG-TDSO-8-2 for the TLE4997A8D Grade1

1.1 Features

- The TLE4997A8D Grade1 provides an integration of two individual programmable Linear Hall sensor IC's with ratiometric analog output signal in one package.
- 20-bit Digital Signal Processing (DSP)
- Digital temperature compensation
- 12-bit overall resolution
- Operating automotive temperature range -40°C to 125°C
- Low drift of output signal over temperature and lifetime
- Programmable parameters stored in EEPROM with single-bit error correction:
  - Magnetic range and sensitivity (gain), polarity of the output slope
  - Offset
  - Bandwidth
  - Clamping levels
  - Customer temperature compensation coefficients for all common magnets
  - Memory lock
- Re-programmable until memory lock
- Supply voltage 4.5-5.5 V (4-7 V extended range)
- Operation between -200 mT and +200 mT within three ranges
- Reverse-polarity and overvoltage protection for all pins
- Output short-circuit protection
- On-board diagnostics (wire breakage detection, EEPROM error, overvoltage)
- Digital readout of internal temperature and magnetic field values in calibration mode
- Programming and operation of multiple sensors with common power supply
- Two-point calibration of magnetic transfer function
- Precise calibration without iteration steps
- High immunity against EMC and ESD

Table 1-1 Ordering Information

Product Name	Marking	Ordering Code	Package
TLE4997A8D Grade1	-	-	PG-TDSO-8-2

1.2 Target Applications

- Robust replacement of potentiometers: No mechanical abrasion, resistant to humidity, temperature, pollution and vibration
- Linear and angular position sensing in automotive and industrial applications with highest accuracy requirements
- Suited for ASIL applications such as pedal position, throttle position and steering torque sensing
- High-current sensing e.g. for battery management or motor control

1.3 Pin Configuration

Figure 1-2 shows the location of the Hall elements in the chip pin configuration of the package.

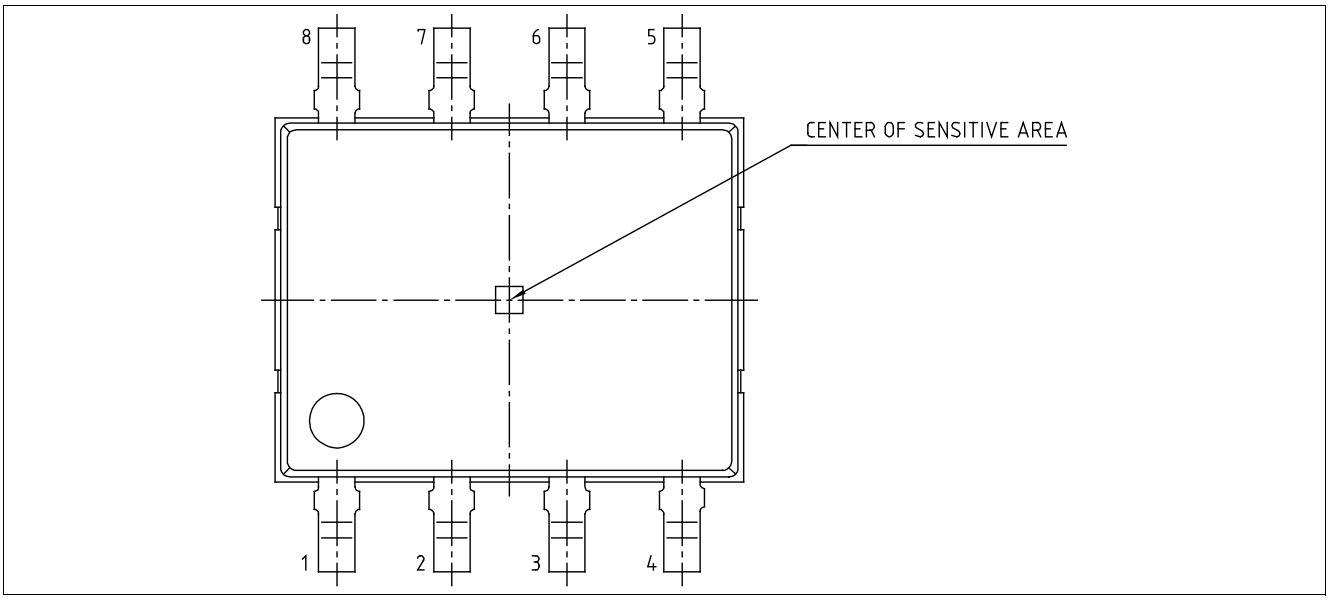

Figure 1-2 Pin Configuration of PG-TDSO-8-2 package

Table 1-2 TLE4997A8D Grade1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	n/c	not connected (connection to GND is recommended)
2	V_{DD}	Supply voltage / programming interface (top die)
3	GND	Ground (top die)
4	OUT	Output / programming interface (top die)
5	OUT	Output / programming interface (bottom die)
6	GND	Ground (bottom die)
7	V_{DD}	Supply voltage / programming interface (bottom die)
8	n/c	not connected (connection to GND is recommended)

2 General

2.1 Block Diagram

Figure 2-1 shows is a simplified block diagram.

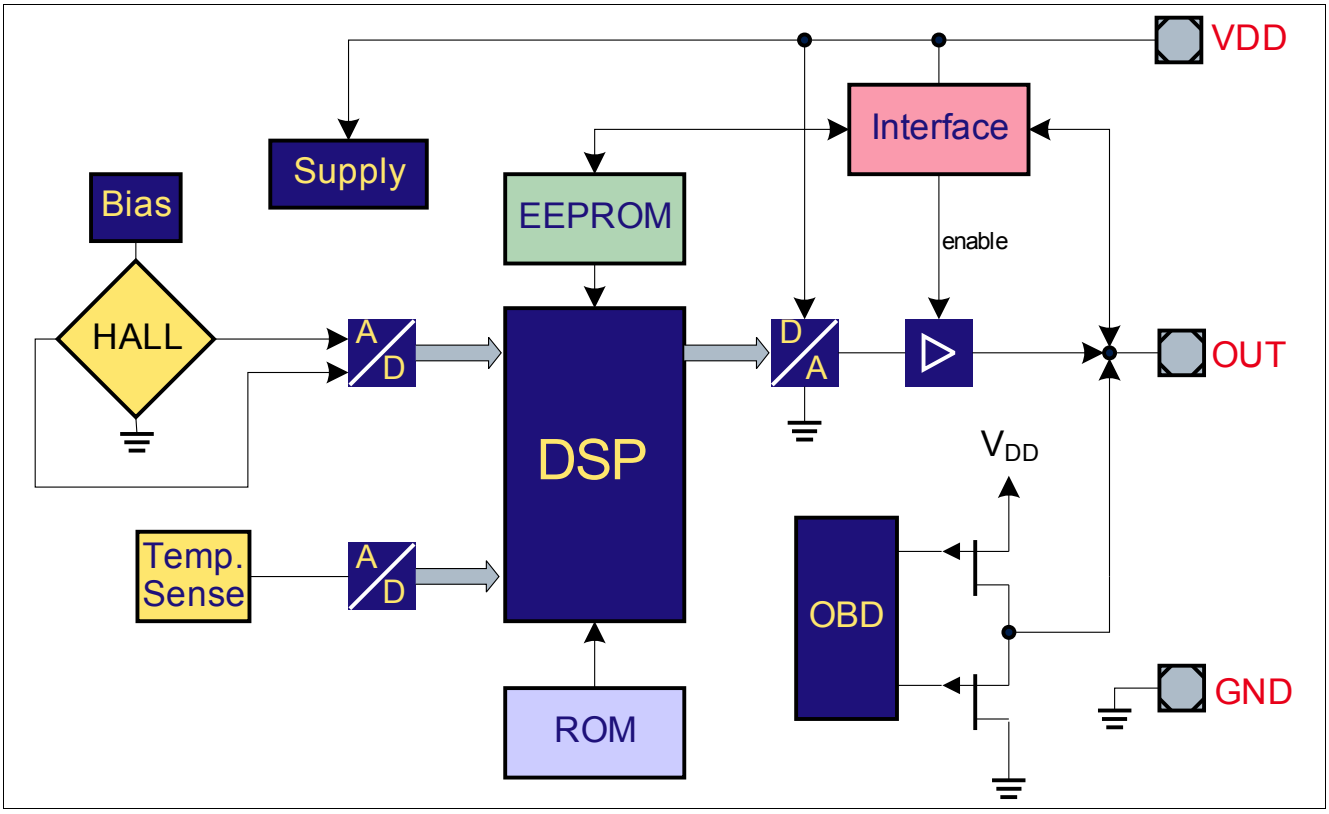

Figure 2-1 Block Diagram of the TLE4997A8D Grade1 with the ratiometric analog output interface

2.2 Functional Description

The linear Hall IC TLE4997A8D Grade1 has been designed specifically to meet the requirements of highly accurate angle and position detection, as well as for current measurement applications.

The sensor provides a ratiometric analog output voltage, which is ideally suited to Analog-to-Digital (A/D) conversion with the supply voltage as a reference.

The IC is produced in BiCMOS technology with high voltage capability and also provides reverse polarity protection.

Digital signal processing using a 16-bit DSP architecture together with digital temperature and analog stress compensation guarantees excellent stability over the whole temperature range and life time.

The minimum overall resolution is 12 bits. Nevertheless, some internal stages work with resolutions up to 20 bits.

2.3 Principle of Operation

- A magnetic flux is measured by a Hall-effect cell
- The output signal from the Hall-effect cell is converted from analog to digital signals
- The chopped Hall-effect cell and continuous-time A/D conversion ensure a very low and stable magnetic offset
- A programmable low-pass filter to reduce noise
- The temperature is measured and A/D converted
- Temperature compensation is done digitally using a second-order function
- Digital processing of the output value is based on zero field and sensitivity value
- The output value range can be clamped by digital limiters
- The final output value is D/A converted
- The output voltage is proportional to the supply voltage (ratiometric DAC)
- An On-Board-Diagnostics (OBD) circuit connects the output to V_{DD} or GND in case of errors

2.4 Further Notes

Product qualification is based on “AEC Q100 Rev. G” (Automotive Electronics Council - Stress test qualification for integrated circuits).

2.5 Transfer Functions

The examples in **Figure 2-2** show how different magnetic field ranges can be mapped to the desired output value ranges.

- Polarity Mode:
  - **Bipolar**: Magnetic fields can be measured in both orientations. The limit points do not necessarily have to be symmetrical around the zero field point
  - **Unipolar**: Only north- or south-oriented magnetic fields are measured
- Inversion: Both gain can be set to positive values, negative values or positive/negative values.

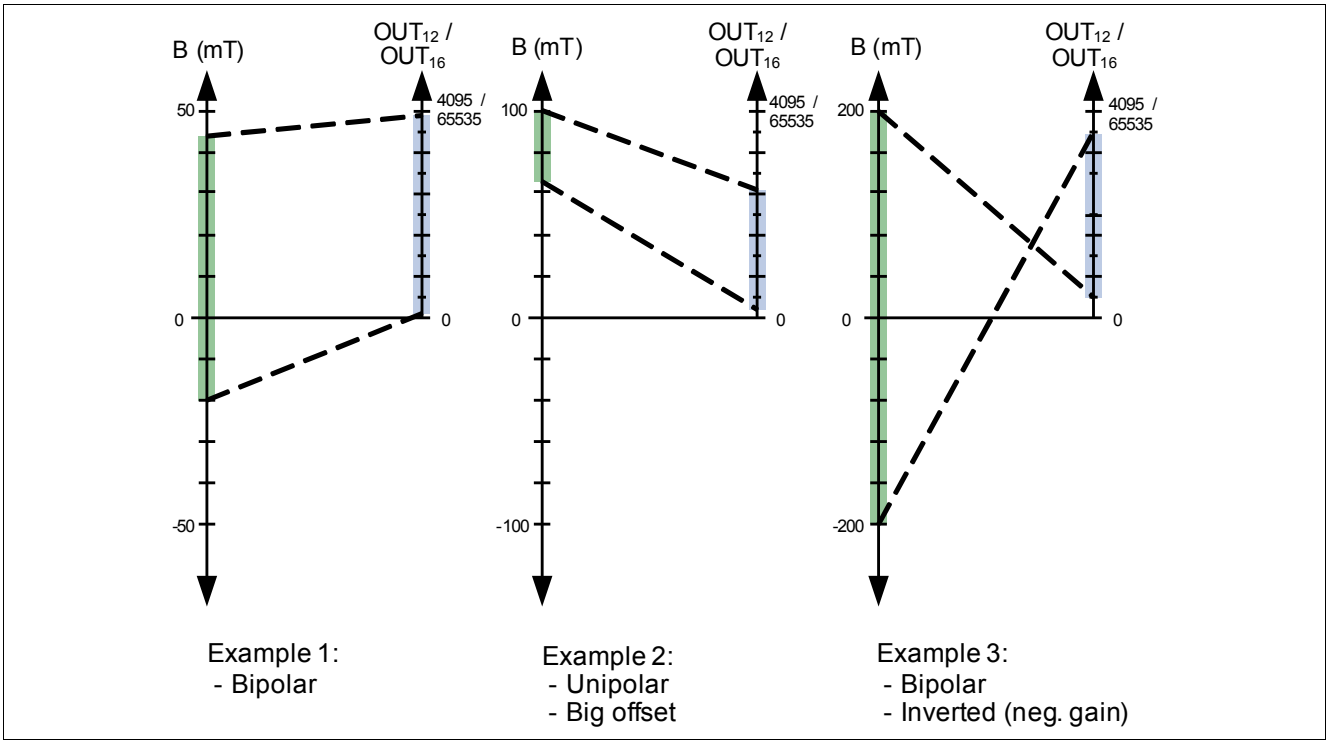

Figure 2-2 Examples of Operation

3 Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction temperature	T_J	- 40	–	140[1)]	°C	Grade 1
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-20[2)]	–	20[3)]	V	[4)] R_{THja} ≤ 150 K/W
Supply current @ overvoltage	I_{DDov}	–	–	52	mA	
Supply current @ reverse voltage	I_{DDrev}	-75	–	–	mA	
Voltage on output pin with respect to ground (V_{SS})	V_{OUTov}	-16[5)]	–	16[3)]	V	R_{THja} ≤ 150 K/W V_{OUT} may be > V_{DD}
Magnetic field	B_{MAX}	-	–	1	T	
ESD protection	V_{ESD}	-		+/- 2	kV	According HBM JESD22-A114-B[6)]

1) For limited time of 96 h. Depends on customer temperature lifetime cycles. Please ask for support by Infineon.

2) max 24 h @ -40°C ≤ Ta < 30°C
max 10 min. @ 30°C ≤ Ta < 80°C
max 30 sec. @ 80°C ≤ Ta < 125°C

3) max. 24 h @ T_J < 80°C.

4) Guaranteed by laboratory characterization, tested at ±18V.

5) Max. 1 ms @ T_J < 30°C; -8.5 V for 100 h @ T_J < 80°C.

6) 100 pF and 1.5 kΩ

4 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4997A8D Grade1. All parameters described in the following sections refer to these operating conditions if applicable or unless otherwise indicated.

Table 4-1 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4.5	–	5.5	V	
		4[1)]	–	7	V	Extended range
Output current	I_{OUT}	-1	–	1	mA	[2)]
Load resistance	R_L	10 10	– –	– –	kΩ	Pull-down to GND Pull-up to V_{DD}
Load capacitance	C_L	0	–	210	nF	
Junction temperature[3)]	T_J	- 40	–	140	°C	Example for profil see **Table 4-2**

1) May have reduced EMC robustness.

2) For V_{OUT} within the range of 5% ... 95% of V_{DD}.

3) $R_{THja} \leq 150$ K/W.

Note: Keeping signal levels within the limits described in this table ensures operation without overload conditions.

Table 4-2 Example for Ambient Temperature Profile [1)]

Temperature /°C	Active Lifetime / h
-40°C ..<20°C	100
20°C .. <60°C	600
60°C .. <90°C	8000
90°C .. <110°C	2000
110°C .. <125°C	1000
125°C	300

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results.

5 Electrical, Thermal and Magnetic Parameters

Table 5-1 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage range	V_{OUT}	5 6	–	95 94	% of V_{DD}	for $T_A \leq 120°C$ for $T_A > 120°C$
Supply current	I_{DD}	3	7.5	10	mA	1)
Output current @ OUT shorted to supply lines	I_{OUTsh}	-30	–	30	mA	for operating supply voltage range only
Zero field voltage	V_{ZERO}	-100	–	100	%	of V_{DD} 2)
Zero field voltage drift	ΔV_{ZERO}	-10	–	10	mV	In lifetime 3)
		-10	–	10	mV	error band over temp. 3)
Ratiometry error	E_{RAT}	-0.25	–	0.25	%	of V_{DD} 4)5)
Thermal resistance PG-TDSO-8-2	R_{thJA}	–	150	–	K/W	junction to air
	R_{thJC}	–	85	–	K/W	junction to case
Power-on time 6)	t_{Pon}	–	–	1	ms	$\Delta V_{OUT} \leq \pm 5\%$ of V_{DD}
			–	10		$\Delta V_{OUT} \leq \pm 1\%$ of V_{DD}
Power-on reset level	V_{DDpon}	2	–	4	V	
Output DAC quantization	ΔV_{OUT}		1.22		mV	@ V_{DD} = 5 V
Output DAC resolution	–		12		bit	
Output DAC bandwidth	f_{DAC}	–	3.2	–	kHz	interpolation filter
Differential non-linearity	DNL	-1	–	1	LSB	of output DAC
Output noise (rms)	V_{noise}	–	–	3	mV	7)
Signal delay	t_{SD}	–	–	250	µs	@ 100 Hz 8)

1) Also in extended V_{DD} range. For V_{OUT} within the range of 5%... 95% of V_{DD}, I_{OUT}= 0mA.

2) Programmable in steps of 1.22 mV (@ V_{DD} = 5 V).

3) For Sensitivity S ≤ 25 mV/mT. For higher sensitivities the magnetic offset drift is dominant. This means that for the pre calibrated (typical) 60mV/mT sensitivity the typical output drift might be given due to the allowed magnetic offset tolerance up to ±0.4mT x 60 mV/mT = ±24 mV.

4) For 4.5 V≤ $V_{DD} \leq$ 5.5 V and within nominal V_{OUT} range

5) For the maximum error in the extended voltage range

6) Response time to set up output data at power on when a constant field is applied. The first value given has a ±5% error, the second value has a ±1% error.

7) 100 mT range, sensitivity 60mV/mT, internal LP filter 244 Hz, B = 0 mT, T = 25 °C.

8) A sinusoidal magnetic field is applied, V_{OUT} shows amplitude of 20% of V_{DD}, no LP filter is selected.

Note: Take care of possible voltage drops on the V_{DD} and V_{OUT} line degrading the result. Ideally, both values are acquired and their ratio is calculated to gain the highest accuracy. This method should be used especially during calibration.

Magnetic Parameters

Table 5-2 Magnetic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sensitivity	S[1)]	±12.5	–	±300	mV/mT	programmable[2)]
Sensitivity error band over temperature	S_E	-2		2	%	[3)]
Magnetic field range	MFR	±50	±100[4)]	±200	mT	programmable[5)]
Integral nonlinearity	INL	–	–	±15	mV	= ± 0.3% of V_{DD}[6)]
Magnetic offset	B_{OS}	–	±100	±400	µT	[7)8)9)]
Magnetic offset drift	ΔB_{OS}	–	±1	±5	µT/°C	error band[8)]

1) Defined as ΔV_{OUT} / ΔB, @ V_{DD} = 5 V and T_J = 25°C.
2) Programmable in steps of 0.024%.
3) Residual sensitivity error band over temperature when using minimum 2 temperatures. Valid for 0h in dry state only. Dry is defined after following baking process: 60minutes at T=125°C.
4) This range is also used for temperature and offset pre-calibration of the IC.
5) Depending on offset and gain settings, the output may already be saturated at lower fields.
6) INL = V_{OUT} - V_{OUT}, lse with V_{OUT}, lse = least square error fit of V_{OUT}.
Valid in the range (5% of V_{DD}) < V_{OUT} < (95% of V_{DD}) for TJ ≤ 105°C
7) In operating temperature range and over lifetime.
8) For Sensitivity S > 25 mV / mT. For lower sensitivities, the zero field voltage drift is dominant.
9) Measured at ±100 mT range.

5.1 Magnetic Field Direction Definition

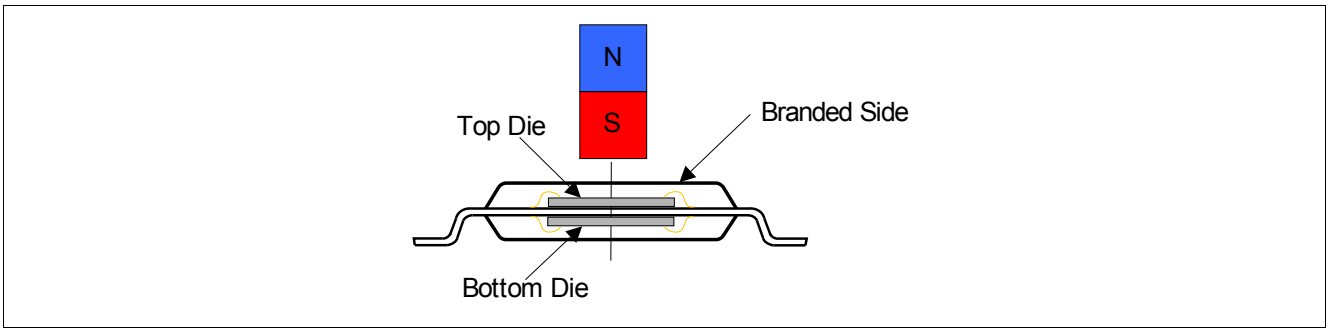

Figure 5-1 Definition of magnetic field direction of the PG-TDSO-8-2

Without reconfiguration the bottom die measures the inverted field value of the top die. This leads to a characteristics as shown in **Figure 5-2**.

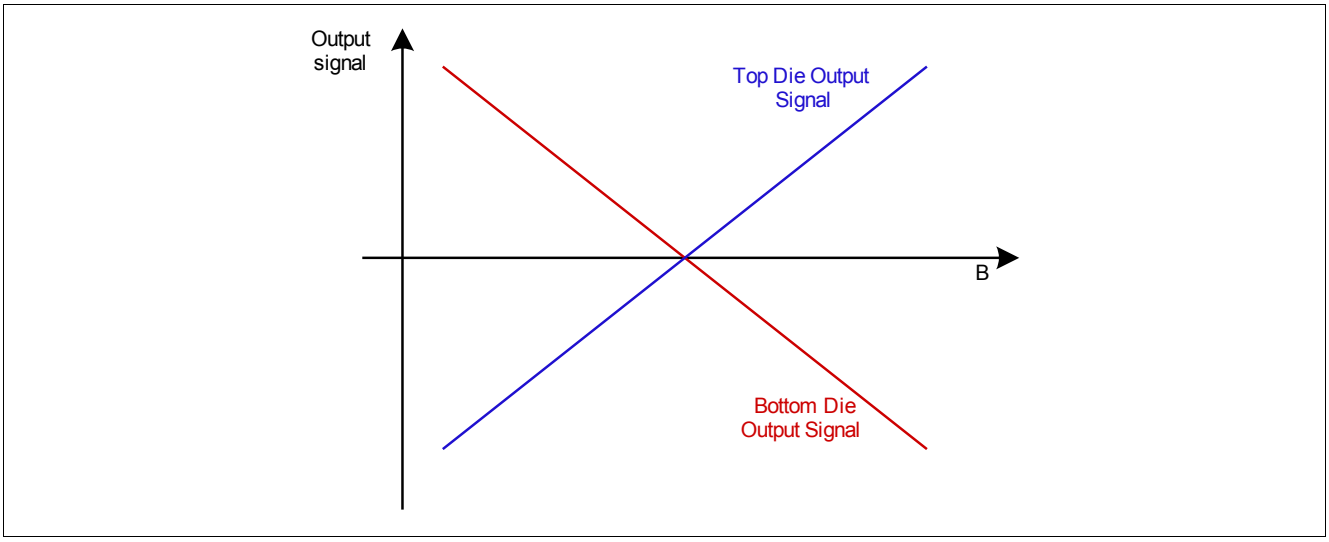

Figure 5-2 Example of the dual die output signaling

6 Application Circuit

shows the connection of two Linear Hall sensors to a micro controller.

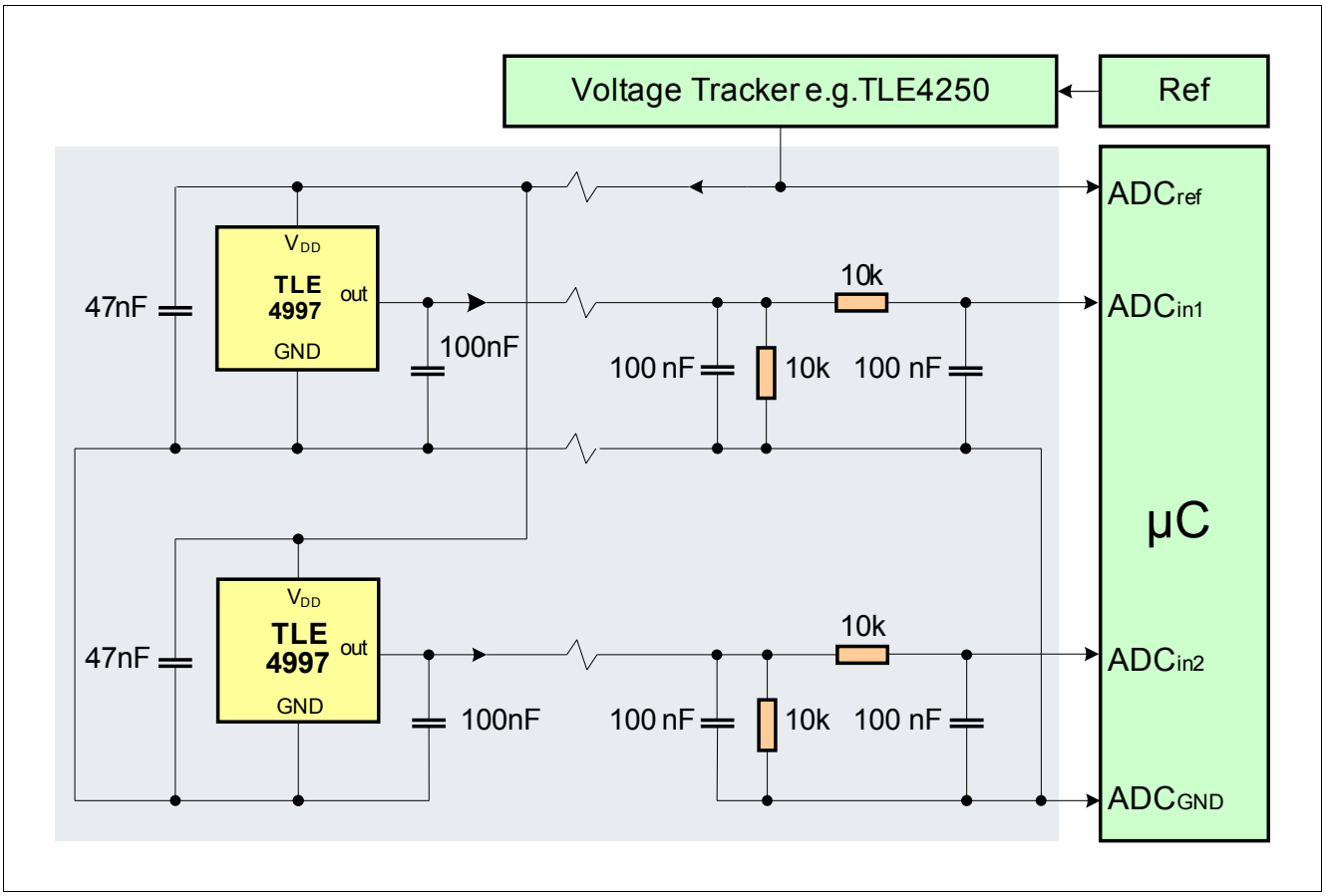

Figure 6-1 Application Circuit

Note: For calibration and programming, the interface has to be connected directly to the OUT pin.

7 PG-TDSO-8-2 Package Outlines

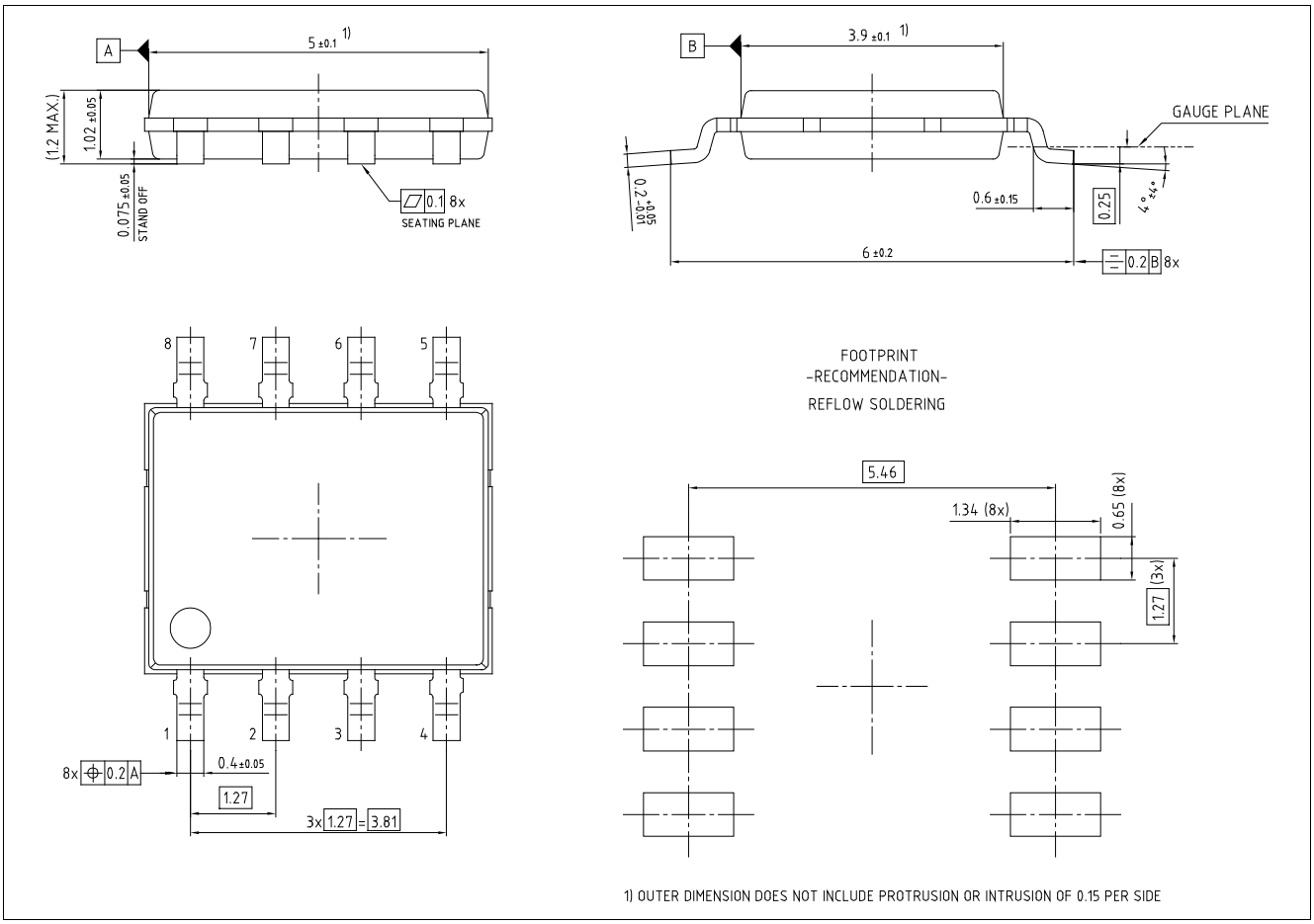

Figure 7-1 PG-TDSO-8-2 (PG-TDSO-Plastic Green Thin Dual Small Outline), Package Dimensions

7.1 Distance Chip to package

Figure 7-2 shows the distance of the chip surface to the PG-TDSO-8-2 surface.

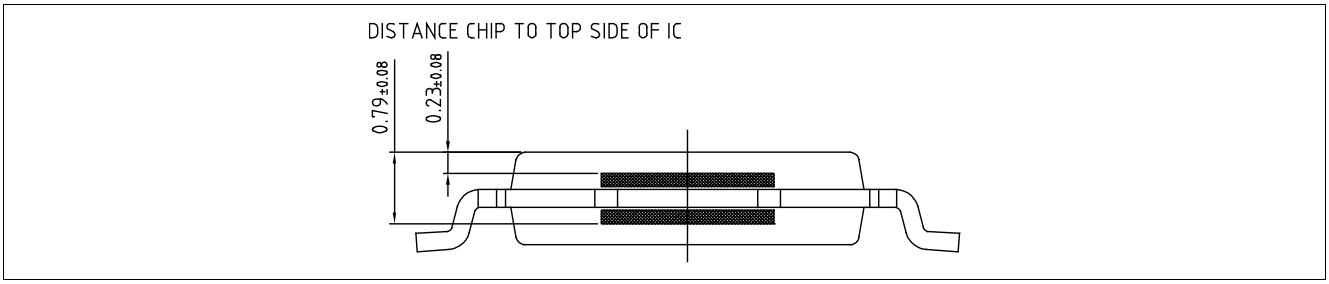

Figure 7-2 Distance of chip surface to package surface

7.2 Moisture Sensitivity Level (MSL)

The PG-TDSO-8-2 fulfills the MSL level 3 according to IPC/JEDEC J-STD-033B.1.

8 PG-TDSO-8-2 Package Marking

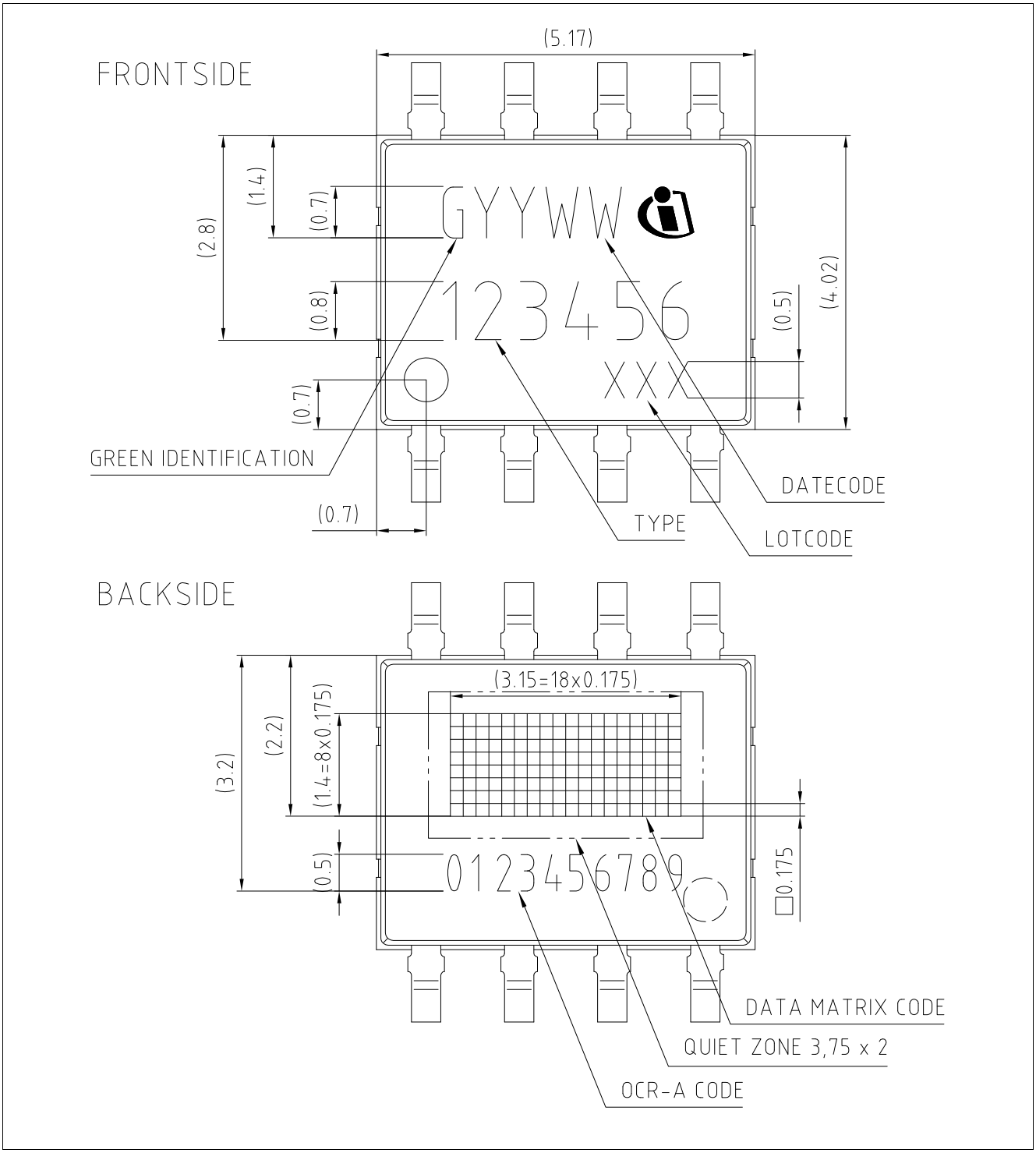

Figure 8-1 PG-TDSO-8-2 (PG-TDSO-Plastic Green Thin Dual Small Outline), Package Marking

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