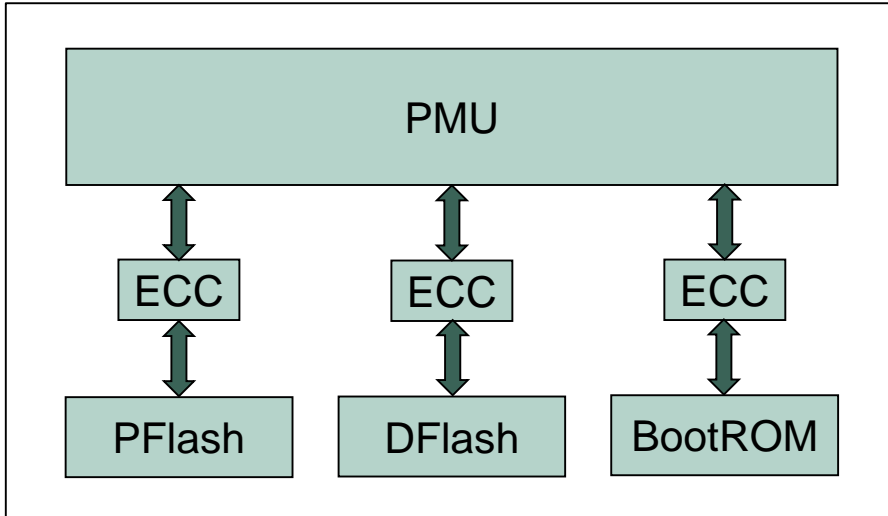


PMU

Program Memory Unit

AURIX™ TC2xx Microcontroller Training
V1.0 2019-03





Highlights

PMU enables reading out of several Program Flash (PFlash), Data Flash (DFlash) banks or BootROM.

PMU enables writing to the flashes through command sequencer and controls the flash accesses for safety and security through protections.

Key Features

HS3P cell functionality

Command sequence interface

Very high ECC correction capabilities

Customer Benefits

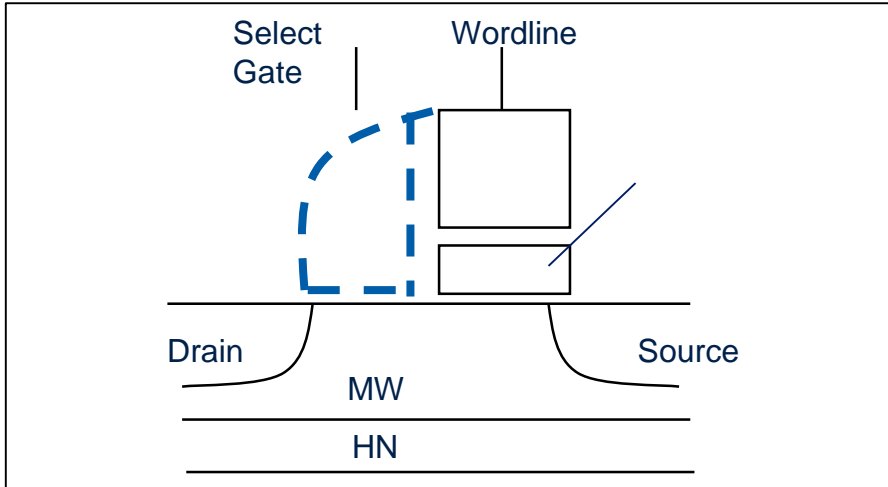
Fast Programming. For 1 MB burst, it needs ~1 s

All operations except memory mapped reads are performed with command sequences

ASIL-D optimized ECC for detection of >99% of faults in the white-noise model for PFlash

PMU

HS3P cell functionality



- > **HS3P (Hot Source 3 Poly) Cell Features**
- > **Program = Source Side Injection**
 - Fast (10 μ s) with low current (10 μ A)
- > **Erase = FN (Fowler Northeim)**
 - Well Erase (same as UCP cell)
- > **2T (two transistor) cell**
 - No Over-Erase-Algorithm (OEA) needed

> **Motivation**

- Improve Erase and Programming times
- Reduce complexity (no OEA, EEPROM handling)
- Improve competitiveness in particular for small module densities

> **Customer benefits**

- Fast Erase times (1 MB: HS3P (65 nm): <2 s, UCP (90 nm) ~ 20 s)
- Fast Programming (1 MB: HS3P (65 nm): ~1 s*, UCP (90 nm) ~ 20 s) *burst mode

Command sequence interface

List of commands for Flash control	
Reset to Read	Erase Logical Sector Range
Enter Page Mode	Verify Erased Logical Sector Range
Load Page	Resume Prog/Erase
Write Page	Disable Protection
Write Page Once	Resume Protection
Write Burst	Clear Status

- › All Flash operations except memory mapped reads are performed with command sequences. Every write access to the data flash memory range is interpreted as command cycle belonging to a command sequence
- › Write accesses to the PFlash memory range are refused with bus error
- › Command sequences consist of 1 to 9 command cycles. The command interpreter checks that a command cycle is correct in the current state of command interpretation, else a sequence error is reported
- › When the command sequence is accepted, the last command cycle finishes read mode and the Flash bank transitions into command mode

Very high ECC correction capabilities

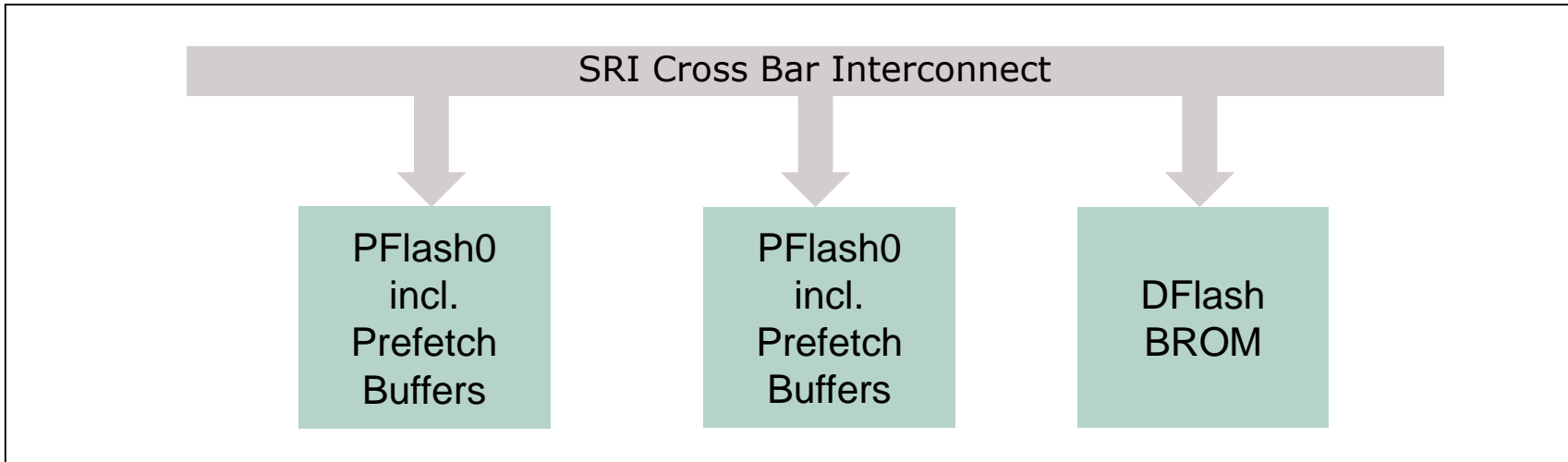
The data in Flash is stored with ECC codes. These are automatically generated when the data is programmed. When data is read, these codes are evaluated.

Program Flash

- › DEC-TED (Double Error Correction, Triple Error Detection) capabilities. Each block of 256 data bits is accompanied with a set of ECC bits
- › PFlash Safety ECC Details
 - Correction of 1-bit and 2-bit errors
 - Detection of 3-bit errors
 - Detection of >99% of all error vectors in the white noise error model
 - Detection of >99% of all-0 and all-1 cases
 - Detection of addressing errors

Data Flash

- › TEC-QED (Triple Error Correction, Quad Error Detection) capabilities. Each block of 64 data bits is accompanied with a set of ECC bits
- › DFlash Safety ECC Details
 - Correction of 1-bit, 2-bit and 3-bit errors
 - Detection of 4-bit errors
 - All-0 (data and ECC) is a correct code vector
 - All-1 (data and ECC) is a valid code vector
 - Address errors are not detected



- › All PFlash banks and DFlash/BROM can be read in parallel via dedicated SRI interface(s)
- › Access control for safety and security for all assigned memories
- › All PFlash banks have Prefetch Buffers implemented for improved read throughput to achieve higher system performance

Application Example

Simplified sequence for programming



Overview

- › “Clear Status” to clear flags
- › “Enter Page Mode”
- › Check for Page Mode status bit or error
- › Repeat “Load Page” until the page is filled
- › “Write Page”
- › Check for Program status bit or error
- › Wait for Busy bit
- › Check for Program Verification bit
- › Fail if Operational error is set

Advantages

- › Easy sequence of commands to perform all the programming steps
- › Each command has a notification bit to check when the operation is completed
- › Several kind of error bits to check during the sequence

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