

Customer training workshop: Device Configurator_Clock configuration

TRAVEO™ T2G CYT4BF series Microcontroller Training
V2.0.0 2023-04



Please read the [Important notice and warnings](#) at the end of this document

Scope of work

- › This document helps application developers understand how to use the clock configuration of the Device Configurator as part of creating a ModusToolbox™ application
 - The Device Configurator is part of a collection of tools included with the ModusToolbox™ software. It provides a GUI to configure the target device.

- › ModusToolbox™ tools package version
 - 3.0.0
- › Device Configurator version
 - 4.0
- › Device
 - The TRAVEO™ T2G CYT4BFBCH device is used in this code example.
- › Board
 - The TRAVEO™ T2G KIT_T2G-B-H_EVK board is used for testing.

- › **Clock system for TRAVEO™ T2G body high has the following features:**
 - Supports high and low-speed clocks, using both internal and external clock sources.
 - Internal real time clock (RTC) for the clock input.
 - Supports phase-locked loop (PLL) and frequency-locked loop (FLL) to generate clocks that operate the internal circuit at a high speed.
 - Supports a function to monitor clock operation and to measure the clock difference of each clock with reference to a known clock.

Introduction (contd.)

› **Clock configuration in Device Configurator:**

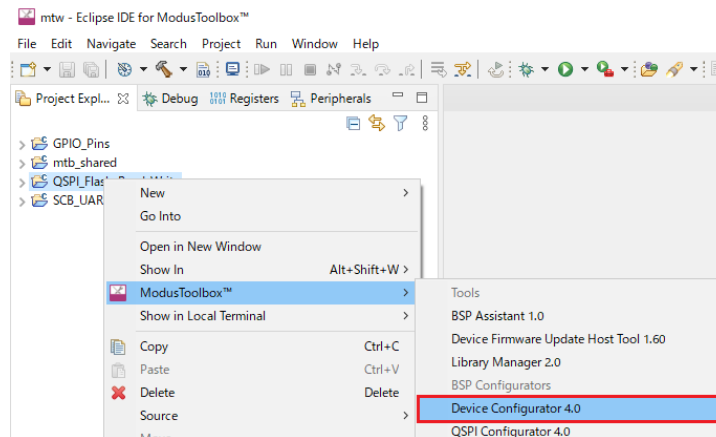
- The device configurator allows to configure the following clocks:
 - System clocks
 - FLL
 - PLL0/1 (200MHz PLL), PLL400M0/1 (400MHz PLL)
 - High-frequency clocks
 - CLK_HF0 to CLK_HF7
 - Input clocks
 - ECO, EXTCLK, ILO0, ILO1
 - IMO (locked enabled by default because it is not supported)
 - WCO (enabled on startup timing)
 - Miscellaneous clocks
 - CLK_ALT_SYS_TICK, CLK_BAK, CLK_LF, ECO pre-scaler etc
 - Peripheral clock dividers
 - Peripheral clock dividers (8-bit, 16-bit, and 24.5-bit)

Launch the Device Configurator

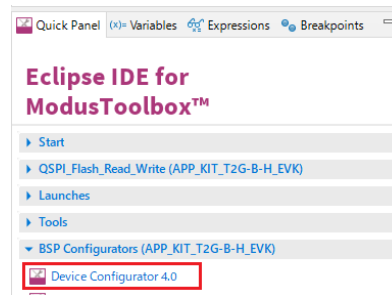
> From Eclipse IDE

You can launch the Device Configurator by following either of these methods:

- a) Right-click on the project in the Project Explorer and select ModusToolbox™ > Device Configurator <version>



- b) Click the Device Configurator link in the Quick Panel



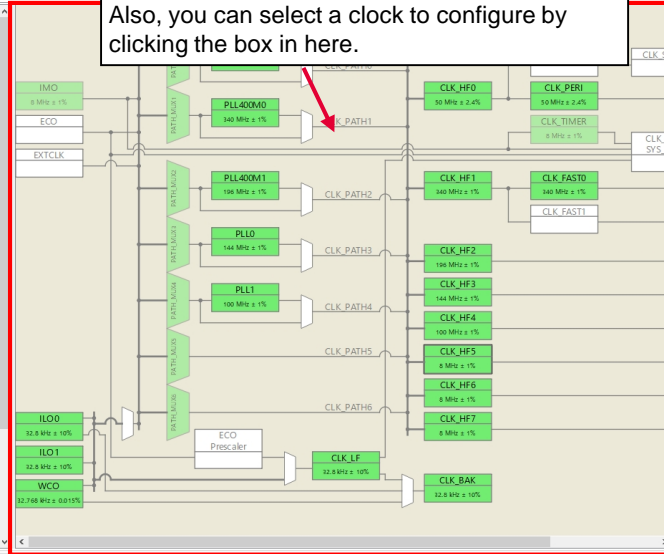
Device Configurator for clock configuration

> Device Configurator view – System tab

- Configure each of the clocks (system clocks, high-frequency clocks, input clocks, miscellaneous clocks)

Select the used clock, such as system clocks, high-frequency clocks, and input clocks.

Show the output frequency by current setting. Also, you can select a clock to configure by clicking the box in here.



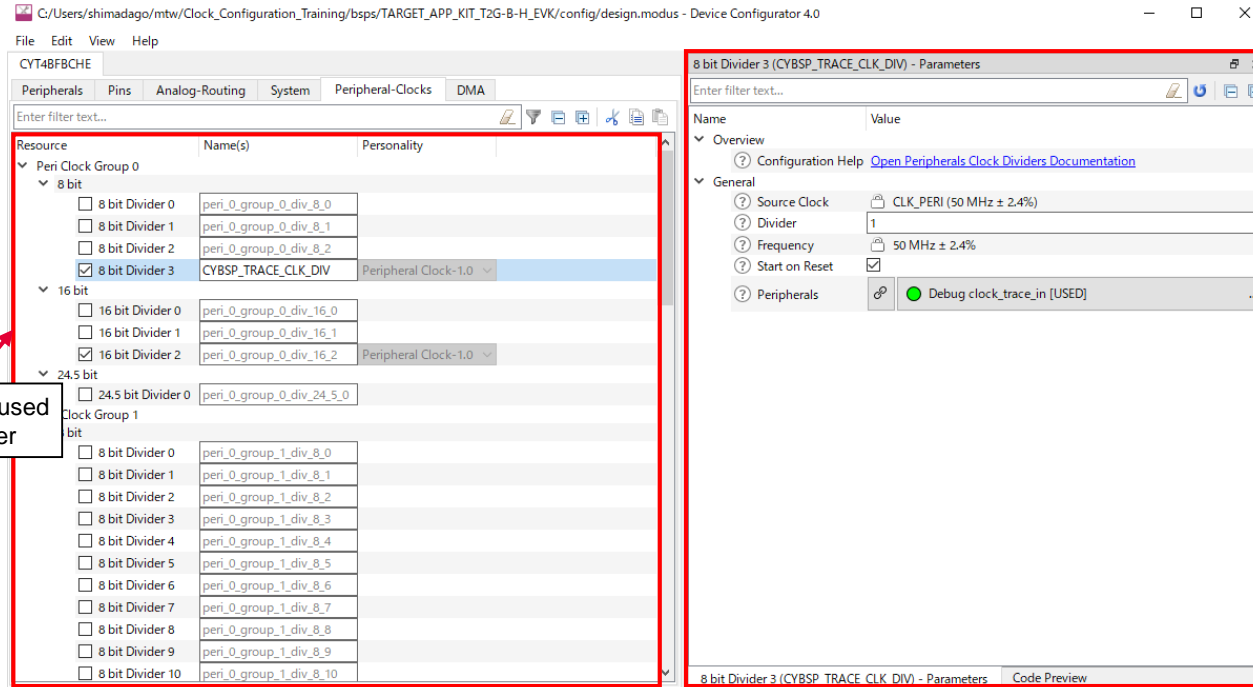
Configure the parameters of selected clock

If you select the check box of the resource clock to be used, it reflects in the clock supply system diagram in the middle window, and the details are displayed in the parameter window

Device Configurator for clock configuration (contd.)

› Device Configurator view – Peripheral-Clocks tab

– Configure peripheral clock dividers



Select the used clock divider

Configure the parameters of the selected divider, and display setting in the Code Preview tab

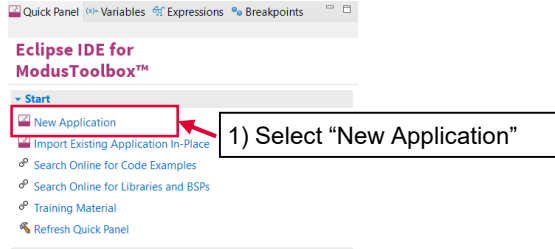
What the Device Configurator can do for Clock Settings

- › **Follow these steps to use the Device Configurator for clock setting:**
 - Save the file to generate source code.
 - The Device Configurator generates code into a "GeneratedSource" directory in your Eclipse IDE application, or in the same location you saved the *.modus file for non-IDE applications. That directory contains the necessary source (.c) and header (.h) files for the generated firmware, which uses the relevant driver APIs to configure the hardware.
 - No additional settings are required as the clock settings use a preconfigured structure in Device Configurator. It is set in the ***cybsp_init()*** function in main.c.

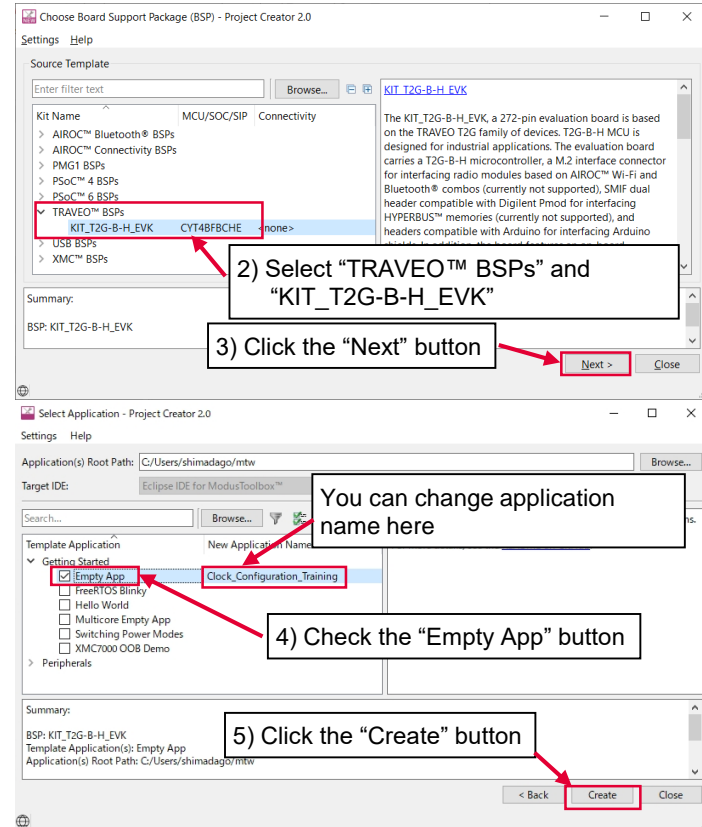
Clock configuration

> Create project

- 1) Click “New Application” in the Quick Panel and open the Choose Board Support Package (BSP) window



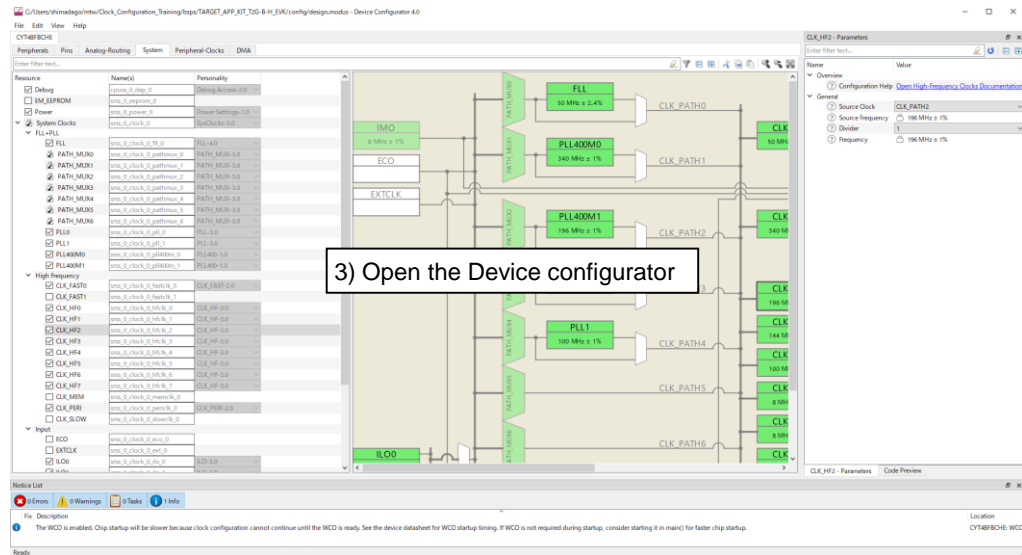
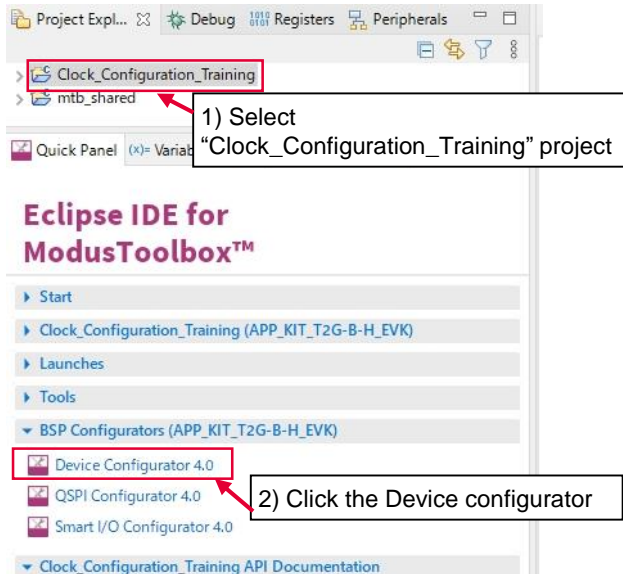
- 2) Select “TRAVEO™ BSPs” and “KIT_T2G-B-H_EVK”
- 3) Click the “Next” button and open the Application window
- 4) Check the “Empty App” button
In this use case, it changes to “Clock_Configuration_training”. You can change the application name.
- 5) Click the Create button to start application creation



Clock configuration (contd.)

› Launch the Device Configurator

- 1) Select the “Clock_configuration_training” project.
- 2) Click the Device configurator in the Quick Panel
- 3) Then, open the Device Configurator window



Setting example: CPU clocks

> Use case

- Input clocks
 - IMO: 8.0000 MHz
- System clocks
 - PLL400M0: Input ECO, Output 100.000 MHz
 - PLL400M1: Input ECO, Output 350.000 MHz
- High-frequency clocks
 - CLK_HF0: Input PLL400M0 (CLK_PATH1), Output 100.000 MHz (Divide by 1)
 - CLK_HF1: Input PLL400M1 (CLK_PATH2), Output 350.000 MHz (Divide by 1)
- Output
 - CLK_MEM: Output 100.000 MHz (Divide CLK_HF0 by 1)
 - CLK_SLOW: Output 100.000 MHz (Divide CLK_MEM by 1), connected to CM0+ clock input
 - CLK_FAST0: Output 350.000 MHz (Divide CLK_HF1 by 1), connected to CM7 instance 0 clock input.
 - CLK_FAST1: Output 350.000 MHz (Divide CLK_HF1 by 1), connected to CM7 instance 1 clock input

Setting example: CPU clocks (contd.)

> Input clocks

Input	srss_0_clock_0_*	ECO-3.0
<input checked="" type="checkbox"/> ECO	srss_0_clock_0_eco_0	ECO-3.0
<input type="checkbox"/> EXTCLK	srss_0_clock_0_ext_0	
<input checked="" type="checkbox"/> ILO0	srss_0_clock_0_ilo_0	ILO-3.0
<input checked="" type="checkbox"/> ILO1	srss_0_clock_0_ilo_1	
<input checked="" type="checkbox"/> IMO	srss_0_clock_0_imo_0	IMO-3.0
<input checked="" type="checkbox"/> WCO	srss_0_clock_0_wco_0	WCO-3.0

IMO - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open SysClk Documentation
General	
Frequency	8 MHz ± 1%

Setting example: CPU clocks (contd.)

> System clocks (PATH_MUX1/2, PLL400M0/1)

The image shows a configuration tool interface for setting system clocks. It consists of three main parts:

- Component Selection:** A tree view under 'FLL+PLL' shows the selection of:
 - PATH_MUX1 (for PLL#0 input)
 - PATH_MUX2 (for PLL#1 input)
 - PLL400M0
 - PLL400M1
- PATH_MUX1 - Parameters:** The 'Source Clock' parameter is set to 'IMO'.
- PATH_MUX2 - Parameters:** The 'Source Clock' parameter is set to 'IMO'.
- PLL400M0 - Parameters:** The 'Desired Frequency (MHz)' is set to '100.000'.
- PLL400M1 - Parameters:** The 'Desired Frequency (MHz)' is set to '350.000'.

Setting example: CPU clocks (contd.)

> High-frequency clocks (CLK_HF1, CLK_HF2)

High Frequency

<input checked="" type="checkbox"/>	CLK_FAST0	srss_0_clock_0_fastclk_0	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_FAST1	srss_0_clock_0_fastclk_1	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_HF0	srss_0_clock_0_hfclk_0	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF1	srss_0_clock_0_hfclk_1	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF2	srss_0_clock_0_hfclk_2	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF3	srss_0_clock_0_hfclk_3	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF4	srss_0_clock_0_hfclk_4	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF5	srss_0_clock_0_hfclk_5	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF6	srss_0_clock_0_hfclk_6	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF7	srss_0_clock_0_hfclk_7	CLK_HF-3.0

Select CLK_HF0

Select CLK_HF1

CLK_HF0 - Parameters

Enter filter text...

Name	Value
Source Clock	CLK_PATH1
Source Frequency	100 MHz
Divider	1
Frequency	100 MHz

Select CLK_PATH1 as Source Clock

Divide by 1

CLK_HF1 - Parameters

Enter filter text...

Name	Value
Source Clock	CLK_PATH2
Source Frequency	350 MHz
Divider	1
Frequency	350 MHz

Select CLK_PATH2 as Source Clock

Divide by 1

You can see output clock after divider setting

Setting example: CPU clocks (contd.)

> Output (CLK_MEM, CLK_SLOW, CLK_FAST0/1)

High Frequency

<input checked="" type="checkbox"/>	CLK_FAST0	srss_0_clock_0_fastclk_0
<input checked="" type="checkbox"/>	CLK_FAST1	srss_0_clock_0_fastclk_1
<input checked="" type="checkbox"/>	CLK_HF0	srss_0_clock_0_hfclk_0
<input checked="" type="checkbox"/>	CLK_HF1	srss_0_clock_0_hfclk_1
<input checked="" type="checkbox"/>	CLK_HF2	srss_0_clock_0_hfclk_2
<input checked="" type="checkbox"/>	CLK_HF3	srss_0_clock_0_hfclk_3
<input checked="" type="checkbox"/>	CLK_HF4	srss_0_clock_0_hfclk_4
<input checked="" type="checkbox"/>	CLK_HF5	srss_0_clock_0_hfclk_5
<input checked="" type="checkbox"/>	CLK_HF6	srss_0_clock_0_hfclk_6
<input checked="" type="checkbox"/>	CLK_HF7	srss_0_clock_0_hfclk_7
<input checked="" type="checkbox"/>	CLK_MEM	srss_0_clock_0_memclk_0
<input checked="" type="checkbox"/>	CLK_PERI	srss_0_clock_0_periclk_0
<input checked="" type="checkbox"/>	CLK_SLOW	srss_0_clock_0_slowclk_0

Select each clocks

CLK_MEM - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open Mem Clock Documentation
General	
Source Clock	100 MHz
Divider	1
Frequency	100 MHz

Divide by 1

CLK_SLOW - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open Slow Clock Documentation
General	
Source Clock	100 MHz
Divider	1
Frequency	100 MHz

Divide by 1

CLK_FAST0 - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open Fast Clock Documentation
General	
Source Clock	CLK_HF1 (350 MHz)
Integer Divider	1
Fractional Divider	0
Frequency	350 MHz

Divide by 1

CLK_FAST1 - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open Fast Clock Documentation
General	
Source Clock	CLK_HF1 (350 MHz)
Integer Divider	1
Fractional Divider	0
Frequency	350 MHz

Divide by 1

Setting example: I2S clock

> Use case

- Input clocks
 - ECO: 16.0000 MHz
- System clocks
 - PLL400M1: Input ECO, Output 196.608 MHz
- High-frequency clocks
 - CLK_HF5: Input PLL400M1 (CLK_PATH2), Output 196.608 MHz (Divide by 1)
- Output
 - Audio (I2S): Output 24.576 MHz (Divide CLK_HF5 by 8)

Setting example: I2S clock (contd.)

> Input clocks

Select ECO		
<input checked="" type="checkbox"/>	ECO	srss_0_clock_0_eco_0 ECO-3.0
<input type="checkbox"/>	EXTCLK	srss_0_clock_0_ext_0
<input checked="" type="checkbox"/>	ILO0	srss_0_clock_0_ilo_0 ILO-3.0
<input checked="" type="checkbox"/>	ILO1	srss_0_clock_0_ilo_1 ILO-3.0
<input checked="" type="checkbox"/>	IMO	srss_0_clock_0_imo_0 IMO-3.0
<input checked="" type="checkbox"/>	WCO	srss_0_clock_0_wco_0 WCO-3.0

ECO - Parameters

Enter filter text...

Name:

Overview

- Configuration Help [Open ECO Documentation](#)

General

Frequency (MHz)	16.0000
Accuracy (±ppm)	0
Accuracy (±%)	0
Drive Level (µW)	100
Equivalent Series Resistance ESR (ohm)	50
Crystal Shunt Capacitance C0 (pF)	0
Parallel Load Capacitance Cload (pF)	18

Connections

Input		P21[2] analog (CYBSP_ECO_IN) [USED] ...
Output		P21[3] analog (CYBSP_ECO_OUT) [USED] ...

Setting example: I2S clock (contd.)

> System clocks (PATH_MUX2, PLL400M1)

The screenshot shows three windows from a configuration tool:

- Left Window:** A tree view under 'FLL+PLL'. 'PATH_MUX2' and 'PLL400M1' are selected and highlighted with red boxes. Callouts point to them: 'Select PATH_MUX2 for PLL#0 input' and 'Select PLL400M1'.
- Middle Window (PATH_MUX2 - Parameters):** Shows the 'General' tab with 'Source Clock' set to 'ECO'. A red box highlights 'ECO' with a callout: 'Select the ECO'.
- Right Window (PLL400M1 - Parameters):** Shows the 'General' tab with 'Configuration' set to 'Automatic' and 'Desired Frequency (MHz)' set to '196.608'. A red box highlights '196.608' with a callout: 'Set 196.608 MHz'.

Setting example: I2S clock (contd.)

> High-frequency clocks (CLK_HF5) and audio (I2S) output

High Frequency

<input checked="" type="checkbox"/>	CLK_FAST0	srss_0_clock_0_fastclk_0	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_FAST1	srss_0_clock_0_fastclk_1	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_HF0	srss_0_clock_0_hfclk_0	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF1	srss_0_clock_0_hfclk_1	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF2	srss_0_clock_0_hfclk_2	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF3	srss_0_clock_0_hfclk_3	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF4	srss_0_clock_0_hfclk_4	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF5	srss_0_clock_0_hfclk_5	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF6	srss_0_clock_0_hfclk_6	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF7	srss_0_clock_0_hfclk_7	CLK_HF-3.0

Select CLK_HF5

CLK_HF5 - Parameters

Enter filter text...

Name	Value
Overview	Configuration Help Open High-Frequency Clocks Documentation
General	<ul style="list-style-type: none"> Source Clock: CLK_PATH2 (Select CLK_PATH2 as Source Clock) Source Frequency: 196.608 MHz Divider: 8 (Divide by 8) Frequency: 24.576 MHz Clock Output: <unassigned>

You can see output clock after divider setting

Setting example: ADC clock

> Use case

- Input clocks
 - IMO: 8.0000 MHz
- System clocks
 - PLL400M1: Input IMO, Output 196 MHz
- High-frequency clocks
 - CLK_HF2: Input PLL400M1 (CLK_PATH2), Output 196 MHz (Divide by 1)
- Output (Peripheral Clock Group 1)
 - 16 bit Divider 0: Output 13.07 MHz (Divide CLK_HF2 by 15)
- See the EVTGEN_trigger_ADC application for operation

Setting example: ADC clock (contd.)

> Input clocks

Input		
<input checked="" type="checkbox"/>	ECO	srss_0_clock_0_eco_0 ECO-3.0
<input type="checkbox"/>	EXTCLK	srss_0_clock_0_ext_0
<input checked="" type="checkbox"/>	ILO0	srss_0_clock_0_ilo_0 ILO-3.0
<input checked="" type="checkbox"/>	ILO1	srss_0_clock_0_ilo_0 ILO-3.0
<input checked="" type="checkbox"/>	IMO	srss_0_clock_0_imo_0 IMO-3.0
<input checked="" type="checkbox"/>	WCO	srss_0_clock_0_wco_0 WCO-3.0

Select IMO

IMO - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open SysCk Documentation
General	
Frequency	8 MHz ± 1%

Confirm Input Clock is 8.000 MHz

8 MHz ± 1%

Setting example: ADC clock (contd.)

> System clocks (PATH_MUX2, PLL400M1)

Component List:

Component	Source	Destination
FLL	srss_0_clock_0_fil_0	FLL-4.0
PATH_MUX0	srss_0_clock_0_pathmux_0	PATH_MUX-3.0
PATH_MUX1	srss_0_clock_0_pathmux_1	PATH_MUX-3.0
PATH_MUX2	srss_0_clock_0_pathmux_2	PATH_MUX-3.0
PATH_MUX3	srss_0_clock_0_pathmux_3	PATH_MUX-3.0
PATH_MUX4	srss_0_clock_0_pathmux_4	PATH_MUX-3.0
PATH_MUX5	srss_0_clock_0_pathmux_5	PATH_MUX-3.0
PATH_MUX6	srss_0_clock_0_pathmux_6	PATH_MUX-3.0
PLL0	srss_0_clock_0_pll_0	PLL-3.0
PLL1	srss_0_clock_0_pll_1	PLL-3.0
PLL400M0	srss_0_clock_0_pll400m_0	PLL400-1.0
PLL400M1	srss_0_clock_0_pll400m_1	PLL400-1.0

PATH_MUX2 - Parameters

Name	Value
Source Clock	IMO
Source Frequency	8 MHz ± 1%

PLL400M1 - Parameters

Name	Value
Source Frequency	8 MHz
Low Frequency Mode	false
Configuration	Automatic
Desired Frequency (MHz)	196.000
Optimization	Min Power
Feedback (16-200)	73
Reference (1-16)	1
Output (2-16)	3
Fraction divider (0-16777215)	8388608
Fraction Dither	false
Fraction Enable	true
Actual Frequency	196 MHz ± 1%

Setting example: ADC clock (contd.)

> High-frequency clocks (CLK_HF2)

High Frequency

<input checked="" type="checkbox"/>	CLK_FAST0	srss_0_clock_0_fastclk_0	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_FAST1	srss_0_clock_0_fastclk_1	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_HF0	srss_0_clock_0_hfclk_0	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF1	srss_0_clock_0_hfclk_1	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF2	srss_0_clock_0_hfclk_2	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF3	srss_0_clock_0_hfclk_3	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF4	srss_0_clock_0_hfclk_4	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF5	srss_0_clock_0_hfclk_5	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF6	srss_0_clock_0_hfclk_6	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF7	srss_0_clock_0_hfclk_7	CLK_HF-3.0

Select CLK_HF2

CLK_HF2 - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help Open High-Frequency Clocks Documentation	
General	
Source Clock	CLK_PATH2
Source Frequency	196 MHz
Divider	1
Frequency	196 MHz

Select CLK_PATH2 as Source Clock

Divide by 1

You can see output clock after divider setting

Setting example: ADC clock (contd.)

> Output (Peripheral Clock Group 1)

Resource	Name(s)	Personality
<ul style="list-style-type: none"> <ul style="list-style-type: none"> > 8 bit > 16 bit > 24.5 bit 		
<ul style="list-style-type: none"> <ul style="list-style-type: none"> > 8 bit > 16 bit 		
<input checked="" type="checkbox"/> 16 bit Divider 0	peri_0_group_1_div_16_0	Peripheral Clock-1.0
<input type="checkbox"/> 16 bit Divider 1	peri_0_group_1_div_16_1	
<input type="checkbox"/> 16 bit Divider 2	peri_0_group_1_div_16_2	

Select 16 bit Divider 0

16 bit Divider 0 - Parameters

Enter filter text...

Name	Value
<ul style="list-style-type: none"> <ul style="list-style-type: none"> Configuration Help Open Peripheral General <ul style="list-style-type: none"> Source Clock CLK_HF2 (196 MHz ± 1%) Divider 15 Frequency 13.07 MHz ± 1% Start on Reset Peripherals 12-bit SAR ADC 0 clock_sar (ADC) [USED] 	<div style="border: 1px solid black; padding: 2px; display: inline-block;">Divide by 15</div> <div style="border: 1px solid black; padding: 2px; display: inline-block;">Select connection peripheral (SAR ADC0)</div>

You can see output clock after divider setting

Setting example: CAN FD clock

> Use case

- Input clocks
 - ECO: 16.0000 MHz
- System clocks
 - PLL400M1: Input ECO, Output 200 MHz
- High-frequency clocks
 - CLK_HF2: Input PLL400M1 (CLK_PATH2), Output 200 MHz (Divide by 1)
- Output (Peripheral Clock Group 1)
 - 16 bit Divider 0: Output 40 MHz (Divide CLK_HF2 by 5)
- See the CAN_FD application for operation

Setting example: CAN FD clock (contd.)

> Input clocks

Input	srss_0_clock_0_...	...
<input checked="" type="checkbox"/> ECO	srss_0_clock_0_ext_0	
<input type="checkbox"/> EXTCLK	srss_0_clock_0_ext_0	
<input checked="" type="checkbox"/> ILO0	srss_0_clock_0_ilo_0	ILO-3.0
<input checked="" type="checkbox"/> ILO1	srss_0_clock_0_ilo_1	ILO-3.0
<input checked="" type="checkbox"/> IMO	srss_0_clock_0_imo_0	IMO-3.0
<input checked="" type="checkbox"/> WCO	srss_0_clock_0_wco_0	WCO-3.0

ECO - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open ECO Documentation
General	
Frequency (MHz)	16.0000
Accuracy (\pm ppm)	0
Accuracy (\pm %)	0
Drive Level (μ W)	100
Equivalent Series Resistance ESR (ohm)	50
Crystal Shunt Capacitance C0 (pF)	0
Parallel Load Capacitance Cload (pF)	18
Connections	
Input	P21[2] analog (CYBSP_ECO_IN) [USED] ...
Output	P21[3] analog (CYBSP_ECO_OUT) [USED] ...

Setting example: CAN FD clock (contd.)

> System clocks (PATH_MUX1, PLL400M1)

The image shows three screenshots from a configuration tool:

- Left Screenshot:** A tree view under 'FLL+PLL'. The 'PATH_MUX2' and 'PLL400M1' items are highlighted with red boxes. A callout box points to 'PATH_MUX2' with the text 'Select PATH_MUX2 for PLL#0 input'. Another callout box points to 'PLL400M1' with the text 'Select PLL400M1'.
- Middle Screenshot:** The 'PATH_MUX2 - Parameters' window. The 'Source Clock' is set to 'ECO', which is highlighted with a red box. A callout box points to 'ECO' with the text 'Select the ECO'.
- Right Screenshot:** The 'PLL400M1 - Parameters' window. The 'Desired Frequency (MHz)' is set to '200.000', which is highlighted with a red box. A callout box points to '200.000' with the text 'Set 200 MHz'.

Setting example: CAN FD clock (contd.)

> High-frequency clocks (CLK_HF2) and Peripheral group 1 Output

High Frequency

<input checked="" type="checkbox"/>	CLK_FAST0	srss_0_clock_0_fastclk_0	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_FAST1	srss_0_clock_0_fastclk_1	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_HF0	srss_0_clock_0_hfclk_0	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF1	srss_0_clock_0_hfclk_1	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF2	srss_0_clock_0_hfclk_2	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF3	srss_0_clock_0_hfclk_3	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF4	srss_0_clock_0_hfclk_4	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF5	srss_0_clock_0_hfclk_5	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF6	srss_0_clock_0_hfclk_6	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF7	srss_0_clock_0_hfclk_7	CLK_HF-3.0

Select CLK_HF2

CLK_HF2 - Parameters

Enter filter text...

Name	Value
Overview	
Configuration Help	Open High-Frequency Clocks Documentation
General	
Source Clock	CLK_PATH2
Source Frequency	200 MHz
Divider	1
Frequency	200 MHz

Select CLK_PATH2 as Source Clock

Divide by 1

You can see output clock after divider setting

Setting example: CAN FD clock (contd.)

> Output (Peripheral Clock Group 1)

Resource	Name(s)	Personality
<ul style="list-style-type: none"> <ul style="list-style-type: none"> > 8 bit > 16 bit > 24.5 bit <ul style="list-style-type: none"> > 8 bit <ul style="list-style-type: none"> <input checked="" type="checkbox"/> 16 bit Divider 0 <input type="checkbox"/> 16 bit Divider 1 <input type="checkbox"/> 16 bit Divider 2 <input type="checkbox"/> 16 bit Divider 3 	<ul style="list-style-type: none"> <ul style="list-style-type: none"> <ul style="list-style-type: none"> peri_0_group_1_div_16_0 peri_0_group_1_div_16_1 peri_0_group_1_div_16_2 peri_0_group_1_div_16_3 	<ul style="list-style-type: none"> Peripheral Clock-1.0

Select 16 bit Divider 0

16 bit Divider 0 - Parameters

Enter filter text...

Name	Value
<ul style="list-style-type: none"> <ul style="list-style-type: none"> Configuration Help Open Peripherals Clock Dividers Documentation <ul style="list-style-type: none"> General Source Clock <input type="checkbox"/> CLK_HF2 (200 MHz) Divider <input type="text" value="5"/> Frequency <input type="text" value="40 MHz"/> Start on Reset <input checked="" type="checkbox"/> Peripherals <input type="checkbox"/> Channel 1 clock_can (CANFD) [USED] 	<ul style="list-style-type: none"> Divide by 5 Select connection peripheral (CANFD)

You can see output clock after divider setting

Setting example: UART clock

› Use case

- Input clocks
 - IMO: 8.0000 MHz
- System clocks
 - PLL400M1: Input IMO, Output 196 MHz
- High-frequency clocks
 - CLK_HF2: Input PLL400M1 (CLK_PATH2), Output 196 MHz (Divide by 1)
- Output
 - Peripheral group 1: Output 920.2 kHz (Divide CLK_HF2 by 213)
- See the SCB_UART_Transmit_and_Receive_using_DMA application for operation

Setting example: UART clock (contd.)

> Input clocks

A screenshot of a configuration menu titled 'Input'. It lists several clock sources with checkboxes and dropdown menus. The 'IMO' option is selected and highlighted with a red box. A red arrow points from the 'IMO' box to a text box that says 'Select IMO'. Other options include ECO, EXTCLK, ILO0, ILO1, and WCO.

Checkbox	Label	Internal Name	Version
<input checked="" type="checkbox"/>	ECO	srss_0_clock_0_eco_0	ECO-3.0
<input type="checkbox"/>	EXTCLK	srss_0_clock_0_ext_0	
<input checked="" type="checkbox"/>	ILO0	srss_0_clock_0_ilo_0	ILO-3.0
<input checked="" type="checkbox"/>	ILO1	srss_0_clock_0_ilo_1	ILO-3.0
<input checked="" type="checkbox"/>	IMO	srss_0_clock_0_imo_0	IMO-3.0
<input checked="" type="checkbox"/>	WCO	srss_0_clock_0_wco_0	WCO-3.0

A screenshot of the 'IMO - Parameters' dialog box. The 'Frequency' field is highlighted with a red box and contains the text '8 MHz ± 1%'. A red arrow points from this box to another text box that says 'Confirm Input Clock is 8.000 MHz'. The dialog also shows a search bar and an 'Overview' section with a link to 'Open SysClk Documentation'.

IMO - Parameters

Enter filter text...

Name	Value
Frequency	8 MHz ± 1%

Setting example: UART clock (contd.)

> System clocks (PATH_MUX2, PLL400M1)

The screenshot shows the Infineon configuration tool interface. On the left, a tree view under 'FLL+PLL' shows the selection of 'PATH_MUX2' and 'PLL400M1'. Annotations indicate 'Select PATH_MUX2 for PLL#0 input' and 'Select PLL400M1'. The main area shows two configuration windows:

- PATH_MUX2 - Parameters:** The 'Source Clock' is set to 'IMO', annotated with 'Select the IMO'. The 'Source Frequency' is '8 MHz ± 1%'.
- PLL400M1 - Parameters:** The 'Desired Frequency (MHz)' is set to '196.000', annotated with 'Set 196 MHz'. The 'Actual Frequency' is '196 MHz ± 1%'.

Setting example: UART clock (contd.)

> High-frequency clocks (CLK_HF2) and Peripheral group 1 Output

High Frequency

<input checked="" type="checkbox"/>	CLK_FAST0	srss_0_clock_0_fastclk_0	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_FAST1	srss_0_clock_0_fastclk_1	CLK_FAST-2.0
<input checked="" type="checkbox"/>	CLK_HF0	srss_0_clock_0_hfclk_0	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF1	srss_0_clock_0_hfclk_1	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF2	srss_0_clock_0_hfclk_2	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF3	srss_0_clock_0_hfclk_3	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF4	srss_0_clock_0_hfclk_4	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF5	srss_0_clock_0_hfclk_5	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF6	srss_0_clock_0_hfclk_6	CLK_HF-3.0
<input checked="" type="checkbox"/>	CLK_HF7	srss_0_clock_0_hfclk_7	CLK_HF-3.0

Select CLK_HF2

CLK_HF2 - Parameters

Enter filter text...

Name	Value
Overview	Configuration Help Open High-Frequency Clocks Documentation
General	
Source Clock	CLK_PATH2
Source Frequency	196 MHz
Divider	1
Frequency	196 MHz

Select CLK_PATH2 as Source Clock

Divide by 1

You can see output clock after divider setting

Setting example: UART clock (contd.)

> Output (Peripheral Clock Group 1)

Resource	Name(s)	Personality
<ul style="list-style-type: none"> ▼ Peri Clock Group 0 <ul style="list-style-type: none"> > 8 bit > 16 bit > 24.5 bit ▼ Peri Clock Group 1 <ul style="list-style-type: none"> 8 bit <ul style="list-style-type: none"> <input checked="" type="checkbox"/> 8 bit Divider 0 <input type="checkbox"/> 8 bit Divider 1 	<ul style="list-style-type: none"> peri_0_group_1_div_8_0 peri_0_group_1_div_8_1 	<ul style="list-style-type: none"> Peripheral Clock-1.0

Select 8 bit Divider 0

8 bit Divider 0 - Parameters

Enter filter text...

Name Value **Divide by 213**

▼ Overview

Configuration Help [Open Peripherals Clock Dividers Documentation](#)

▼ General

Source Clock **CLK HF2 (196 MHz ± 1%)**

Divider **213**

Frequency **920.2 kHz ± 1%**

Start on Reset

Peripherals **Serial Communication Block (SCB) 3 clock (KIT_UART) [USED]**

You can see output clock after divider setting

References

Datasheet

- › [CYT4BF datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family](#)

Architecture Technical reference manual

- › [TRAVEO™ T2G automotive body controller high family architecture technical reference manual](#)

Registers Technical reference manual

- › [TRAVEO™ T2G Automotive body controller high registers technical reference manual](#)

PDL/HAL

- › [PDL](#)

- › [HAL](#)

Training

- › [TRAVEO™ T2G Training](#)

Application note

- › Clock configuration setup for TRAVEO™ T2G family MCUs in ModusToolbox™ (Doc No. 002-35303)

Revision History

Revision	ECN	Submission Date	Description of Change
**	7845000	2022/12/07	Initial release
*A	7897805	2023/04/05	Updated to change IMO to ECO for CAN FD use case in “Setting example: CAN FD clock”.

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