

SPU

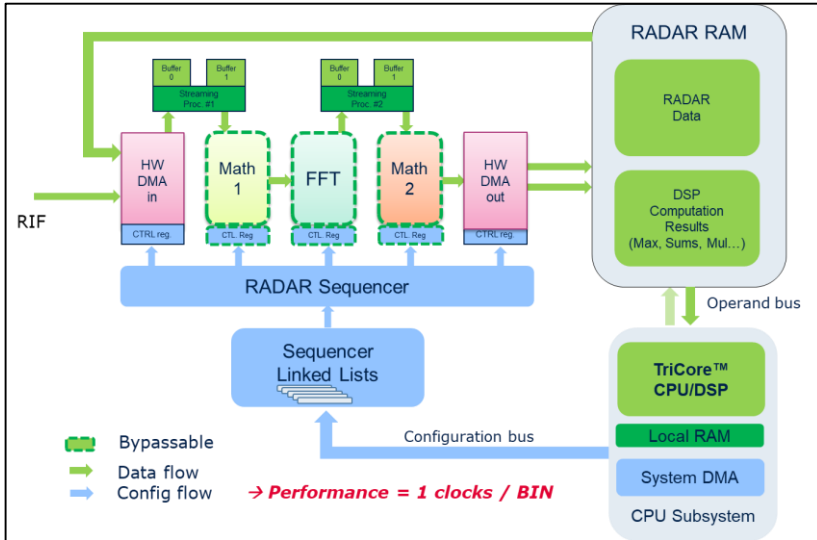
Signal Processing Unit

AURIX™ TC3xx Microcontroller Training
V1.0 2020-06



SPU

Signal processing Unit



Highlights

- > The SPU processes ADC data coming from the RIF. The SPU can also take input from the radar memory thus enabling recirculation of the data
- > Pipeline processing centered around the FFT engine with pre and post processing modules tailored for radar application

Key Features

Pipeline processing tailored for radar applications

3D input DMA

Radar sequencer

Customer Benefits

- > Fast Radar signal processing with no CPU intervention
- > Fast and seamless Data Cube manipulation
- > Limited CPU intervention to load and trigger new SPU configuration

Pipeline processing tailored for radar applications

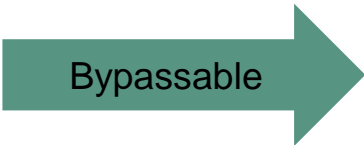
HW
DMA
In

- >2 alternative data sources:
 - ADC conversion results
 - Radar RAM → 3D DMA

Math
1

- Complex vector multiplication
- Complex windowing
- Multiple antenna support
- Support for modulation schemes

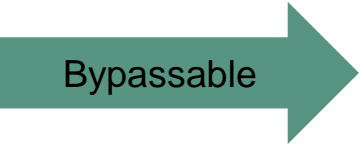
Bypassable



FFT

- FFT type (Real, Complex)
- FFT length (4 up to 2048)
- FFT precision (16bits) or 32bits)

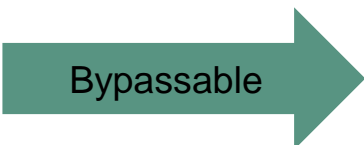
Bypassable



Math
2

- Power domain / Complex domain
- Integration (NCI / DBF)
- Threshold (simple / CFAR)
- Local Max
- Statistics...

Bypassable



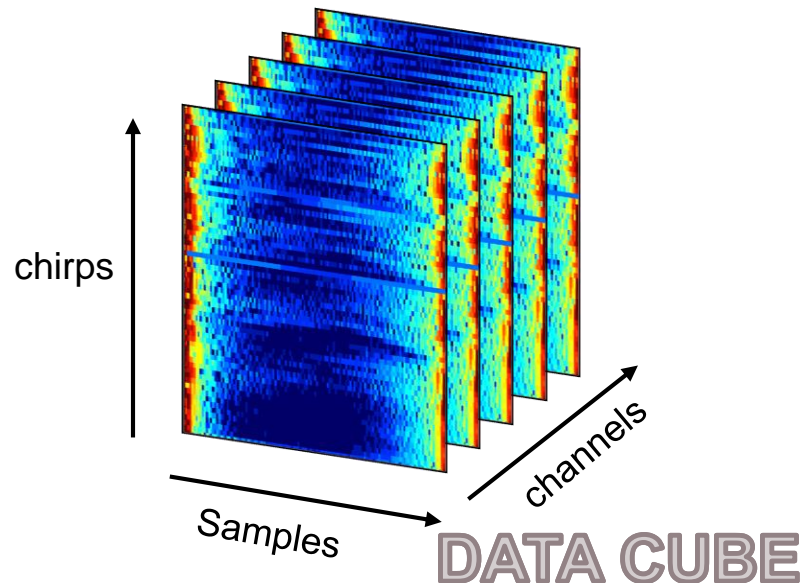
HW
DMA
out

- Allows to select which Data are saved to radar memory
- Bin rejection (range cut off / CFAR)
- In place FFT option

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3D input DMA

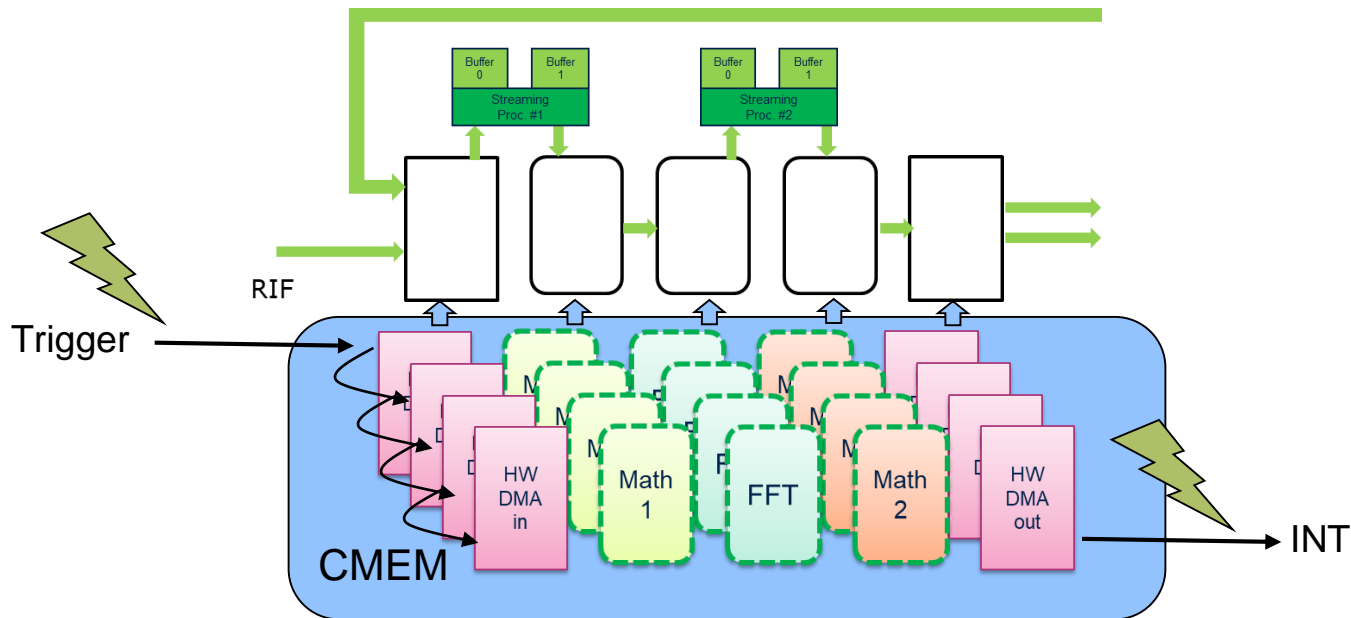
- › The SPU is able to reload the data from the radar memory following the 3 radar dimensions: fast time, slow time, channels
- › It implements inner loop, outer loop, sample loop
 - Fully configurable base address, inner loop increment and outer loop increment
 - Configured by Radar sequencer



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Radar sequencer

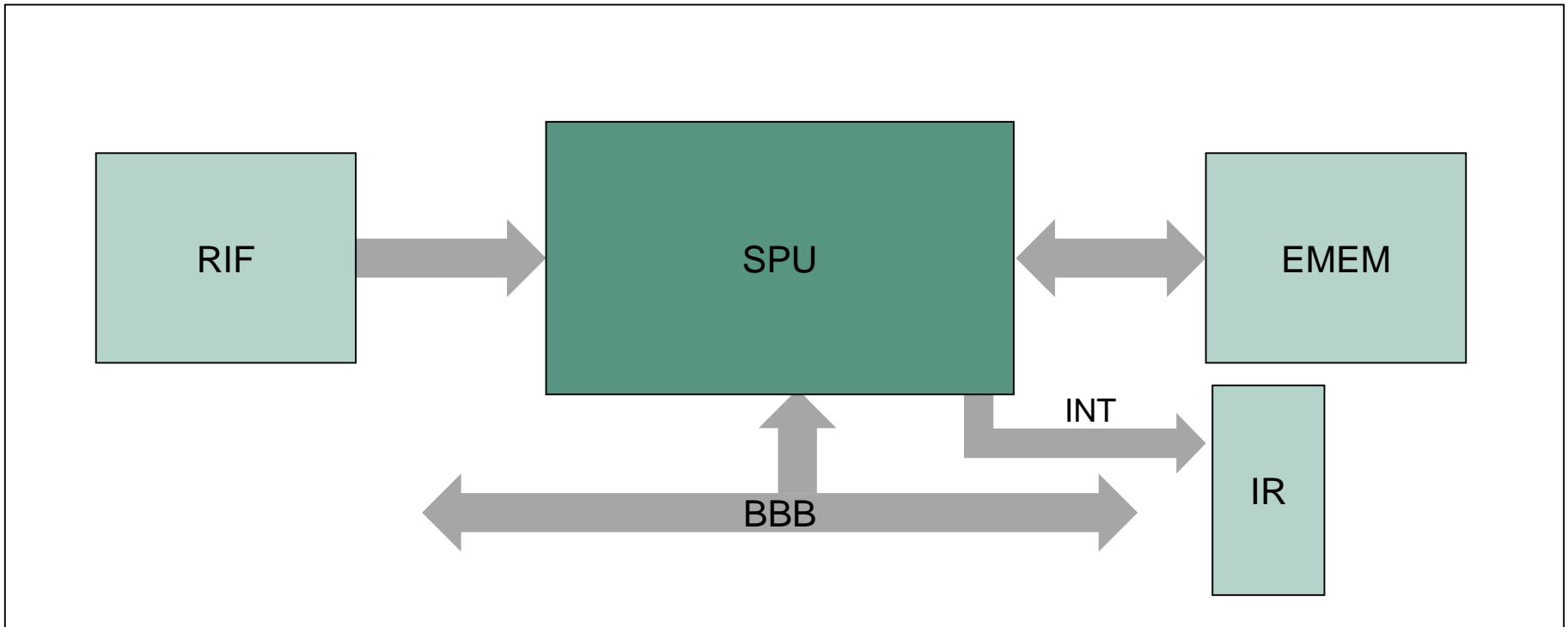
- > The dedicated configuration memory (CMEM) can hold multiple SPU configurations stored as linked list. Execution starts upon configured trigger, the configurations are pushed sequentially in the SPU registers. The system is notified at the end by an interrupt signal.
- > The CMEM can hold multiple linked lists



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System integration

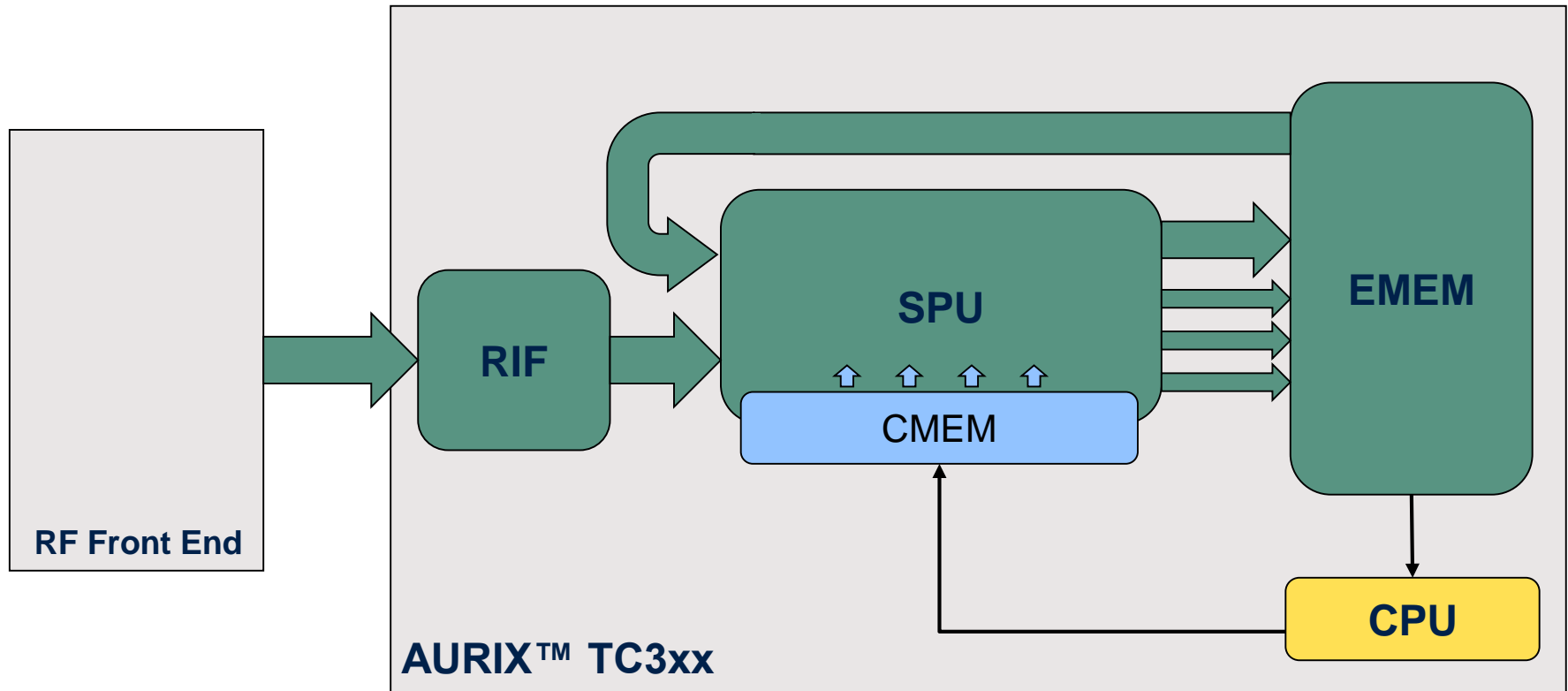
- › The SPU is directly connected to the RIF and the EMEM to enable the fastest data processing
- › The SPU can be accessed through the BBB and generate signals to the Interrupt Router



Application example

SPU hardware requests

- › In this example, data is processed following the configuration programmed in the CMEM. Result is retrieved by CPU directly in the radar memory



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