Customer Training Workshop

TRAVEO™ T2G Flash

Q1 2024

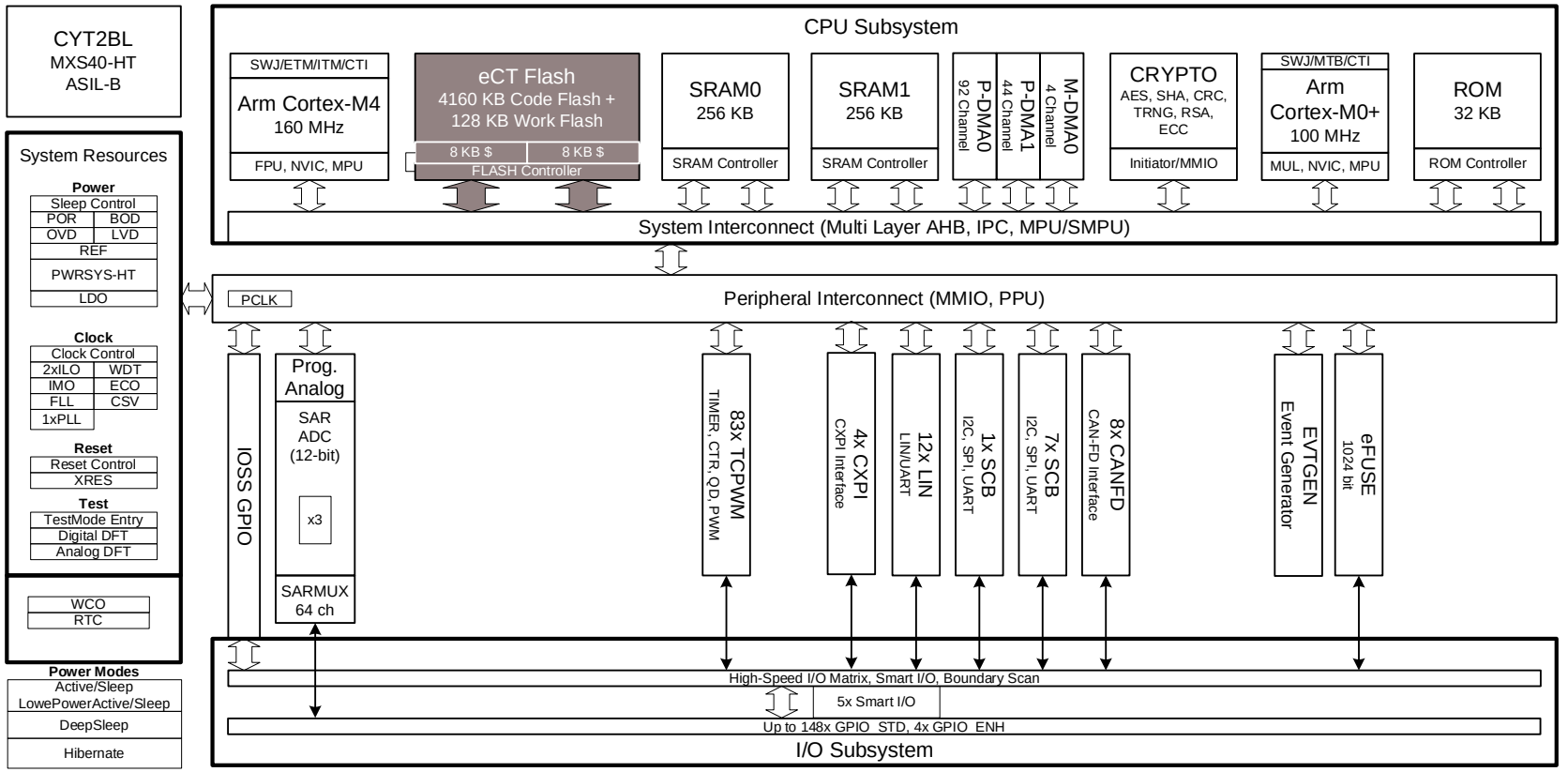
Target products

– Target product list for this training material

Family category	Series	Code flash memory size
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B6	Up to 576KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B7	Up to 1088KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2B9	Up to 2112KB
TRAVEO™ T2G Automotive Body Controller Entry	CYT2BL	Up to 4160KB
TRAVEO™ T2G Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
TRAVEO™ T2G Automotive Body Controller High	CYT4BF	Up to 8384KB
TRAVEO™ T2G Automotive Body Controller High	CYT6BJ	Up to 16768KB
TRAVEO™ T2G Automotive Cluster	CYT3DL	Up to 4160KB
TRAVEO™ T2G Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to TRAVEO™ T2G Body Controller Entry

– Flash is part of the CPU subsystem.

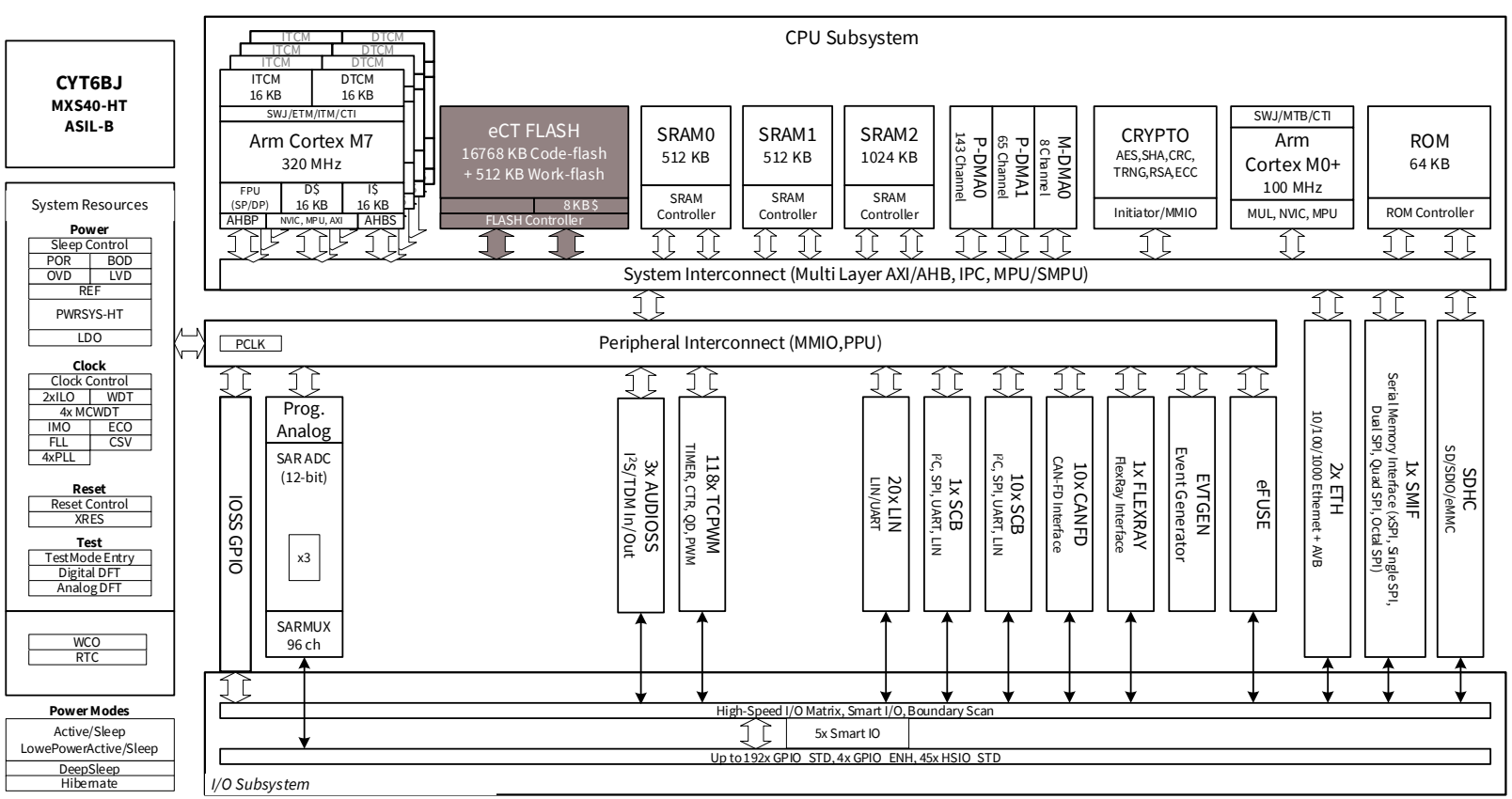


Hint Bar

Review TRM chapters 8 and 9 for additional details

Introduction to TRAVEO™ T2G Body Controller High

– Flash is part of the CPU subsystem.

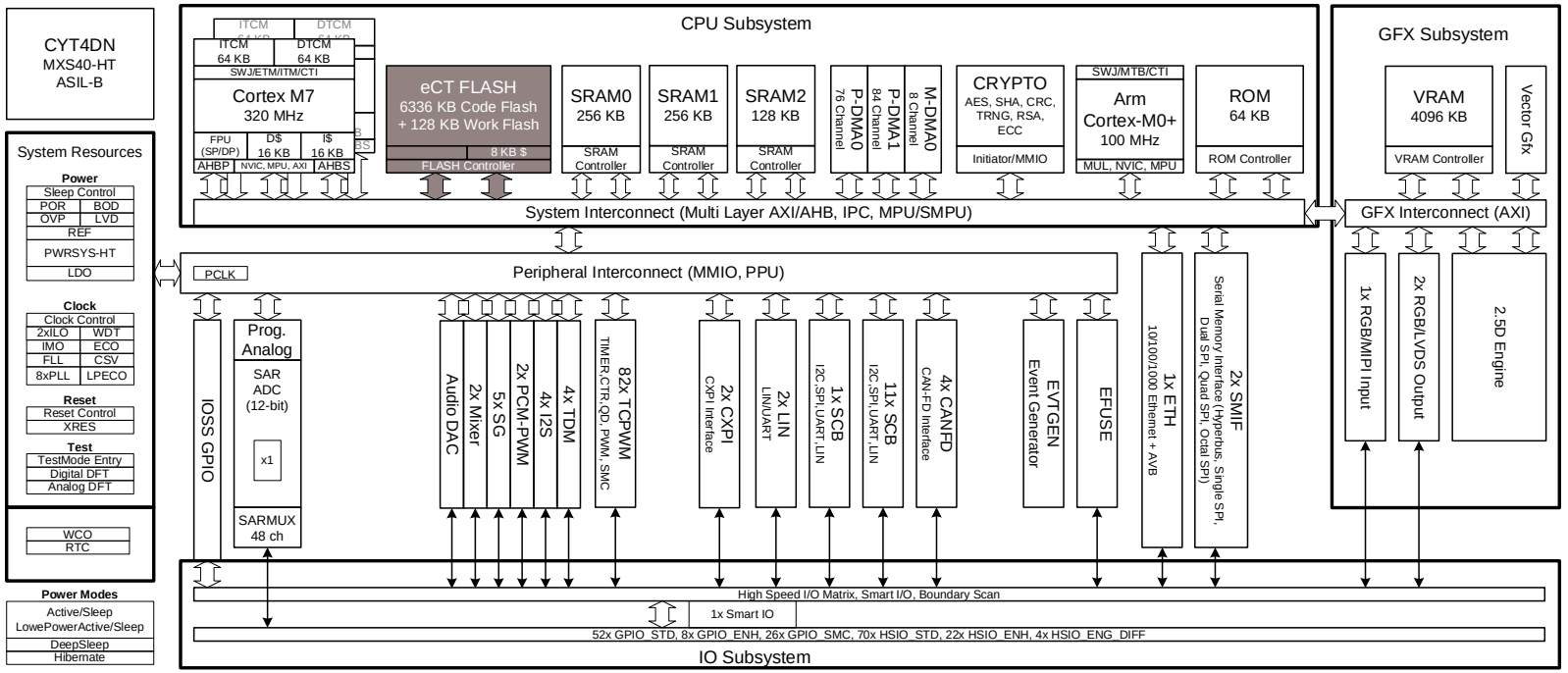


Hint Bar

Review TRM chapters 8 and 9 for additional details

Introduction to TRAVEO™ T2G Cluster

– Flash is part of the CPU subsystem.



Hint Bar

Review TRM chapters 8 and 9 for additional details

Flash overview

- TRAVEO™ T2G has Code Flash and Work Flash
  - Code flash is for storing application code
  - Work flash is for storing data or critical parameters
- Cache
  - CYT2B6/B7/B9/BL
    - 8-KB cache for CM0+ and CM4, located in the flash controller
    - Read-only capacity with an LRU replacement scheme
  - CYT3BB/4BB/4BF/6BJ/3DL/4DN
    - CM0+: 8-KB cache in flash; read-only capacity with an LRU replacement scheme
    - CM7: CPU has its own caches (16-KB I-cache/16-KB D-cache)
- Flash Wait States
  - CYT2B6/B7/B9/BL
    - 0 wait cycle for CLK_HF1 ≤ 100 MHz
    - 1 wait cycle for 100 MHz < CLK_HF ≤ 160 MHz
  - CYT3BB/4BB/4BF/6BJ/3DL/4DN
    - 0 wait cycle for CLK_MEM2 ≤ 100 MHz
    - 1 wait cycle for 100 MHz < CLK_MEM ≤ 200 MHz

Hint Bar

Review TRM chapters 8 and 9 for additional details

[1] High-frequency clock
[2] Memory clock. This clock is a divided version of CLK_HF.

Flash overview

Feature	Code Flash				Work Flash			
	CYT2B6/ B7/B9/BL	CYT3BB/ 4BB/4BF	CYT6BJ	CYT3DL/ 4DN	CYT2B6/B 7/B9/BL	CYT3BB/ 4BB/4BF	CYT6BJ	CYT3DL/ 4DN
Memory Size	Up to 4160KB (4032KB + 128KB)	Up to 8384KB (8128KB + 256KB)	Up to 16768KB (16768KB + 512KB)	Up to 6336KB (6080KB + 256KB)	Up to 128KB (96KB + 32KB)	Up to 256KB (192KB + 64KB)	Up to 512KB (384KB + 128KB)	Up to 128KB (96KB + 32KB)
Program Size	64-bit, 256-bit, 4096-bit				32-bit			
ECC Function	64-bit + 8-bit Single-Error Correction/Double-Error Detection (SECDED)				32-bit + 7-bit Single-Error Correction/Double-Error Detection (SECDED)			
Erase Sector Size	32 KB for large sector and 8KB for small sector				2 KB for large sector and 128 bytes for small sector			
Security	Supported				Supported			
Single Bank and Dual Bank Modes	Supported				Supported			
Reading While Programming/ Erasing	Supported				Supported			
Program/Erase cycles/ Data Retention Time @ 85 °C	1,000/20 years				250,000/10 years			

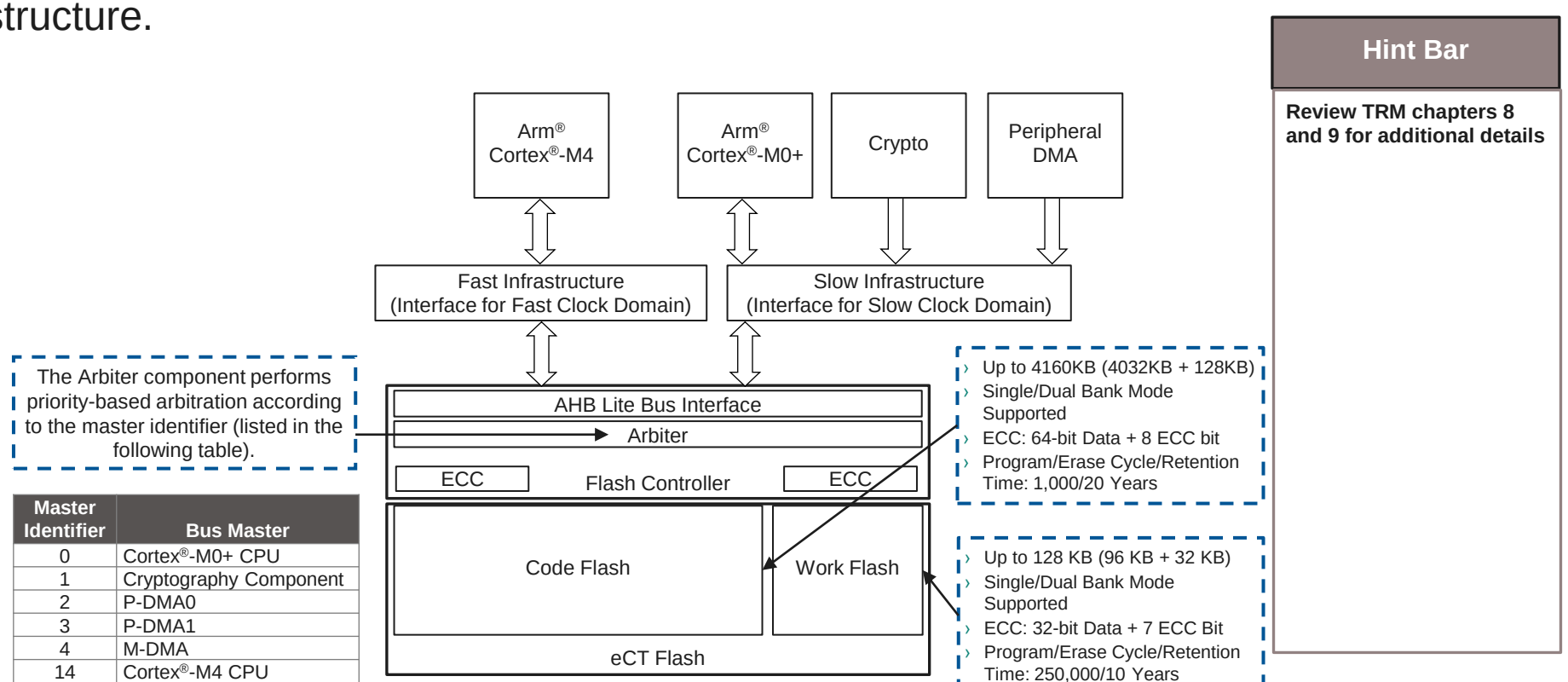
Hint Bar

Review TRM chapters 8 and 9 Flash for additional details

Review the Device Security section for additional details on security

CYT2B6/B7/B9/BL block diagram

– Arm® Cortex® -M4 and Cortex® -M0+ core can access code flash and work flash via fast/slow infrastructure.



Master Identifier	Bus Master
0	Cortex®-M0+ CPU
1	Cryptography Component
2	P-DMA0
3	P-DMA1
4	M-DMA
14	Cortex®-M4 CPU
15	DAP Tap Controller

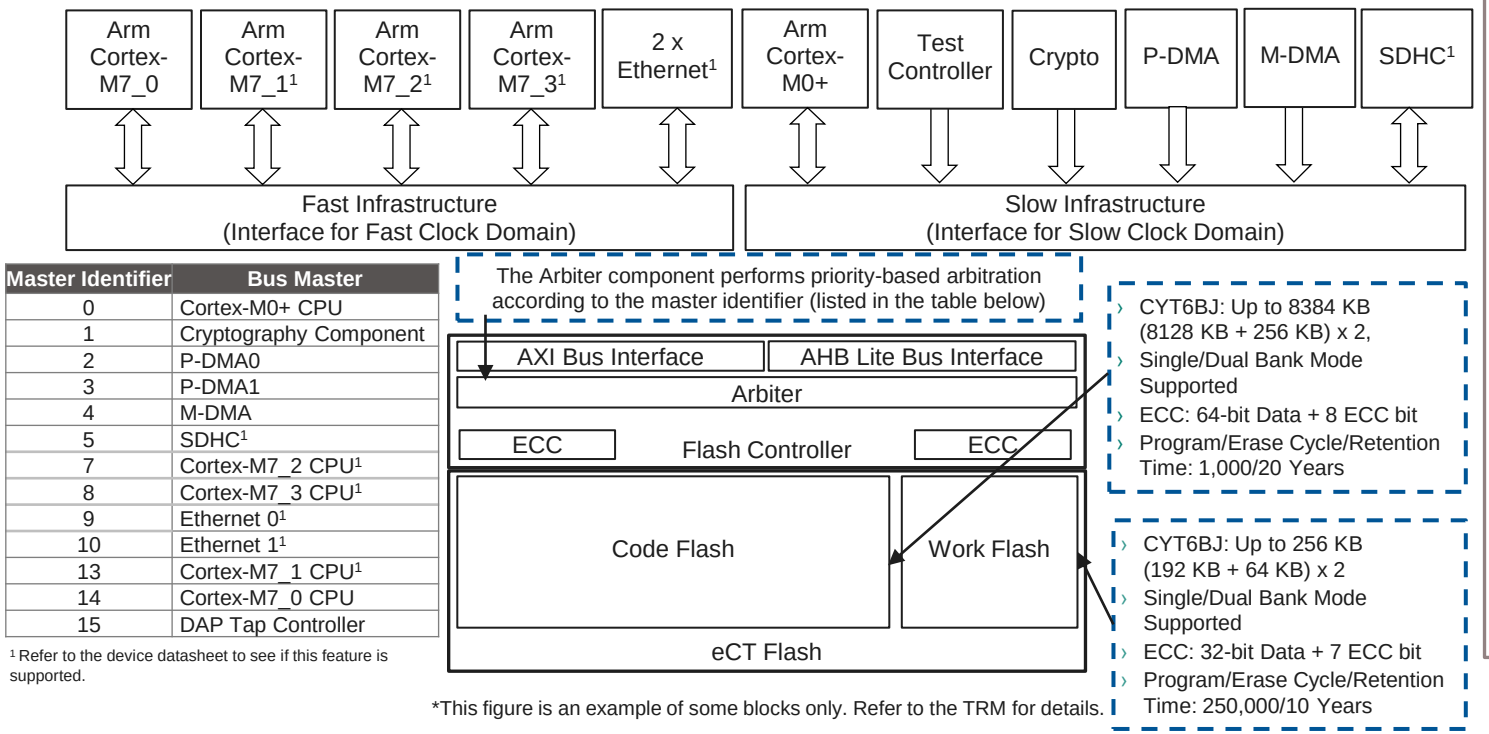
*This figure is an example of some blocks only. Refer to the TRM for details.

Hint Bar

Review TRM chapters 8 and 9 for additional details

CYT3BB/4BB/4BF/6BJ/3DL/4DN block diagram

– Arm® Cortex®-M7, and Cortex®-M0+ cores can access code flash and work flash via fast/slow infrastructure.



Master Identifier	Bus Master
0	Cortex-M0+ CPU
1	Cryptography Component
2	P-DMA0
3	P-DMA1
4	M-DMA
5	SDHC[1]
7	Cortex-M7_2 CPU[1]
8	Cortex-M7_3 CPU[1]
9	Ethernet 0[1]
10	Ethernet 1[1]
13	Cortex-M7_1 CPU[1]
14	Cortex-M7_0 CPU
15	DAP Tap Controller

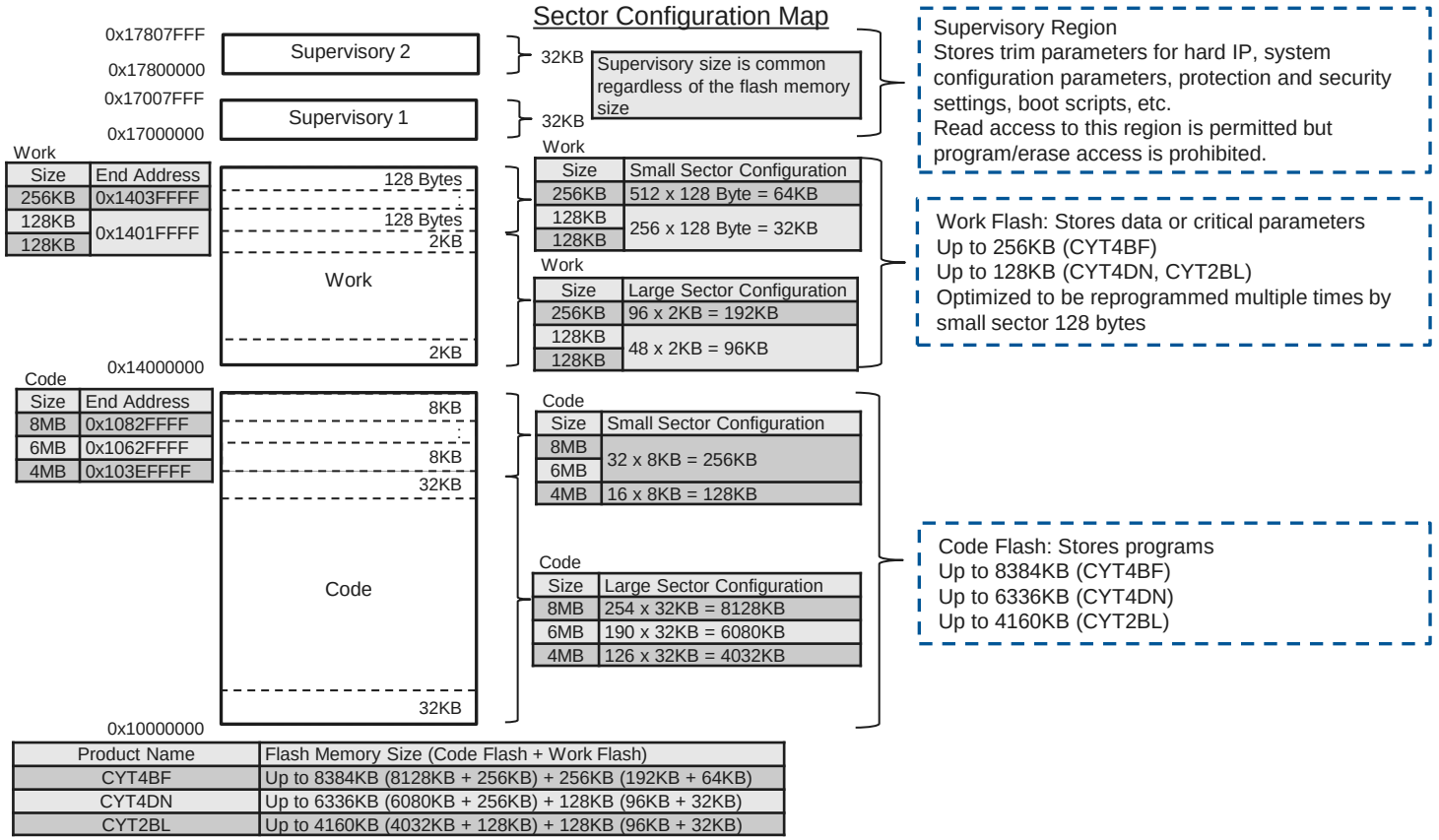
[1] Refer to the device datasheet to see if this feature is supported.

*This figure is an example of some blocks only. Refer to the TRM for details.

Hint Bar

Review TRM chapters 8 and 9 for additional details

Sector configuration



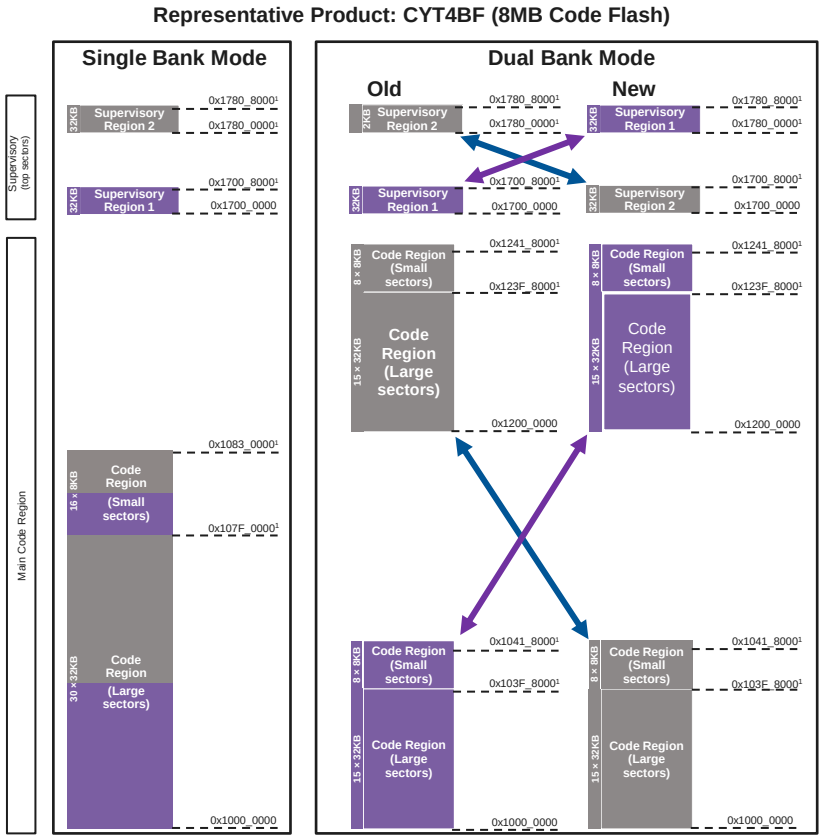
Product Name	Flash Memory Size (Code Flash + Work Flash)
CYT4BF	Up to 8384KB (8128KB + 256KB) + 256KB (192KB + 64KB)
CYT4DN	Up to 6336KB (6080KB + 256KB) + 128KB (96KB + 32KB)
CYT2BL	Up to 4160KB (4032KB + 128KB) + 128KB (96KB + 32KB)

Example of 8MB/6MB/4MB. For other products, refer to the respective TRMs.

Hint Bar

Review TRM chapters 8 and 9 for additional details

Bank modes



- Single Bank mode: Entire code and supervisory logical regions are mapped as single contiguous address regions
- Dual Bank mode: Split into two halves, and each half is presented as a separate address region. Can be swapped to support same-location firmware upgrades
  - Old: CPU executes from a current software (Violet region) while the higher sectors are programmed with a new software image (Blue region)
  - New: When the CPU reboots, the user code changes the main map field, such that the CPU is executed from the new Blue region
- Dual Bank mode enables writing to the other bank while executing flash
- Work flash and code flash both support Dual Bank mode
- Mapping of work flash is independent of mapping of code flash

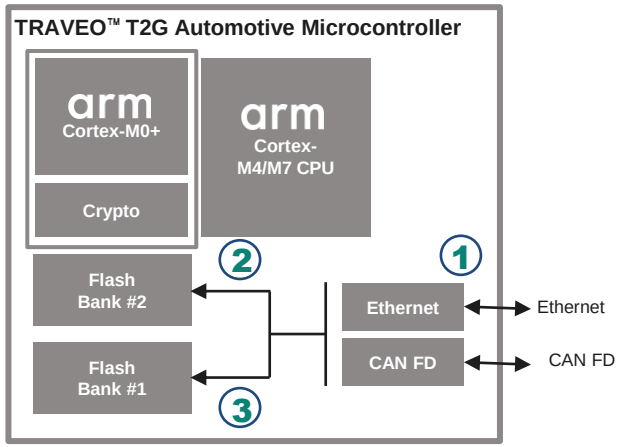
Hint Bar

Review TRM chapters 8 and 9 for additional details

[1] Example of 8MB. The end address is different for other code flash memory sizes. For details, refer to the TRM.

Remap functionality

- Software can control the remap functionality, which enables writing during flash execution in both bank modes
  - The higher and lower physical banks are swapped in the main flash region
- Use Case
  - FOTA[1]: The CPU executes from a current software image in the lower bank while the higher bank is programmed with a new software image. When the CPU reboots, the ROM boot code changes the REMAP field such that the CPU executed from the new image is on the higher bank.



1. Software update data is received via any communication interface
2. Update data can be stored in the internal Flash Bank #2. The vehicle sends a command to switch to the new software version at the next ignition cycle. The new software version is activated
3. The previous version is still available in internal Flash Bank #1 and can be reused as a roll-back solution

Hint Bar

Review TRM chapters 8 and 9 for additional details

[1] Firmware-Over-The-Air

Error-Correcting Code (ECC)

- ECC implements Single-Error Correction/Double-Error Detection (SECDED)
  - Default setting of ECC checking for code flash and work flash interface is “Enable”
  - Behavior at Double-Error Detection
    - For CPU bus transfers, notify with bus error generation[1]
    - For non-CPU bus transfers, notify with bus error generation
  - Code flash: 64-bit data + 8 ECC bits
  - Work flash: 32-bit data + 7 ECC bits
- Fault report structure
  - Both correctable and non-correctable ECC errors are reported to the fault structure in the same way. All data correction and recovery are left to the ISR. There is no hardware support for writing corrected data back to flash
  - Use Case
    - SEC Report: Log the error counts
    - DED Report: Report to NMI
- Error injection
  - It is possible to generate ECC error by providing an error injection address and error injection data register
  - Use Case
    - As initial diagnosis of ECC before running the application
    - To test the error recovery routines

Hint Bar

Review TRM chapters 8, 9, and 15 for additional details

Interrupt service routine (ISR)

Nonmaskable interrupt (NMI)

[1] It depends on FLASH_CTL register, MAIN_ERR_SILENT bit

Comparison between CYT2BL, CYT4BF, CYT6BJ and CYT4DN

Features	CYT2BL	CYT4BF	CYT6BJ	CYT4DN
Code flash memory size	4160 KB (4032 KB + 128 KB)	8384 KB (8128 KB + 256 KB)	16768 KB (16256 KB + 512 KB)	6336 KB (6080 KB + 256 KB)
Work flash memory size	128 KB (96 KB + 32 KB)	256 KB (192 KB + 64 KB)	512 KB (384 KB + 128 KB)	128 KB (96 KB + 32 KB)
Bus interface	AHB-Lite	AXI, AHB-Lite		
Cache	CM0+ and CM4 inside Flash	CM0+: Cache inside Flash CM7: CPU has own caches (I-Cache, D-Cache)		
Flash wait states	0 wait cycle for CLK_HF ≤ 100 MHz 1 wait cycle for 100 MHz < CLK_HF ≤ 160 MHz	0 wait cycle for CLK_MEM ≤ 100 MHz 1 wait cycle for 100 MHz < CLK_MEM ≤ 200 MHz		
Bus master priority of arbiter	0: Cortex®-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 14: Cortex®-M4 CPU 15: DAP Tap Controller	0: Cortex®-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 5: SDHC 9: Ethernet 0 10: Ethernet 1 13: Cortex®-M7_1 CPU 14: Cortex®-M7_0 CPU 15: DAP Tap Controller	0: Cortex®-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 5: SDHC 7: Cortex®-M7_2 CPU 8: Cortex®-M7_3 CPU 9: Ethernet 0 10: Ethernet 1 13: Cortex®-M7_1 CPU 14: Cortex®-M7_0 CPU 15: DAP Tap Controller	0: Cortex®-M0+ CPU 1: Cryptography Component 2: P-DMA0 3: P-DMA1 4: M-DMA 9: Ethernet 0 10: JPEG Decoder 11: AXI DMA 12: VIDEO Subsystem 13: Cortex®-M7_1 CPU 14: Cortex®-M7_0 CPU 15: DAP Tap Controller
ECC (SEC/DED)	Code flash: 64-bit + 8-bit and Work flash: 32-bit + 7-bit			
Bank modes	Supported			
Reading while programming/erasing	Supported			
Security	Supported			
Program/Erase cycles/ Data Retention Time @ 85 °C	Code flash: 1,000 cycles/20 years Work flash: 250,000 cycles/10 years			

Revision History

Revision	ECN	Submission Data	Description of Change
**	6123648	09/03/2018	Initial release
*A	6402267	12/06/2018	Added the note descriptions. Updated the Introduction for CYT2B5/B7, added the Introduction for CYT2B9 and CYT4BF. Added Block Diagram for CYT4BF of slide 10. Added Comparison between CYT2B7 and CYT4BF of slide 16. Fixed the title from Traveo ™ Flash to Traveo ™ II Flash.
*B	6662240	08/27/2019	Removed Erase and Program time. Removed CYT2B5. Added CYT4DN (page 2, 5, 6, 7, 9, 10, 15).
*C	7051755	12/21/2020	Updated page 2, 3, 6, 7, 8, 9, 10
*D	8014521	03/19/2024	Updated page 2, 3, 4, 5, 6, 7, 9, 12, 15 Fixed the title from Traveo™ Flash to TRAVEO™ T2G Flash.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