Customer Training Workshop Traveo™ II Body High and Cluster 2D Clock System

Q4 2020

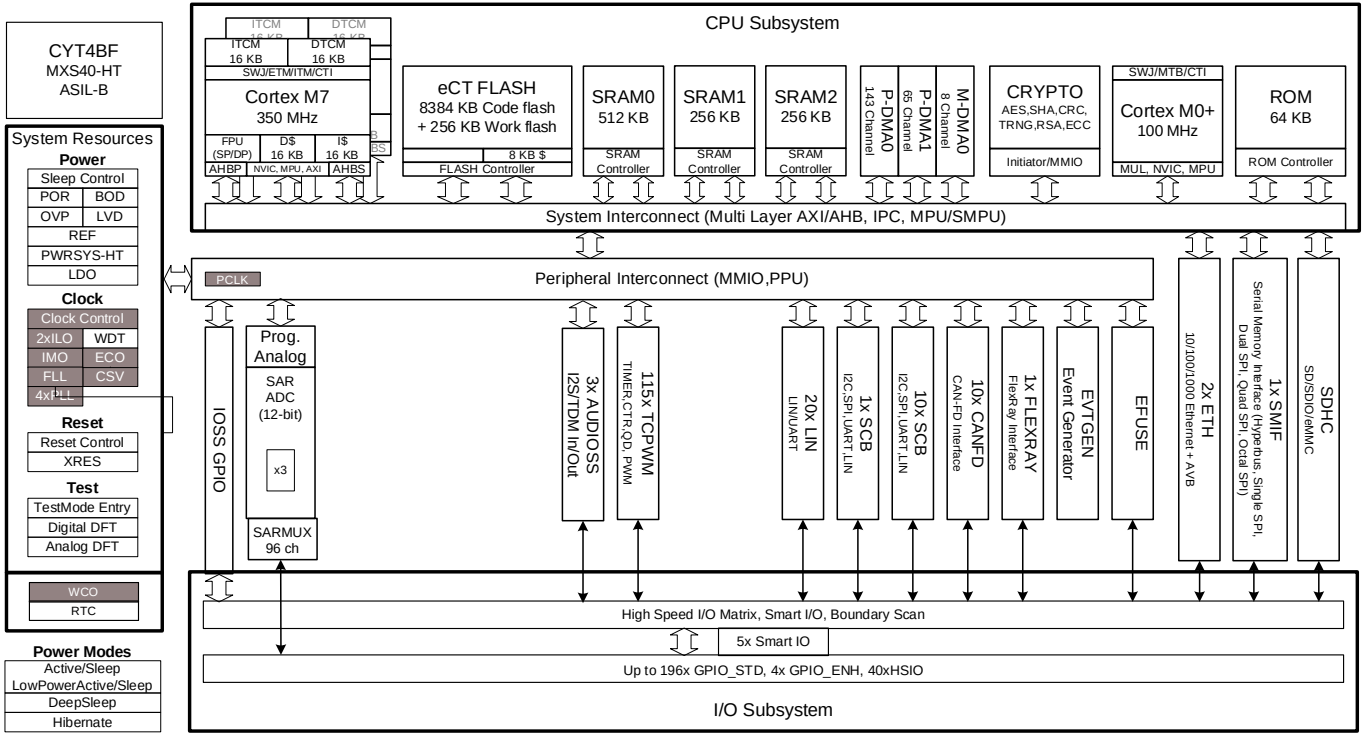
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Body Controller High

› The clock system is part of the System Resources block



Hint Bar

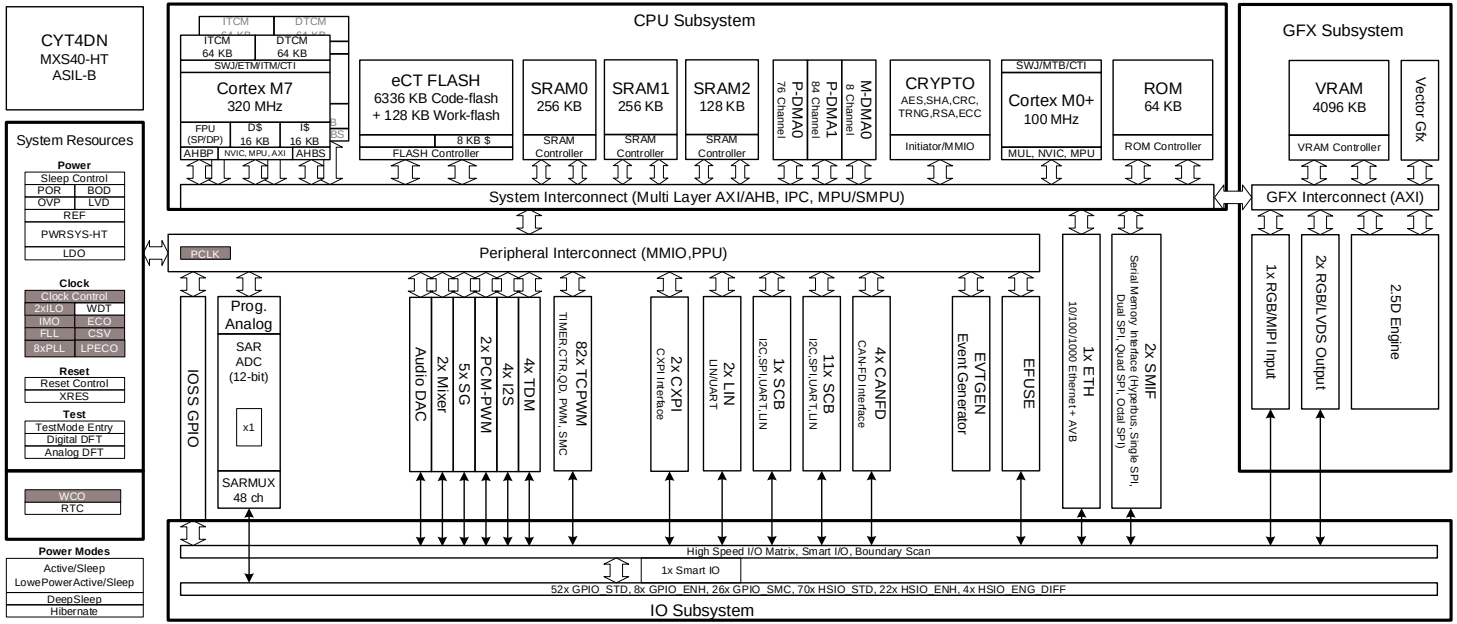
Review TRM chapter 18 for additional details

Training section reference

Clock System for Traveo II Body Entry

Introduction to Traveo II Cluster

› The clock system is part of the System Resources block



Hint Bar

Review TRM chapter 18 for additional details

Clock System Overview

- Features
  - Internal clock sources
    - IMO: Internal main oscillator (8 MHz)
    - ILO0/1: Internal low-speed oscillator (32.768 kHz)
  - External clock sources
    - ECO: External crystal oscillator
    - WCO: Watch crystal oscillator
    - EXT_CLK : External clock generated using a signal through the I/O pin
      Also possible to output the internal clock
    - LPECO[1]: Low-power external crystal oscillator
  - Clock generation
    - Phase-locked loops (PLL) - with and without SSCG[2] and fractional operation[3]
    - Frequency-locked loop (FLL)
  - Clock supervision (CSV) to detect clock abnormality
  - Clock calibration counter

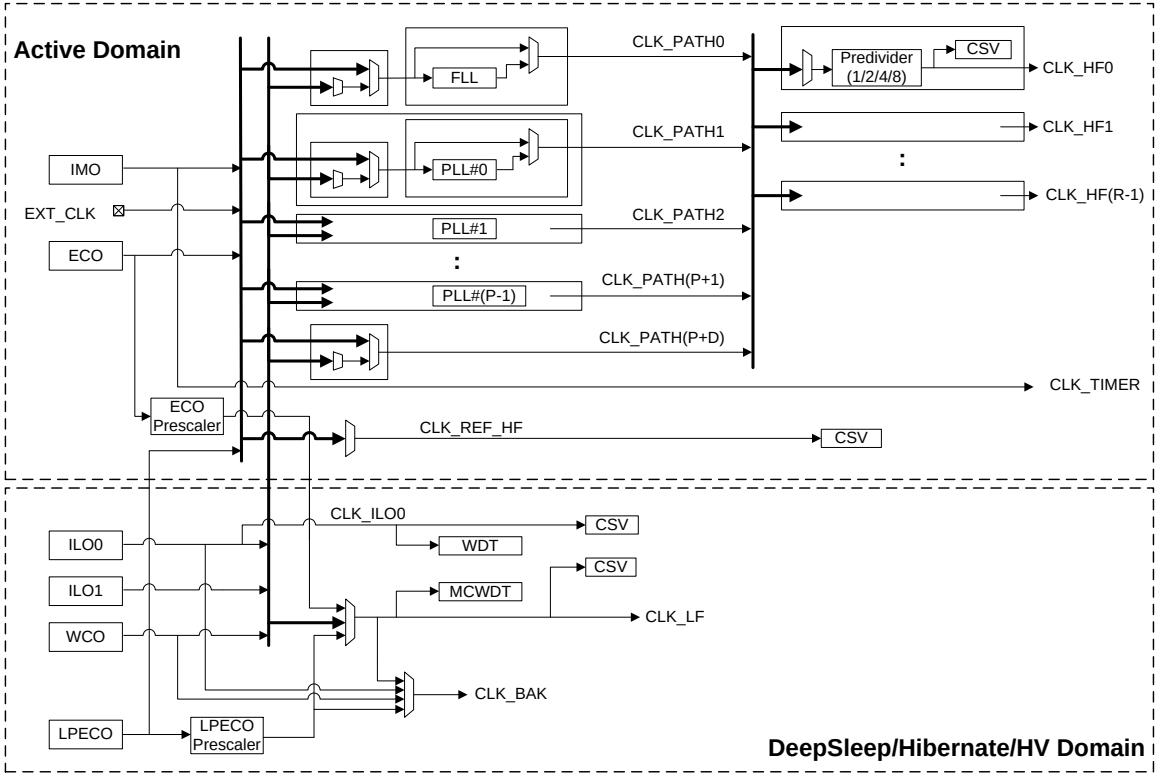
Hint Bar

Review TRM chapter 18 for additional details

[1] CYT4BF dose not have LPECO
[2] Spread Spectrum Clock Generation
[3] Fractional operation provides an output frequency that is a fractional multiple of the input frequency

Clock System Block Diagram

- Clock system components



Legend:

D: The number of direct select paths

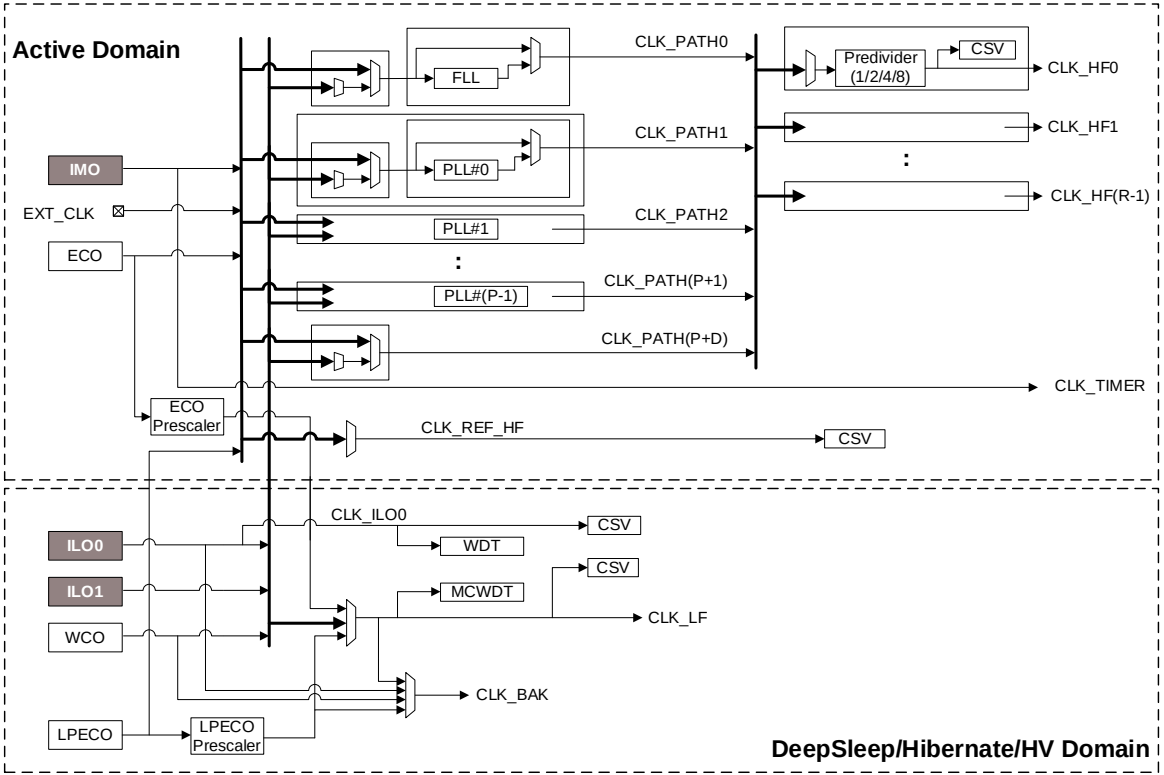
P: The number of PLLs

R: The number of clock roots (CLK_HF)

See the device datasheet for the number of D, P, and R

Clock System Block Diagram

- Clock system components
  - Internal clock sources
    - IMO
    - ILO 0/1



Internal Clock Sources (1/2)

- IMO: Internal main oscillator
  - Produces an 8-MHz fixed-frequency clock
  - An accurate, high-speed internal (crystal-less) oscillator
  - Available only in Active and Sleep modes
  - Default clock source after POR or any other reset
  - Used by PLLs to generate a wide range of high-frequency clocks
  - Enabled and disabled by register[1]
    - Default is ENABLE[2]

Hint Bar

Review TRM section 18.2 for additional details

Refer to the datasheet for additional details on AC specification

[1] IMO should not be disabled if it is the source of the clock path to CLK_HF[0]
[2] Refer to the Register TRM (CLK_IMO_CONFIG) for additional details

Internal Clock Sources (2/2)

- ILO 0/1: Internal low-speed oscillator
  - ILO0
    - Produces a 32.768-kHz nominal fixed-frequency clock
    - Low power and low accuracy
    - Available in all power modes
    - Always the source of the watchdog timer (WDT)[1]
  - ILO1
    - Used for ILO0 clock monitoring
    - Parameters for ILO1 are the same as ILO0

Hint Bar

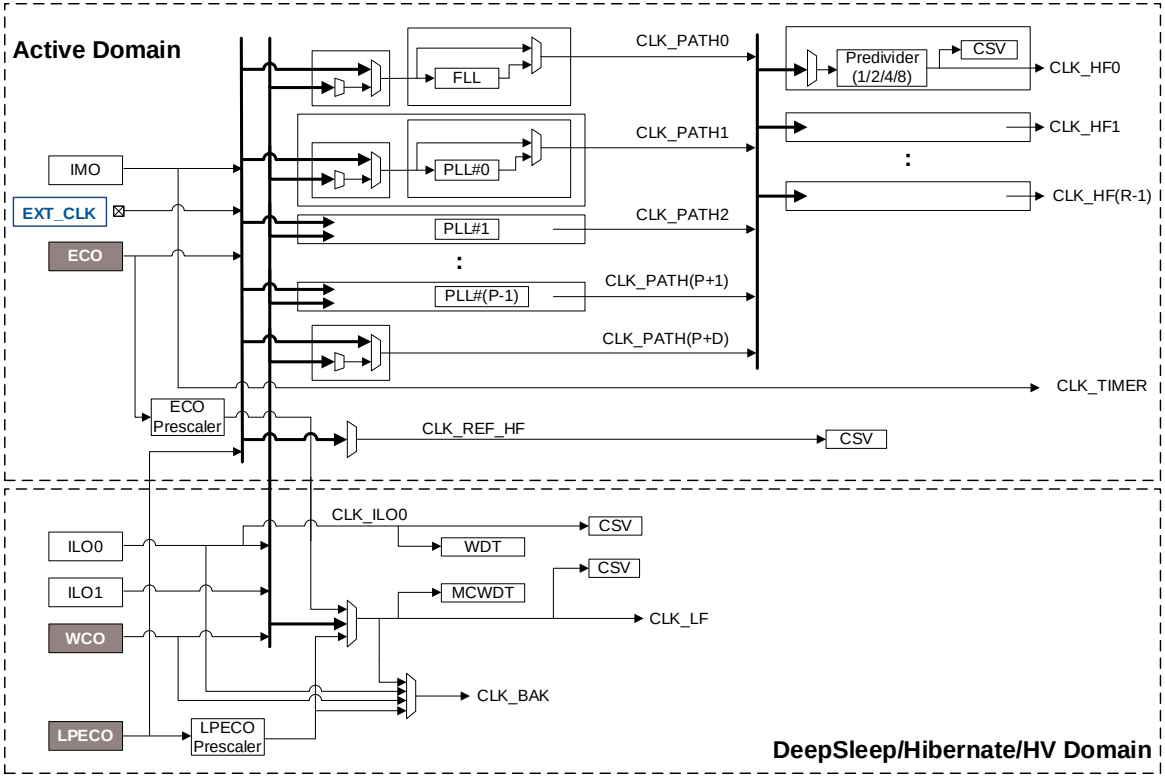
Review TRM section 18.2 for additional details

Refer to the datasheet for additional details on AC specification

[1] Always leave the ILO enabled because it is the source of the watchdog timer

Clock System Block Diagram

- Clock system components
  - External clock sources
    - ECO
    - WCO
    - EXT_CLK
    - LPECO



External Clock Sources (1/3)

- ECO: External crystal oscillator
  - Contains an oscillator to drive an external up to 33.34-MHz crystal
  - Used by PLLs to generate a wide range of high-frequency clocks
  - ECO prescaler
  - ECO trimming
  - Enabled and disabled by register[1]
    - Default is DISABLE
- WCO: External low-frequency watch crystal oscillator
  - Highly accurate 32.768-kHz clock source
  - Primary clock source for the real-time clock (RTC)
  - Enabled and disabled by register[2]
    - Default is DISABLE

Hint Bar

Review TRM section 18.2 for additional details

Refer to the datasheet for additional details on AC specification

[1] Refer to the Register TRM (CLK_ECO_CONFIG) for additional details
[2] Refer to the Register TRM (CTL) for additional details

External Clock Sources (2/3)

- ECO Trimming
  - ECO supports a wide variety of crystals and ceramic resonators
  - ECO can be configured by register[1]
    - The following trim bit fields can be configured to control the maximum peak oscillation voltage across the crystal (V_P), the transconductance (gm), and the nominal frequency (f):
      - ATRIM (Amplitude Trim by AGC)
      - GTRIM (Gain Trim)
      - WDTRIM (Watchdog Trim)
      - FTRIM (Filter Trim)
      - RTRIM (Feedback Resistor Trim)

$$Max\ peak\ value:\ V_P = \frac{\sqrt{\frac{D_L}{2ESR}}}{\pi f (C_0 + C_L)}$$

f: Fundamental frequency of the crystal (XTAL)

D_L: Maximum drive level of XTAL

ESR: Equivalent series resistance

C_0: Shunt capacitance of XTAL

C_L: Parallel load capacitance of XTAL

$$Transconductance:\ g_m > 20 \times ESR \times (2\pi \times f)^2 \times (C_0 + C_L)^2$$

$$Negative\ resistance:\ |R_{neg}| = \frac{g_m \times 4 \times {C_L}^2}{(2\pi \times f)^2 \times (4 \times {C_L}^2 + 4 \times CL \times C_0)^2}$$

Hint Bar

Review TRM section 18.2 for additional details

[1] Refer to the Register TRM (CLK_ECO_CONFIG2) for additional details

External Clock Sources (3/3)

- EXT_CLK: External clock
  - 0.25- to 100-MHz[1] clock that can be sourced from a designated I/O pin
  - Can be used as the source clock for either the PLL or FLL
  - Can be used as the output for the internal clock (CLK_HF3 is available)
  - When using a pin as input or output to EXT_CLK, I/O must be set appropriately
- LPECO: Low-power external crystal oscillator
  - 3.99- to 8.01-MHz clock source
  - Support only cluster product
  - Can operate in Active, LPACTIVE, Sleep, LPSLEEP, DeepSleep, and Hibernate
  - Can generate CPU and peripheral clock source in conjunction with PLLs
  - Can use a real-time-clock (RTC) source instead of WCO
  - LPECO prescaler
  - Enabled and disabled by register[2]
    - Default is DISABLE

Hint Bar

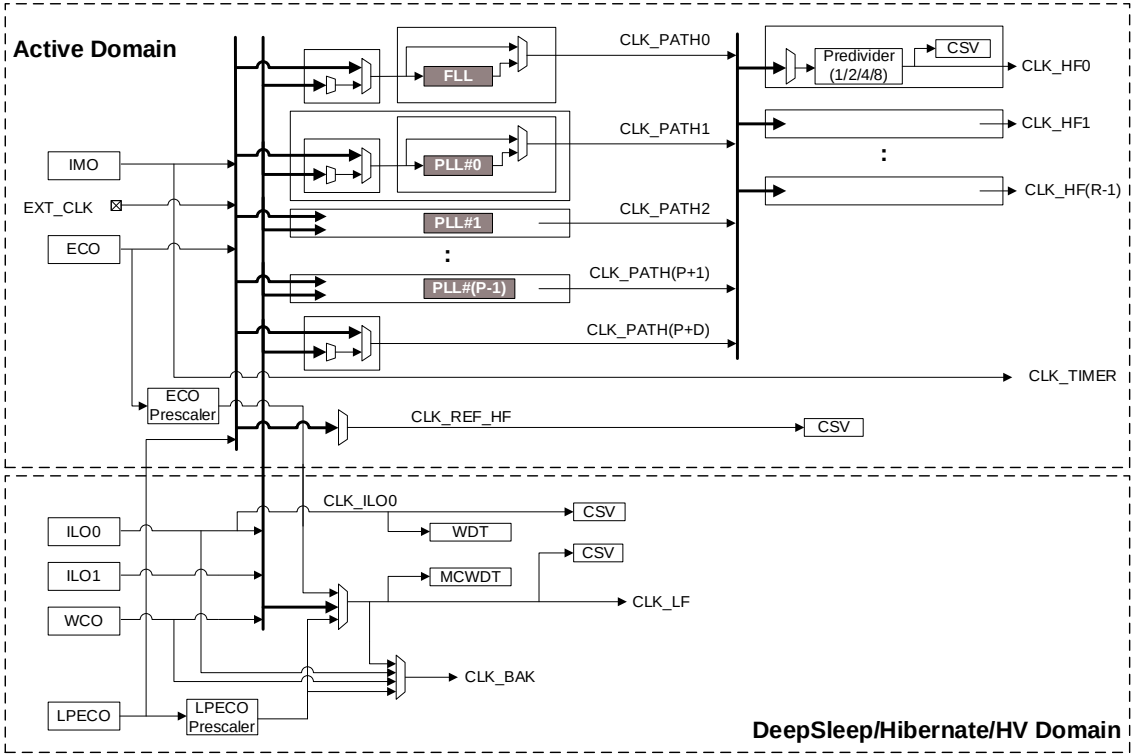
Review TRM section 18.2 for additional details

Refer to the datasheet for additional details on AC specification

[1] Refer to datasheet for the target product
[2] Refer to the Register TRM (BACKUP_LPECO_CTL) for additional details

Clock System Block Diagram

- Clock system components
  - High-speed clock generation
    - PLL
    - FLL



Clock Generation

- PLL: Phase-locked loop
  - Input clock can be IMO (8 MHz), ECO, or EXT_CLK
  - Two types of PLL: PLL and PLL400
  - PLL without SSCG and fractional operation[1]
    - Input clock range: 3.988 to 33.34 MHz (CYT4BF)[2]
    - Output clock range: 11 to 200 MHz (CYT4BF)[2]
  - PLL400 with SSCG and fractional operation[1]
    - Input clock range: 3.988 to 33.34 MHz (CYT4BF)[2]
    - Output clock range: 25 to 350 MHz (CYT4BF)[2]
    - Supports down spread
    - 24-bit fractional divider[3]
    - SSCG and fractional operation are enabled and disabled by register[4]
      - Default is Disable

Hint Bar

Review TRM section 18.3 and Register TRM for additional details

Refer to the datasheet for additional details on AC specification

Output clock range of PLL400 changes depending on spreading configuration

[1] Refer to the device datasheet for number and location each PLL type
[2] Refer to the device datasheet for the target product
[3] Refer to the Register TRM (PLL400_CONFIG2 register) for additional details
[4] Refer to the Register TRM (CLK_PLL400M_CONFIG2 and CLK_PLL400M_CONFIG3 registers) for additional details

Clock Generation

- FLL: Frequency-locked loop
  - Input clock can be IMO (8 MHz), ECO, or EXT_CLK
  - A counter with a current-controlled oscillator (CCO)
    - Starts up (locks) faster and uses lower power than the PLL
    - The lock tolerance is user adjustable
  - The parameters on the FLL configuration are as follows:
    - Input clock range: 0.25 to 80 MHz (CYT4BF)[1]
    - Output clock range: 24 to 100 MHz (CYT4BF)[1]
  - FLL is set by ROM boot, and FLL can reduce startup time

Hint Bar

Review TRM section 18.3 and Register TRM for additional details

Refer to the datasheet for additional details on AC specification

[1] Refer to the device datasheet for the target product

Connection Table for PLL Type and CLK_PATH

› PLL connection table

CLK_PATH	CYT4BF	CYT4DN
	PLL Type	PLL Type
CLK_PATH1	PLL400#0	PLL400#0
CLK_PATH2	PLL400#1	PLL400#1
CLK_PATH3	PLL#2	PLL400#2
CLK_PATH4	PLL#3	PLL400#3
CLK_PATH5	Not supported	PLL400#4
CLK_PATH6	Not supported	PLL#5
CLK_PATH7	Not supported	PLL#6
CLK_PATH8	Not supported	PLL#7

Hint Bar

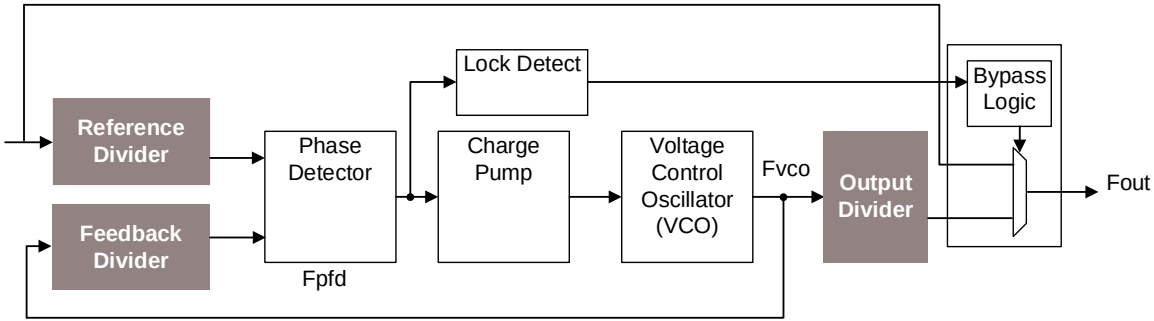
Review TRM section 18.3 and Register TRM for additional details

Refer to the datasheet for additional details

Clock Generation PLL (1/4)

› PLL configuration parameters (CYT4BF)[1]

Parameters	PLL w/o SSCG and Fractional Operation	PLL with SSCG and Fractional Operation
Fref	3.988 to 33.34 MHz	3.988 to 33.34 MHz
Fout (Fvco/Output divider)	11 to 200 MHz	25 to 350 MHz
Fpfd (Fref/Reference divider)	4 to 8 MHz	8 to 20 MHz
Fvco (Fpfd * Feedback divider)	170 to 400 MHz	400 to 800 MHz



Hint Bar

Review TRM section 18.3.1, 18.3.2, and Register TRM for additional details

Fout range changes depending on spreading configuration

Fpfd range changes depending on fractional divider configuration

[1] Refer to the device datasheet for the target product

Clock Generation PLL (2/4)

- Configuration example for PLL without SSCG and Fractional Operation
  - In this case, 200-MHz clock (Fout) is generated from the 8-MHz input clock (Fref)

	Fref	Fout	Fpfd	Fvco
Frequency	8 MHz	200 MHz = Fvco/2	4 MHz = Fref/2	400 MHz = Fpfd x 100
Divider Setting	-	Output Divider[1]: 2	Reference Divider[1]: 2	Feedback Divider[1]: 100

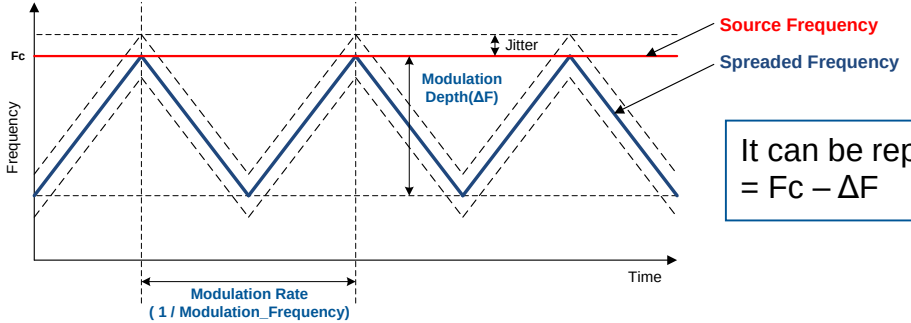
Hint Bar

Review TRM section 18.3.1, 18.3.2, and Register TRM for additional details

[1] Refer to the Register TRM (CLK_PLL_CONFIG register) for additional details of PLL without SSCG and fractional operation
Refer to the Register TRM (PLL400_CONFIG register) for additional details of PLL with SSCG and fractional operation

Clock Generation PLL (3/4)

- Configuration for SSCG
  - Spread energy contained in the narrow band of the clock source to a wide band



It can be represented as Fout = Fc – ΔF

  - The parameters on the PLL configuration[1] are as follows:
    - Modulation Depth: Between -3%, -2%, -1%, or - 0.5%
    - Modulation Rate: Between Fpfd/4096, Fpfd/2048, Fpfd/1024, or Fpfd/512
    - Modulation Type: Down-spread mode only
- Advantage
  - Reduces the peak spectral amplitude of the fundamental and the harmonics to lower radiated emission from the clock source

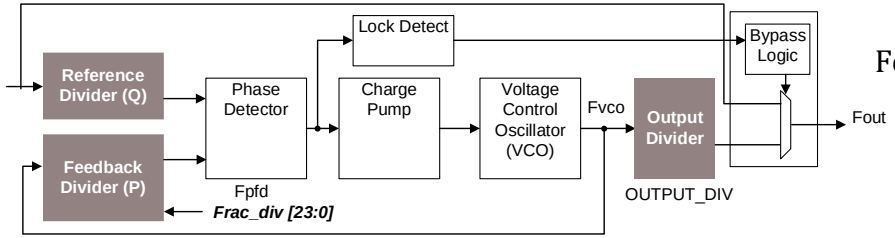
Hint Bar

Review TRM section 18.3.2.1 and Register TRM for additional details

[1] Refer to the Register TRM (PLL400_CONFIG3 register) for additional details

Clock Generation PLL (4/4)

- Configuration for fractional operation
  - PLL400 has a 24-bit fractional divider
    - Set according to the following formula
    - Accuracy is only guaranteed for the upper 21 bits
- Configuration example for fractional operation
  - In this case, 196.608-MHz clock (Fout) is generated from the 8-MHz input clock (Fref)



$$Fout = \frac{Fref}{Q} \times \frac{P + Frac\_div}{OUTPUT\_DIV}$$

$$= \frac{8-MHz}{1} \times \frac{73+0.727999985}{3}$$

$$= 196.608 - MHz$$

	Fref	Q	P	Frac_div	OUTPUT_DIV	Fout
Value	8 MHz	1	73	0.727999985 = 12213813 / 2^24	3	196.608 MHz
Setting	-	Reference Divider[1]: 1	Feedback Divider[1]: 73	FRAC_DIV[2]: 12213813	Output Divider[1]: 3	-

- Advantage
  - Can generate source clock of the sampling frequency (e.g., 96 kHz) in the sound system

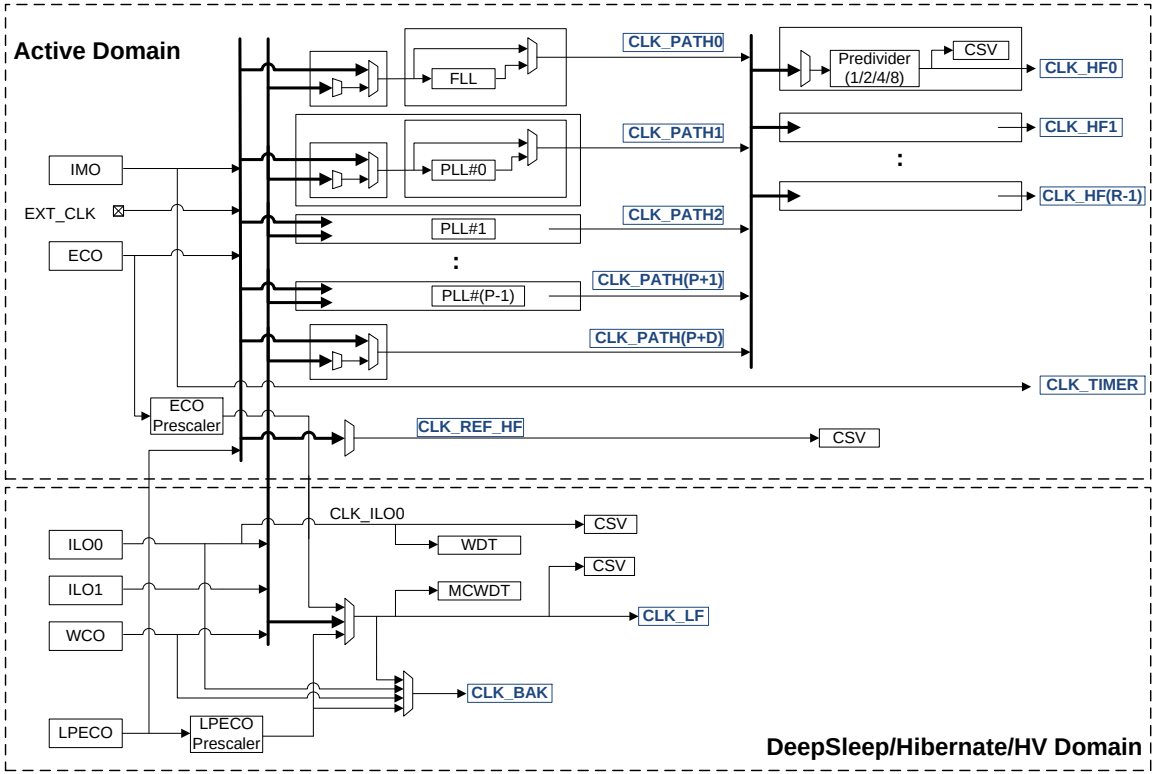
Hint Bar

Review TRM section 18.3.2.2 and Register TRM for additional details

[1] Refer to the Register TRM (PLL400_CONFIG register) for additional details
[2] Refer to the Register TRM (PLL400_CONFIG2 register) for additional details

Clock System Block Diagram

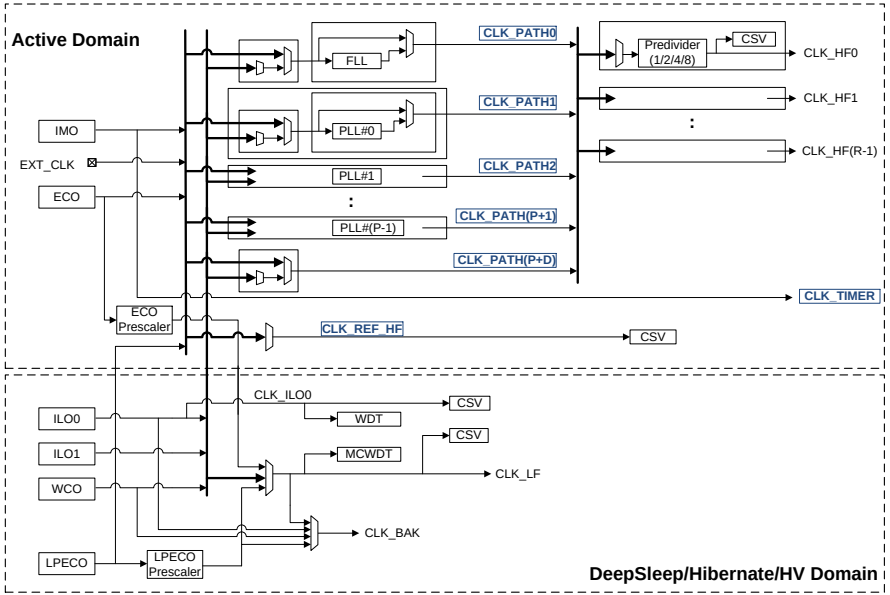
- Clock system components
  - Clock trees
    - CLK_PATHx
    - CLK_HFx
    - CLK_REF_HF
    - CLK_LF
    - CLK_BAK
    - CLK_TIMER



Active Domain Clock Trees

Clock distribution

- CLK_PATHx
  - Input sources for the CLK_HFx roots
  - CLK_PATH0 contains the FLL output
    Up to 100 MHz (using FLL)
  - CLK_PATH1 to (P+1) contains the PLL output[1]
    - Up to 200 MHz when using PLLs without SSCG and fractional operation
    - Up to 350 MHz when using PLLs with SSCG and fractional operation
  - CLK_PATH (P+D) is a connection to root clocks
    Up to 33.34 MHz (using ECO)
- CLK_REF_HF
  - Selects IMO, ECO, EXT_CLK
  - Typically selects the IMO (8 MHz)
  - Used as reference clock for CSV_CLK_HF0 to R-1 (CLK_HF 0 to R-1 clock supervision)
- TIMER_CLK
  - CLK_IMO is input source for CLK_TIMER
  - Used as source clock of SysTick timer in CPU

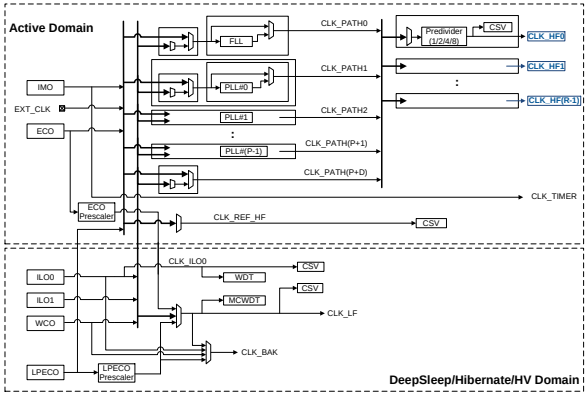


[1] Refer to the device datasheet for the target product

CLK_HF Clock Trees

› CLK_HFx can select CLK_PATHx as source clock by register[1]

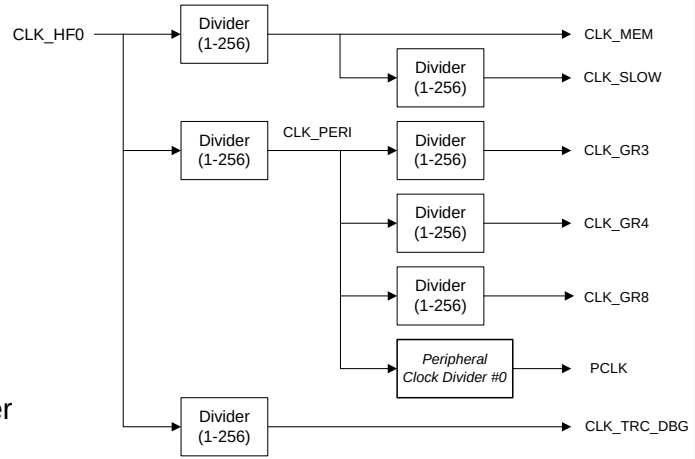
CLK Path	Usage Function	
	CYT4BF	CYT4DN
CLK_HF0	Root clock for CPUSS, PERI (CLK_MEM, CLK_SLOW, CLK_PERI)	Root clock for CPUSS, PERI (CLK_MEM, CLK_SLOW, CLK_PERI)
CLK_HF1	CM7 CPU Core#0, CM7 CPU Core#1	CM7 CPU Core#0, CM7 CPU Core#1
CLK_HF2	Peripheral clock root other than CLK_PERI	Peripheral clock root other than CLK_PERI
CLK_HF3	Event generator, clock output on EXT_CLK pins (when used as output)	Event generator, clock output on EXT_CLK pins (when used as output)
CLK_HF4	Ethernet Channel#0 and Channel#1 internal clock	Ethernet Channel#0 internal clock
CLK_HF5	I2S channel#0, I2S channel#1, I2S channel# Channel#0 TSU, Ethernet Channel#1 TSU	Sound Subsystem #0 root clock, ETH0 TSU clock (CLK_IF_SRSS0)
CLK_HF6	Root clock for SDHC, SMIF interface clock	Sound Subsystem #1 root clock (CLK_IF_SRSS1)
CLK_HF7	Not connect	Sound Subsystem #2 root clock (CLK_IF_SRSS2)
CLK_HF8	Not supported	SMIF#0 root clock
CLK_HF9	Not supported	SMIF#1 root clock
CLK_HF10	Not supported	Video Subsystem root clock
CLK_HF11	Not supported	Display#0 root clock
CLK_HF12	Not supported	Display#1 root clock
CLK_HF13	Not supported	Not connect



[1] Refer to the Register TRM (CLK_ROOT_SELECT) for additional details

CLK_HF Distribution (1/2)

- CLK_HF0[1] distribution
  - Distributed to CLK_MEM, CLK_SLOW, CLK_PERI, and CLK_TRC_DBG
  - CLK_MEM
    - Source clock for CPUSS fast infrastructure
    - Up to 200 MHz[2]
  - CLK_SLOW
    - Source clock for CPUSS slow infrastructure such as CM0+, Crypto, DMAs, test controller, and some peripherals[3]
    - Up to 100 MHz
  - CLK_PERI
    - Source clock for some peripherals via divider
    - Up to 100 MHz
  - PCLK and CLK_GR
    - Source clock for peripheral functions via divider
  - CLK_TRC_DBG
    - Source clock for trace components in debug infrastructure
    - Runs only when debugger is connected



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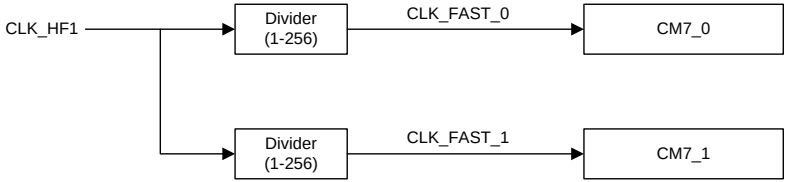
Training section references:

CPU Subsystem

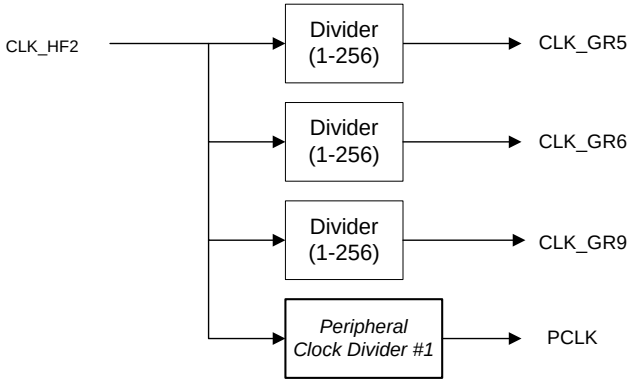
[1] CLK_HF0 can be enabled and disabled by register. CLK_HF0 is always enabled as the clock source of CPU
[2] Refer to the device datasheet for the target product
[3] eFuse and SRSS registers

CLK_HF Distribution (2/2)

- CLK_HF1 distribution
  - Root clock for the CM7 CPUs
  - Distributed to CLK_FAST_0 and CLK_FAST_1
  - Divider setting is possible independently for each M7 CPU



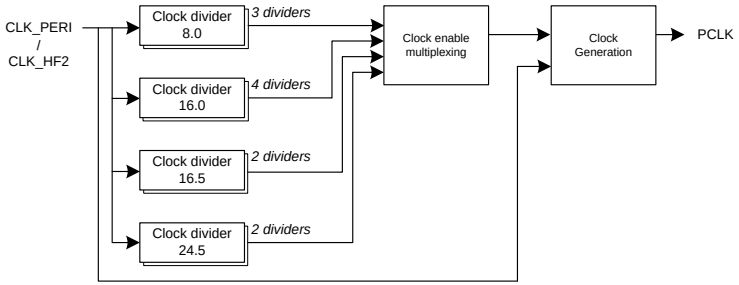
- CLK_HF2 distribution
  - Input clock for peripheral clock dividers
  - Root clock such as CAN FD, LIN, SCB, SAR ADC



Peripheral Clock Distribution

- PERI Clock Divider
  - Output of dividers can be routed to any peripheral
  - Two dividers
    - Peripheral clock divider#0
      - Input clock: CLK_PERI
      - Used for IOSS, TCPWM, and CPUSS
    - Peripheral clock divider#1
      - Input clock: CLK_HF2
      - Used for CAN FD, LIN, SCB, and SAR ADC
  - Four types of dividers[1]
    - 8-bit divider[2]
    - 16-bit divider[2]
    - 16.5-bit divider[2]
    - 24.5-bit divider[2]
  - Supports fractional clock dividers
  - Phase aligning
    - Can be phase-aligned with any of the other (enabled) clock dividers

Peripheral clock divider structure



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Review TRM section 18.6 for additional details on clock numbers, which are assigned for each peripheral

Clock dividers can be configured through the following registers:

DIV_8_CTL

DIV_16_CTL

DIV_16_5_CTL

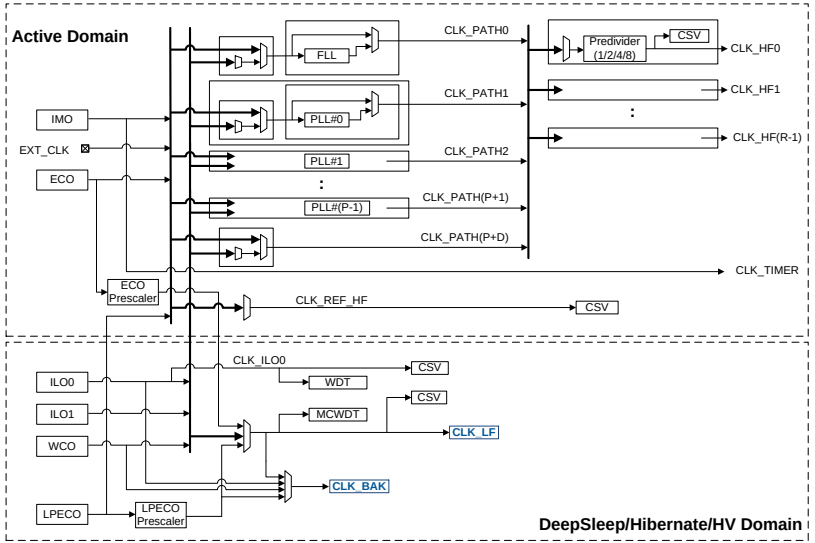
DIV_24_5_CTL

Clock Enable multiplexers can be configured through CLOCK_CTL registers, which are assigned for each peripheral

[1] Not all dividers are supported
[2] The supported number of each divider differs between Peripheral clock divider#0 and Peripheral clock divider#1

DeepSleep/Hibernate/HV Domain Clock Trees

- Clock distribution
  - CLK_LF
    - Selects ILO0, ILO1, WCO, LPECO
    - Input source for MCWDT
    - Used as reference clock for CSV_ILO (CLK_ILO0 clock supervision)
  - CLK_BAK
    - Selects CLK_LF, ILO0, ILO1, WCO, LPECO
    - Input source for RTC[1] clock



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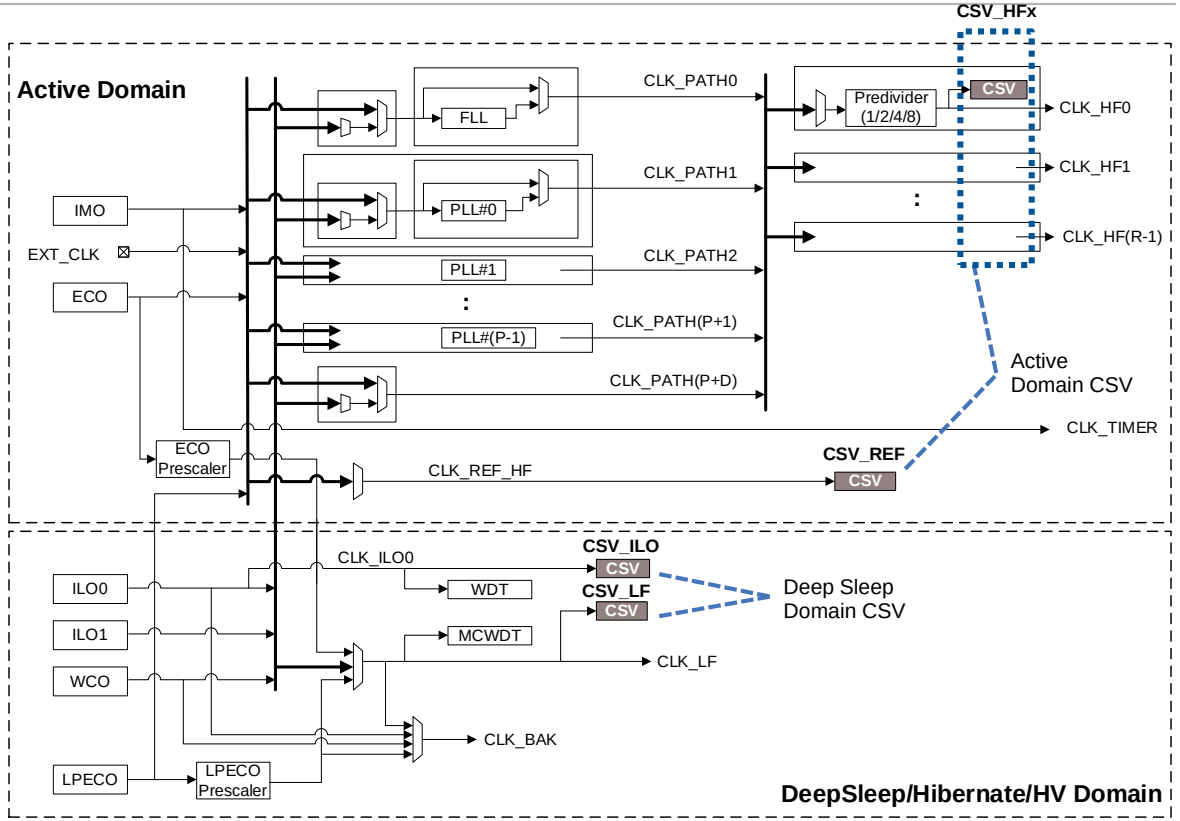
Multi-counter watchdog timer (MCWDT)

Training section references: Watchdog Timer

[1] Typically, WCO is connected to RTC. CLK_LF can also connect to RTC

Clock System Block Diagram

- Clock system components
  - Clock supervision (CSV) allows one clock to be monitored with another clock (reference clock)
  - Monitored clock sources
    - CLK_HFx
    - CLK_REF_HF
    - CLK_ILO0
    - CLK_LF
  - CSV power domain
    - Active domain CSV
    - DeepSleep domain CSV

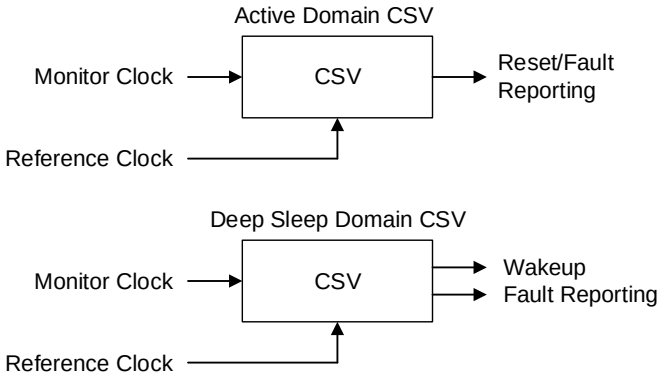


Clock Supervision (1/2)

- Checks if the frequency of the monitored clock is within the allowed frequency window
  - Uses a reference clock to supervise the behavior of the monitor clock

CSV Components	Monitor Clock	Reference Clock	Note
CSV_HFx	CLK_HFx	CLK_REF_HF	CLK_REF_HF is selected the IMO or EXT_CLK or ECO CLK_REF_HF is typically selected the IMO (default)
CSV_REF	CLK_REF_HF	CLK_ILO0	–
CSV_ILO	CLK_ILO0	CLK_LF	CLK_LF is selected WCO or ILO1 or ECO Pre-scaler
CSV_LF	CLK_LF	CLK_ILO0	–

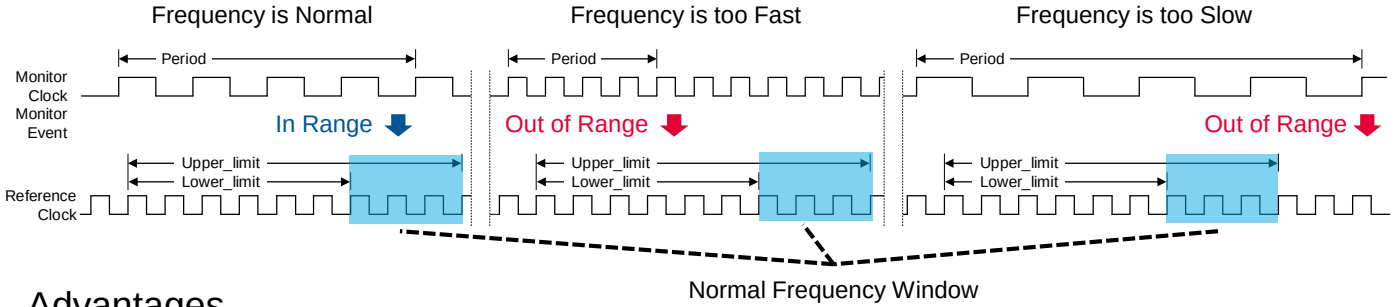
  - Active domain CSV: CSV_HF0/1 and CSV_REF
    - Automatically stops during DeepSleep and restarts by wakeup
    - "Wait" function to monitor startup time[1]
    - Possible to generate a reset or a fault report
  - DeepSleep domain CSV: CSV_ILO, CSV_LF
    - Operates during Active and DeepSleep
    - Generates wakeup and fault reports
  - All CSVs are initially off



[1] Need to prevent a false error detection at startup

Clock Supervision (2/2)

- CSV operation
  - The monitored clock generates a Monitor event (Period) and the reference clock generates a lower and upper limit
  - The Monitor event is compared against a lower limit/upper limit
  - An error is reported if the Monitor event ≤ lower limit or the Monitor event > upper limit



- Advantages
  - Detects clock stop, too fast, and too slow by frequency window
  - Monitors clock in Active, Sleep, and DeepSleep power modes with Active domain CSV and DeepSleep domain CSV
  - Can achieve ASIL-B

Hint Bar

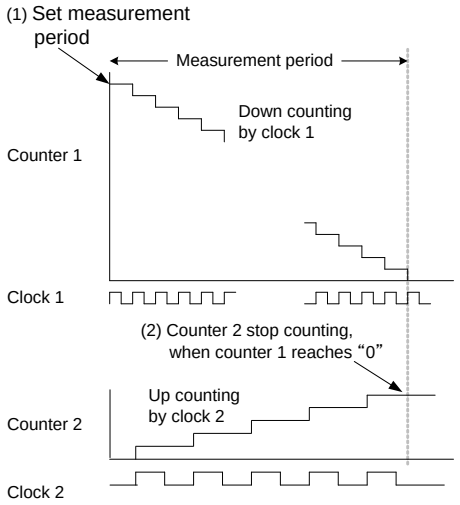
The monitor clock and the reference clock are asynchronous (typical). Therefore, the frequency window needs to account for the maximum clock tolerance

Clock Calibration Counter

- Clock Calibration Counter Operation
  - Two counters: Counter1 and Counter2
    - Counter1 is clocked by clock1 (reference clock)
    - Counter2 is clocked by clock2 (measurement clock)
  - Counter1 sets the measurement period by the count number of clock1 (1)
  - Counter2 indicates the count number of clock2 during the measurement period (2)
  - Clock2 frequency can be calculated using the following formula with two counter values

$$\text{clock2frequency} = \frac{\text{Counter2value}}{\text{Counter1value}} \times \text{clock1frequency}$$

  - All clock sources are available for these two clocks (clock1 and clock2)
- Use Case
  - Measure a low-accuracy clock such as the ILO using a high-accuracy clock such as the ECO



Hint Bar

Review TRM section 18.7 for additional details

Count Clock1 and 2 can be selected through the CLK_OUTPUT_FAST register

Appendix

Comparison Between CYT2BL, CYT4BF, and CYT4DN (1/4)

Features		CYT2BL	CYT4BF	CYT4DN
IMO		Supported		
ECO		Supported		
ILO 0		Supported		
ILO 1		Supported		
WCO		Supported		
LPECO		Not implemented		Supported
FLL	Number of FLL	1		
	Input Range	0.25 to 80 MHz		0.25 to 100 MHz
	Output Range	24 to 100 MHz		
PLL	Number of PLL	1	2	3
	Input Range	3.988 to 33.34 MHz		
	Output Range	11 to 160 MHz	11 to 200 MHz	
PLL400	Number of PLL	Not implemented	2	5
	Input Range	Not implemented	3.988 to 33.34 MHz	
	Output Range	Not implemented	25 to 350 MHz (*)	25 to 400 MHz
	SSCG	Not implemented	Yes	
	Fractional Operation	Not implemented	Yes	

(*) Spreading off

Comparison Between CYT2BL, CYT4BF, and CYT4DN (2/4)

Features		CYT2BL	CYT4BF	CYT4DN
CLK Trees Source Clock	CLK_PATH 0	FLL		
	CLK_PATH 1	PLL	PLL400	
	CLK_PATH 2	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL400	
	CLK_PATH 3	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL	PLL400
	CLK_PATH 4	Not implemented	PLL	PLL400
	CLK_PATH 5	Not implemented	ECO,IMO,EXT_CLK,WCO, ILO0/1	PLL400
	CLK_PATH 6	Not implemented		PLL
	CLK_PATH 7	Not implemented		PLL
	CLK_PATH 8	Not implemented		PLL
	CLK_PATH 9	Not implemented		ECO,IMO,EXT_CLK,WCO, ILO0/1,LPECO
	CLK_REF_HF	ECO,IMO,EXT_CLK		ECO,IMO,EXT_CLK, LPECO
	CLK_TIMER	CLK_HF0, IMO	IMO	
	CLK_LF	ILO0/1, WCO, ECO		ILO0/1, WCO, ECO, LPECO
	CLK_BAK	CLK_LF, ILO0, WCO		CLK_LF, ILO0, WCO, LPECO

Comparison Between CYT2BL, CYT4BF, and CYT4DN (3/4)

Features		CYT2BL	CYT4BF	CYT4DN
CLK Distribution	CLK_HF0	CPUSS clocks, PERI, and AHB infrastructure	CPUSS (Memories, CLK_SLOW, Peripherals)	CPUSS (Memories, CLK_SLOW, Peripherals)
	CLK_HF1	Event Generator	CPUSS (Cortex-M7 CPU 0, 1)	CPUSS (Cortex-M7 CPU 0, 1)
	CLK_HF2	Not connect	CAN FD, FlexRay, LIN, TCPWM, SCB, SAR ADC	CAN FD, CXPI, LIN, SCB, SAR ADC
	CLK_HF3	Not implemented	Event Generator	Event Generator
	CLK_HF4	Not implemented	Ethernet	Ethernet
	CLK_HF5	Not implemented	Audio subsystem	Sound Subsystem #0
	CLK_HF6	Not implemented	SDHC Interface, SMIF	Sound Subsystem #1
	CLK_HF7	Not implemented	Not connect	Sound Subsystem #2
	CLK_HF8	Not implemented	Not implemented	SMIF #0
	CLK_HF9	Not implemented	Not implemented	SMIF #1
	CLK_HF10	Not implemented	Not implemented	Video Subsystem
	CLK_HF11	Not implemented	Not implemented	Video Display #0
	CLK_HF12	Not implemented	Not implemented	Video Display #1
	CLK_HF13	Not implemented	Not implemented	Not connect

Comparison Between CYT2BL, CYT4BF, and CYT4DN (4/4)

Features		CYT2BL	CYT4BF	CYT4DN
Clock Divider	Number of Dividers	1	2	
	Fractional Clock Divider	24.5-bit dividers		16.5-bit dividers, 24.5-bit dividers
	Phase Aligning	Supported		
Clock Supervision		Supported		
Calibration Counter		Supported		

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6400993	12/7/2018	Initial release
*A	6633414	7/22/2019	Added slide 4,12 Updated Figure slide 6, 7, 10, 13, 19, 20, 22, 23, 25, 26 Updated slide 2, 5, 13, 15 - 17, 21, 22, 24, 25, 28, 32 – 34
*B	7060646	01/06/2021	Updated slide 2-5, 9, 11, 13, 15-17, 21-23, 25, 30, 32-35