TLE4986C-XTS-M47

Programmable True Power On Sensor

Data Sheet

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Revision History	
Page or Item	**Subjects (major changes since previous revision)** **TLE4986C-XTS-M47 Data Sheet Rev1.0 (2014-10-02)**
Revision 1.1, 2014-11-07	
Page 27	Chapter 7.1/ Package Outline udapted
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1 Overview

1.1 Features

- Hall switching sensor to measure speed or phase of pole/tooth wheels
- Digital output signal (voltage interface)
- Mono-cell chopped Hall system
- TPO True Power On functionality
- TIM Twisted Independent Mounting
- Dynamic self-calibrating algorithm
- IST Individual Switching Threshold
- End-of-line programmable switching points
- EEPROM for various algorithm options
- TC of back-bias magnet pre-programmed
- High resistance to mechanical stress
- Enhanced immunity against ESD and EMC
- Improved µ-cut capability
- Enhanced operating temperature range
- Module package PG-SSO-3-52

1.2 Description

The TLE4986C is an active Hall sensor ideally suited for camshaft applications and similar industrial applications such as speedometer. Its basic function is to map either a tooth or a notch into a unique electrical output state. It has an electrical trimming option for post-fabrication trimming in order to achieve true power on capability even in the case of production spreads such as different magnetic configurations or misalignment. An additional self-calibration module has been implemented to achieve optimum accuracy during normal running operation. It comes in a three-pin package for the supply voltage and an open drain output.

Table 1 Version

Type	Marking	Ordering Code	Package
TLE4986C-XTS-M47	86BAC2	SP001062648	PG-SSO-3-52

2 General

2.1 Pin Configuration and Sensitive Area

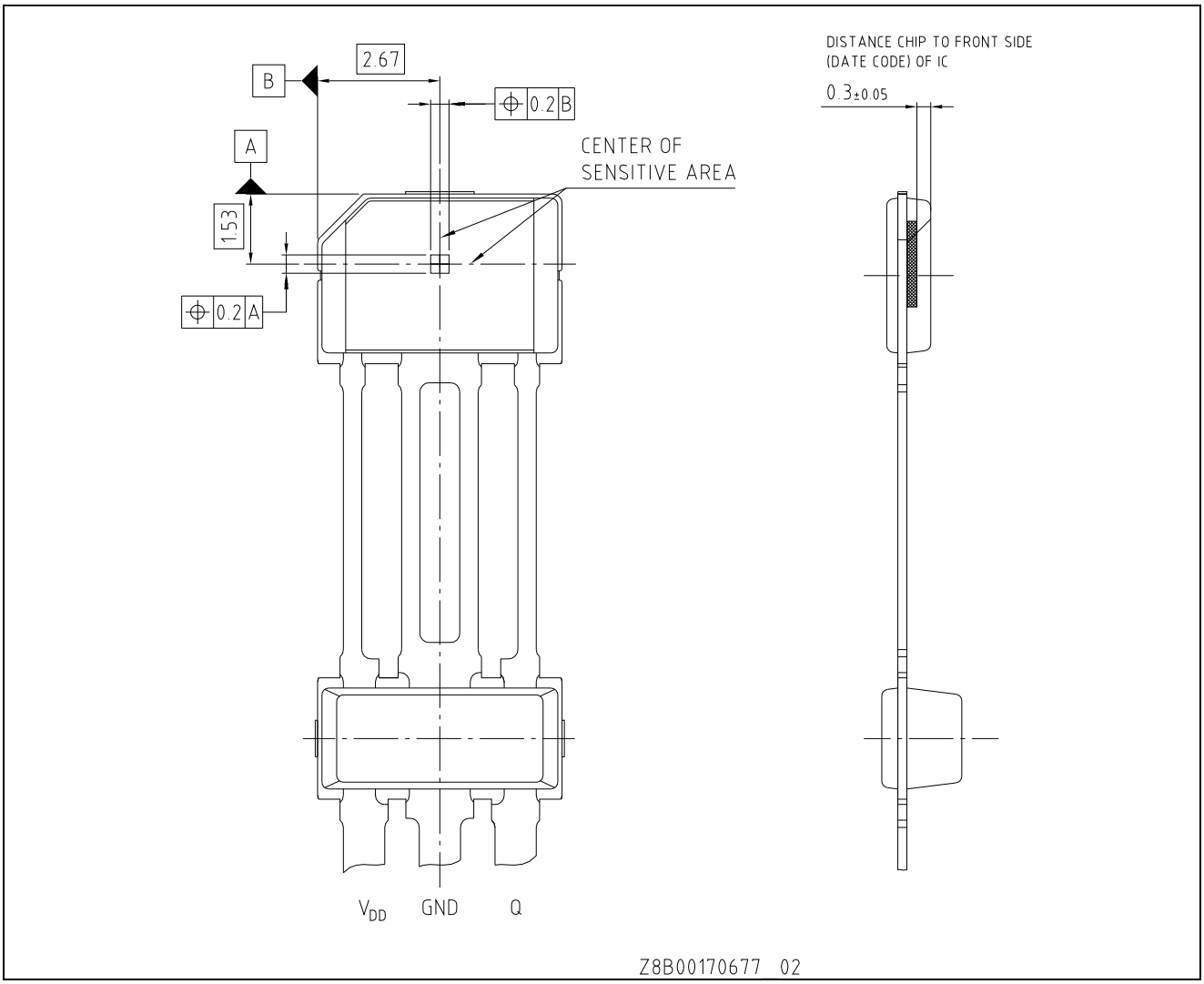

Figure 1 Pin configuration and sensitive area

Table 2 Pin Description

Pin Number	Symbol	Function
1	V_s	Supply Voltage
2	GND	Ground
3	V_{OUT} (Q)	Open Drain Output

2.2 Definition of the Magnetic Field

The magnetic field of a permanent magnet exits from the north pole and enters the south pole. If a north pole is attached to the backside of the TLE4986C, the field at the sensor position is positive, as shown in **Figure 2**.

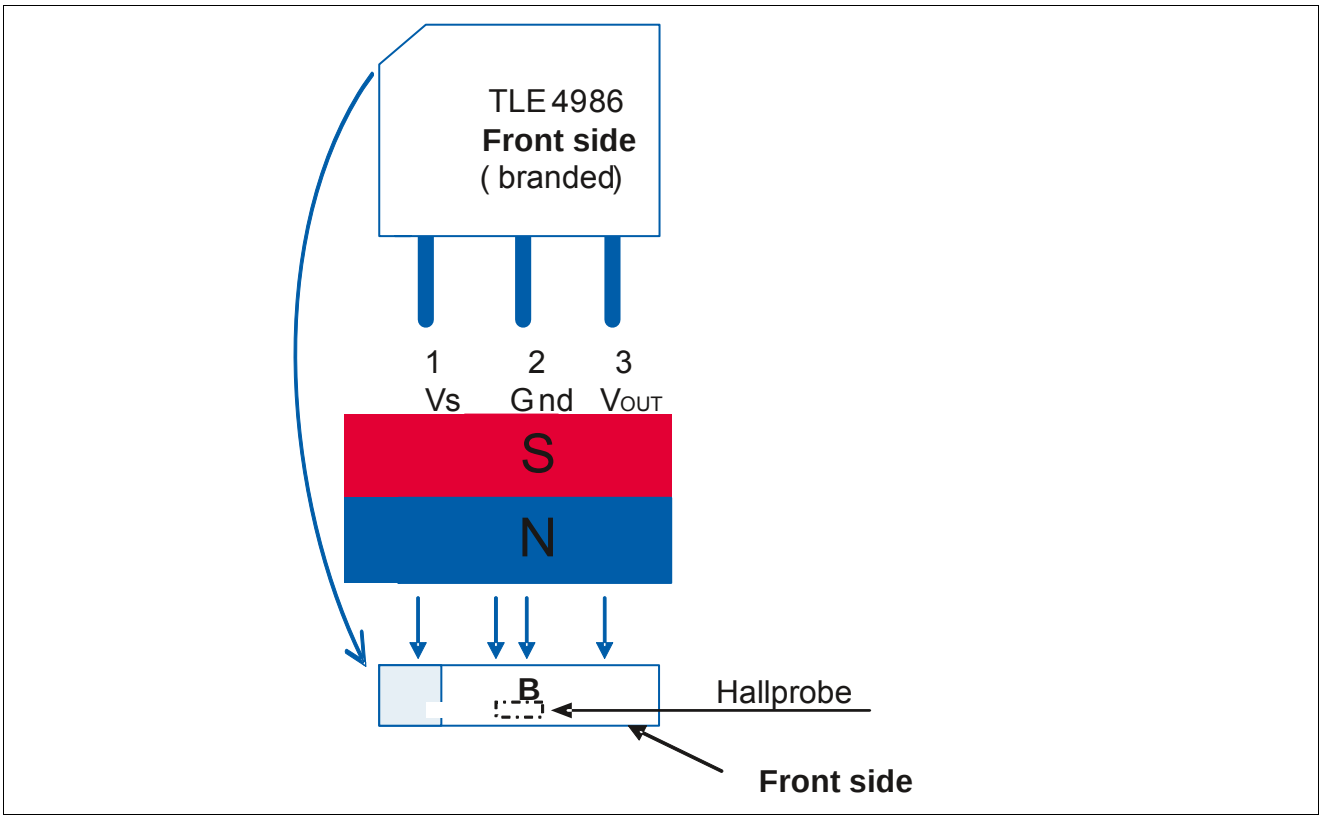

Figure 2 Definition of the Positive Magnetic Field Direction

2.3 Functional Description

The basic operation of the TLE4986C is to map a „large" positive magnetic field (tooth) into a "low" electrical output signal and to map a „weak" positive magnetic field (notch) into a "high" electrical output. Optionally the other output polarity can be chosen by programming the EEPROM. A magnetic field is considered as positive if the North Pole of a magnet shows towards the rear side of the IC housing. Since backbias-reduced magnetic configurations still show significant flux densities in one distinct direction the circuit is optimized for one flux direction in order to provide an optimal signal to noise behavior.

For understanding the operation of the TLE4986C three different phases have to be considered:

- Initial operation after power up. This phase will be referred to as „initial phase".
- Operation following the initialisation before having full information about the target wheel. This phase will be referred to as "precalibrated phase".
- Normal operation with running target wheel. This phase will be referred to as „calibrated phase".

2.4 Initial Phase

The magnetic information is derived from a chopped Hall amplifier. The threshold information comes from a EEPROM-register that may be programmed at any time. The magnetic information is compared against the threshold and the output state is set correspondingly. Some hysteresis is introduced in order to avoid false switching due to noise.

In case that EEPROM is only pre-programmed by the supplier (EEPROM has not been programmed by the customer) the chip starts an auto-search for the actual magnetic value. The initial threshold value is set to this magnetic value. This feature can be used to find a TPO-value for providing correct programming information to the chip simply by setting the chip in front of a well-defined static target. In this case a moving target wheel is not necessary.

In case there is the EEPROM programming by the customer, the open drain output will be turned on or off by comparing the magnetic field against the pre-programmed value.

In case of EEPROM failure, after power on the open drain will be high ohmic for typical 2.6ms and then permanently locked to output low level.

2.5 Precalibrated Phase

The pre-calibrated phase follows the initial phase, where the IC permanently monitors the magnetic signal. It reliably detects minima (caused by a notch) and maxima (caused by a tooth) when the variation of the signal is larger than the DNC (Digital Noise Constant), of values proportional to 25% of the amplitude, but not smaller than DNCmin. Once the IC has found a pair of min / max values it calculates the optimum threshold level and adjusts the system offset in such a way, that the switching occurs on this level. The internal offset update algorithm checks also the magnetic edge in that point in time when an offset update is to be released. Positive updates of the offset are released only at magnetic falling edges, negative offset updates only on magnetic rising edges. Otherwise an update on the wrong magnetic edge may cause additional switching. The threshold adjustment is performed through increments limited to a certain value, in order to avoid totally wrong updates caused by large signal disturbances (EMC-events or similar). The sum of these updates is programmable to either 48mT or 96mT maximum value. The optimum threshold level may differ depending on the target wheel. For example, for regular gearwheels the magnetic signal is close to a sinusoid and the optimum threshold value can be considered as 50% value, which is the mean value between minimum and maximum signal. Depending on the starting position (start angle), especially for wheels showing imperfections, e.g. such as run-out or overshoot, the last updated switching threshold in precalibrated mode can have different values depending on power-on position. This is a consequence of the continuous offset updates with the new found pairs of min / max. But further threshold adaption is performed in calibrated phase (described in next chapter) either based on the highest maxima/ lowest minima or averaged extrema over multiple revolutions to a level, that is finally independent from the starting position. For camshaft wheels an optimum threshold may be at a different percent-value in order to have minimum phase error over airgap variations. See **Figure 8** for definition of this dynamic switching level.

In case that the initial EEPROM-value does not lead to a switching of the IC because it is slightly out of the signal range the IC nevertheless does its threshold value correction in the background. After having corrected for a sufficient amount the IC will start its output switching. The output switching includes some hysteresis in order to avoid false switching.

If the IC has been pre-programmed only, it uses the default 51.17% value between the minimum and the maximum as a switching level.

2.6 Calibrated Phase

After a programmable number of switching events (2, 4...16, 18...30, 32...62, 64) the accuracy is considered to be quite high. At this time the chip is switched into a calibrated phase where only minor threshold corrections are allowed.

In this phase a period of a programmable number (1,2..15,16..32) of maxima is taken into account to find the range of the magnetic signal. Depending on the programming, the absolute minimum and maximum within this period, or the average values of the minima and maxima will be used to calculate the threshold. The threshold correction per cycle is limited to 1LSB or to a value proportional to the amplitude of the magnetic field, which can be programmed additionally.

At any time a maxima or a minima can be disregarded for the threshold calculation if it does not fit within the range defined by previously detected extrema, if this feature has been enabled by corresponding EEPROM programming.

Update filter algorithms are programmable and provide configurability for the calibration process. The programmability refers to the minimum distance from the current threshold to the one calculated to enable calibration and the necessary succession of the threshold updates directions for up to 4 consecutive periods.

The purpose of these strategies are to avoid large offset deviations by having single magnetic disturbances. Also irregularities of the target wheel are cancelled out, since the minimum and maximum values are derived over at least one full revolution of the wheel. The duration until achieving the final phase accuracy on one side depends on the choosen algorithm variant via EEPROM setting, but also strongly depends on the mounting air gap and the used camshaft wheel geometry, i.e. the number of teeth, tooth to notch ratio etc, as well as its mechanical accuracy. The output switching is done at the threshold level without visible hysteresis in order to achieve maximum accuracy. Nevertheless the chip has some internal protection mechanisms in order to avoid multiple switching due to noise.

2.7 Changing the Phase of Operation

Every time after power up the chip is reset into the initial phase. Subsequent phases (pre-calibrated, calibrated) are entered consecutively as described before. In addition, a plausibility check is implemented in order to enable some self-recovery strategy in case of unexpected events.

The IC checks if there is signal activity seen by the digital logic and at the same time there is no switching at the output. An event trigger is activated if there are 2 maxima and 2 minima (counting always starts with a maxima) detected without output switching, that means that the IC is reset into the initial mode (see **Chapter 2.8.3**).

The IC checks if the necessary threshold update is larger than a calculated value proportional with the magnetic field amplitude, equivalent to loosing calibration. If the digital circuitry detects this condition as met, the IC is reset into the pre-calibrated phase.

2.8 Reset

There are several conditions, which can lead to a reset condition. For the IC behavior we have to distinguish between a “output hold mode”, a “long reset”, a “short reset” and a “software reset”.

2.8.1 Output Hold Mode

This operating mode means that the output is held in the actual state and there is no reset on the digital part performed. This state will be released after the IC reaches his normal operation condition again and goes back into the operating mode he was before.

The following conditions lead to the output hold mode:

- A drop in the supply voltage to a value less than 2.4 V but higher than 2.0 V for a time not longer than 1 µs to 2 µs.

2.8.2 Long Reset

This reset means a total reset of the analogue as well as for the digital part of the IC. The output is forced to its default state (“high”). This condition remains for less than 1 ms. After this time the IC is assumed to run in a stable condition and enters the initial phase where the output represents the state of the target wheel (EEPROM value).

The following conditions lead to a long reset:

- Power-on condition.
- Low supply voltage: In case of drop of the supply voltage to values less than 2.4V for a time longer than 500µs, a total reset of the analog as well as for the digital part of the IC will occur.

2.8.3 Short Reset

This reset means a reset of the digital circuitry. The output remains locked in the state it had before the triggering of the short reset for 50 µs. During this time the BTPO is loaded. After 50 µs the IC goes to initial phase. For an pre-programmed device (BTPO not programmed by customer) the output is locked in its current state for 1200 µs during which internally successive approximation is performed. After this time interval the device goes to initial phase. Then the output is released again and represents the state of the target wheel (EEPROM value).

The following conditions lead to a short reset:

- If there are two min- and two max-events found without a switching event at the output (counting always starts with a maxima).

2.8.4 Software Reset

This reset can be performed in the testmode through the serial-interface. The IC output is then used as data output for the serial interface.

The following condition lead to a software reset:

- There is a reset applied through the serial Interface

The table bellow shows an overview over the behavior of the output under certain conditions.

Table 3 Output Behavior Under Certain Conditions

	Pre-Programmed		Programmed	
	Noninverted	**Inverted**	**Noninverted**	**Inverted**
Output hold mode	Q_{n-1} [1)]	–	Q_{n-1}	Q_{n-1}
Long reset	High	–	High	High
Short reset	Q_{n-1}	–	Q_{n-1}	Q_{n-1}
Initial phase	High (self calibration)	–	Normal TPO	Inverted TPO
Precalibrated phase	Normal[2)]	–	Normal	Inverted[3)]
Calibrated phase	Normal	–	Normal	Inverted

1) Q_{n-1} = State of output before a reset occurs
2) Normal = "low" if $B > B_{Threshold}$; "high" if $B < B_{Threshold}$
3) Inverted = "high" if $B > B_{Threshold}$; "low" if $B < B_{Threshold}$

2.8.5 Voltage drop capability (µCut)

For supply voltage drops in the specified range (see **Figure 3** and specification in **Table 7**) the device is capable to keep the last digital data information prior to the event. The output is undefined during the voltage drop time, but after the voltage returned to normal operating condition the previous data information as internally stored will be presented. The voltage drop functionality is available after the first calibration window in the calibration phase has been performed.

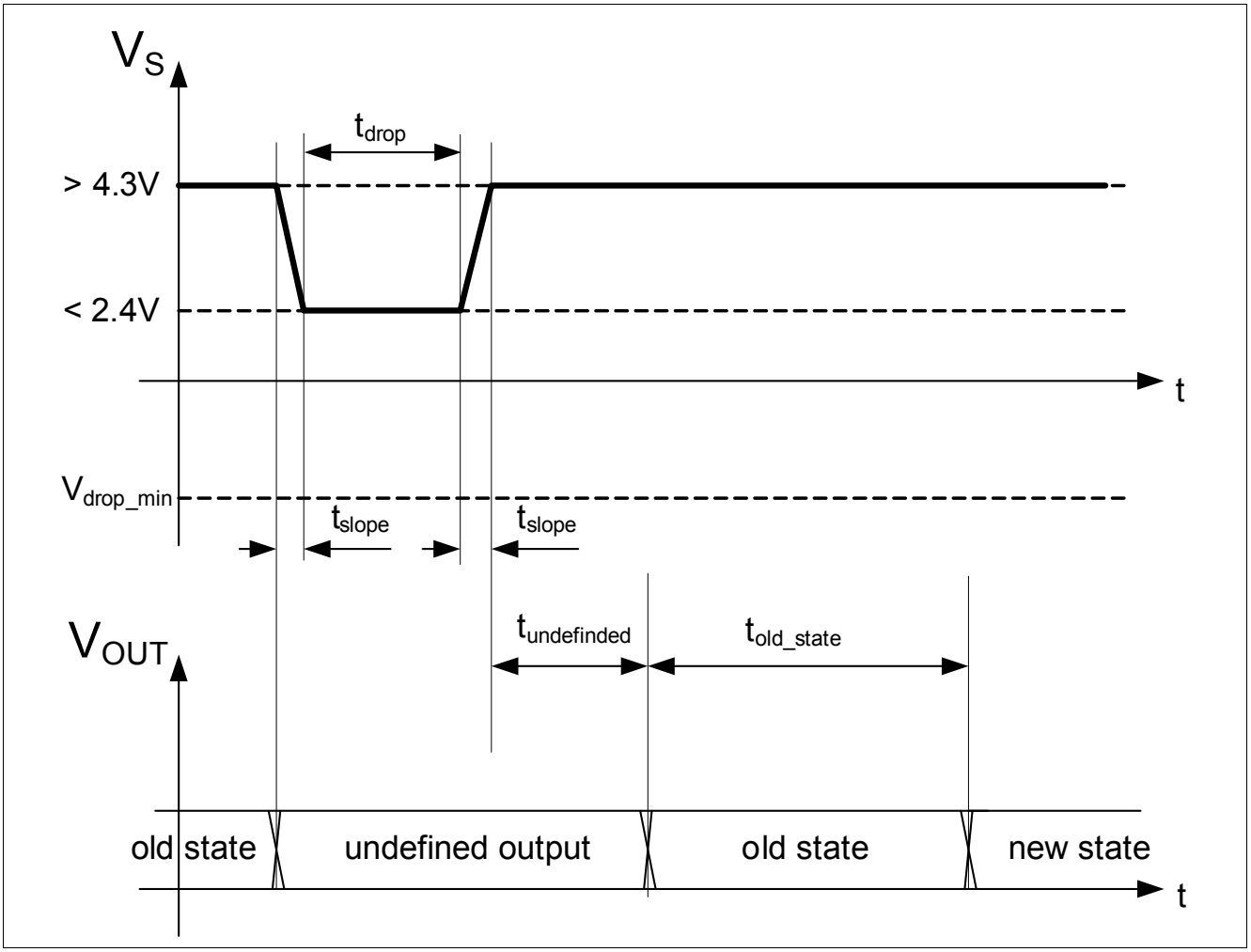

Figure 3 Voltage Drop Capability

2.9 Hysteresis Concept

There are two different hysteresis concepts implemented in the IC, which can be set in the EEPROM, in the part only accessible for Infineon. Default setting is the hidden hyteresis.

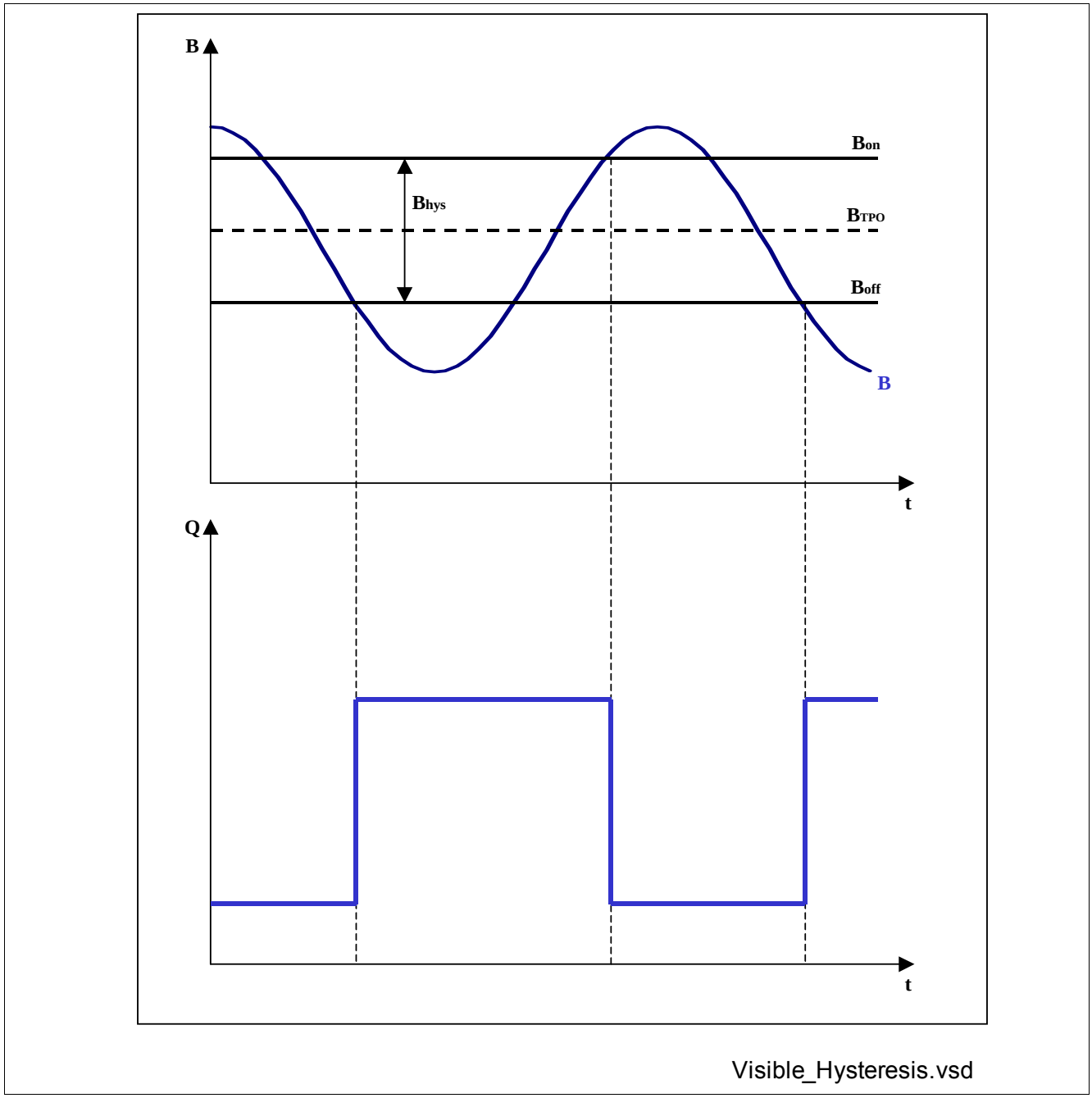

Figure 4 Visible Hysteresis

The visible hysteresis, meaning that the output switching levels are changed between two distinct values (depending on the direction of the magnetic field during a switching event), whenever a certain amount of the magnetic field has passed through after the last switching event. See **Figure 4** for more details.

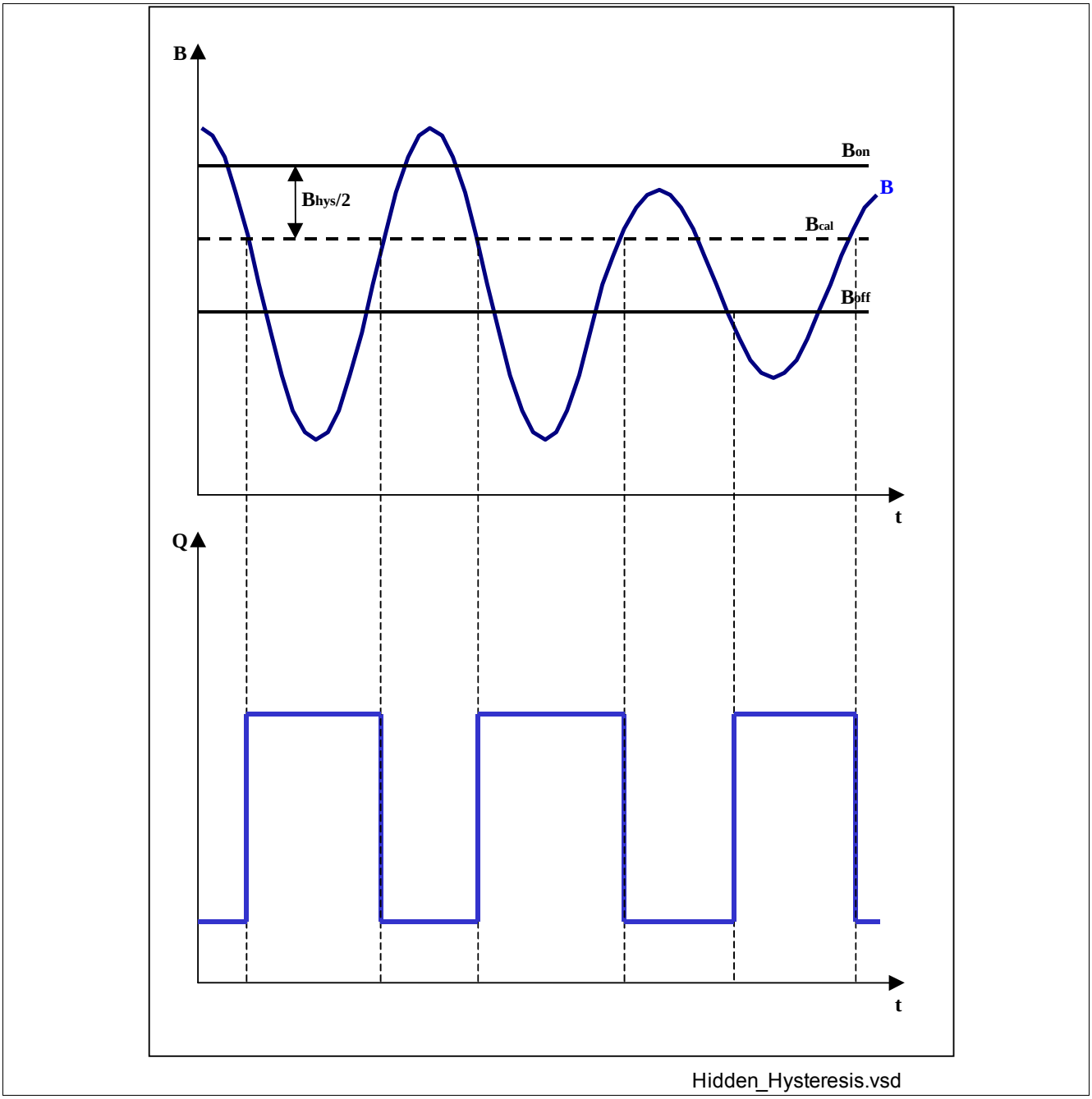

Figure 5 Hidden Hysteresis

The second form of hysteresis is called hidden hysteresis. This means, that the hysteresis cannot be observed from outside. If the value of the switching level does not change, the output always switches at the same level. However, inside the IC there are two distinct levels close above and below the switching level, which are used to arm the output. This level can be programmed by having 2 options (for details see magnetic parameters). Hence, if the value of the magnetic field crosses the lower of these hysteresis levels, then the output will be able to switch if the field crosses the switching level. After this switching event the output is disabled until the value of the magnetic field crosses one of the two hysteresis levels. If it crosses the upper hysteresis level, then the output is armed again and can switch if the magnetic field crosses the switching level. On the other hand, if the magnetic field does not reach the upper hysteresis level, but the lower hysteresis level is crossed again after a switching event, then the output is allowed to switch, so that no tooth is lost. However, this causes an additional phase error. For more details see **Figure 5**.

The IC can be alternately programmed to exhibit an adaptive hysteresis behavior:

The value of the hysteresis (B_{on} - B_{off}) will be proportional to the magnetic signal amplitude and not lower than the specified minimum level. For more details see **Figure 6**

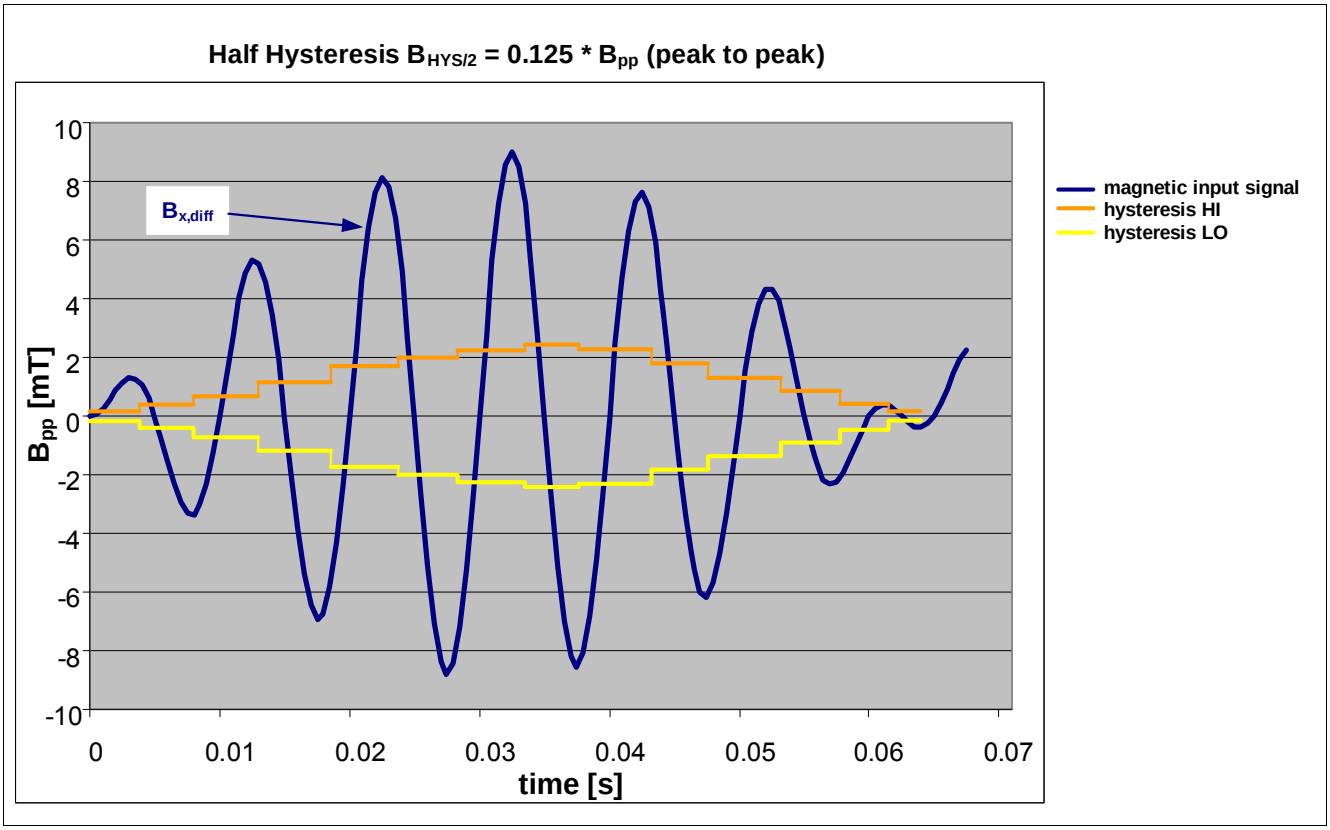

Figure 6 Adaptive Hysteresis

2.10 Serial Interface

The serial interface is used to program the chip. At the same time it can be used to provide special settings and to read out several internal registers status bits. The interface description consists of a physical layer and a logical layer. The physical layer describes format, timing and voltage information, whereas the logical layer describes the available commands and the meaning of bits, words and addresses.

2.11 Physical Interface Layer

The data transmission is done over the $V_{s\text{-}pin}$, which generates input information and clock timing, and the $V_{out\text{-}pin}$, which delivers the output data. Generally the interface function is disabled; this means, that in normal operation including normal supply distortion the interface is not active and therefore the chip operates in its normal way.

2.11.1 Data Transmission

Commands are sent to the IC through pulse modulation of V_{S_IC} between two voltage levels V_S, high and V_S, low. Commands are sent in series of 17 pulses corresponding to 16 bit words: each of the first 16 pulses is decoded as 0's or 1's internally, depending on the pulse duty cycle, with MSB transmitted first LSB last. A logical "1" is represented by a long (2/3 of one period) "high" voltage level (higher than 12 V) on the supply followed by a short (1/3 of one period) "low" voltage level (lower than 5 V), whereas a logical "0" is represented by a short "high" level on the supply followed by a long "low" level. At the same time this high/low voltage combination, which forms in fact a bit, acts as a serial interface clock which clocks out logical high / low values on the output. We recommend a period length of around 200 µs per bit.

End of word is indicated by a long (we recommend longer than 200 µs, first 30 µs should be higher than 5 V and the rest lower than 5 V) "low" supply. Please note, that for communicating 16 bits of data 17 $V_{S\text{-}pulses}$ are necessary. If more than 16 input bits are transmitted the output bits are irrelevant (transmission buffer empty) whereas the input bits remain valid and start overwriting the previously transmitted bits. In any case the last 17 transmitted bits are interpreted as transmitted data word (16 bits) + 1 stop bit.

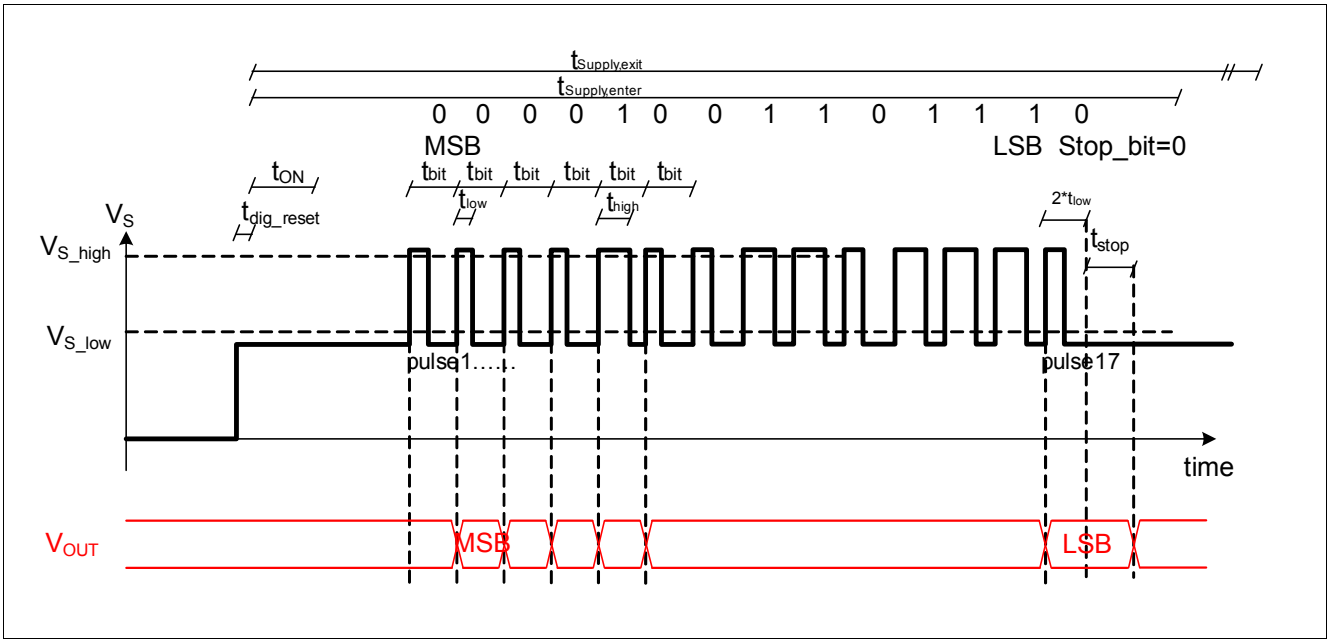

Figure 7 Serial Protocol

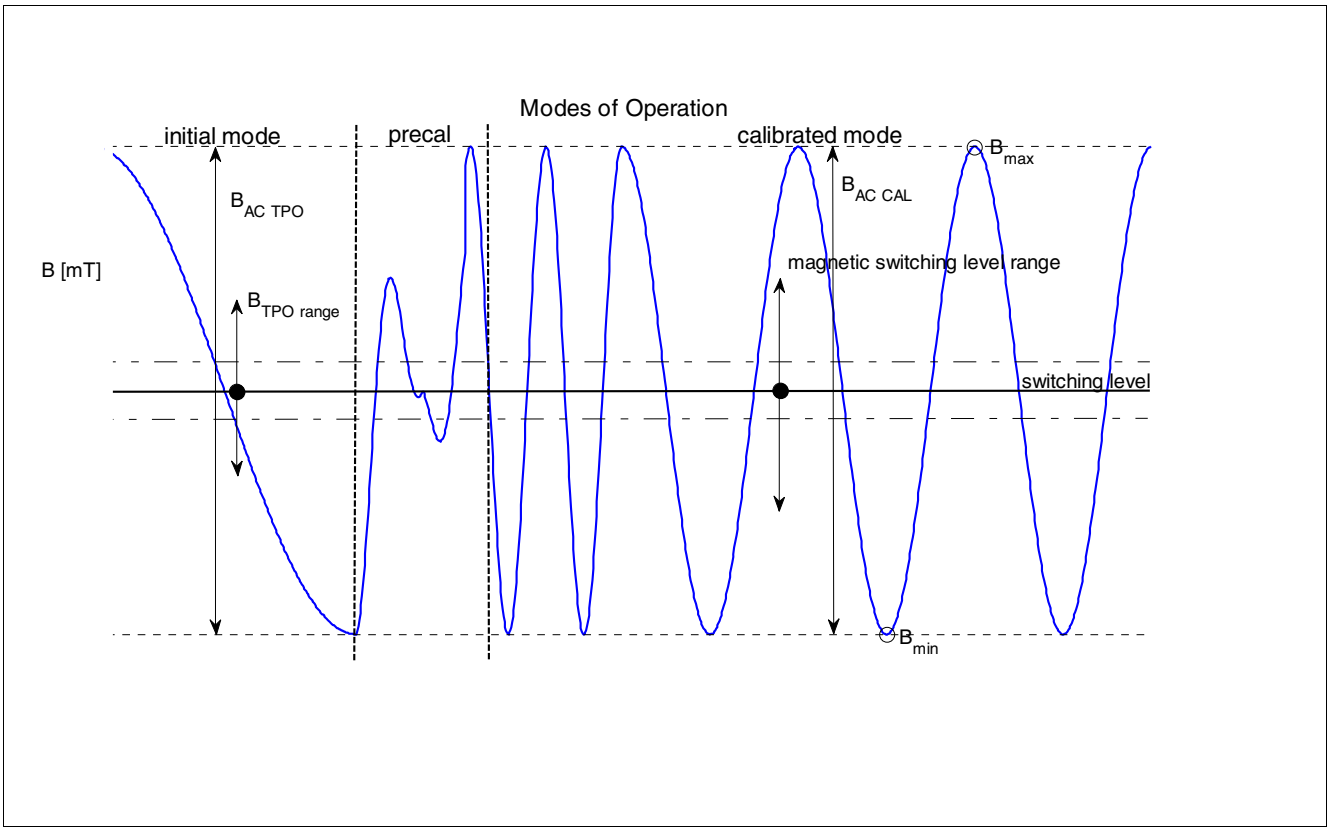

Figure 8 Phases of Operation

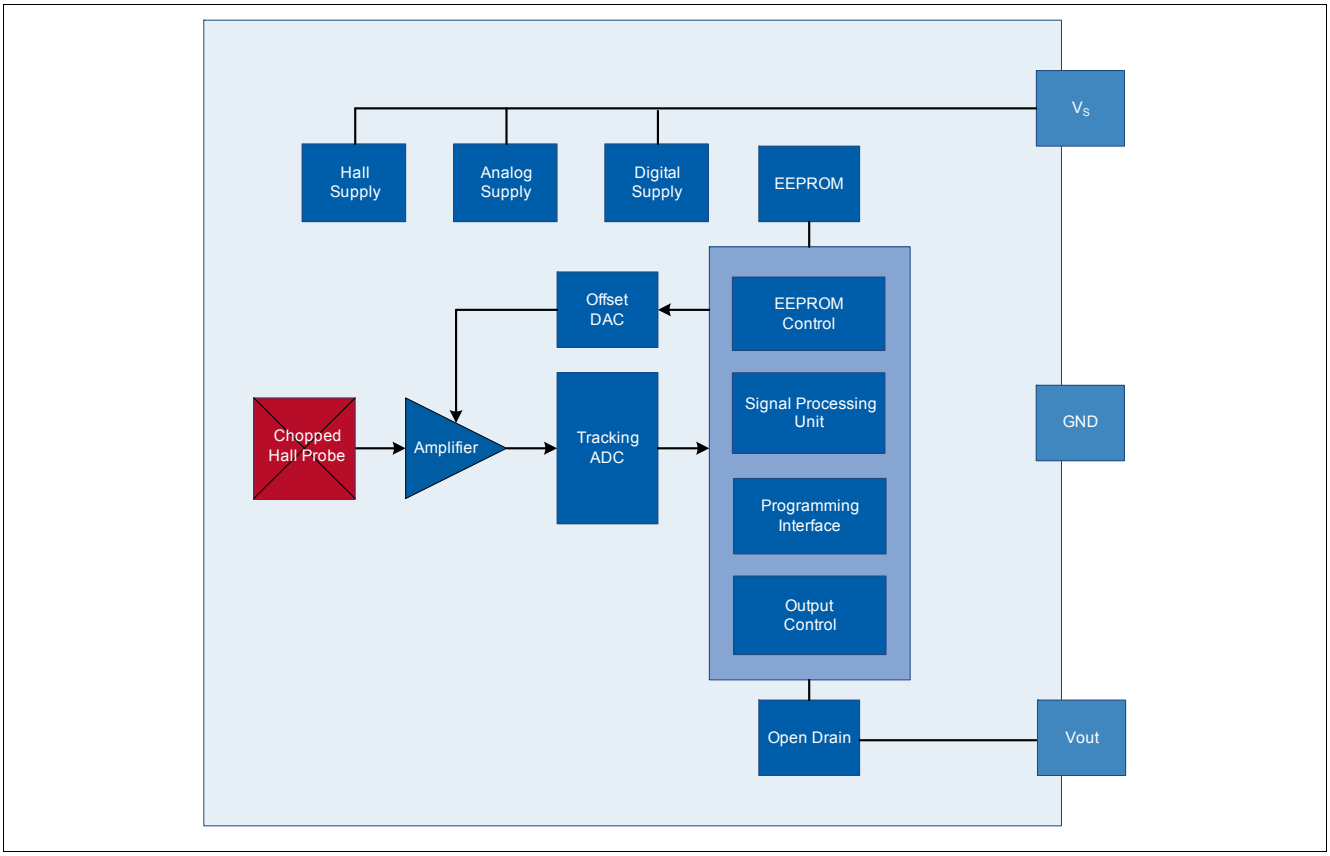

Figure 9 Block Diagram

3 General Characteristics

3.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltages						
Supply voltage	V_S	-18	–	18	V	Continuos
	$V_{S\ AC}$	-24	–	24	V	1 hour max, R_{Series} ≥ 100 Ω
		-26	–	26	V	5 min, R_{Series} ≥ 100 Ω
		-28	–	28	V	60 s max, R_{Series} ≥ 100 Ω
Output OFF voltage	V_{OUT_OFF}	-0.5	–	18	V	Continuos
		–	–	24	V	1 hour max, R_{Load} ≥ 500 Ω
		–	–	26	V	5 min, R_{Load} ≥ 500 Ω
		–	–	28	V	60 s max, R_{Load} ≥ 500 Ω
Output ON voltage	V_{OUT_ON}	–	–	16	V	Current internal limited by short circuit protection (72h@TA<40°C)
		–	–	18	V	Current internal limited by short circuit protection (72h@TA<40°C
		–	–	26	V	Current internal limited by short circuit protection (72h@TA<40°C
Currents						
Continuos output current	I_{OUT}	-50	–	50	mA	–
Temperatures						
Junction temperature range	T_J	-40	–	175	°C	Exposure time: max. 2500h at T_J=175°C
		–	–	195	°C	Exposure time: max. 10x1h at T_J=195°C additive to other lifetimes
Thermal Resistance						
Thermal resistance junction - air	R_{THJA}		–	190	K/W	–
Induction						
Magnetic field induction	B_Z	-5	–	5	T	Magnetic pulse during magnet magnetization. Valid 5 s with T_A= 80°C
ESD Resistivity						
ESD compliance	ESD_{HBM}	-6	–	6	kV	HBM[1)]

1) ESD susceptibility, HBM according to EIA/JESD 22-A114B

Note: Stresses above the max values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

All parameters specified in the following sections refer to these operating conditions unless otherwise specified.

Table 5 General Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltages						
Supply Voltage with supply resistance R_s (AC ... application circuit)	$V_{S\ AC}$	4.9	–	18	V	R_{Series} = 100 Ω
Supply Voltage without supply resistance R_s	V_S	4.3	–	18	V	–
Continuos Output Off voltage	V_{OUT_OFF}	-0.3	–	18	V	–
Currents						
Continuous output On current	I_{OUT_ON}		–	20	mA	Load
Capacitance						
Capacitance between IC supply & ground pins	C_1	42.3	47	51.7	nF	Capacitor type X8R, rated voltage =50 V[1)]
Output capacitance between IC output and ground pins	C_2	4.23	4.7	5.17	nF	Capacitor type X8R, rated voltage =50 V[1)]
Resistance						
Series resistance on supply line of the IC	R_{Series}	0	–	100	Ω	V_S=13.5 V ; no R_S needed for 5 V applications
Programming						
Maximum No. of EEPROM programming cycles	N_{PROG}	–	–	100	n	–
Magnetic Signal						
Magnetic signal frequency range for camshaft applications	F_{CAM}	0	–	5000	Hz	–
Temperatures						
Normal operating junction temperature	T_J	-40	–	175	°C	Exposure time: max. 2500h at T_J=175°C
Storage temperature	$T_{Storage}$	-60		170	°C	Without sensor function
Ambient temperature range for device features reading and programming	T_{RDPROG}	15	25	80	°C	At customer.
Temperature variations between engine stop and restart.	ΔT_{SG}	–	–	60	°C	Device powered continuously

1) Specified at room temperature, test condition at 25°C with 1V at 1kHz

Note: In the operating range the functions given in the functional description are fulfilled

3.2.1 Temperature Coefficient

Table 6 Temperature Coefficients

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Programmable temperature coefficient of BTPO	TC_{BTPO}	-1400	–	-200	ppm/K	Range to compensate TCmagnet, typical -600 ppm/K
Deviation to programmed temperature coefficient of BTPO	ΔTC_{BTPO}	-300	–	300	ppm/K	TC deviation -40°C to 150°C[1)]
		-1.95	–	1.95	%	TC deviation at -40°C[1)]
		-3.75	–	3.75	%	TC deviation at 150°C See **Figure 10**

1) ±300 ppm/K (±1.95%) @ -40°C guaranteed by design referred to second order TC_{BTPO} compensation.Furthermore this compensation comprises the adjustment to second order effect of magnet

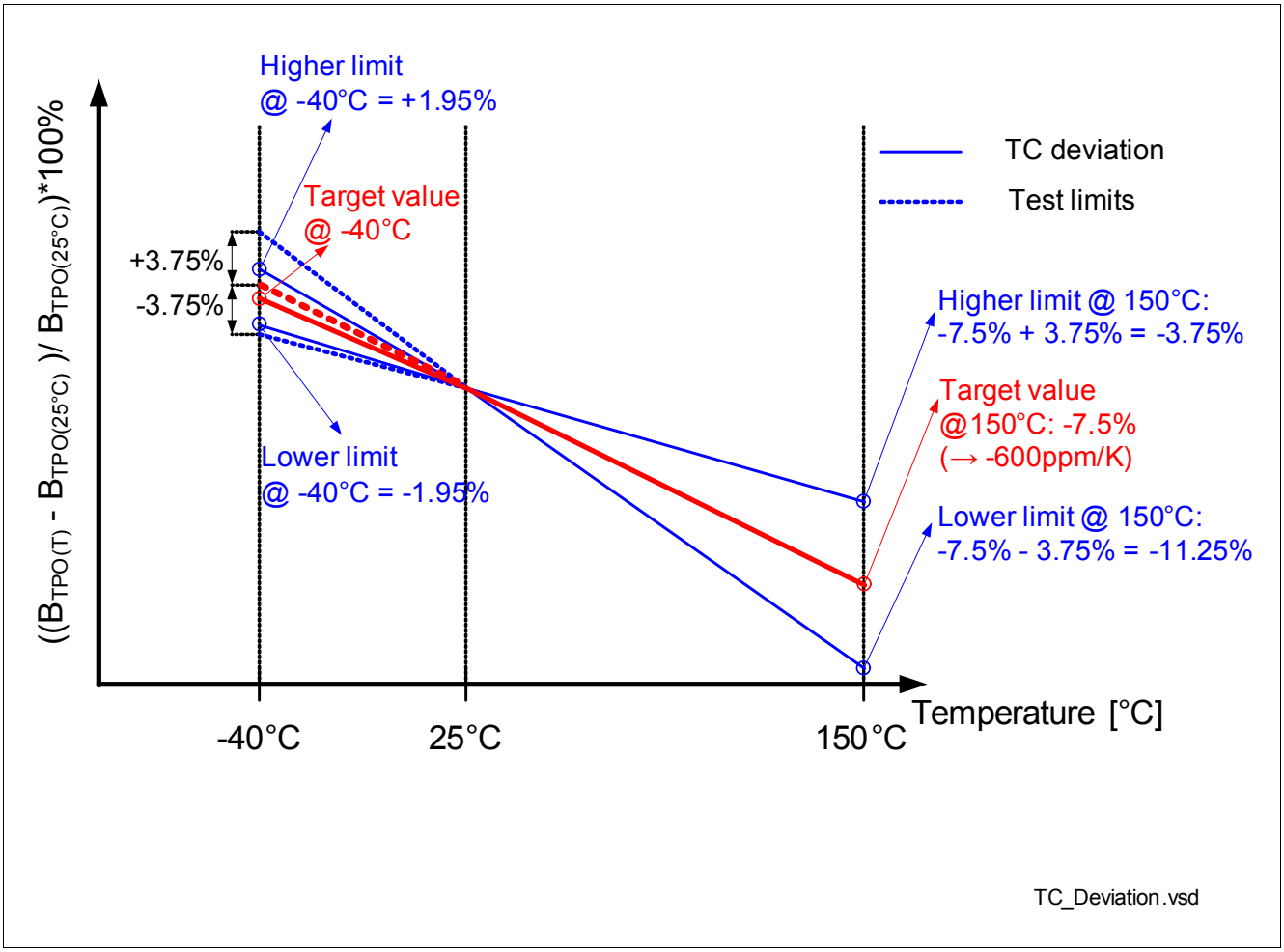

Figure 10 Temperature Coefficient of TPO Switching Point

4 Electrical and Magnetic Characteristic

All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to V_{DD} = 12 V and T_A = 25°C

Table 7 Electrical and Magnetic Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltages						
Output saturation voltage	V_{Qsat}	–	0.25	0.5	V	I_{Out} = 20 mA
		–	-	0.4	V	I_{Out} = 15 mA
		–	-	0.3	V	I_{Out} = 10 mA
		–	-	0.2	V	I_{Out} = 5 mA
Clamping voltage V_S-Pin	V_{Sclamp}	42	65	–	V	–
Clamping voltage V_{Out}-Pin	$V_{OUTclamp}$	42	50	60	V	I_{Out} = 2 mA
Analog reset voltage	V_{Sreset}	–	3	3.3	V	–
Voltage drop (µCut)						
Voltage drop	V_{drop_min}	0	-	2.4	V	at 25°C, start from operating condition
Voltage drop time	t_{drop}	-	-	100	µs	
		-	-	110	µs	T_J <30°C
Voltage drop slope	t_{slope}	-	-	3	µs	
Undefined output state	$t_{undefined}$	-	-	70	µs	
Old output state	t_{old_state}	-	-	150	µs	
Currents						
Output leakage current	$I_{Outleak}$	–	0.1	10	µA	V_Q = 18 V
Current limit for short circuit protection	$I_{Outshort}$	30	50	80	mA	–
Supply current	I_S	4	5.5	7	mA	
Supply current @ 24 V	I_{Smax}	–	–	8	mA	R_{Series} ≥ 100 Ω
Temperature						
Junction temperature limit for output protection	T_{prot}	195	210	230	°C	–
Times						
Output rise time	t_{rise} [1)]	4.5	8.7	13	µs	V_{Sout} = 4.5 .. 24V R_{Load} = 1.2 kΩ valid between 20% - 80%
Output fall time	t_{fall} [1)]	2.2	3.8	5.4	µs	V_{Sout} = 12 V R_{Load} = 1.2 kΩ valid between 20% - 80%
Output fall time	t_{fall} [1)]	0.9	1.6	2.3	µs	V_{Sout} = 5 V R_{Load} = 1.2 kΩ valid between 20% - 80%

Table 7 Electrical and Magnetic Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power on time	t_{on}	–	0.56	1	ms	Programmed device. Time to achieve specified B_{TPO}- accuracy. During this time the output is locked
		1.1	1.6	2.1		Pre-programmed device (as delivered by IFX to customer). During this time the output is locked to high
		2.2	3.4	4.6		Device with EEPROM failure. During this time the output is locked to high. After this time the output will be locked to low
Delay time of output to magnetic edge	t_d	10	17	24	µs	
Temperature drift of delay time of output to magnetic edge	Δt_d	-3.6	–	3.6	µs	Not additional to t_d
Clock frequency of digital part	f_{clk}	-	6	-	MHz	
Clock frequency used by the chopper	$f_{chopper}$	-	375	-	kHz	
Slope of magnetic edge	ΔB/Δt	-	–	2	mT/µs	Magnetic signal edge is not allowed to rise faster (otherwise tracking ADC is not able to follow)
Full scale range of the offset-DAC	FSR_{ODAC}	141	189	237	mT	Typ. B_{ODAC_0} = -35 mT Typ. B_{ODAC_2047} = 155 mT
Full scale range of the offset-DAC	$FSR_{ODACtyp}$	163	189	223	mT	T_j = 25°C
Resolution of programmable threshold in TPO mode	B_{TPO_res}	–	0.092	–	mT	–
Drift of BTPO-point[2)]	ΔB_{TPO}	-2.11	–	2,36	mT	BTPO = 44 mT
Hysteresis Option 1	B_{Hys}	0.4	0.9	1.3	mT	–
Half Hysteresis Option 1	$B_{Hys/2}$	0.2	0.45	0.9	mT	–
Hysteresis Option 2	B_{Hys}	2.5	4	5.1	mT	–
Half Hysteresis Option 2	$B_{Hys/2}$	1.2	2	3.6	mT	–
Adaptive Hysteresis Option 1	$B_{Hys/2}$	–	12.5	–	%	Minimum level: 0.4 mT, percentage of peak to peak amplitude
Adaptive Hysteresis Option 2	$B_{Hys/2}$	–	12.5	–	%	Minimum level: 2.5 mT, percentage of peak to peak amplitude

Table 7 Electrical and Magnetic Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accuracy of threshold in calibration phase[3)]	ΔB_{AC_cal}	-200	–	200	µT	
Adjustment range of switching level	k_0	-	38.67; 51.17; 63.67; 69.92	–	%	Switching point in calibrated phase is digitally determined by: Bcal = Bmin + (Bmax – Bmin) * k0
Magnetic switching level range	B	-20	–	130	mT	Valid for k_0 =51,17%
True power on range	$B_{TPO\ range}$	-20	–	75	mT	Allowed programmable TPOvalues; Hysteresis not included
Magnetic signal swing for TPO-function	B_{AC_TPO}	5.15	–	125	mT_{pp}	BTPO = 44 mT, using hyst. option 1 for min. value
Magnetic signal swing for calibrated phase	B_{AC_cal}	3	–	125	mT_{pp}	Min value depends on hyst. option; Max value depends on k-factor

1) Value of capacitor: 4.7 nF±10%; ceramic: X8R; maximum voltage: 50 V

2) This value shows the deviation from the programmed BTPO value and its temperature coefficient. Included are the package-effect, the deviation from the adjusted temperature coefficient of the BTPO point (resolution of the temperature coefficient and spread of the technology) and the drift of the offset (over temperature and lifetime). Not included is the hysteresis in the initial phase.

3) Systematic deviation due to hysteresis in the filter algorithm of 150µT not included

Note: The listed Electrical and magnetic characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not other specified, typical characteristics apply at Tj = 25 °C and V_S = 12 V.

Table 8 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Effective noise value of the magnetic switching points	B_{neff}	–	33	–	µT	T_j = 25°C[1)]
		–	55	70[2)]	µT	T_j ≤ 175°C[3)], F_{CAM} ≤ 2kHz
		–	-	120[2)]	µT	T_j ≤175°C[3)], F_{CAM} > 2kHz

1) The magnetic noise is normal distributed. The typical value represents the RMS-value and corresponds therefore to 1 Sigma probability of normal distribution. Consequently a 3 Sigma value corresponds to 0.3% probability of appearance.

2) Guaranteed by design, characterized in laboratory

3) The typical value corresponds to the RMS-value at Tj = 175°C. The max value corresponds to the RMS-values in the full temperature range and includes technological spreads.

5 Electromagnetic Compatibility

(values depend on R_{SERIES}!)

Ref: ISO 7637-2; 2nd edition 06/2004; test circuit 1 (See **Figure 11**); conducted on supply line;

ΔB =10 mT (amplitude sinus signal), V_S = 13.5 V, f_B = 100 Hz, T = 25°C, R_{SERIES} ≥ 100 Ω.

Table 9 ISO 7637-2

Parameter	Symbol	Level/Type	Status
Testpulse 1	V_{EMC}	IV / -100 V	C
Testpulse 2a		IV / 100 V	A
Testpulse 2b		IV / 10 V	C
Testpulse 3a		IV / -150 V	A[1)]
Testpulse 3b		IV / 100 V	A[1)]
Testpulse 4		IV / -7 V	A
Testpulse 5a		IV / 86.5 V	C
Testpulse 5b		IV / 86.5 V	A[2)]

1) Output signal overlaid by burst pulse

2) Suppressed V_s* = 35 V

Ref: ISO 7637-3; 1st edition 11/1995; test circuit 1 (See **Figure 11**); coupling clamp;

ΔB =10 mT (amplitude sinus signal), V_S = 13.5 V ± 0.5 V, f_B = 100 Hz, T = 25°C, R_{SERIES} ≥ 100 Ω.

Table 10 ISO 7637-3

Parameter	Symbol	Level / Type	Status
Testpulse 3a	V_{EMC}	IV / -300 V	A[1)]
Testpulse 3b		IV / 300 V	A[1)]

1) Output signal overlaid by burst pulse

6 Application Circuit

The device has two capacitors C1 and C2 already integrated on the lead frame (47nF/4.7nF). These capacitors increase the EMC robustness of the device. It is further recommended to use a serial resistor R_{SERIES} of 100Ω for protection on the supply line. A pull-up resistor R_{LOAD} is mandatory on the output pin and determines the maximum current flowing through the output transistor. A value of 1.2kΩ is recommended. (see **Figure 11**)

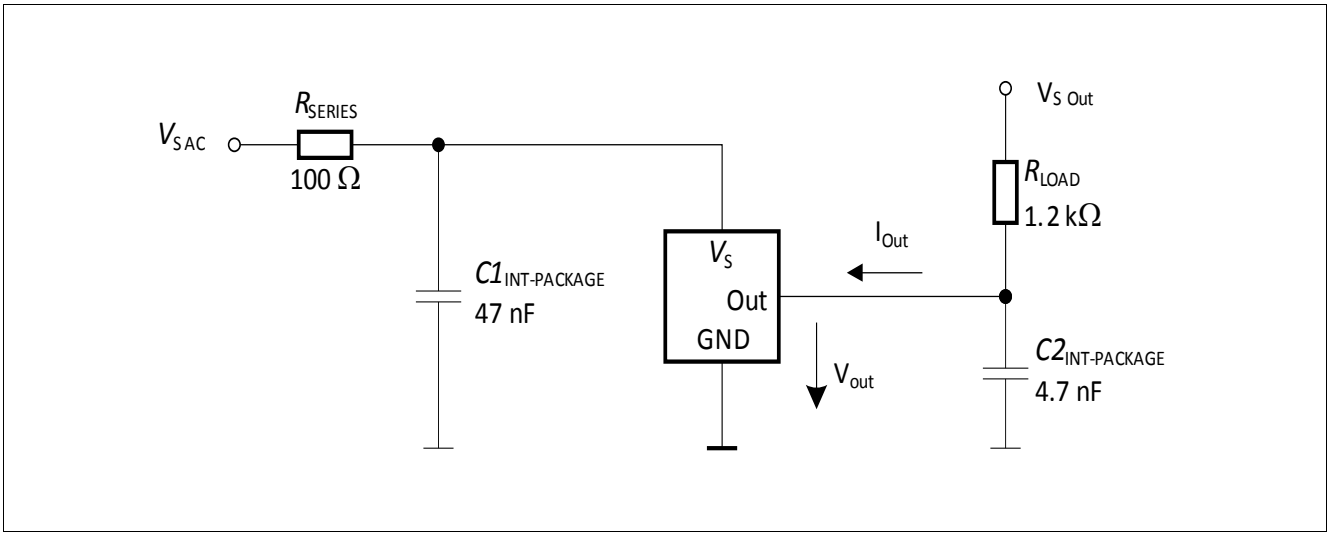

Figure 11 Typical Application Circuit

7 Package Information

Pure tin covering (green lead plating) is used. The product is RoHS (Restriction of Hazardous Substances) compliant and marked with letter G in front of the data code marking and may contain a data matrix code on the rear side of the package (see also information note 136/03). Please refer to your key account team or regional sales if you need further information.

Note: The specification for soldering and welding is defined in the latest revision of application note "Recommendation for Board Assembly-Hallsensor SSO Packages".

7.1 Package Outline

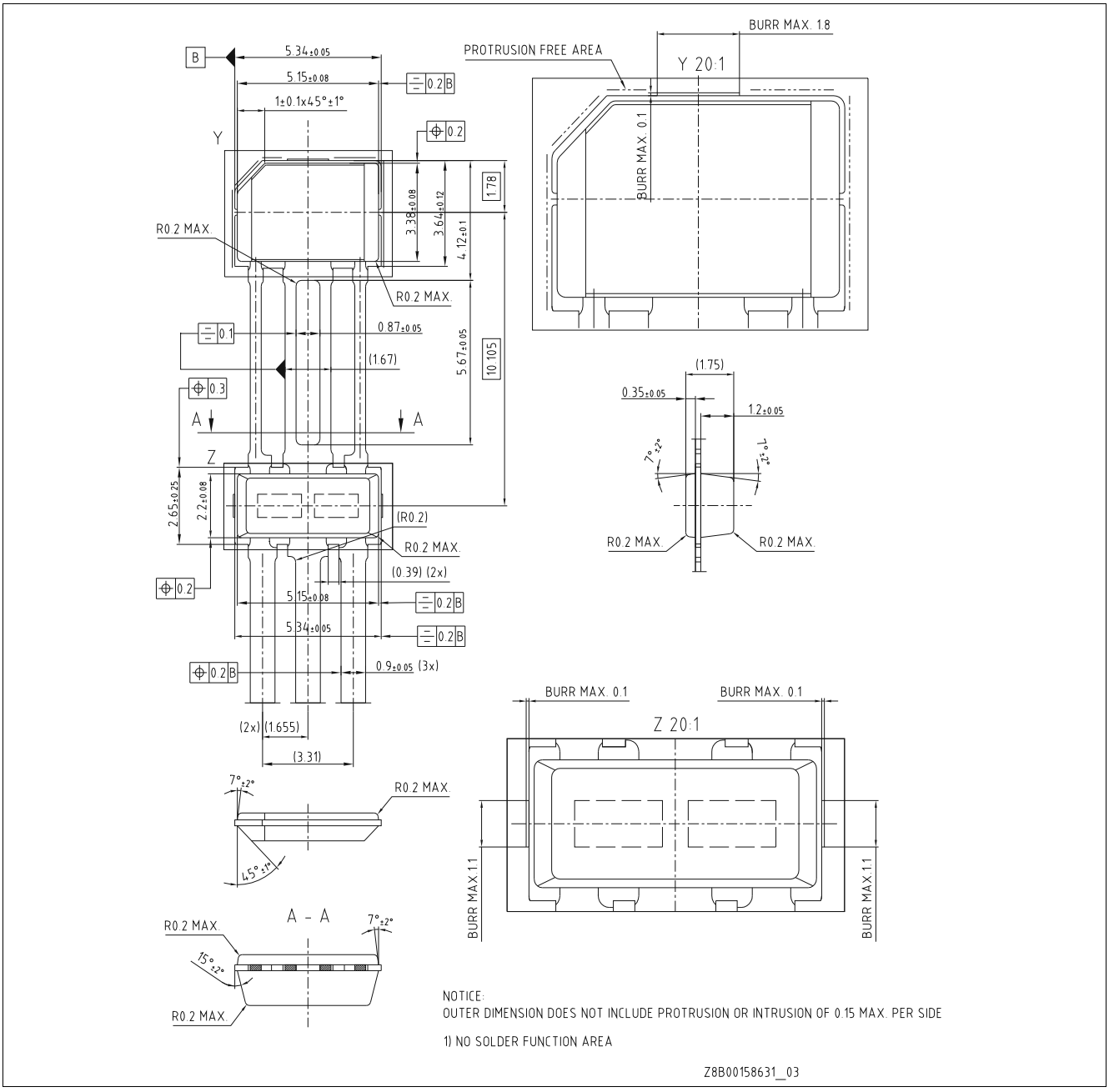

Figure 12 PG-SSO-3-52 (Plastic Green Single Slim Outline), Package Dimensions

7.2 Position of the Hall element

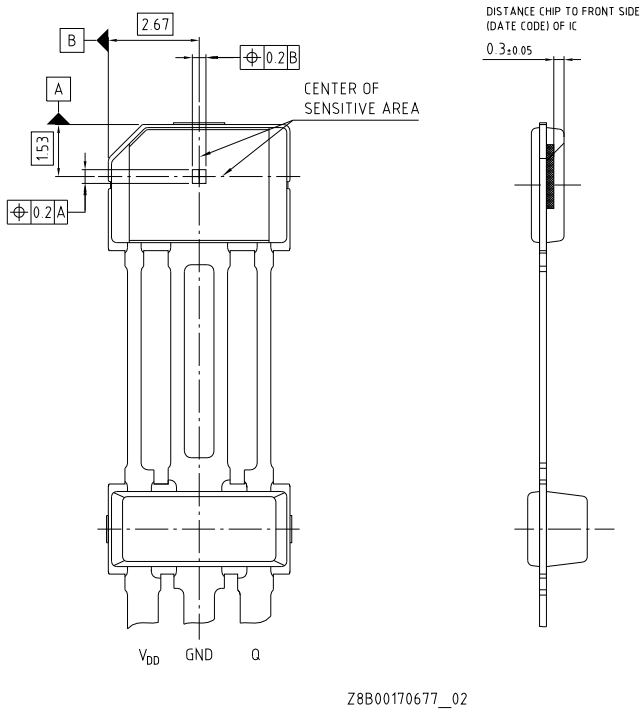

Figure 13 Position of the Hall element in PG-SSO-3-52 and distance to the branded side

7.3 Marking and Data Matrix Code

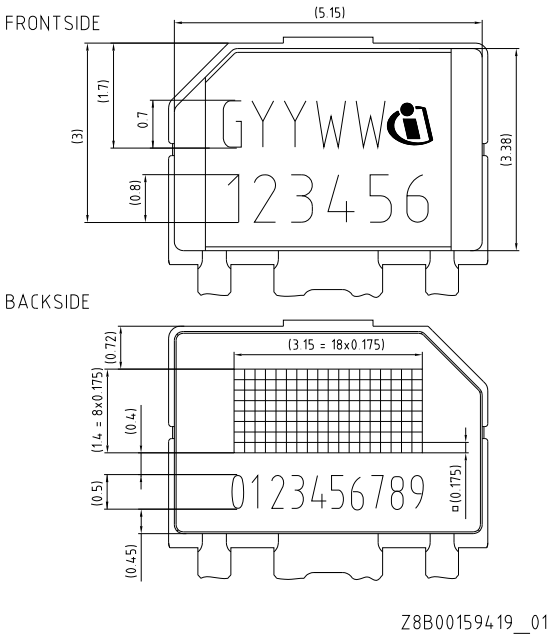

Figure 14 Marking of PG-SSO-3-52 package

7.4 Packing Information

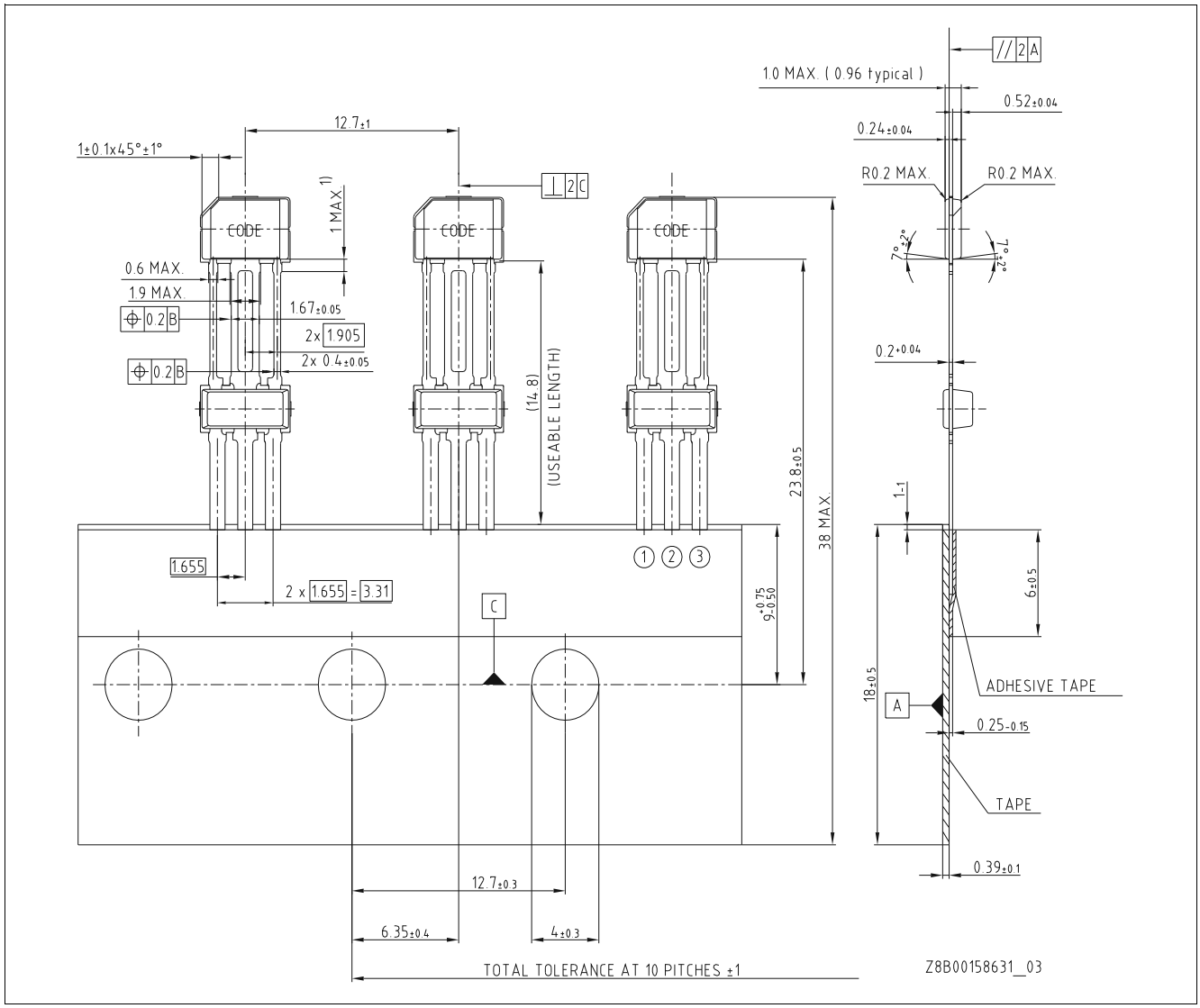

Figure 15 PG-SSO-3-52 Ammopack

8 EEPROM Description

Several options of TLE4986C-XTS-M47 can be programmed via an EEPROM to optimize the sensor algorithm to the individual target wheel and application requirements. There are four main algrithm variants selectable by setting of FUNC xx_B at address 0x01:

- pre-programmed device
- non-adaptive switching threshold
- adaptive switching threshold
- adaptive individual switching threshold (IST)

Further described EEPROM content can have partly different meaning or might be not applicable in dedicated operating conditions.

Table 11 EEPROM address 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KFACT		MGN	PCAL/ KCAL		BTPO										

Table 12 Functional Description

Field	Bit	Type	Description
KFACT	15:14	rw	Defines threshold in calibrated phase 00_B: k = 38.67% 01_B: k = 51.17% 10_B: k = 63.67% 11_B: k = 69.92%
MGN	13	rw	Sets the possible range for threshold update during pre-calibration phase and the value of minimum noise constant DNC for a programmed device DNCmin: MGN=1_B: 5mT MGN=0_B: 2.5mT Maximum threshold update in pre-calibration phase: FUNC=11_B: 96mT*(MGN+1)/PCAL_duration FUNC=01_B: 20mT (FUNC=00_B, pre-programmed: maximum threshold update 1.5mT, DNCmin=2.5mT)
PCAL applicable for FUNC=11_B	12:11	rw	Sets duration of pre-calibration phase: 00_B: PCAL_duration= 2 output transitions 01_B: PCAL_duration= 2*(NTS+1) output transitions 10_B: PCAL_duration= 2*((NTS+1)/2) output transitions 11_B & AVG_EN = 1_B: PCAL_duration= 4*(NTS+1) output transitions 11_B & AVG_EN = 0_B: PCAL_duration 64 output transitions FUNC=00_B: pre-calibration duration 64 output transitions
KCAL applicable for FUNC=01_B	12:11	rw	Defines the target threshold in the pre-calibration phase (sub-phase 1) 00_B: k=6.25% 01_B: k=12.5% 10_B: k=25% 11_B: k=50%
BTPO	10:0	rw	Defines threshold for first switching

Table 13 EEPROM address 0x01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		INV	NTS					AVG_EN	EXTFILT_EN	HYS	ADHYS_EN	UPDFILT_EN	ADSTP_EN	FAST_EN	LOCK

Table 14 Functional Description

Field	Bit	Type	Description
FUNC	15:14	rw	00_B: pre-programmed device 01_B: adaptive individual switching threshold (IST, see **Chapter 8.6**) 10_B: non-adaptive threshold 11_B: adaptive threshold
INV	13	rw	1_B: sets inverted output polarity
NTS bit 12:10 not used with FUNC=01_B	12:8	rw	Number of maxima between two ODAC corrections in calibrated phase when AVG_EN=1_B (number of teeth, length of calibration window). Number of output transitions between two ODAC corrections in calibrated phase when AVG_EN=0_B. It influences the number of output transitions to be considered in pre-calibrated phase 00000_B: 1 maxima/2 transitions 00001_B: 2 maxima/4 transitions 00010_B: 3 maxima/6 transitions 00011_B: 4 maxima/8 transitions ... 11111_B: 32maxima/ 64 transitions
AVG_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	7	rw	Set to “1” enables averaging algorithm (see **Chapter 8.1**)
EXTFILT_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	6	rw	Set to “1” enables extrema filtering algorithm (see **Chapter 8.2**)
HYS	5	rw	Setting of fixed hysteresis level (ADHYS_EN = 0_B) or minimum hysteresis level (ADHYS_EN = 1_B) for programmed device 0_B: B_{Hys}_typ=0.9mT (hysteresis option 1) 1_B: B_{Hys}_typ=4mT (hysteresis option 2)
ADHYS_EN	4	rw	1_B: adaptive hysteresis, full hysteresis value is 25% of the peak-to-peak magnetic signal, minimum value given by setting of HYS bit 0_B: fixed hysteresis
UPDFILT_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	3	rw	Set to “1” enables update filtering (see **Chapter 8.3**)

Table 14 Functional Description

Field	Bit	Type	Description
ADSTP_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	2	rw	Set to “1” enables adaptive steps feature (see **Chapter 8.4**)
FAST_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	1	rw	Set to “1” enables fast calibration feature (see **Chapter 8.5**)
LOCK	0	rw	Set to “1” locks EEPROM

8.1 Averaging Algorithm

To calculate the threshold within the calibrated phase, valid maxima and minima within a calibration window are taken into account. The length of the calibration window is given by the setting of the NTS bit. In case the averaging algorithm is activated (AVG_EN = 1_B), the average of the maxima and minima within the calibration window is used for threshold calculation. For AVG_EN = 0_B, the value of the absolute maxima and minima is used.

In the pre-calibration phase with AVG_EN bit set, averaging takes place until end of the pre-calibrated phase. The average value of the amplitude is used for threshold update calculation.

8.2 Extrema Filtering Algorithm

With extrema filtering algorithm enabled (EXTFILT_EN = 1_B) a special algorithm is performed which determines whether a detected extrema (maxima or minima) is considered as valid or invalid.

Only valid extrema are taken into account within the pre-calibration phase and within a calibration window in calibrated phase. Within a calibration window, the average value of the amplitude is taken from the previous calibration window and new minima or new maxima are only considered as valid if they are in between a tolerance interval, centered on the average of the previous calibration window. The tolerance is expressed as a percentage of the average amplitude and is a function of the k-factor value as defined in **Table 15**:

Table 15 Conditions for extrema filtering algorithm

k-factor	Percentage of amplitude
00_B	± 30.67%
01_B	± 24.42%
10_B	± 18.17%
11_B	± 15.04%

In case a single extrema is outside this interval, it is neglected for the averaging and threshold calculation. Only in case that two (or more) consecutive extrema are outside, they are taken as valid and included in the calculations. This process is continued for each calibration window.

In the pre-calibration phase, the interval for evaluation of valid extrema is twice as large as in the calibration phase. Averaging starts at the beginning of the pre-calibration phase and each new extrema is evaluated whether it’s valid

or not. Similar to calibrated phase, only single extrema outside the interval can be invalid. Two consecutive extrema are taken as valid.

8.3 Update Filtering

In calibrated phase, there are several options for the magnitude of the offset update when a offset correction is necessary. This can be adjusted with the UPDFILT_EN bit together with the setting of AVG_EN.

The **Table 16** shows the different options:

Table 16 Options for offset update size in calibrated phase

Update filtering mode	EEPROM setting
Offset update in calibrated phase is limited to 1LSB. The offset update is only performed in case of four consecutive calibration windows give the same direction of the offset update with a magnitude larger than 1LSB.	AVG_EN = 0_B
An offset update is possible after each calibration window. The magnitude of the offset update is determined by the setting of the ADSTP_EN bit (see **Chapter 8.4**)	AVG_EN = 1_B; UPDFILT_EN = 0_B
An offset update is only possible in case of two consecutive calibration windows give an offset change in the same direction with magnitude larger than 1LSB. The magnitude of the offset update is determined by **Table 18**	AVG_EN = 1_B; UPDFILT_EN = 1_B; ADSTP_EN = 1_B
An offset update is only possible in case of two consecutive calibration windows give an offset change in the same direction. The magnitude of the required offset update for the first decision must meet the condition in **Table 17**. If this condition is met, the magnitude of the performed offset update is 1LSB.	AVG_EN = 1_B; UPDFILT_EN = 1_B;ADSTP_EN = 0_B

Table 17 Conditions for offset update in conservative mode

Magnetic field	Required offset update
< 15mT	> 1LSB
< 30mT	> 2LSB
< 60mT	> 4LSB
>60mT	> 8LSB

8.4 Adaptive Steps Feature

The magnitude of the performed offset update can be configured with the setting of the ADSTP_EN bit.

Table 18 Offset update size in calibrated phase

ADSTP_EN bit	Magnetic field	Maximum offset update
0	-	1LSB
1	< 15mT	1LSB
1	< 30mT	2LSB
1	< 60mT	4LSB
1	>60mT	8LSB

8.5 Fast Calibration Feature

With fast calibration feature enabled (FAST_EN = 1_B) a special algorithm is performed in calibrated phase in case the difference between the new calculated threshold and the old threshold exceeds a certain percentage of the signal amplitude, given by **Table 19**. In this case, the device starts with a new pre-calibration phase but uses the last threshold as starting value (not BTPO).

Table 19 Conditions for fast calibration feature

k-factor	Percentage of amplitude
00_B	± 17.79%
01_B	± 18.74%
10_B	± 17.35%
11_B	± 15.77%

If this fast calibration feature is enabled, the device recovers much faster after a disturbance (air gap jump) and reaches the correct switching threshold. The switching events with incorrect phase information are minimized. In case the fast calibration feature is disabled, a disturbance causes the device to stay in calibrated phase but it may take longer time until the correct switching threshold is reached again (depending on the setting of the UPDFILT_EN bit) and incorrect phase information may be obtained during this time.

8.6 Individual Switching Threshold (IST)

The EEPROM setting FUNC=01_B at address 0x01 enables the individual tooth switching mode (IST, Individual Switching Threshold), where the device is capable to switch in calibrated mode with two, three or four individually found threshold levels, for achieving the optimum phase accuracy when using target wheels with two, three or four pairs of tooth and notch. Every of up to four teeth has a unique switching threshold, based on the individually found maximum of the respective tooth, while the minimum value is taken as the average over all minima within the calibration window.

The pre-calibration procedure starts after power up, wherein the first switching event is performed at programmed BTPO. Then the sensor permanently monitors the magnetic signal and detects minima (caused by a notch) and maxima (caused by a tooth) over a specified number of output transitions. The pre-calibration procedure is divided into two sub-phases, in sub-phase 1 a k-factor as set in KCAL is used for all teeth in order to ensure safe switching before the individual thresholds are used. This sub-phase lasts at least 2*(NTS+1) output switching events and the algorithm checks that NTS+1 maxima have been detected after the detection of the first minimum. This is done in order to ensure that an initial value for each individual thresholds has been computed during sub-phase 1. These thresholds will be applied starting with sub-phase 2.

In pre-calibration sub-phase2 the IC performs corrections for all the individual teeth and a k-factor as set in KFACT is used for computing the ODAC value. The duration of sub-phase 2 is given by a minimum of NTS+1 detected maxima. During this sub-phase the ODAC is allowed for high updates in order to adapt from a KCAL regulation target to a KFACT regulation target. While the IC calculates and updates the threshold based on found pairs of min / max values, the internal offset update algorithm also checks the magnetic edge, which means that positive ODAC updates are released only at magnetic falling edges and negative ODAC updates only on magnetic rising edges (update rule).

After reaching the calibrated phase a calibration window lasts a number of detected maxima equal to the number of teeth (NTS+1) and the individual (delta) threshold register update is performed individually for each maximum accordingly. If the direction of the individual threshold update is constant within the last 4 decisions, considering also the current one, than for the considered maximum the update is performed with 1 LSB in the corresponding direction. For ODAC updates the filtering is performed as described in Table 17, row AVG_EN = 1_B; UPDFILT_EN = 1_B; ADSTP_EN = 0_B independently of the actual settings of these EEPROM bits.

w w w . i n f i n e o n . c o m

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