# Driving decarbonization and digitalization. Together.



# Principal Engineer

# Job description

Expert in implementing Scan insertion, LPCT, LBIST, Hybrid-TK, Compression Logic and DRC analysis of implemented Testability logic structures.

In your new role you will:

- Responsible for SoC DFT Architecture definition/implementation/verification /silicon debug of SoC/Full Chip.
- Need to **implement Scan insertion, LPCT, LBIST, Hybrid-TK, Compression Logic and DRC** analysis of implemented Testability logic structures.
- Responsible for ATPG, DRC analysis, Test coverage debug, Memory BIST implementation and verification.
- Owner ship of **JTAG/BSCAN/iJTAG, P1500 implementation and verification,** Stuck-at/TDF/Bridging/Cell-aware/iddq fault models.
- Good debug skills in ZERO delay and SDF based scan/MBIST/JTAG simulations.
- Hands on experience in analysis and debug of above-mentioned test domains.
  Hands of experience in post silicon debug of scan/MBIST patterns/yield fall out

## Profile

You are best equipped for this task if you have:

- ASIC flow understanding.
- Experienced in LEC, CLP, power analysis flow is preferred
- The ability to work as an individual and as part of a team to deliver complex SoCs starting from the creation of the DFT spec, implementation, verification, and Post silicon debug.
- In addition, be self-motivated with the initiative to seek constant improvements in the **DFT design methodologies**.
- The candidate must also possess strong initiative, analytical/problem solving skills, team working skills, ability to multitask and be able to work within a diverse team environment.
- Scripting skills such as PERL/TCL/Python are preferred

#### Degree & Discipline:

• BE/B.Tech Electrical/Electronic or ME/M Tech in VLSI design.

**Experience in Industry:** 

#### At a glance

Location:	Bangalore BTP (India)
Job ID:	HRC0929486
Start date:	as soon as possible
Entry level:	5+ years
Type:	Full time
Contract:	Permanent

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# Job ID: HRC0929486

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• 12+ years of in DFT implementation, verification and post silicon debug areas.

### Why Us

#### #WeAreIn for driving decarbonization and digitalization.

As a global leader in semiconductor solutions in power systems and IoT, Infineon enables game-changing solutions for green and efficient energy, clean and safe mobility, as well as smart and secure IoT. Together, we drive innovation and customer success, while caring for our people and empowering them to reach ambitious goals. Be a part of making life easier, safer and greener. **Are you in?** 

#### We are on a journey to create the best Infineon for everyone.

This means we embrace diversity and inclusion and welcome everyone for who they are. At Infineon, we offer a working environment characterized by trust, openness, respect and tolerance and are committed to give all applicants and employees equal opportunities. We base our recruiting decisions on the applicant 's experience and skills.

Please let your recruiter know if they need to pay special attention to something in order to enable your participation in the interview process.

Click here for more information about Diversity & Inclusion at Infineon.

