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QUALITY, ROBUSTNESS AND RELIABILITY OF 600 V GAN-ON-SI POWER DEVICES

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Significant discussion has recently centered on the revolutionary performance capabilities of GaN based power devices compared to the incumbent silicon-based alternatives. It has been frequently demonstrated that such GaN based HEMTs provide remarkably improved performance of essentially any power conversion circuit in terms of density and efficiency. The development of thick, crack-free GaN epitaxy on standard thickness Si substrates, together with device fabrication in high volume silicon CMOS factories, has opened the potential for highly cost-competitive high voltage devices as well. The simultaneous combination of advantages in efficiency, density, and cost over silicon based devices presents an apparently overwhelming compelling competitive advantage, which should drive rapid and widespread adoption throughout the power electronics industry.

However, little discussion has occurred regarding the quality, robustness and reliability of these 600 V rated GaN-on-Si based devices. Some proponents of SiC devices have suggested that such GaN devices cannot be reliable, due to the 10^9 cm^{-2} threading dislocations present, caused by the significant lattice mismatch between the epitaxial film and substrate. Others have shown catastrophic failure mechanisms thought to be caused by reverse piezoelectric phenomenon.

To date, the simultaneous achievement of long-term robustness under applied fields and stability of device on-resistance under fast switching conditions has not been presented. The relationship between device leakage behavior through breakdown to the robustness of the device in high voltage switching applications has yet to be clearly discussed. Here, these issues are addressed for one such GaN-on-Si technology platform, namely International Rectifier s GaNpowIR .

Due to continuous improvement in silicon based power semiconductor devices in over four decades, the expectation is that they are robust in the application with respect to variations in applied voltage transients, short circuit events, drive condition faults and generally hard switching conditions. These requirements translate into such device characteristics as large, preferably square, forward and reverse bias safe operating areas, significant avalanche current stability, stable threshold voltages with sufficient standoff from dv/dt induced parasitic turn-on, as well as, minimized minority carrier injection (e.g. Qrr).

Clearly, any new power device technology will be expected to provide similar levels of robustness in circuit applications as the incumbent silicon based devices. In addition, more than four decades of high volume production has allowed the quality and long-term reliability of silicon based devices to approach zero defect levels, with correspondingly small rates of field failures. While it should not be expected that any new technology will achieve the same levels without significant production volumes to drive the requisite learning, it is expected that a reasonably high level of quality be achieved prior to release of products on these new technology platforms. The requisite introductory quality level will depend on the application in which the devices are used.

For instance, it is clear that a lower introductory quality level is required to support consumer goods than automotive or aerospace applications. Commercial, light industrial and heavy industrial applications fall respectively between these former extreme market segments. Though it is common for start-ups in the compound semiconductor supply field to target the high reliability or heavy industrial application markets due to the high average selling price provided, it is clearly a futile commercial effort for an emerging technology. Of course, high average selling prices are often required to cover the significantly high cost of fabricating the novel material and technology based devices.

In the case of International Rectifier s GaNpowIR platform, significant effort has been exerted to reduce the cost of producing GaN based power HEMTs. This has been achieved through the use of efficient multi-wafer hetero-epitaxy of AlGaN alloys on standard silicon substrates with high yield of crack free, low distortion, thick (2-5 m) epitaxial wafers. In addition, device fabrication has been developed in high volume silicon CMOS factories, without the use of gold-based metallurgy or e-beam or lift off based lithography. In this way, the resulting GaNpowIR devices can be made to provide a compelling performance to cost value proposition, even in highly cost-sensitive consumer applications. This allows for the necessary learning and natural progression of the technology to other market segments as the technology matures.

Though several decades of cooperation within the silicon device reliability community has led to the establishment of industry-wide standards for testing, no such effort has even been initiated for GaN based devices. It can be taken as a first approximation that

package dominant testing procedures such as temperature-humidity bias (THB), temperature cycling, thermal shock, intermittent operating lifetime (ITOL) or autoclave based hydroxyl pre-loading are generally applicable for GaN based devices using similar packaging, particularly plastic mold based packages. However, the semiconductor centric stress tests of high temperature reverse bias (HTRB) or high temperature gate bias (HTGB) were specifically designed to correlate accelerated testing (e.g., 150 C at 80% of rated maximum bias for 1000 hours) to the useful lifetime of the part under application conditions (e.g. 85 C for 10 years) assuming an activation energy of the dominant failure mode of about 0.8 eV [1]. While this was determined valid for silicon-based devices and has proven very useful for this technology over many years, it has not been demonstrated valid for GaN-based power HEMTs. It will require significant additional effort to develop equivalently useful testing conditions for this new technology platform.

Recently, there have been several reliability failure mechanisms suggested for GaN based HEMTs. One is the dissociation of the AlGaN barrier layer due to high applied electric field stress, referred to as reverse piezo-electric phenomenon [2]. This mechanism is catastrophic to device behavior leading to physical destruction of the device in short times on the order of seconds to hours.

Pitting along the periphery of the gate structure is followed by loss of continuity in the two-dimensional electron gas conduction layer between source to drain, rendering the device useless. This phenomenon has been shown to exist for metal-gated device structures. We have previously reported that no physical or electrical evidence for this failure mechanism has been found in IR s GaNpowIR low and mid voltage devices, which use an insulated gate structure [3]. This author has suggested that this may be explained using a different model for the observed degradation of the metal-gated devices, namely electromigration. Since the proponents of the reverse piezo-electric model have found a critical voltage required to produce the effect of some 20-40 V, electrons would gather enough energy across such an applied voltage to knock constitute atoms of the AlGaN layer out of their lattice sites. Together with the very high current density found for such metal-gate structures, on the order of 1 mA/mm gate width, localized with nanometers of the gate edge, this electron-atom collision induced displacement mechanism could explain the observed lattice damage.

Regardless of the actual mechanism involved, it is clear that this failure mechanism is not of first order concern in insulated gate GaN based HEMTs as constructed by IR. This is further shown by the **Fig. 1** data demonstrating very stable gate leakage current per gate width of less than 1 pA/mm, measured at -20 Vg and stressed under -50 V gate bias for 1500 hours at room temperature, for several representative discrete depletion mode 600 V rated large area (Wg > 100mm) power devices.

Another proposed reliability failure mechanism, namely that of threading dislocation induced breakdown or leakage across the hetero-epitaxial III-V layers, is not supported by experimental evidence. **Fig. 2** shows the total drain leakage current per gate width (Wg> 100 mm) for representative devices measured at +480 V with -20 V on the gate during long term stress of the same bias conditions at room temperature over a period of greater than 2500 hrs. As can be seen from the stable low leakage of < 100 nA/mm gate width, there is no evidence to date of the role of threading dislocation induced epitaxial layer breakdown. In fact, the t=0 device breakdown voltage of all such devices studied occurs at average applied field across the epitaxial structure of > 2 MV/cm and does not breakdown across the epitaxial layers, rather occurs at the surface of the device. This data does not support the assertion made by proponents of SiC based device technology that threading dislocations in GaN based HEMTs limit the breakdown field strength to less than 1 MV/cm or the device leakage behavior to > 10 A/mm in these 600 V rated devices.

A recently discussed failure mechanism for GaN based HEMTs, studied using metal gate device structures, is time-dependent dielectric breakdown behavior (TTDB) [4]. In this phenomena, initially stable device structures exhibit increasing levels of leakage, especially in the form of noisy leakage current spikes, until finally a catastrophic failure of the device is observed. **Fig. 3** shows four terminal leakage current measured for a representative 600 V rated device stressed at 650 V drain bias and -20 V gate bias over a period of 72 hours at room temperature. The device shows no evidence of failure in this extended time period for the current spikes previously reported for studies of metal gate device structures, even under such extreme applied bias conditions. The use of insulated gates and optimized device structures is suggested to have significantly improved the performance of this technology in regards to such TTDB phenomena.

From a practical standpoint, the behavior of the cascoded device structure, using a 600 V rated GaN based power device and a low voltage enhancement mode silicon device, under characteristic stress conditions is of interest. **Fig. 4** shows the drain leakage current per gate length, Wg, of such a switch configuration for a population of representative devices under a drain bias of +480 V and 0 V gate bias for 1000 hrs. The cascode switch leakage is very stable at less than 100 nA/mm Wg. **Fig. 5** shows the cascode switch on resistance, measured at a drain current of 10 A, over the same 1000 hr period, also demonstrating excellent stability under applied off-state stress of 480 V.

Low ON-Resistance

It should be noted that these same device structures have been shown to have negligible dynamic on-resistance (<5 %), measured within 1 µs of the off-on transition, even for off-state voltages of 500 V [5]. Therefore, this represents the first demonstrated case of the achievement of simultaneous long-term device stability under high voltage bias and negligible dynamic on-resistance for 600 V rated GaN based HEMTs. Other device parametric characteristics of the cascade switch of threshold voltage and control gate leakage are determined by the properties of the low voltage silicon device.

Note that these 600 V rated GaN based power devices demonstrate at least the same stability under stress at temperatures of 150 C under identical bias conditions as found for room temperature stress.

There remains considerable effort to demonstrate intrinsic and functional long term reliability for GaN based power devices at the quality levels enjoyed by the considerably more mature silicon based counterparts. However, it can be shown that the failure

mechanisms of reverse piezoelectric degradation of the metal-gate structure, the hypothesized threading dislocation limitation to breakdown voltage and device leakage behavior, as well as the time- dependent dielectric breakdown phenomenon found in metal-gate GaN based HEMT structures, were not evident during the first 1000 hours of operation of the 600 V rated GaN devices based on IR s GaNpowIR technology.

References:

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