# C65LP & C65LPX

## 65 nm Low Power CMOS Technology Platform

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Never stop thinking

C65

# Infineon's Technology Engine for today and the coming years for Mobile Communication, Broadband Access Applications, and ASIC Design Solutions

# Infineon Stands for Customer Orientation
# Target Markets & Applications / Core Competencies

Automotive, Industrial & Multimarket

**Car Electronics:** power train, safety management, body & convenience, infotainment,
**Power control:** distributed power generation, automation / motor control, transportation, power supplies, medical, building control,
**Chipcard & Security:** communications, payment, identification, entertainment

Communication Solutions

**Wireless communications:** mobile phones, cellular base stations, cordless telephones, RF technology for short, medium and long-range distances, TV receivers, navigation,
**Wireline communications:** Voice and broadband data communications, integrated voice and data communications, wireless infrastructure, home networks

Customers

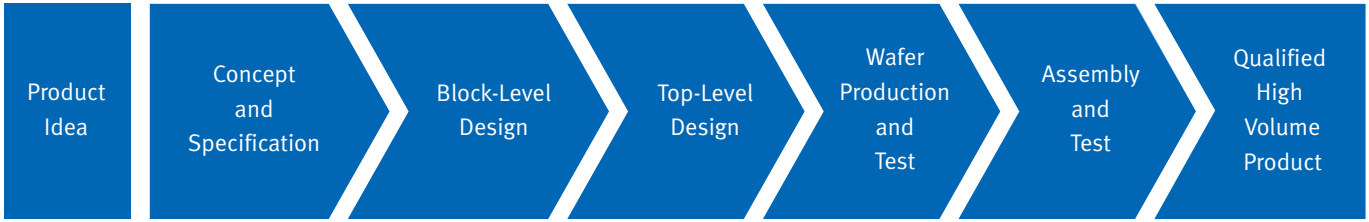
Analog/Mixed Signal

RF

Power

Embedded Control

# Complete Offering over the Value Chain




**Support & Services from / organized by Infineon Technologies**

- Process design kit (PDK)
- Concept reviews
- Design and layout reviews
- Advanced Algorithms & Architectures
- Design Methodology/Flow
- Concept and specification
- Design and layout services
- IP blocks
- Test development
- Libraries
- Manufacturing services
- Logistics
- Quality
- Assembly and test
- Physical Failure Analysis
- Reliability

# Design System, Tools, Methods, Environment

## Fully integrated design system

- "Exportable" + flexible design infrastructure
- Leading RF design and highly optimized low power methodology
- Fast cycle time from RTL to chip
- Re-usable IP macros leveraging IFX' ASSP roadmaps
- Netlist and RTL sign-off procedures with tight parameter bands and small margins for most efficient designs
- DFM – Design for Manufacturability
- Open for integration of 3rd party IP, blocks & macros

## Intimate technology know-how for full exploitation of multi-sourcing with Silicon Foundry manufacturing partners for first time right designs

- Methodology to assess cost, performance, leakage/power of target manufacturing platform and site
  - Simulation environment for frontend (device) and backend technology
  - Testchip architectures for accurate model-hardware correlation
- Area-optimized standard cell and IO libraries
- Performance-optimized standard cell and IO libraries
- Highly configurable memories, optimized for lowest standby power, small area and high yield
- Digital and analog circuit and system know-how for custom solutions
- Big variety of silicon-proven Infineon-own or 3rd party IP blocks as MCUs, DSP, ADC, DAC, PLL, RF, VCO, DCO, HS-Phys, memories etc.

# C65LP & C65LPX Technology Platform at a glance ...

- 65 nm CMOS Technology for Logic, SRAM, Analog/Mixed-Signal, RF and high-voltage Applications
- Specialized High Density Technologies for Low-Power/Low-Leakage/RF (C65LP) and Performance-optimized Low-Power/Low-Leakage/RF based on rotated substrate technology (C65LPX)

| Device Families | Core Supply | I/O | Analog | RF |
|---|---|---|---|---|
| **C65LP**<br>Low Power & RF | 1.2 V<br>(0.9 ... 1.32 V) | 1.8 V, 2.5 V, 3.3 V, 5.0 V | 1.3 V, 2.5 V, 3.6 V | 1.3 V, 2.5 V |
| **C65LPX**<br>Low Power & RF | 1.2 V<br>(0.9 ... 1.32 V) | 1.8 V, 2.5 V, 3.3 V, 5.0 V | 1.3 V, 2.5 V, 3.6 V | 1.3 V, 2.5 V |

- Temperature range: -40 ... +125°C for 10 years operational lifetime
- Average gate density: 2 libraries useable in parallel with
  700 k/mm² (performance-optimized)
  900 k/mm² (density-optimized)

# C65LP & C65LPX Manufacturing Strategy

- We maintain manufacturing flexibility and secure supply by a multi-sourcing Si-foundry capability characterized by the
  - Ability to deliver with compatible designs from several fabs
  - Business continuity to sustainable satisfy volume demand
  - Negotiation & bargaining power made available by various sources
- 65 nm is the 1st IFX CMOS logic technology generation managing the transition phase from an IDM towards ‘Fabless’ by multi-sourcing

# C65LP & C65LPX Platform Feature Set

| | | | | | | |
|---|---|---|---|---|---|---|
| **FBEOL** | **Wirebond Packaging**<br>50 µm pad pitch | **Flip Chip Packaging**<br>150 µm bump pitch | **Wafer-Level BGA Packaging**<br>400 µm ball pitch | **Vertical Probing**<br>Array 80/140 µm<br>Inline 80µm | **Cantilever Probing**<br>Inline 50 µm | **MEMS-Style Probing**<br>Array 120 µm<br>Inline 50 µm |

| | | | |
|---|---|---|---|
| **BEOL** | **BEOL Caps** | **Al Metal Level** (for pads & routing) | **12x Pitch Cu Metal Level**<br>(for inductors & power routing) |
| | | **4x Pitch Cu Metal Levels** (in FSG dielectric) | |
| | **MIM Caps** | **2x Pitch Cu Metal Levels** (in low k dielectric) | |
| | | **1x Pitch Cu Metal Levels** (in low k dielectric) | |

| | | | | | |
|---|---|---|---|---|---|
| **Design System** | **Leading Edge Modeling & Technology Package**<br>Physical non-binned models, full A/MS/RF characterization, MC, full- & semi-custom design | **High Density Libraries**<br>900 kGates/mm² | **High Density SP-SRAM** | **Sync. High Speed Via-ROM** | **State-of-the-art I/O Libraries**<br>CMOS, USB, MIPI, … |
| | | **High Performance Libraries**<br>700 kGates/mm² | **High Performance SP-SRAM** | **High Performance DP-SRAM** | **State-of-the-art Design Flow**<br>InWay 5.2 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **FEOL** | **CORE**<br>**1.2 V**<br>Low $V_t$ | **CORE**<br>**1.2 V**<br>Regular $V_t$ | **CORE**<br>**1.2 V**<br>High $V_t$ | **PASSIVES**<br>Poly & diffusion resistors, salicided-blocked transistors and resistors, paras. bipolar, diodes, varactors, thin & thick oxide capacitors, … | **Poly eFuse** | **I/O**<br>**1.8/2.5/3.3 V** | **HV-I/O**<br>**5 V** |

# C65LP & C65LPX Design System

## Standard Cells – Features and Benefits

- Targeted for IFX low $V_t$ (LVT), regular $V_t$ (RVT) and high $V_t$ (HVT) process
- Available for typ. $V_{DD}$ voltage range from 1.0 V ... 1.32 V, slow mode at 0.9 V
- Optimized for performance and leakage current
- MULTI $V_t$ to reduce leakage (HVT and RVT are mixable, RVT and LVT are mixable)
- Accurate front end UDSM modeling for 100% first silicon success
- Hand-crafted, optimized for performance and place & route fully exploiting the process
- Optimized for synthesis
- Big variety of special cells, e.g. level-shifters, logic-switches, gated clock, scan version for every FF, ...

## Memories & Compilers – Features and Benefits

- Low leakage Single Port SRAMs, Dual Port SRAMs, via programmable ROMs and memory switches, typ. $V_{DD}$ voltage range from 1.0 V ... 1.32 V
- Memory architectures for $V_{DDmin}$ = 0.9 V
- Full integration into InWay design flow and comfortable WEB interface
- Highly configurable and flexible aspect ratios
- Edge-sensitive synchronous interfaces
- Area and yield optimized, over routable in metal 5
- Power efficient with leakage-only static power (sleep & power-off modes)
- Special features (e.g. bit write enable, antenna diodes, BIST)
- Electrical fusing and scalable word redundancy (High Density Fault Repair SP-SRAM)
- Dense SP-SRAM cell for $V_{DD}$ = 1.2 V ± 10%
- Micro (XS) SRAM architectures for optimized area and performance

## I/O-Interfaces – Features and Benefits

- Based on the widely automated view generation, dimensioning and verification method
- Offers a big set of standard I/O cell libraries, e.g. CMOS 1.8 V / 2.5 V / 3.3 V, $I^2C$ (1.8 V / 2.9 V), LVDS, ...
- Extended range of standard I/O macros, e.g. MIPI-, MVI interfaces, FS-/HS-USB, high voltage interfaces, ...
- Special cells for WLB and Flipchip
- Further options upon request

# C65LP & C65LPX Design Kit

| | | |
|---|---|---|
| **General** | Design Package Release | v1.6.5 (C65LP) & v1.7 (C65LPX) |
| | Cadence Release | 5.1 |
| | Platform | Solaris, Linux |
| | Methodology | Full Custom (Analog Mixed Signal Flow) and Semi Custom design style |

| | | |
|---|---|---|
| **Libraries** | IFX Standard Device Libraries | IFXdevsymbol, IFXdevlayout |
| | Technology Dependent Device Library | Special CMOS Library<br>(varactors, inductors, DeMOS, MOScap, VPPcap) |
| | Technology Dependent Cell Library | Area-optimized standard cell libraries (9-track)<br>Performance-optimized standard cell libraries (12-track)<br>SP-SRAM / XS-SP-SRAM, DP-SRAM / XS-DP-SRAM, ROM<br>Efuse macro and redundancy wrapper |

| | | |
|---|---|---|
| **Modeling** | General | BSIM 4.3 / BSIM 4.5 |
| | Active Models | Scaleable models for RF-optimized geometries<br>Subcircuit models with substrate parasitic and RF noise |
| | Passive Models | Inductors, scaleable varactor models, VPPcap |
| | Statistical Simulation | Monte-Carlo modeling supported |

| | | |
|---|---|---|
| **Supported Tools** | Schematic Entry | Composer |
| | Analog & RF Simulation | Spectre (RF), Titan and NanoSim |
| | Monte Carlo Simulation | Spectre Direct and Titan |
| | Mixed Signal Simulation | ADMS |
| | Layout Creation | Virtuoso-XL |
| | Floorplanning | BlastPlan |
| | Synthesis | BlastCreate |
| | Digital Simulation | ModelSim |
| | Place & Route | VCAR, BlastFusion, Talus |
| | Layout Verification | Calibre |
| | RCX Parasitic Extaction | Assura, StarRC, QRC |

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Published by Infineon Technologies AG

Ordering No. B192-H9085-X-X-7600
NB08-1030