EiceDRIVER™ gate driver 1EDI3026AS

Single channel isolated IGBT driver

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AEC Qualified | RoHS | ISO 26262 compliant

Features

- Galvanic isolated IGBT driver using coreless transformer technology
- Single channel driver for IGBTs up to 1200 V
- Low propagation delay 60 ns typically
- Split outputs TON and TOFF for independent turn-on and turn-off slew rates
- Integrated booster with up to 20 A peak current rail-to-rail output
- Integrated active Miller clamp supports unipolar switching
- Configurable external soft turn-off functionality
- 12- bit ADC for temperature measurement or DC link measurement
- CMTI up to 150 V/ns up to ±1200 V
- Reinforced insulation 8 kV peak according to DIN EN IEC 60747-17 (VDE 0884-17):2021-10
- 5.7 kV rms insulation according to UL 1577
- Combined secondary side active short circuit (ASC) and ADC input pin
- Integrated safety features up to ASIL B:
  - Safety pins on primary side and secondary ASC
  - Overcurrent protection (OCP) including BIST
  - Gate monitoring and output stage monitoring
  - Shoot-through protection with integrated timeout
  - Primary supply monitoring UVLO
  - Secondary supply monitoring VCC2, VEE2 for OVLO and UVLO
- DATA interface for detailed error diagnosis and ADC readout via PWM signal
- 3.3 V and 5 V compatible I/O logic supply
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL B
- Green Product (RoHS compliant)

Potential applications

- Traction inverters for HEV and EV
- Auxiliary inverters for HEV and EV

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The EiceDRIVER™ gate driver 1EDI3026AS is a high voltage galvanic isolated IGBT driver designed for high voltage automotive applications. The device is based on Infineon's coreless transformer (CT) technology providing 8 kV galvanic insulation between low voltage and high voltage domains.

The IC supports up to 1200 V IGBTs. The device features a powerful output stage of up to 20 A peak current required for high power switches. A split output stage (TON, TOFF) allows different slew rates for switching on and switching off due to separate gate resistors.

The low voltage domain (primary side) supports logic levels of 5 V as well as 3.3 V. At the high voltage domain (secondary side) it can drive the gate of IGBTs directly. A short propagation delay of only 60 ns and a minimum pulse width of 150 ns offer high a switching frequency with minimum distortion of the PWM signal.

The OCP protection together with the configurable external soft turn-off feature prevents IGBT destruction in short-circuit events.

The integrated active Miller clamping stage up to 10 A allows unipolar supply of the IGBT.

The device features a 12-bit ADC for temperature measurements or DC link measurements. Furthermore, the DATA interface provides detailed error diagnosis through a PWM signal.

The overcurrent protection (OCP) ensures that the device switches off the power switch safely, if the current exceeds the threshold configured via R_{SENSE}.

A large panel of integrated safety related features simplifies the design of ASIL D compliant systems. Safety inputs (SI1, SI2) at the primary side control the transition of the system to safe state. Additionally, the device offers a secondary side active short circuit (ASC) pin to trigger safe state also from the secondary side.

Type	Package	Marking
1EDI3026AS	PG-DSO-20	1EDI3026AS

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1 Block diagram

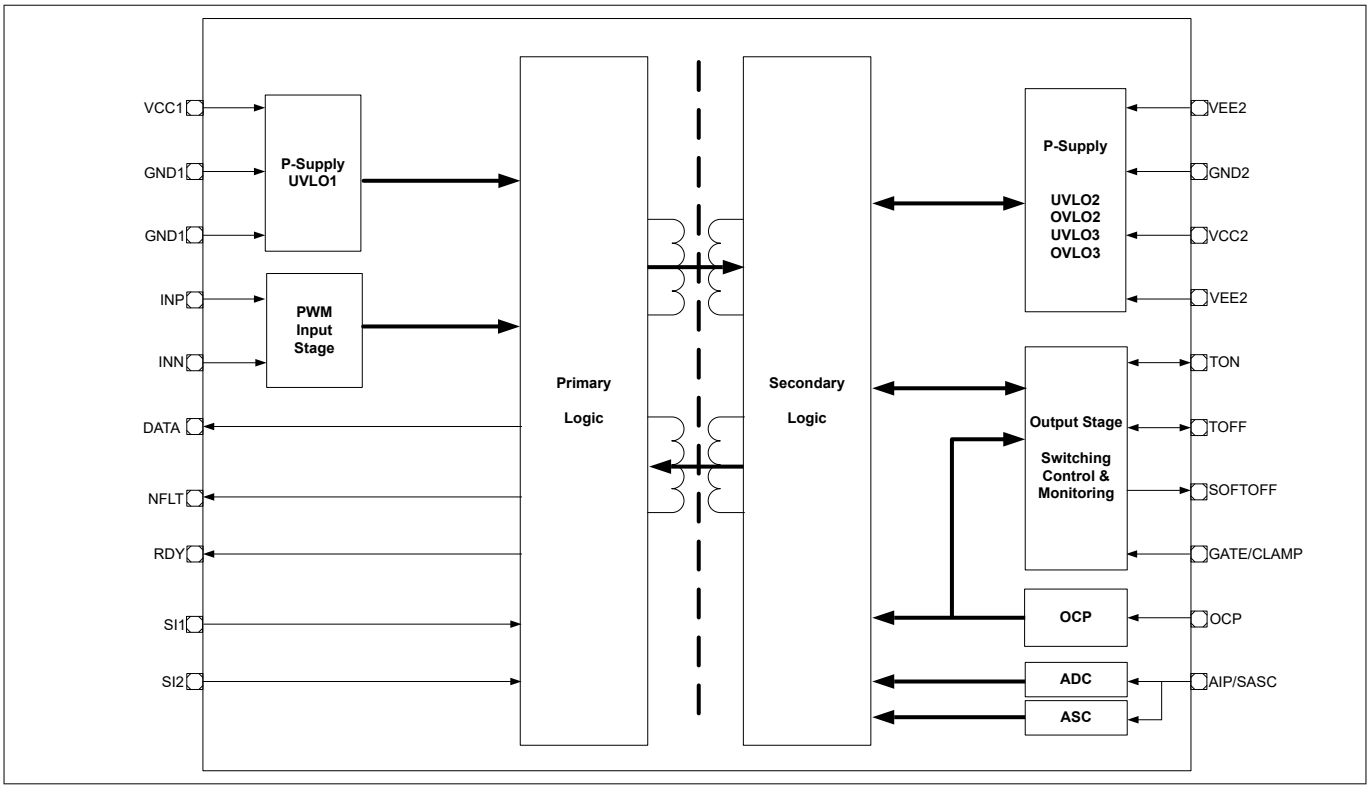

Figure 1 Block diagram

2 Pin configuration

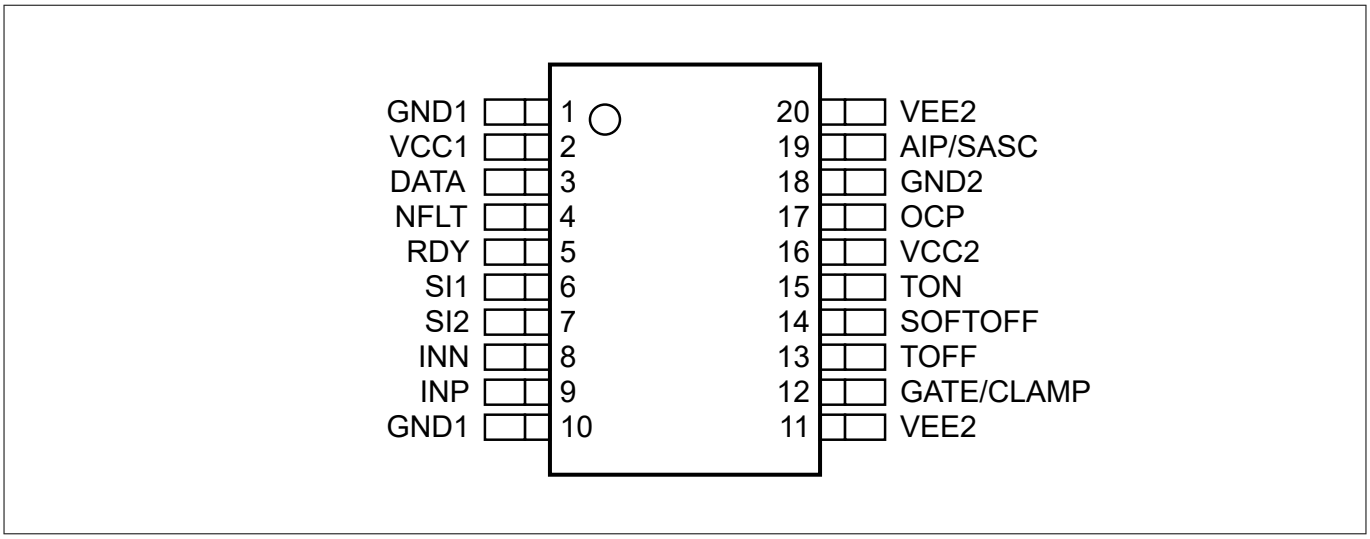

Figure 2 Pin assignment

2.1 Pin definitions and functions

Table 1 Pin definitions and functions

Pin #	Pin name	I/O configuration	Voltage class	Function
1	GND1	Ground	Primary ground	Ground connection of the primary side.
2	VCC1	Supply	Primary supply	5 V/3.3 V power supply for the primary side referred to GND1.
3	DATA	Push-pull Output	VCC1	Shows ADC or diagnosis data. Provides a PWM signal according to the data on ADC or diagnosis.
4	NFLT	Open Drain Output	VCC1	Reports failure events triggered by overcurrent protection. As a result the pin is driven to low. Has to be connected to VCC1 with an external pull-up resistance.
5	RDY	Open Drain Output	VCC1	Reports voltage failure events on UVLO1, UVLO2, OVLO2, UVLO3, OVLO3, Life Sign Lost, Output Stage Error and Gate Monitoring Error. As a result this pin is driven to low. Has to be connected to VCC1 with an external pull-up resistance.
6	SI1	Input internal Pull down	VCC1	Safety input to control the output stage via the primary side to achieve a system safe state. Shall be connected to the corresponding SI2 input of the opposing gate driver inside a halfbridge topology.
7	SI2	Input internal Pull down	VCC1	Safety input to control the output stage via the primary side to achieve a system safe state. Connect to the corresponding SI1 input of the opposing gate driver inside a halfbridge topology.

(table continues...)

Table 1 (continued) Pin definitions and functions

Pin #	Pin name	I/O configuration	Voltage class	Function
8	INN	Input Internal Pull up	VCC1	The inverting PWM signal is used for monitoring the shoot through protection inside a halfbridge topology. Connect to INP of the opposing gate driver inside a halfbridge topology. If not used connect to GND1.
9	INP	Input Internal Pull down	VCC1	The non-inverting PWM signal of the driver to drive the secondary side output stage voltage.
10	GND1	Ground	Primary ground	Ground connection of the primary side.
11	VEE2	Supply	Secondary supply	Negative power supply for the secondary side referred to GND2. Connect to GND2 for unipolar operation.
12	GATE/ CLAMP	Input	VCC2	Monitors the gate of the power switch and clamps the gate to VEE2 if the threshold V_{CLAMP} is reached.
13	TOFF	Input/Output	VEE2	Switches the power switch gate to VEE2 according to the PWM low input on INP.
14	SOFTOFF	Output	VEE2	The SOFTOFF is activated in case a OCP or gate monitoring error is present. Clamps the voltage to VEE2.
15	TON	Input/Output	VCC2	Switches the power switch gate to VCC2 according to the PWM high input on INP.
16	VCC2	Secondary supply	VCC2	Positive power supply for the secondary side referred to GND2.
17	OCP	Input Internal Pull up through current source	VCC2	Monitors current through a sense emitter via shunt resistor.
18	GND2	Ground	Secondary ground	Ground connection for the secondary side.
19	AIP/ SASC	Input	VCC2	ADC input to monitor temperatures at the power switch. An internal current source supplies the external components. The active short circuit function controls the output voltage of TON to VCC2.
20	VEE2	Supply	Secondary supply	Negative power supply for the secondary side referred to GND2. Connect to GND2 for unipolar operation.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Positive power supply (primary)	V_{VCC1_MAX}	-0.3	–	7	V	Referenced to GND1	PRQ-42
Positive power supply (secondary)	V_{VCC2_MAX}	-0.3	–	30	V	Referenced to GND2	PRQ-43
Negative power supply (secondary)	V_{VEE2_MAX}	-13	–	0.3	V	Referenced to GND2	PRQ-44
Power supply voltage difference (secondary) VCC2-VEE2	$V_{VCC2-VEE2\_MAX}$	–	–	40	V		PRQ-45
Voltages on any I/O pin on primary side (INP, INN, SI1, SI2, DATA, NFLT, RDY)	V_{INx_MAX}	-0.3	–	V_{VCC1} + 0.3	V	Referenced to GND1	PRQ-46
AIP/SASC voltage	$V_{AIP/SASC\_MAX}$	-0.3	–	V_{VCC2} +0.3	V	Referenced to GND2	PRQ-47
OCP	V_{OCPP_MAX}	-0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-50
Maximum GATE/CLAMP voltage	$V_{GATE/CLAMP\_MAX}$	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-52
SOFTOFF voltage	$V_{SOFTOFF\_MAX}$	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-603
TON voltage	V_{OUT_MAX}	V_{VEE2} - 0.3	–	V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-53

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TOFF voltage	V_{OFF_MAX}	V_{VEE2} - 0.3		V_{VCC2} + 0.3	V	Referenced to GND2	PRQ-602
TON high maximum current	I_{OUTH_MAX}	-20	–	–	A	t_{MAX} = 500 ns, non-repetitive	PRQ-54
TOFF low maximum current	I_{OUTL_MAX}	–	–	20	A	t_{MAX} = 500 ns, non-repetitive	PRQ-702
GATE/CLAMP low maximum current	$I_{Gate/Clamp\_Max}$	–	–	10	A	t_{MAX} =500 ns, non-repetitive	PRQ-56
Short circuit clamping maximum current on GATE/CLAMP, SOFTOFF, TON, TOFF	I_{SC_MAX}	–	–	2	A	t_{MAX} =3 µs, 20 repetitions, 100ms between repetitions	PRQ-727
Current on output logic pins (DATA, RDY, NFLT)	$\lvert I_{OUTx\_MAX}\rvert$	–	–	10	mA		PRQ-57
HBM robustness, all pins	V_{ESD_HBM1}		–	2	kV	Human Body Model "HBM" robustness according to AEC-Q100-002	PRQ-669
CDM robustness, all pins	V_{ESD_CDM1}		–	500	TC	Charged Device Model "CDM" robustness according to AEC-Q100-011 Rev D. "TC" corresponds to "Test Condition" according to AEC-Q100-011.	PRQ-58
CDM robustness, corner pins (GND1, VEE2)	V_{ESD_CDM2}		–	750	TC	Charged Device Model "CDM" robustness according to AEC-Q100-011 Rev D. "TC" corresponds to "Test Condition" according to AEC-Q100-011.	PRQ-668
Storage temperature	T_{s_MAX}	-55	–	150	°C		PRQ-59

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified). Absolute maximum ratings are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Absolute maximum ratings are not subject to production test, specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction temperature	T_{J_MAX}	-40	–	150	°C		PRQ-60
SOFTOFF low maximum sink current	$I_{SOFTOFF\_low\_Max}$	–	–	3	A	t_{MAX} = 100 ns, non-repetitive	PRQ-730

3.2 Functional range

Table 3 Functional range

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Primary power supply	V_{VCC1}	3	–	5.5	V	Referenced to GND1[1)]	PRQ-61
VCC1 ramp-up rate	t_{RP1}	–	–	200	V/ms		PRQ-62
Secondary positive power supply	V_{VCC2}	13.5	15	17	V	Referenced to GND2[2)]	PRQ-593
VCC2 ramp-up slew rate	t_{RP2}	–	–	100	V/ms		PRQ-65
Negative power supply	V_{VEE2}	-9	-5	0	V	Referenced to GND2[3)]	PRQ-66
VEE2 ramp up slew rate	t_{RP3}	-100	–	–	V/ms		PRQ-67
Secondary Power supply voltage difference VCC2-VEE2	$V_{VCC2-VEE2}$	–	–	25	V		PRQ-574
Junction temperature	T_J	-40	–	150	°C		PRQ-69

(table continues...)

Table 3 (continued) Functional range

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Common mode transient immunity	dV_{ISO}/dt	-150	–	150	kV/µs	For voltages up to +/-1200 V	PRQ-70
Voltages on any I/O pin on primary side (INP, INN, SI1, SI2, DATA, RDY, NFLT)	V_{INx}	0	–	V_{VCC1}	V	Referenced to GND1	PRQ-71

1) For V_{VCC1} crossing V_{UVLO1L_1} the UVLO1 reaction is performed.
2) For V_{VCC2} crossing V_{OVLO2H_x} or V_{UVLO2L_x} the OVLO2 or UVLO2 reaction is performed respectively.
3) For V_{VEE2} crossing V_{OVLO3H_x} or V_{UVLO3L_x} the OVLO3 or UVLO3 reaction is performed respectively.

***Note**: Within the functional range the IC operates as described in the circuit descriptions. Continuous switching operation of the output stage is possible. Electrical characteristics stated within the following sections are specified within the conditions given in the electrical characteristics table. The reaction to undervoltage and overvoltage protection is only performed when exiting the functional range.*

3.3 Thermal characteristics

Table 4 Thermal characteristics

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal Resistance Junction to Ambient (25°C)	$R_{TH-JA,25°C}$	–	88	–	K/W	T_{amb} = 25 °C	PRQ-78
Thermal Resistance Junction to Ambient (125°C)	$R_{TH-JA,125°C}$	–	73	–	K/W	T_{amb} = 125 °C	PRQ-79

(table continues...)

Table 4 (continued) Thermal characteristics

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal Resistance Junction to Case Top	$R_{TH-JC-TOP}$	–	50	–	K/W	25 °C ≤ T_{amb} ≤ 125 °C	PRQ-81
Ψ - Pseudo Thermal Resistance Junction to Case Top	Ψ_{JC-TOP}	–	21	–	K/W	25 °C ≤ T_{amb} ≤ 125 °C	PRQ-83
Transient Thermal Impedance Junction to Ambient	Z_{TH-JA}	–	50	–	K/W	25 °C ≤ T_{amb} ≤ 125 °C, Pulse width t_p ≤ 4 s	PRQ-738

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. R_{TH-JA} and Ψ_{JC-TOP} are simulated on a 2s4p board (35mm x 50mm x 1.5mm) with 35µm copper thickness and 40% metallization on the inner power planes. The copper is split between the primary and secondary side. The device footprint is a direct fan-out on top layer. Only the corner pins are connected with a single via to an internal copper layer.*

3.4 Insulation characteristics

Table 5 Insulation characteristics for reinforced insulation in compliance with DIN EN IEC 60747-17 (VDE 0884-17):2021-10

Description	Symbol	Characteristic	Unit
Installation classification per IEC 60664-1, Table F.1			–
for rated mains voltage ≤ 150 V_{RMS}		I-IV	
for rated mains voltage ≤ 300 V_{RMS}		I-IV	
for rated mains voltage ≤ 600 V_{RMS}		I-III	
for rated mains voltage ≤ 1000 V_{RMS}		I-II	
Climatic classification	–	40/125/21	–
Pollution degree (IEC 60664-1)	–	2	–
Minimum external clearance	CLR	> 8	mm
Minimum external creepage	CPG	> 8	mm
Minimum comparative tracking index	CTI	> 400	–
Maximum rated repetitive peak isolation voltage	V_{IORM}	1767	V_{peak}

(table continues...)

Table 5 (continued) Insulation characteristics for reinforced insulation in compliance with DIN EN IEC 60747-17 (VDE 0884-17):2021-10

Description	Symbol	Characteristic	Unit
Maximum rated transient isolation voltage	V_{IOTM}	8000	V_{peak}
Maximum impulse voltage, tested in air	V_{IMP}	8000	V_{peak}
Maximum surge isolation voltage for reinforced insulation, tested in oil Test voltage in subgroup #1 = 11 kV ≥ 1.3 x V_{IMP}, min. 10 kV	V_{IOSM}	11000	V_{peak}
Input to output test voltage, method b1) $V_{ini,b}$ = 1.2 x V_{IOTM}, $V_{pd(m)} \geq V_{IORM}$ x 1.875, 100% production test, $t_{ini,b}$ = t_m= 1 s	q_{PD}	< 5	pC
Input to output test voltage, method a) $V_{ini,a}$ = V_{IOTM}, $V_{pd(m)} \geq V_{IORM}$ x 1.6 , sample test, t_{ini} = 60 s, t_m = 60 s	q_{PD}	< 5	pC
Isolation resistance at 25 °C ≤ T_{amb} ≤ 125 °C, V_{io} = 500 V	R_{IO}	> 10^{12}	Ω
Isolation resistance at T_S = 150°C, V_{io} = 500 V	R_{IO}	> 10^9	Ω

Table 6 Insulation characteristics recognized according to UL 1577

Parameter	Symbol	Characteristic	Unit
Insulation withstand voltage / 1 min	V_{ISO}	5700	V (rms)
Insulation test voltage / 1 s	V_{ISO}	6000	V (rms)

4 Operating modes and error reactions

4.1 Operating modes diagram

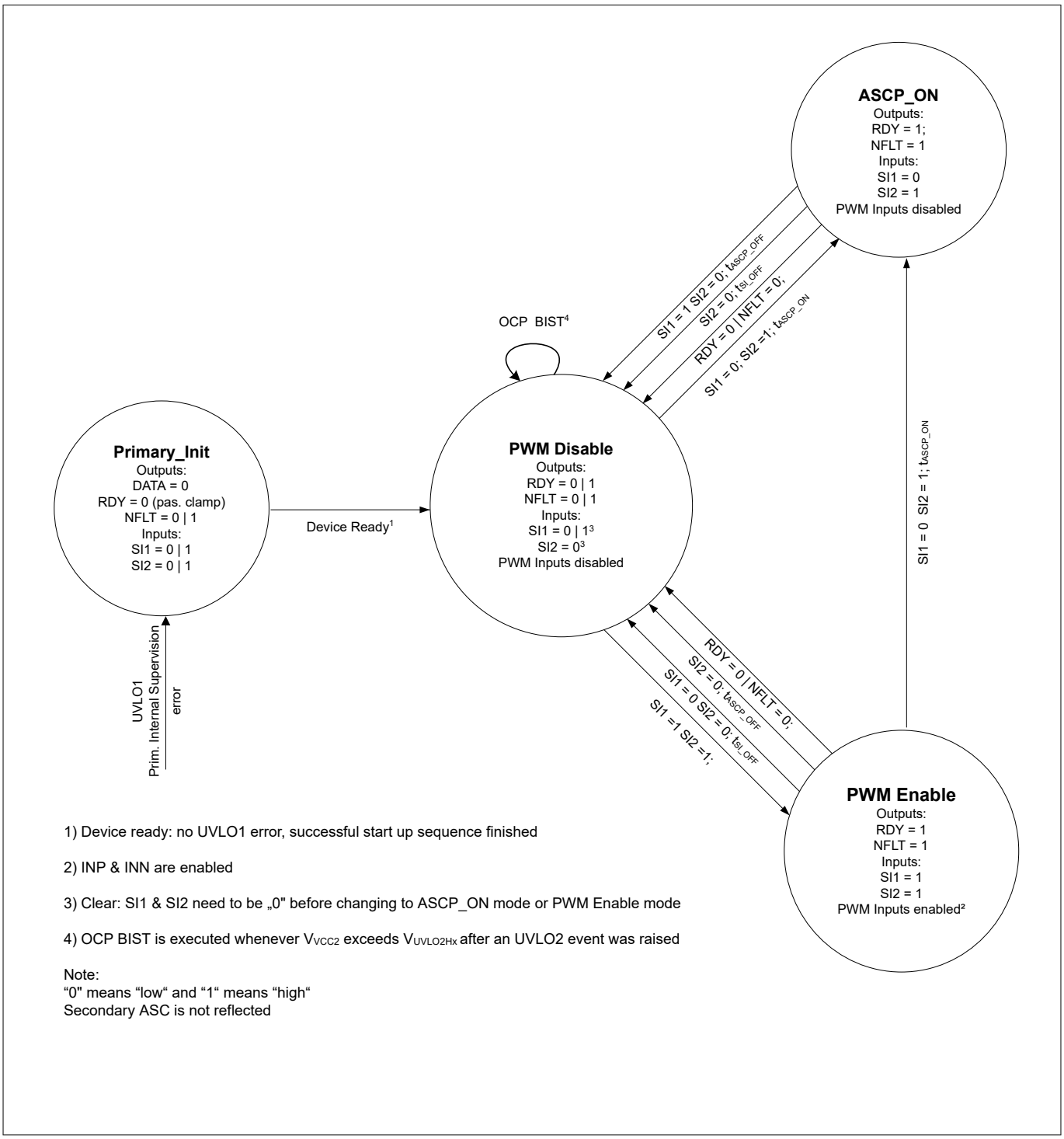

Figure 3 Operating modes diagram

***Note**:*
- *Life sign lost will be detected only if communication has been established once.*
- *External pull-up required on RDY and NFLT (open drain output).*

4.2 Operating modes description

The device has the following modes which it can operate in:

- Primary_Init mode
- PWM Disable mode
- PWM Enable mode
- ASCP_ON mode

Primary_Init mode and start up

The device is in Primary_Init mode at start-up if an primary internal supervision or an UVLO1 error occurs. In both cases it will not operate as the primary die is not ready. DATA is pulled to "low".

PWM Disable mode

- In PWM Disable mode with NFLT = "high" and RDY = "high" no error occurred.
- In PWM Disable mode with NFLT or RDY = "low" an error occurred.

Mode transition to PWM Enable mode

Once in PWM Disable mode the change to PWM Enable mode is done with setting SI1 and SI2 signal to "high". Changing the state of SI2 back to "low" the device is returning into PWM Disable mode.

PWM Enable mode

In PWM Enable mode the output gate voltage is following the signal transitions on INP in case there is no STP keep error between INP & INN input signals.

ASCP_ON mode

Setting SI1 = "low" and SI2= "high" transitions the device state to ASCP_ON mode after a defined delay. During this mode the switching state transition via INP signal is disabled. The output stage is in a stable "high" condition. Changing the state of SI2 to "low" shifts the device back to PWM Disable mode with a defined delay. If an error related to NFLT or RDY occurs, the device is shifted to PWM Disable Mode. A state transition from ASCP_ON mode to PWM Enable mode is prohibited.

Error transitions

The transition from PWM Enable mode or ASCP_ON mode to PWM Disable mode is done according error events which are based on a NFLT error or a RDY error.

4.3 Error classification

The following errors are classified as NFLT error:

- OCP event

In this case NFLT is pulled to "low".

The following errors are classified as RDY error:

- Primary supervision error
- UVLO1 event
- UVLO2 event
- OVLO2 event
- UVLO3 event
- OVLO3 event in case OVLO3 threshold is latched
- Sec. Internal Supervision error
- Output stage monitoring error

- Gate monitoring error
- STP keep error
- Life sign error

In all cases RDY transitions to "low".

4.4 Single failure events in PWM Enable mode and ASCP_ON mode

Table 7 Single failure events in PWM Enable Mode

Failure Event	Device in PWM Enable mode Output stage reaction when TON is "high"	Resulting pin status changes	Device in ASCP_ON mode Output stage reaction when TON is "high"	Resulting pin status changes
OCP error when TON = "high"	Tristate and turn off via SOFTOFF	NFLT = 1 → 0	Tristate and turn off via SOFTOFF	NFLT = 1 → 0
Gate monitoring error	Tristate and turn off via SOFTOFF	RDY = 1 → 0	Tristate and turn off via SOFTOFF	RDY = 1 → 0
OSM error	Tristate	RDY = 1 → 0	Tristate	RDY = 1 → 0
UVLO1	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
UVLO2	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
OVLO2	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
UVLO3	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
OVLO3	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
Prim. internal supervision error	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
Sec. internal supervision error	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
Life sign error	Normal switch-off	RDY = 1 → 0	Normal switch-off	RDY = 1 → 0
STP keep error	Normal switch-off	RDY = 1 → 0	TON stays "high"	RDY = 1 → 1

***Note**:*
- *In case the output stage is off the overcurrent protection is disabled*
- *During an UVLO1 failure event the NFLT pin may also switch to "low"*

5 Primary Side safety control

The device has two dedicated safety inputs on the primary side. The safety inputs control the output stage reaction in the Safety input states table.

Table 8 Safety input states table

Operation Mode	SI1	SI2	Delay	TON/TOFF	Exception
PWM Disable	0	0	t_{SI_OFF}	Low (VEE2)	Primary_Init mode
PWM Disable	1	0	t_{ASCP_OFF}	Low (VEE2)	Primary_Init mode
ASCP_ON Mode	0	1	t_{ASCP_ON}	High (VCC2)	Primary_Init mode or events in 'Single failure events in PWM Enable mode and ASCP_ON mode'
PWM Enable	1	1	-	PWM	Primary_Init mode or events in 'Single failure events in PWM Enable mode and ASCP_ON mode'

***Note**:*
- *"0" means "low"; "1" means "high".*
- *If an error related to NFLT or RDY appeared during state transition including the internal delay of SI1 and SI2, the device follows the predefined emergency turn off sequence.*

The described PWM signal refers to INP/INN signal on primary side input pins.

The safety inputs of the HS and LS driver are cross connected, as follows. In that way, if a primary ASC is triggered, the opposite driver is turning off. Hence a shoot through is avoided.

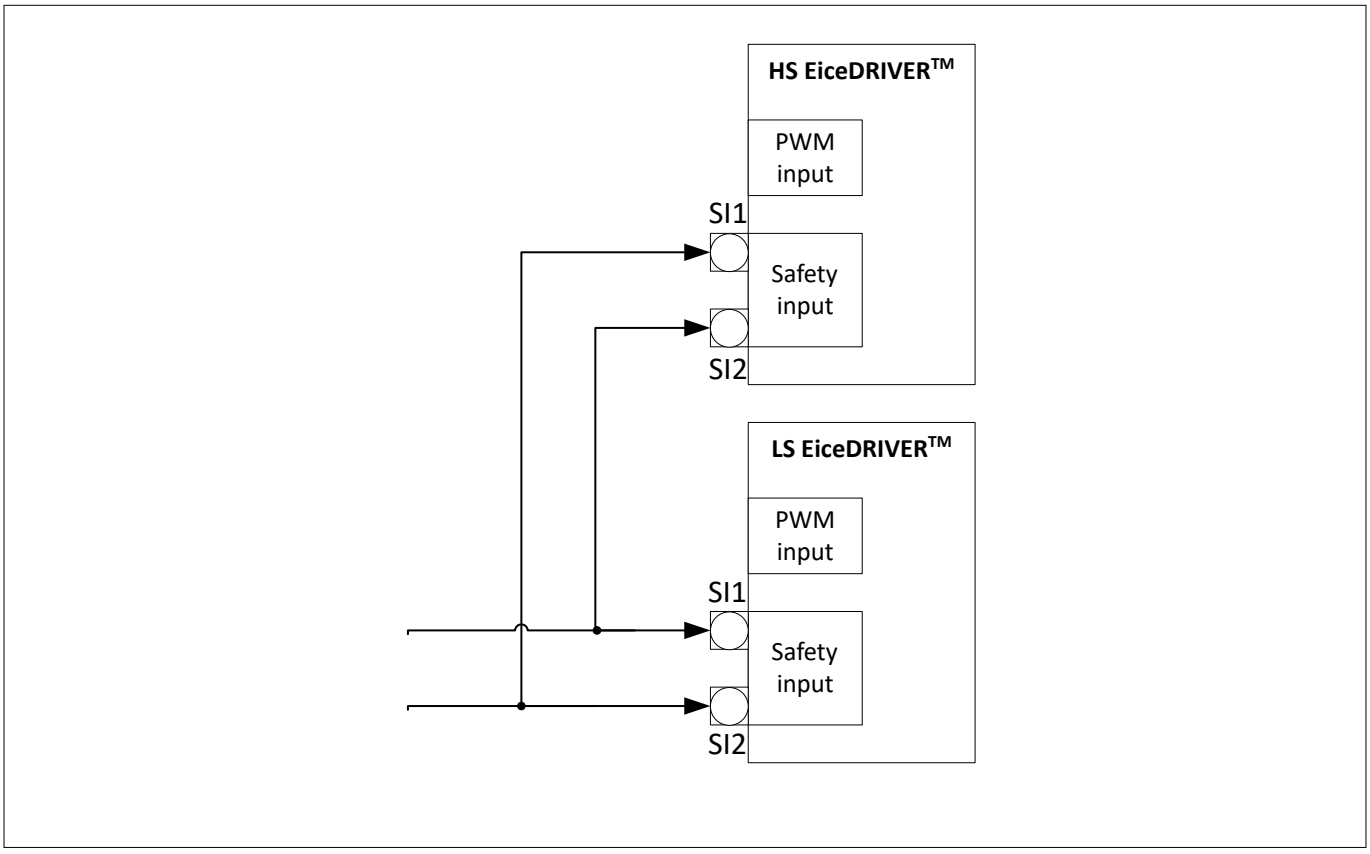

Figure 4 Cross connection of safety inputs in a half bridge configuration

5.1 Functional description of state transitions

PWM Disable mode to PWM Disable mode

The device input triggers to change the operation mode from PWM Disable mode to PWM Disable mode via following state transitions:

- SI2 stays "low" and SI1 = "high".
- SI2 stays "low" and SI1 = "low".

In PWM Disable mode the PWM signal on INP is disabled.

PWM Disable mode to PWM Enable mode

The device input triggers to change the operation mode from PWM Disable mode to PWM Enable mode via following state transition:

- SI1 = "low" to "high" and SI2 = "low" to "high" - see further information in the Note and in Tsafety diagram

Only during PWM Enable mode the PWM signal on INP is a valid input signal for the output stage.

In case INP is "high" before PWM Enable mode is reached after a delay of t_{safety} + $t_{SIglitch}$, TOFF stays "low". TON is activated by next rising edge on INP.

PWM Enable mode to PWM Disable mode

The device can be triggered from PWM Enable mode to PWM Disable mode via safety inputs with following state transitions:

- SI1 = "low" and SI2 = "low". After t_{SI_OFF} delay is elapsed, TON switches ''low''.
- SI1 stays "high" and SI2 = "low". After t_{ASCP_OFF} delay is elapsed, TON switches ''low''.

After internal recognition of the transition via the safety inputs the output stage does not follow the INP signal. In case there is a state transition on INP from "high" to "low" or "low" to "high" during t_{ASCP_OFF} or t_{SI_OFF} this transition is disabled.

PWM Disable mode to ASCP_ON mode

The device can be triggered to change the operation state from PWM Disable mode to ASCP_ON mode via following transition on SI1 and SI2 :

SI1 = "low" and SI2 = "high"

An additional delay is included into this state transition and is defined in t_{ASCP_ON}.

In the PWM Disable and ASCP_ON modes all INP state transitions are ignored.

ASCP_ON mode to PWM Disable mode

The device triggers a state transitions from ASCP_ON mode to PWM Disable mode via following state transitions on SI1 and SI2:

- SI2 = "low". After t_{SI_OFF} delay is elapsed, TON switches ''low''.
- SI1 = "high" and SI2 = "low". After t_{ASCP_OFF} delay is elapsed, TON switches ''low''.

Inside PWM Disable mode and ASCP_ON mode the INP input is ignored.

During t_{SI_OFF} and t_{ASCP_OFF} the output stage is "high".

PWM Enable mode to ASCP_ON mode

The device can trigger a state transition from PWM Enable mode to ASCP_ON mode by setting SI1 to "low".

An additional delay is included and defined in t_{ASCP_ON}.

In case there is a state transition on INP from "high" to "low" or "low" to "high" during t_{ASCP_ON} this transition is ignored.

During t_{ASCP_ON} the last valid INP signal is active on TON/TOFF.

***Note**:* *A direct state transition from ASCP_ON mode to PWM Enable mode is prohibited.*

A direct state transition from PWM Disable mode when SI1 stays "high" by switching SI2 = "high" is prohibited, because when the safety inputs are cross connected to the safety inputs of the opposing gate driver inside a halfbridge topology, the opposing gate driver will otherwise remain in the ASCP_ON mode.

When the device is powered-up with SI1 = SI2 = "high" and the device is ready it transitions directly from PWM Disable into PWM Enable.

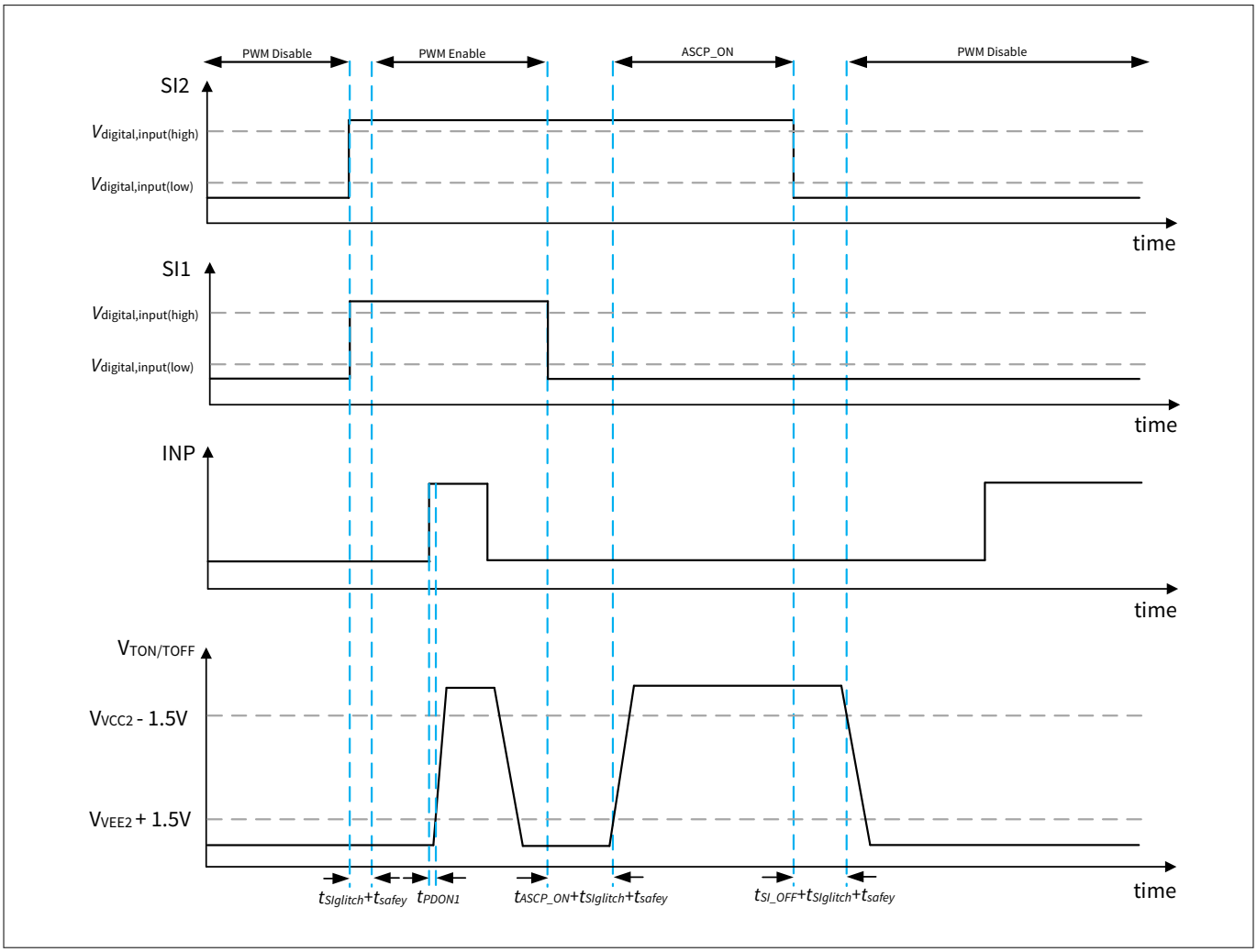

Figure 5 Safety inputs diagram

5.2 Functional description of safety related timings

The device can be switched in between the operating modes via valid signal transitions of SI1 & SI2 from "low" to "high" or "high" to "low".

The safety inputs SI1 and SI2 recognize a valid signal transition in case the signal transition is stable for more than $t_{SIglitch}$.

In case the signal is stable for less than $t_{SIglitch}$ the safety transition timer t_{safety} is not activated and the signal transition is not valid.

At the timestamp of a valid transition from "low" to "high" or "high" to "low" on one safety input a timer starts to count. This time is defined as t_{safety}.

In case of an additional valid signal transition on any safety input during t_{safety} the timer is started again. If there is no additional valid signal transition during t_{safety} on any safety input the state transition is executed.

In case the signal transition is beyond the defined safety transition timer the device is executing the recognized state transition after t_{safety} is elapsed.

The t_{SI_OFF} delay defines the delay between following state transitions:

- from PWM Enable mode to PWM Disable mode via the safety pin transitions SI1 = "low" and SI2 = "low".
- from ASCP_ON mode to PWM Disable mode via the safety pin transitions SI1 stays "low" and SI2 = "low".

The t_{ASCP_ON} delay defines the delay between following state transitions:

- from PWM Enable mode to ASCP_ON mode via the safety pin transitions SI1 = "low" and SI2 stays "high".
- from PWM Disable mode to ASCP_ON mode via the safety pin transitions SI1 stays "low" and SI2 = "high".

The t_{ASCP_OFF} delay defines the delay between following state transitions:

- from PWM Enable mode to PWM Disable mode via the safety pin transitions SI1 stays "high" and SI2 = "low".
- from ASCP_ON mode to PWM Disable mode via the safety pin transitions SI1 = "high" and SI2 = "low".

$t_{SItrans}$ is defined as the minimum time the device needs to stay in the dedicated operation mode state. Switching between states in less than $t_{SItrans}$ is prohibited.

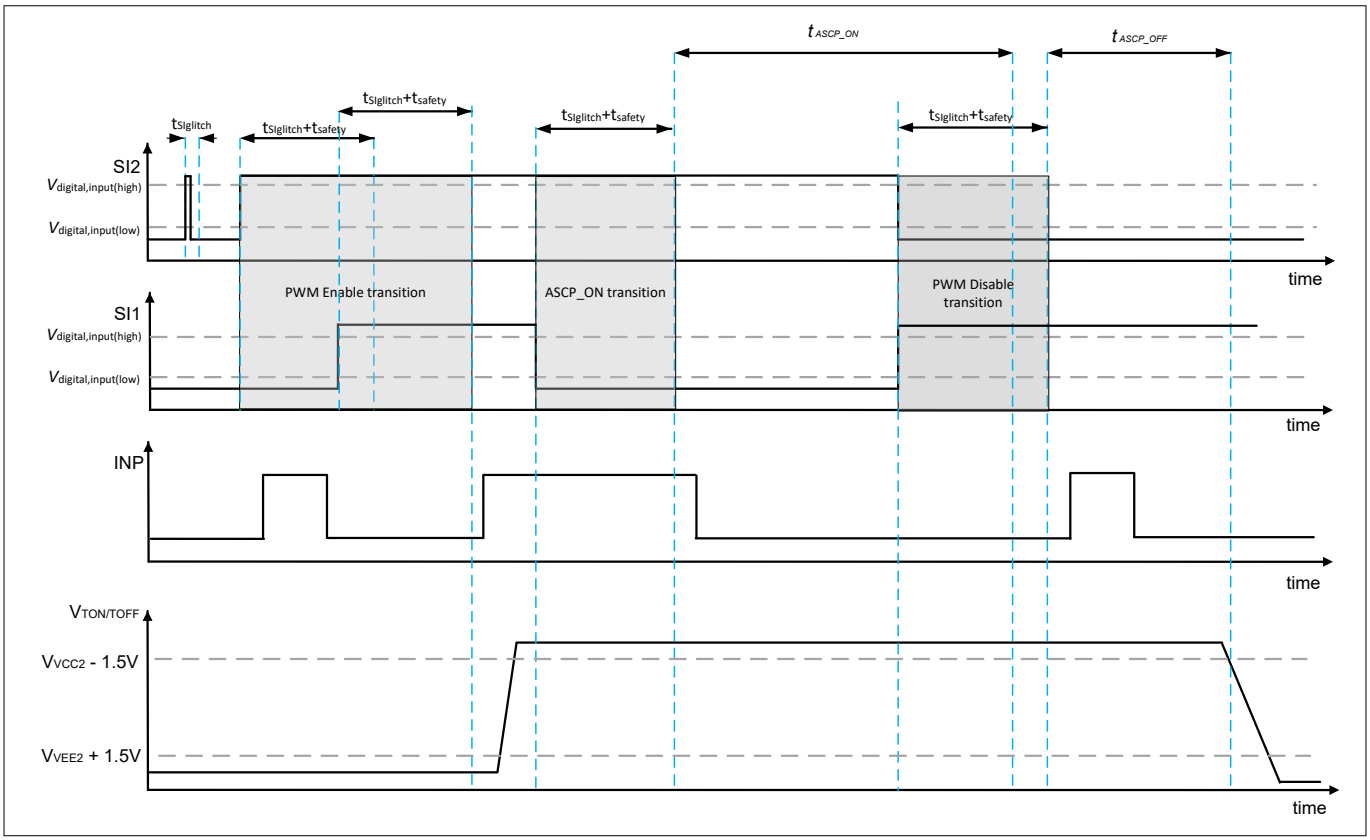

Figure 6 Safety related timing diagram

***Note**: The minimum state transition time $t_{SItrans}$ is not reflected in the timing diagram*

5.3 Electrical characteristics primary side safety control

Table 9 Electrical characteristics primary side safety control

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SI1, SI2 Pull down resistance	R_{PDIN1}	40	48	60	kΩ	V_{SI1} = VCC1 , V_{SI2} = VCC1 , VCC1 = 5V	PRQ-349
SI_OFF delay	t_{SI_OFF}	0.95	1.15	1.35	µs	VCC1 = 5 V, VCC2 = 15 V, VEE2 = -5V, INP = ''high'', SI1 = ''high'' and SI2 = ''high'', start event is SI1 = ''low'' and SI2 = ''low'', after $t_{SIglitch}$+t_{safety} t_{SI_OFF} is elapsed, stop event is TON = VCC2-1.5V, no load	PRQ-665
ASCP ON delay	t_{ASCP_ON}	4.60	5.00	5.45	µs	VCC1 = 5 V, VCC2 = 15 V, VEE2 = -5V, INP = ''low'', SI1 = ''high'' and SI2 = ''high'', start event is SI1 = ''low'' and SI2 = ''high'', after $t_{SIglitch}$+t_{safety} t_{ASCP_ON} is elapsed, stop event is TON = VEE2+1.5V, no load	PRQ-347
ASCP OFF delay	t_{ASCP_OFF}	0.95	1.10	1.35	µs	VCC1 = 5 V, VCC2 = 15 V, VEE2 = -5V, INP = ''high'', SI1 = ''high'' and SI2 = ''high'', start event is SI1 = ''high'' and SI2 = ''low'', after $t_{SIglitch}$+t_{safety} t_{ASCP_OFF} is elapsed, stop event is TON = VCC2-1.5V, no load	PRQ-348
Safety transition timer	t_{safety}	550	670	737	ns	VCC1 = 5 V, VCC2 = 15 V, VEE2 = -5V, INP = high, SI1 = low►high, SI2 = low►high after $t_{safety,max}$	PRQ-358
Safety glitch filter	$t_{SIglitch}$	–	–	20	ns	VCC1 = 5 V, VCC2 = 15 V, VEE2 = -5V, SI1 = SI2 = low►high►low within $t_{SIglitch}$	PRQ-663
Minimum state transition timer	$t_{SItrans}$	8	–	–	µs		PRQ-661

6 Clear functionality

6.1 Functional description clear

In case the device recognizes an error reflected on NFLT or RDY the device operation mode switches to PWM Disable mode. An error is sticky.

All error bits can be cleared by a valid state transition starting from PWM Disable mode with SI1 = "low" and SI2 = "low":

- to PWM Enable mode by SI1 = "high" and SI2 = "high".
- to ASCP_ON mode by SI1 = "low" and SI2 = "high".

If the error reflected on RDY or NFLT disappeared and the internal error bits can be cleared, the device switches back to ASCP_ON mode or PWM Enable mode with the dedicated transition of SI1 and SI2.

Error

The following errors are mapped to an error bit:

- UVLO2
- UVLO3
- OVLO2
- OVLO3
- OCP error
- OSM error
- Gate monitoring error
- STP keep error

The life sign error is raised when the life sign was established once and then lost. The life sign error is not part of the DATA readout.

DATA readout contains the No life sign established bit. The No life sign established bit reflects the instantaneous status of the life sign.

In case of no life sign error is active all active errors remain sticky until a valid clear command.

If the error is present during the clear command, the clear command is not executed.

The device stays in PWM Disable mode and RDY or NFLT stays "low".

The clear command via safety inputs needs to be executed again.

Warning

In case a warning occurred and is recognized by the device it is notified via the diagnostic frame.

If the warning source is gone the warning bit is self-cleared after it was transmitted via the diagnostic frame once.

Warnings do not impact the state of NFLT or RDY.

Even with an activated warning bit the device can execute changes inside the operating states via the valid transitions of SI1 and SI2.

The following warnings are mapped to a warning bit:

- OCP BIST
- Dead time warning
- SASC activation warning
- Bipolar detection warning

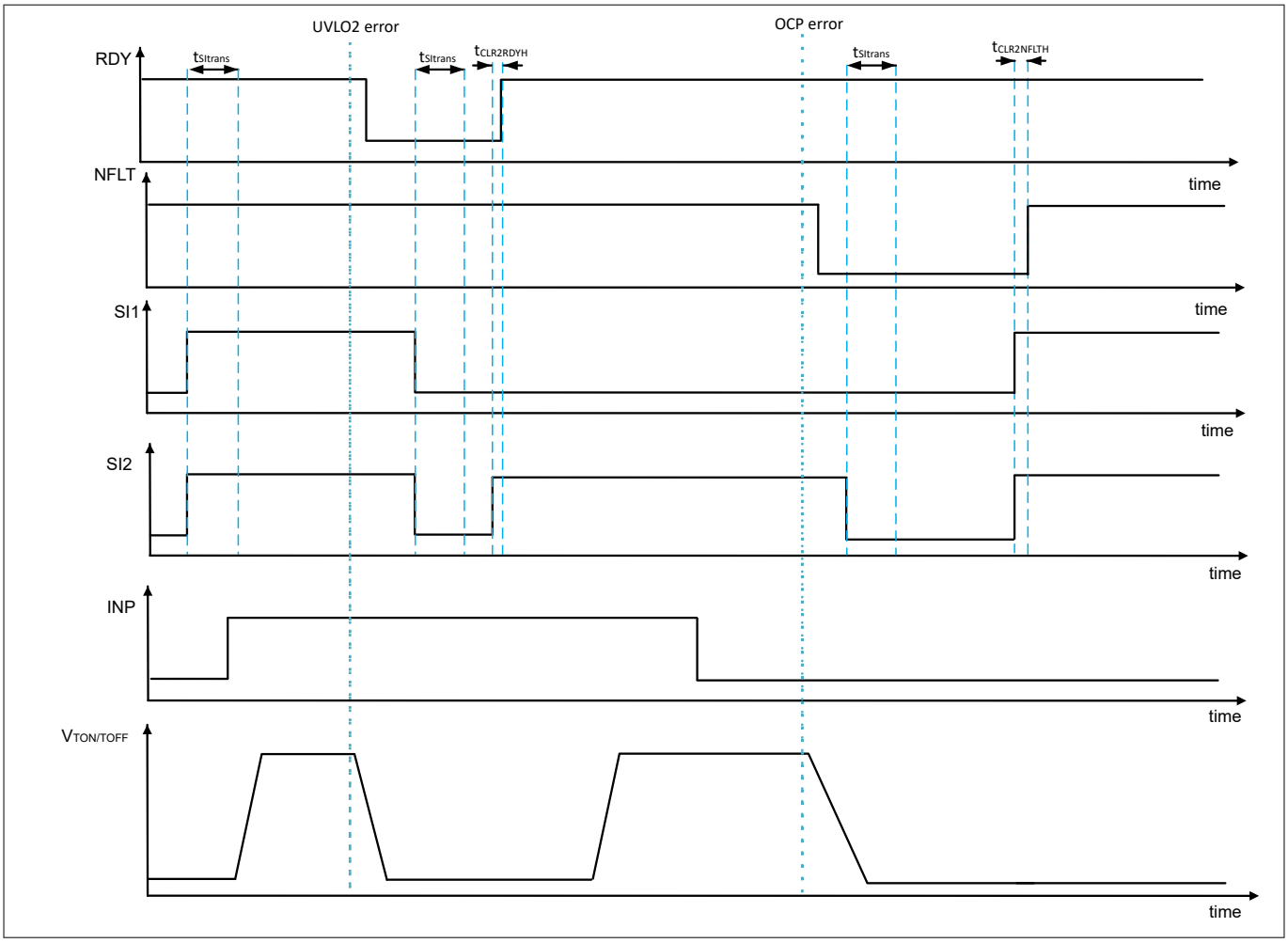

Figure 7 Clear of errors timing diagram

6.2 Electrical characteristics Clear

Table 10 Electrical characteristics Clear

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
clear time to NFLT high	$t_{CLR2NFLTH}$	–	–	1	µs	VCC1=5V; 10kΩ pullup on NFLT to VCC1, SI1 = "low", SI2 = "low" , Start rising edge on SI2 to "high" , Stop rising edge on NFLT to "high"	PRQ-249
clear time to RDY high	$t_{CLR2RDYH}$	–	–	1	µs	VCC1=5V; 10kΩ pullup on RDY to VCC1, SI1 = "low", SI2 = "low" , Start rising edge on SI2 to "high" , Stop rising edge on RDY to "high"	PRQ-658

7 Power supply current consumption

7.1 Functional description power supply current consumption

The device is designed to support two different supply configurations, bipolar supply and unipolar supply.

- In case the unipolar topology is used the device is typically supplied with 15 V on VCC2 and 0 V on VEE2.
- In case the bipolar topology is used the device is typically supplied with 15 V on VCC2 and -5 V on VEE2.

In any case of the mentioned topologies it is recommended to connect the GATE/CLAMP directly to the gate of the power semiconductor to prevent unintended turn on caused by parasitic capacitances of the power switch.

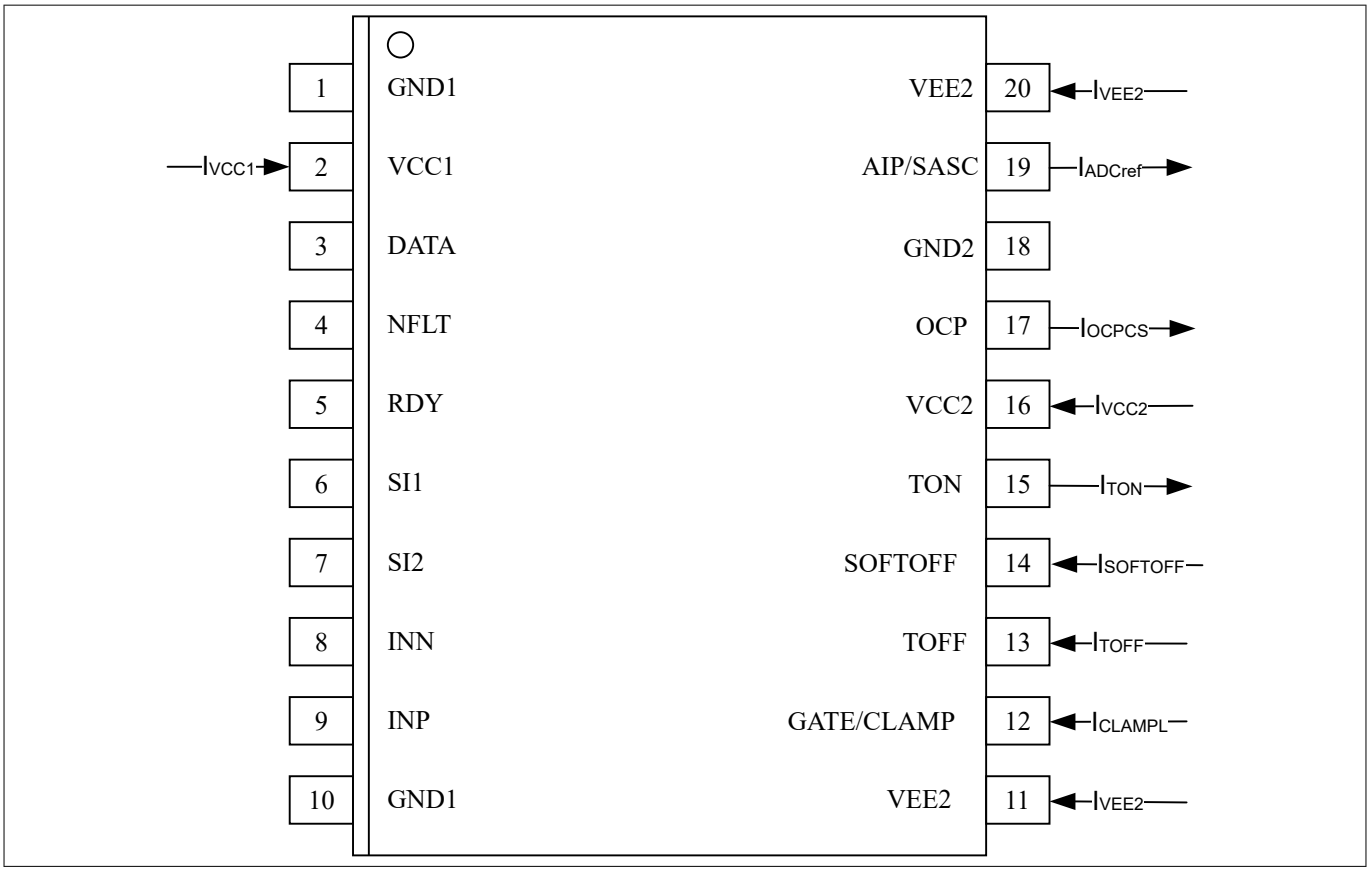

Figure 8 Current direction definition

I_{QVCC1} defines the quiescent current consumption of the primary chip in case it is supplied and in idle mode without INP switching.

I_{OPVCC1_ON} defines the operating current consumption of the primary chip in case it is supplied and the output stage is statically switched to "high".

I_{OPVCC1_OFF} defines the operating current consumption of the primary chip in case it is supplied and the output stage is statically switched to "low".

I_{OPVCC2_ON} defines the operating current consumption of the secondary chip on VCC2 in case it is supplied and the output stage is statically switched to "high".

I_{OPVCC2_OFF} defines the operating current consumption of the secondary chip on VCC2 in case it is supplied and the output stage is statically switched to "low".

I_{OPVEE2_ON} defines the operating current consumption of the secondary chip on VEE2 in case it is supplied and the output stage is statically switched to "high".

I_{OPVEE2_OFF} defines the operating current consumption of the secondary chip on VEE2 in case it is supplied and the output stage is statically switched to "low".

7.2 Electrical characteristics power supply current consumption

Table 11 Electrical characteristics power supply current consumption

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Quiescent Current on VCC1	I_{QVCC1}	3	5	–	mA	PWM Disable mode, all primary I/Os without impact on PWM Disable mode open, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-94
Operating Current VCC1 with TON = "high"	I_{OPVCC1_ON}	–	12	14.5	mA	PWM Enable mode, INN = 0, INP = 1, SI1 = 1, SI2 = 1, outputs open,V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-95
Operating Current VCC1 with TOFF = "low"	I_{OPVCC1_OFF}	–	5.5	7	mA	PWM Enable Mode, INN = 0, INP = 0, SI1, SI2= 1, outputs open, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V	PRQ-96
Operating Current VCC2 with TON = "high"	I_{OPVCC2_ON2}	–	11	13	mA	PWM Enable mode, INN = 0, INP = 1, SI1 = 1, SI2 = 1, other primary outputs open, OCP = "low", Gate shorted to TON, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other secondary pins open	PRQ-675
Operating Current VCC2 with TOFF = "low"	I_{OPVCC2_OFF2}	6	11	13	mA	PWM Enable mode, INN = 0, INP = 1, SI1 = 1, SI2 = 1, other primary outputs open, OCP = "low", Gate shorted to TOFF, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other pins open	PRQ-673
Operating Current VEE2 with TON = "high"	I_{OPVEE2_ON2}	–	1.5	2	mA	PWM Enable mode, INN = 0, INP = 1, SI1 = 1, SI2 = 1, other primary outputs open, OCP = "low", Gate shorted to TON, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other secondary pins open	PRQ-676
Operating Current VEE2 with TOFF = "low"	I_{OPVEE2_OFF2}	0.5	1.5	2	mA	PWM Enable mode, INN = 0, INP = 1, SI1 = 1, SI2 = 1, other primary outputs open, OCP = "low", Gate shorted to TOFF, V_{VCC1} = 5 V, V_{VCC2} = 15 V, V_{VEE2} = -5 V, other secondary pins open	PRQ-677

8 Power supply monitoring

8.1 Functional description power supply monitoring

The time t_{PS2RDY} is defining the time from the detection of an undervoltage or an overvoltage event on any of the monitored voltage rails VCC1 ,VCC2 ,VEE2 until the notification by changing RDY to "low".

8.1.1 Functional description at VCC1

The device is equipped with an undervoltage lockout on the primary supply of VCC1 in order to ensure the correct behavior of the device.

In case the voltage on VCC1 is exceeding $V_{UVLO1,H1}$ the primary side state changes from power down mode into PWM Disable mode.

Note: In all undervoltage conditions SASC signal still works until voltage drops below V_{ASCOFF} at VCC2. Primary ASC via SI1 and SI2 is deactivated in case UVLO1 is detected.

The detection & reaction time $t_{UVLO1OFF}$ is started by crossing the low threshold of undervoltage functionality V_{UVLO1L_1} , and stops when TON = V_{VCC2} - 1.5V. The reaction is taken whether the fault is cleared during $t_{UVLO1OFF}$ or not.

In case the voltage on VCC1 drops below V_{UVLO1L_1} the device changes into Primary INIT mode.

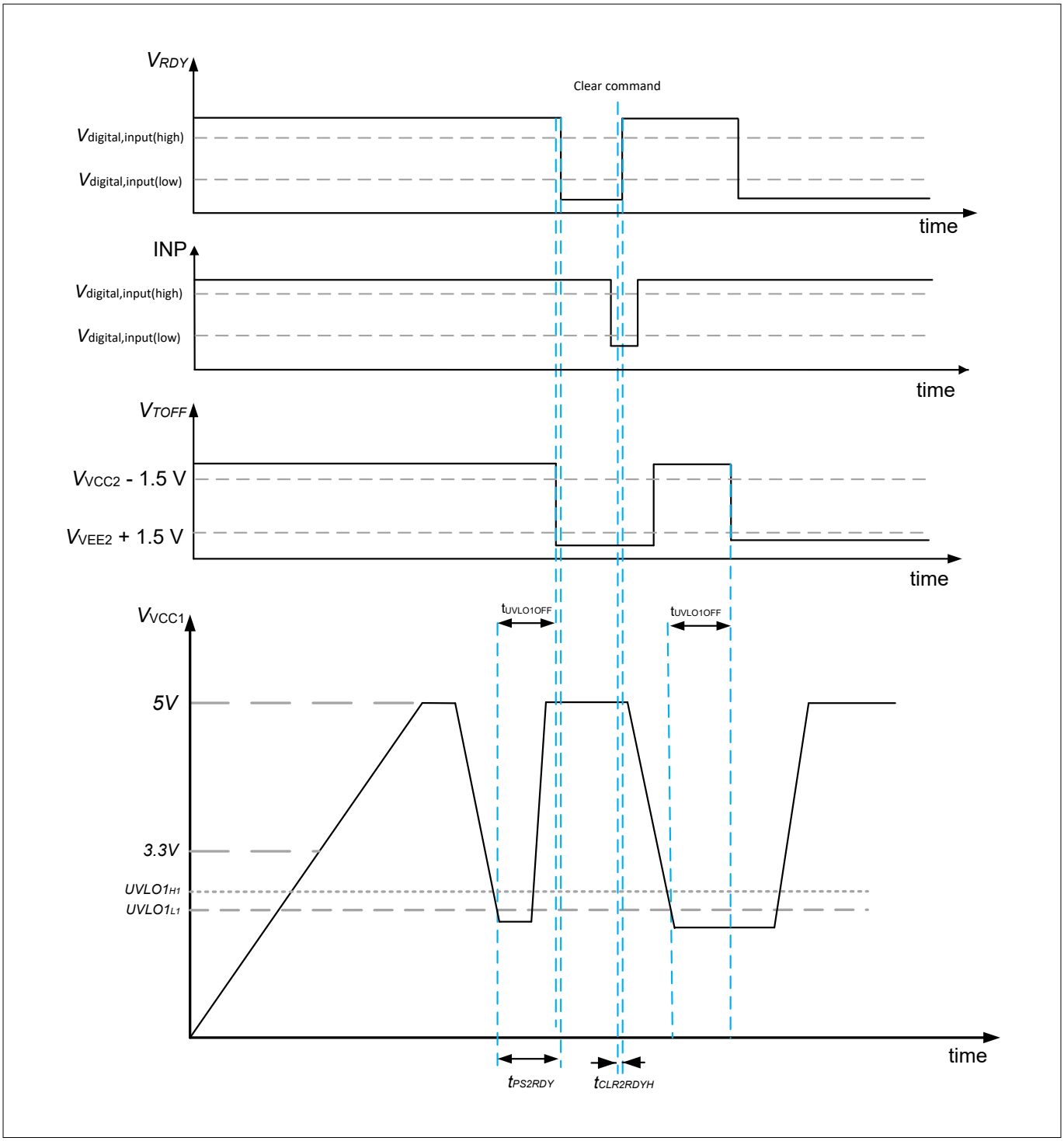

Figure 9 UVLO1 detailed scheme

8.1.2 Functional description at VCC2

The device is equipped with a undervoltage monitoring on VCC2 supply rail to prevent damage of the power switch..

In case an undervoltage on VCC2 is detected, the device executes a regular turn off sequence after $t_{UVLO2OFF}$.

- Primary side input signals on INP and INN are ignored.
- The device changes its operation state to PWM Disable mode.

- RDY is switched to "low" within detection and notification time t_{PS2RDY} .
- Diagnostics are available on DATA output.

If V_{VCC2} decreases below $V_{UVLO2L1}$ the undervoltage lockout gets active.

The detection & reaction time $t_{UVLO2OFF}$ is started by crossing the low threshold of undervoltage functionality V_{UVLO2L_0}, and stops when TON = V_{VCC2} - 1.5V. The reaction is taken whether the fault is cleared during $t_{UVLO2OFF}$ or not.

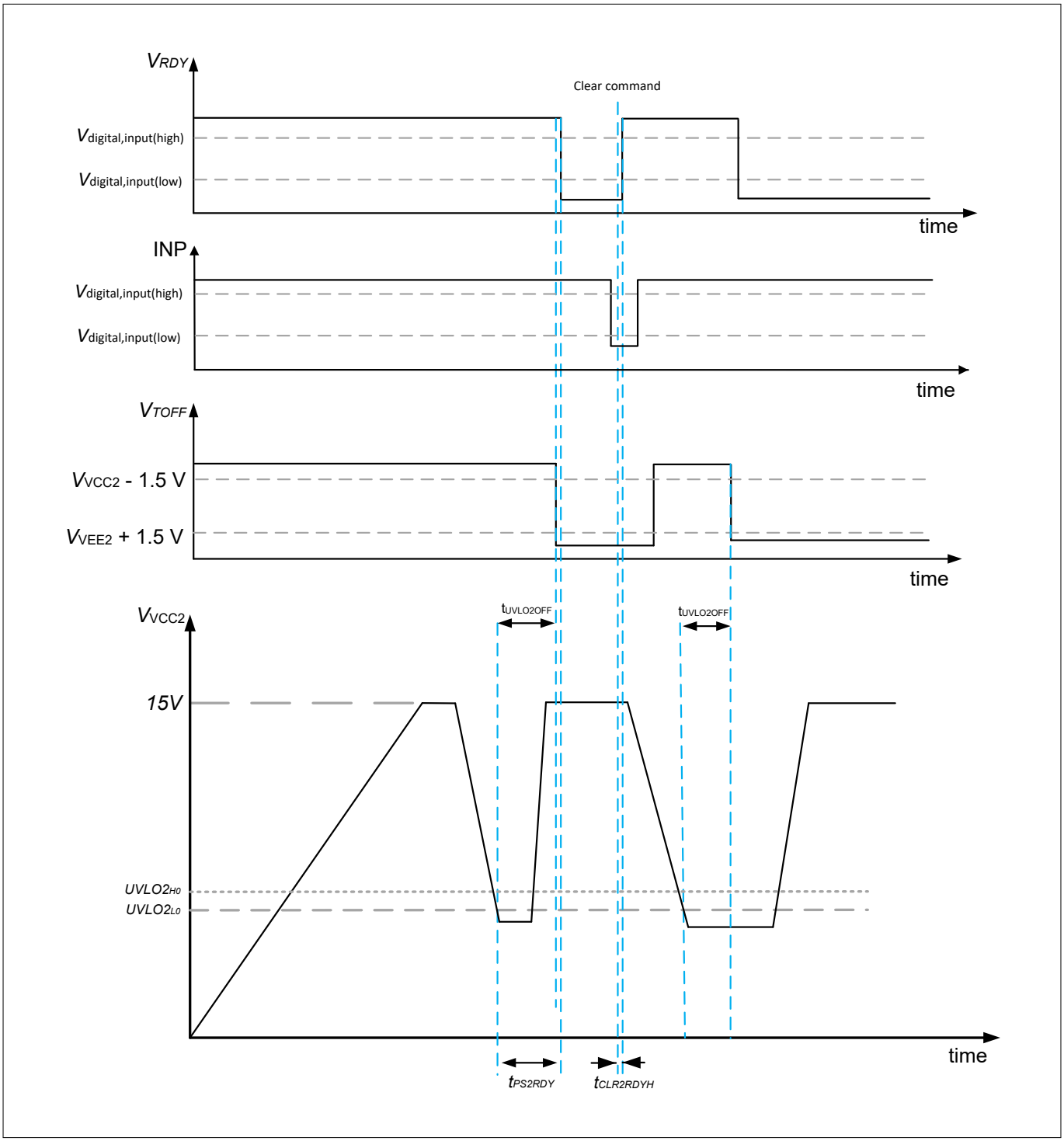

Figure 10 UVLO2 scheme

The device is equipped with an overvoltage lockout for the secondary supply VCC2 in order to prevent damage of the power switch.

8 Power supply monitoring

In case there is an overvoltage on voltage on VCC2 supply, the device executes a regular turn off sequence after $t_{OVLO2OFF}$.

- Primary side input signals on INP and INN are ignored.
- The device changes its operation state to PWM Disable mode.
- RDY is switched to "low" within detection and notification time t_{PS2RDY}.
- Diagnostics are available on DATA output.

Note: SASC signal will overwrite the turn-off command, which may lead to damage of the power switch.

The detection & reaction time $t_{OVLO2OFF}$ is started by crossing the high threshold of overvoltage functionality V_{OVLO2H_0}, and stops when TON = V_{VCC2} - 1.5V. The reaction is taken whether the fault is cleared during $t_{OVLO2OFF}$ or not.

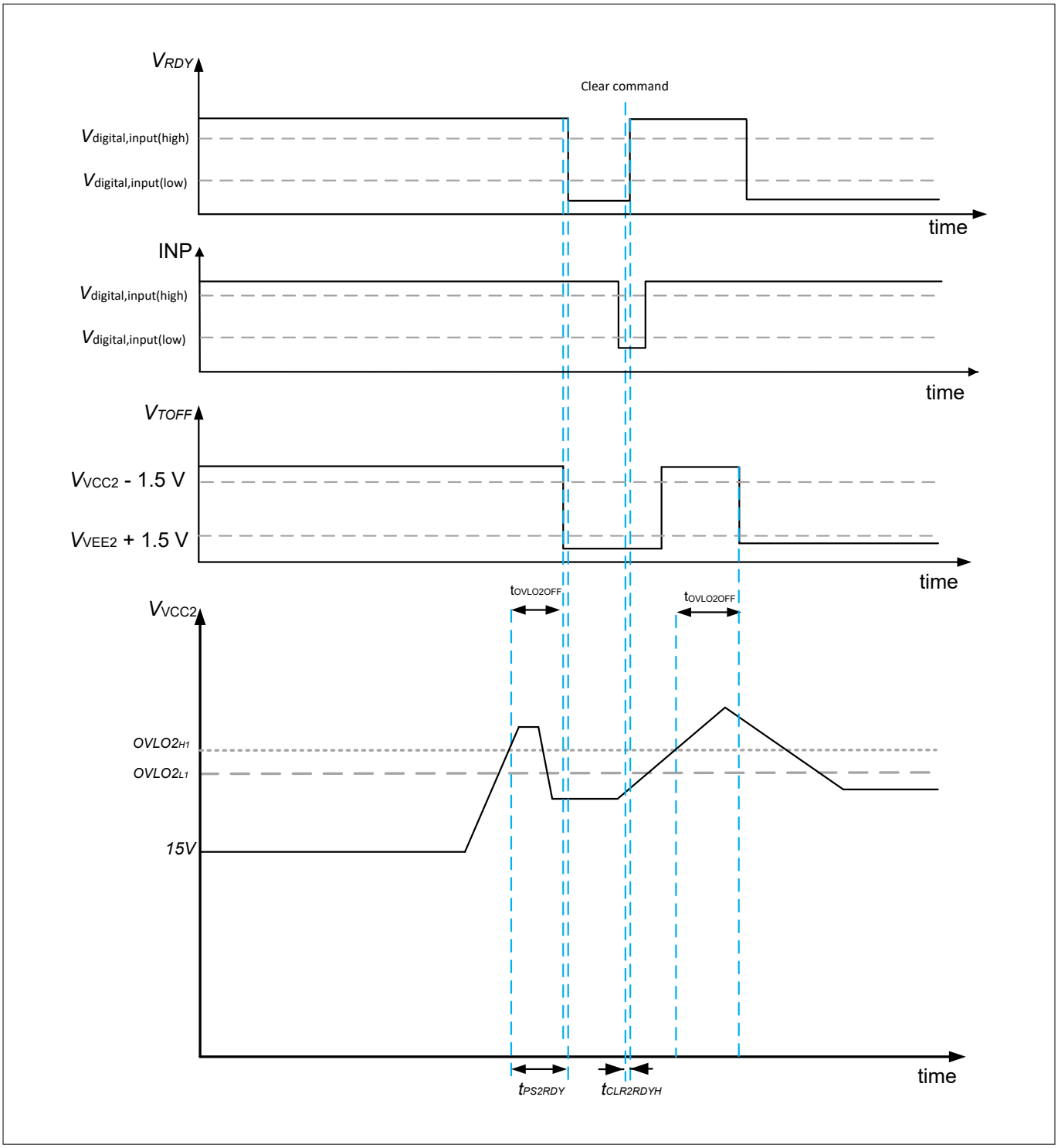

Figure 11 OVLO2 scheme

8.1.3 Functional description at VEE2

The device is equipped with an undervoltage lockout to prevent damage on the power switch.
In case an undervoltage on VEE2 is detected, the device executes a regular turn off sequence after $t_{UVLO3OFF}$.

- Primary side input signals on INP and INN are ignored.
- The device changes its operation state to PWM Disable mode.
- RDY is switched to "low" within detection and notification time t_{PS2RDY}.
- Diagnostics are available on DATA output.

Note: SASC signal will overwrite the turn-off command.

The detection & reaction time $t_{UVLO3OFF}$ is started by crossing the low threshold of undervoltage functionality V_{UVLO3L_1}, and stops when TON = V_{VCC2} - 1.5V. The reaction is taken whether the fault is cleared during $t_{UVLO3OFF}$ or not.

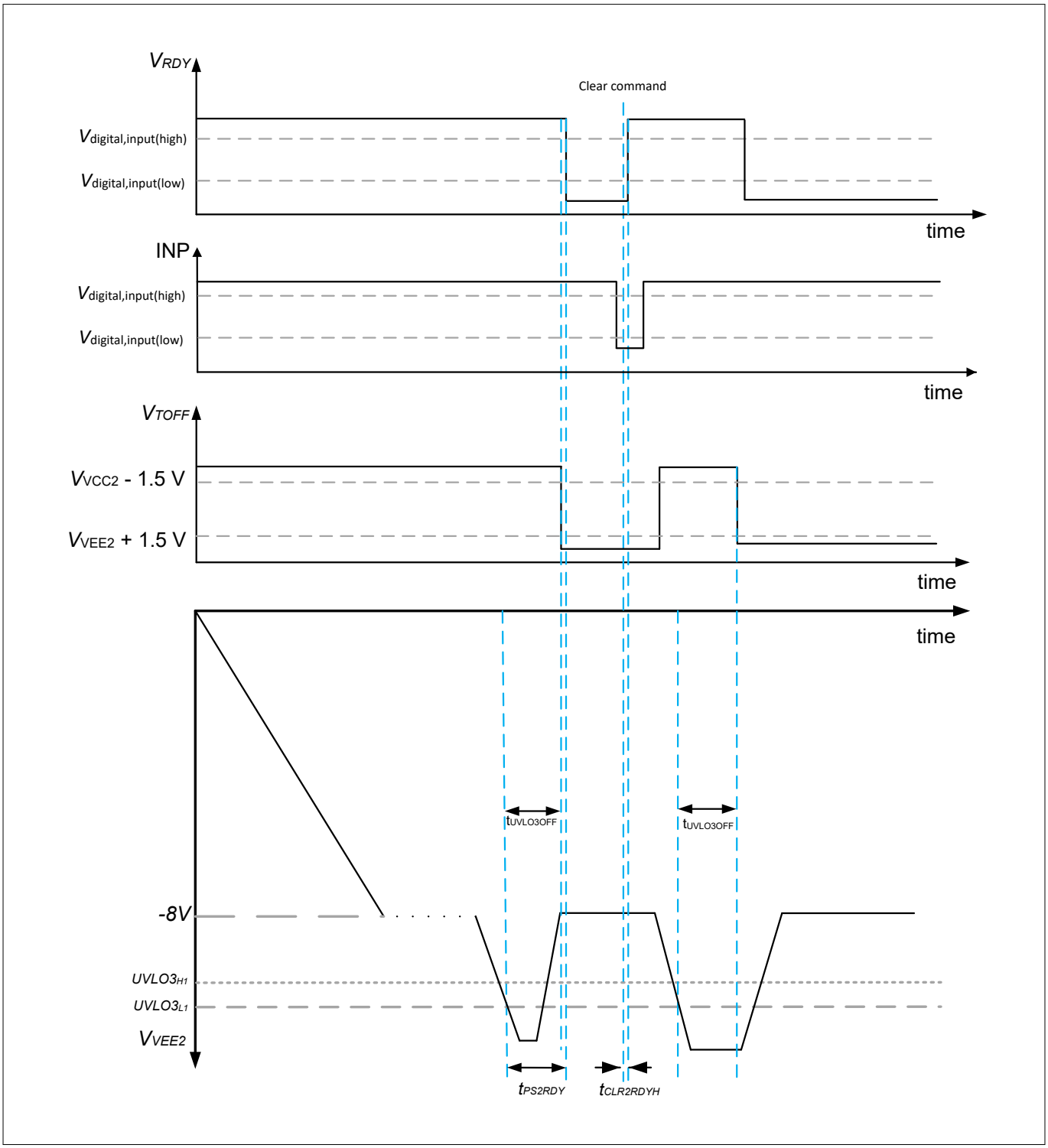

Figure 12 UVLO3 scheme

The device is equipped with an overvoltage lockout for the secondary supply VEE2 to prevent damage of the power switch.

In case an overvoltage on VEE2 is detected, the device executes a regular turn off sequence after $t_{OVLO3OFF}$.

- Primary side input signals on INP and INN are ignored.

- The device changes its operation state to PWM Disable mode.
- RDY is switched to "low" within detection and notification time t_{PS2RDY}.
- Diagnostics are available on DATA output.

Note: SASC signal will overwrite the turn-off command.

In case the threshold of $V_{OVLO3Lx}$ is crossed and the voltage level of VEE2 is stable for at least $t_{VLO,active}$ the crossed $V_{OVLO3Lx}$ threshold is latched and the Bipolar detection warning is set in DATA. Once the threshold is latched the secondary supply VEE2 overvoltage monitoring is active.

This threshold is fixed until the next secondary side power on reset is triggered. The secondary supply VEE2 overvoltage monitoring is not active when the voltage level of VEE2 is higher than $V_{OVLO3Hx}$.

The detection & reaction time $t_{OVLO3OFF}$ is started by crossing the high threshold of overvoltage functionality V_{OVLO3H_0}, and stops when TON = V_{VCC2} - 1.5V. The reaction is taken whether the fault is cleared during $t_{OVLO3OFF}$ or not.

***Note**: The symbol V_{OVLO3} defines all possible overvoltage thresholds on VEE2 supply rail.*

8 Power supply monitoring

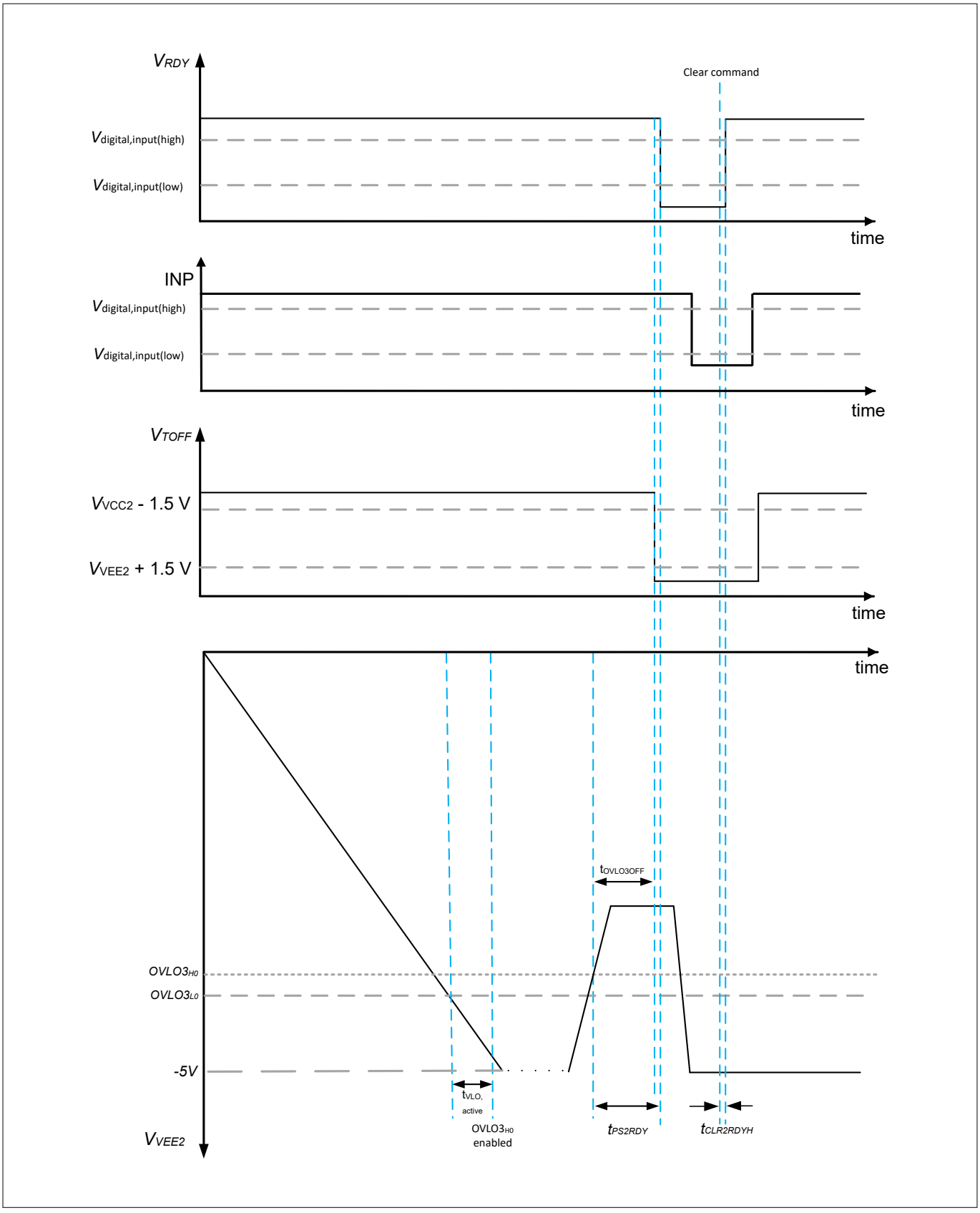

Figure 13 OVLO3 scheme

8.2 Electrical characteristics power supply monitoring

Table 12 Electrical characteristics power supply monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply monitoring detection and notification time	t_{PS2RDY}	–	–	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-183
Voltage lockout threshold activation timer	$t_{VLO,active}$	95	100	106	µs		PRQ-405
UVLO1 threshold low	V_{UVLO1L_1}	2.6	2.75	2.91	V	VCC1, referenced to GND1	PRQ-409
UVLO1 threshold high	V_{UVLO1H_1}	2.71	2.85	2.95	V	VCC1, referenced to GND1	PRQ-160
UVLO1 detection & reaction time	$t_{UVLO1OFF}$	–	500	800	ns	no C_{LOAD}, no R_{LOAD} Start: $V_{VCC1} < V_{UVLO1L\_1}$ with Slewrate = 2 V/µs, Overdrive = +/- 400 mV, Stop: TON = V_{VCC2} - 1.5 V	PRQ-180
UVLO2 threshold low	V_{UVLO2L_0}	11.6	12.0	12.4	V	@ VCC2, referenced to GND2	PRQ-172
UVLO2 threshold high	V_{UVLO2H_0}	12.0	12.4	12.8	V	@ VCC2, referenced to GND2	PRQ-171
UVLO2 detection & reaction time	$t_{UVLO2OFF}$	–	500	800	ns	no C_{LOAD}, no R_{LOAD}, Start: $V_{VCC2} < V_{UVLO2L\_x}$ with Slewrate=10 V/µs; Overdrive=+/-400 mV, Stop: TON = V_{VCC2} - 1.5 V	PRQ-181
OVLO2 threshold low	V_{OVLO2L_1}	17.8	18.4	19.0	V	@ VCC2, referenced to GND2	PRQ-165

(table continues...)

Table 12 (continued) Electrical characteristics power supply monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OVLO2 threshold high	V_{OVLO2H_1}	18.3	19.0	19.4	V	@ VCC2, referenced to GND2	PRQ-164
OVLO2 detection & reaction time	$t_{OVLO2OFF}$	–	500	800	ns	no C_{LOAD}, no R_{LOAD}, Start: $V_{VCC2} > V_{OVLO2H\_x}$ with Slewrate=10 V/µs; Overdrive=+/-400 mV, Stop: TON = V_{VCC2} - 1.5 V	PRQ-568
UVLO3 threshold low	V_{UVLO3L_2}	-10.75	-10.3	-9.9	V	@ VEE2, referenced to GND2	PRQ-410
UVLO3 threshold high	V_{UVLO3H_2}	-9.85	-9.5	-9.1	V	@ VEE2, referenced to GND2	PRQ-411
UVLO3 detection & reaction time	$t_{UVLO3OFF}$	–	500	800	ns	no C_{LOAD}, no R_{LOAD}, Start: $V_{VEE2} < V_{UVLO3L\_x}$ with Slewrate=10 V/µs; Overdrive=+/-400 mV, Stop: TON = V_{VCC2} - 1.5 V	PRQ-182
OVLO3 detection & reaction time	$t_{OVLO3OFF}$	–	600	800	ns	no C_{LOAD}, no R_{LOAD}, Start: $V_{VEE2} > V_{OVLO3H\_x}$ with Slewrate=10 V/µs; Overdrive=+/-400 mV, Stop: TON = V_{VCC2} - 1.5 V OVLO3 threshold is latched	PRQ-567
OVLO3 threshold low	V_{OVLO3L_1}	-3.95	-3.7	-3.5	V	@ VEE2, referenced to GND2	PRQ-725
OVLO3 threshold high	V_{OVLO3H_1}	-3.1	-2.9	-2.75	V	@ VEE2, referenced to GND2	PRQ-726

9 Switching characteristics

The voltage on pin TON ranges to V_{VCC2} (referenced to GND2).
The voltage on pin TOFF ranges to V_{VEE2} (referenced to GND2).
The device enables short pulses on INP with min. duration defined in t_{INPPD}.
The device supports short propagation delay for On and Off switching of t_{PDON1} and t_{PDOFF1}.

9.1 Electrical characteristics switching

Table 13 Electrical characteristics switching

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).
Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Propagation delay - On	t_{PDON1}	55	60	90	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP rising edge at $V_{digital,input(high)}$, Stop: TON rising edge at V_{VEE2} + 1.5 V, no load, no gate resistance	PRQ-106
Propagation delay - Off	t_{PDOFF1}	55	60	90	ns	VCC1 = typ., VCC2 = typ., VEE2 = typ., Start: INP falling edge at $V_{digital,input(low)}$, Stop: TOFF falling edge at V_{VCC2} - 1.5 V, no load, no gate resistance	PRQ-107
Propagation delay distortion	$t_{Prop,dis}$	-20	–	20	ns	t_{PDON1} - t_{PDOFF1}, t_{PDON1} & t_{PDOFF1} measured @ same T_{JUNC}, t_{INPPD} ≥ 150 ns	PRQ-718
Switching frequency	f_{SW}	–	25	500	kHz	Duty cycle limited by t_{INPPD} , V_{VCC2} = 15 V, V_{VEE2} = -5 V, C_{Gate} = 9 nF, R_g = 6 Ω, T_{AMB} = 25°C	PRQ-77
High level output peak current	I_{TON}	- 15	–	–	A	V_{INP} = V_{VCC1}, V_{INN} = V_{GND1}, V_{SI1} = V_{SI2} = V_{VCC1}, V_{VCC2} = 15V, V_{VEE2} = -5 V	PRQ-104
TON RDSON High-side P&N	$R_{DSON-OSHtot}$	0.3	–	1	Ω	N-MOS and P-MOS, voltage drop V_{VCC2} - V_{TON} < 1 V	PRQ-115
TON rise time 90%	t_{Rise1}	–	–	55	ns	no C_{LOAD}, no R_{LOAD}, V_{VCC2} = typ., V_{VEE2} = typ. V_{TON} = V_{VEE2} + 1.5 V to V_{TON} = V_{VCC2} - 1.5 V	PRQ-111
TON rise time 70%	t_{Rise2}	–	–	35	ns	no $C_{LOAD,}$ no R_{LOAD}, V_{VCC2} = typ., V_{VEE2} = typ., V_{TON} = V_{VEE2} + 1.5 V to V_{TON} = V_{VCC2} - 6 V	PRQ-112
TOFF Fall time	t_{Fall}	–	–	45	ns	No C_{LOAD}, no R_{LOAD}, V_{VCC2} = typ., V_{VEE2} = typ., V_{TOFF} = V_{VCC2} - 1.5 V to V_{TOFF} = V_{VEE2} + 1.5 V	PRQ-113
TOFF RDSON	$R_{DSON-OSLN}$	0.07	–	0.35	Ω	N-MOS, voltage drop V_{TOFF} - V_{VEE2} < 1 V	PRQ-116

(table continues...)

Table 13 (continued) Electrical characteristics switching

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
INP high/low duration	t_{INPPD}	150	–	–	ns	V_{VCC1}=typ., V_{VCC2}=typ., V_{VEE2}=typ., 50% to 50%, repetitive pulse propagation, f_{sw} = 30 kHz	PRQ-265

***Note**: The defined minimum/maximum value of I_{TON} is the minimum current which the device delivers under the given conditions. In general the device is capable to deliver higher output currents than the defined minimum. The maximum output current needs to be limited by an external gate resistor to stay inside the defined absolute maximum rating parameters regarding maximum peak current (equivalent energy needs to be considered) and maximum junction temperature.*

10 I/O levels

Table 14 I/O levels

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Primary digital input low level	$V_{digital,input(low)}$	0	–	0.8	V		PRQ-263
Primary digital input high level	$V_{digital,input(high)}$	2	–	V_{VCC1}	V		PRQ-264
Weak pull down resistance INP	R_{PDIN1}	40	48	60.5	kΩ	V_{INP} = VCC1, VCC1 = 5V	PRQ-271
Weak pull up resistance INN	R_{PDINN}	80	100	120	kΩ	V_{INN} = GND1	PRQ-272

11 Shoot Through Protection (STP)

11.1 Functional description STP

The device has an always active Shoot Through Protection (STP) function to prevent both highside and lowside switches to be activated simultaneously.

Exception: If the device is in ASCP_ON mode or in a valid transition to ASCP_ON mode the Shoot Through Protection functionality is disabled and RDY switches to "high".

Setting INN pin to GND1 deactivates the function.

Note: In case INP is shorted to INN and both are activated simultaneously, the output stage might be switched to "high".

If one of the drivers is in ON state, the driver's counterpart PWM input is inhibited, preventing it to turn on.

If the minimum deadtime between INN and INP is less than t_{DEAD} the deadtime is increased internally to t_{DEAD}.

The deadtime warning Bit inside the diagnostic frame is set to "high".

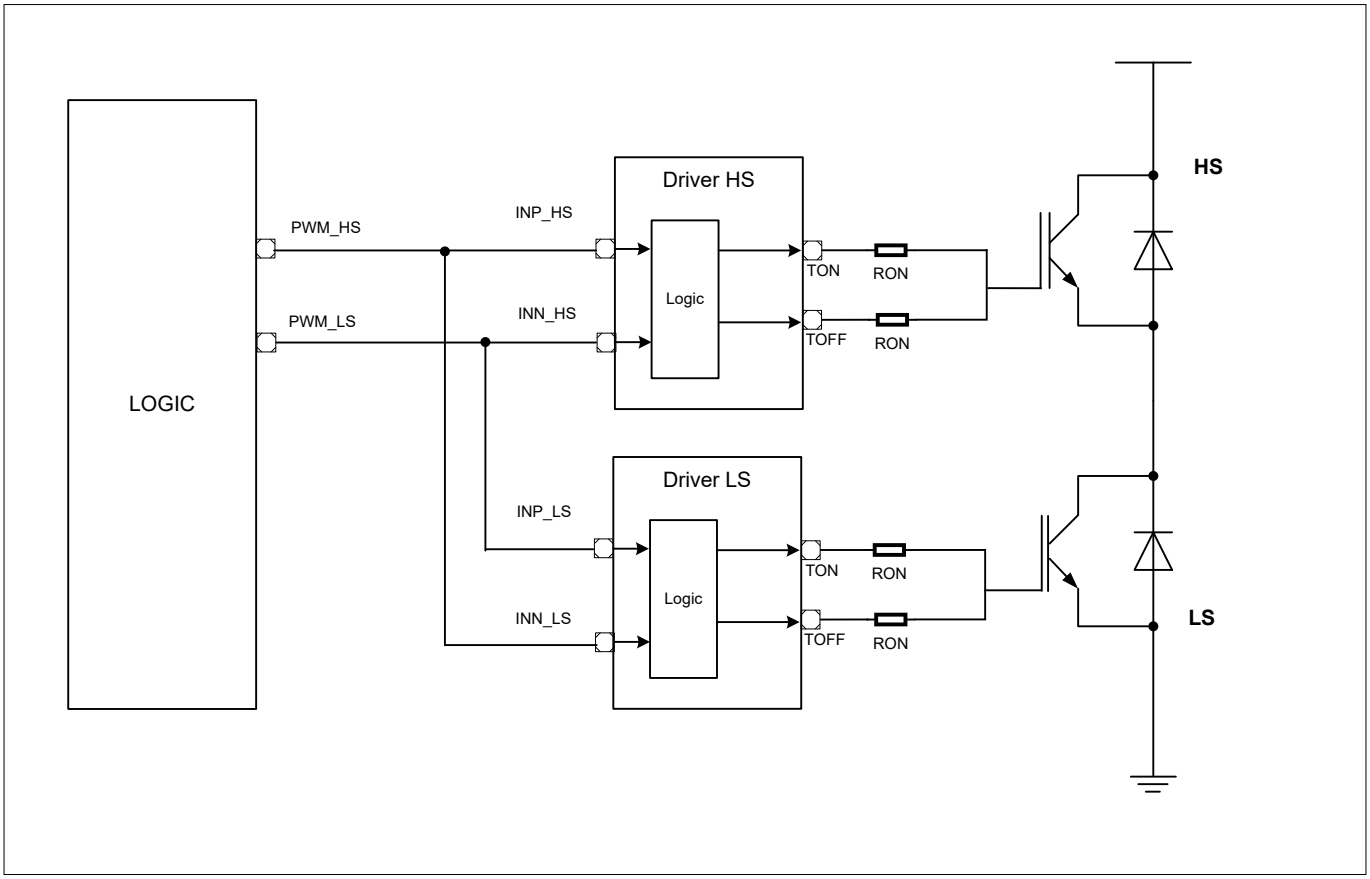

Figure 14 Shoot through protection application schematic

If the maximum keep state time $t_{keepstate,max}$ is exceeded a regular turn-off to VEE2 is executed after $t_{STP2OFF}$ and RDY is set to "low" within $t_{STP2RDY}$.

The STP keep error bit is set to "high". In case STP keep error gets active the Deadtime warning bit is set to "high"

Exception: If the device is in ASCP_ON mode or in a valid transition to ASCP_ON mode the STP keep error is disabled.

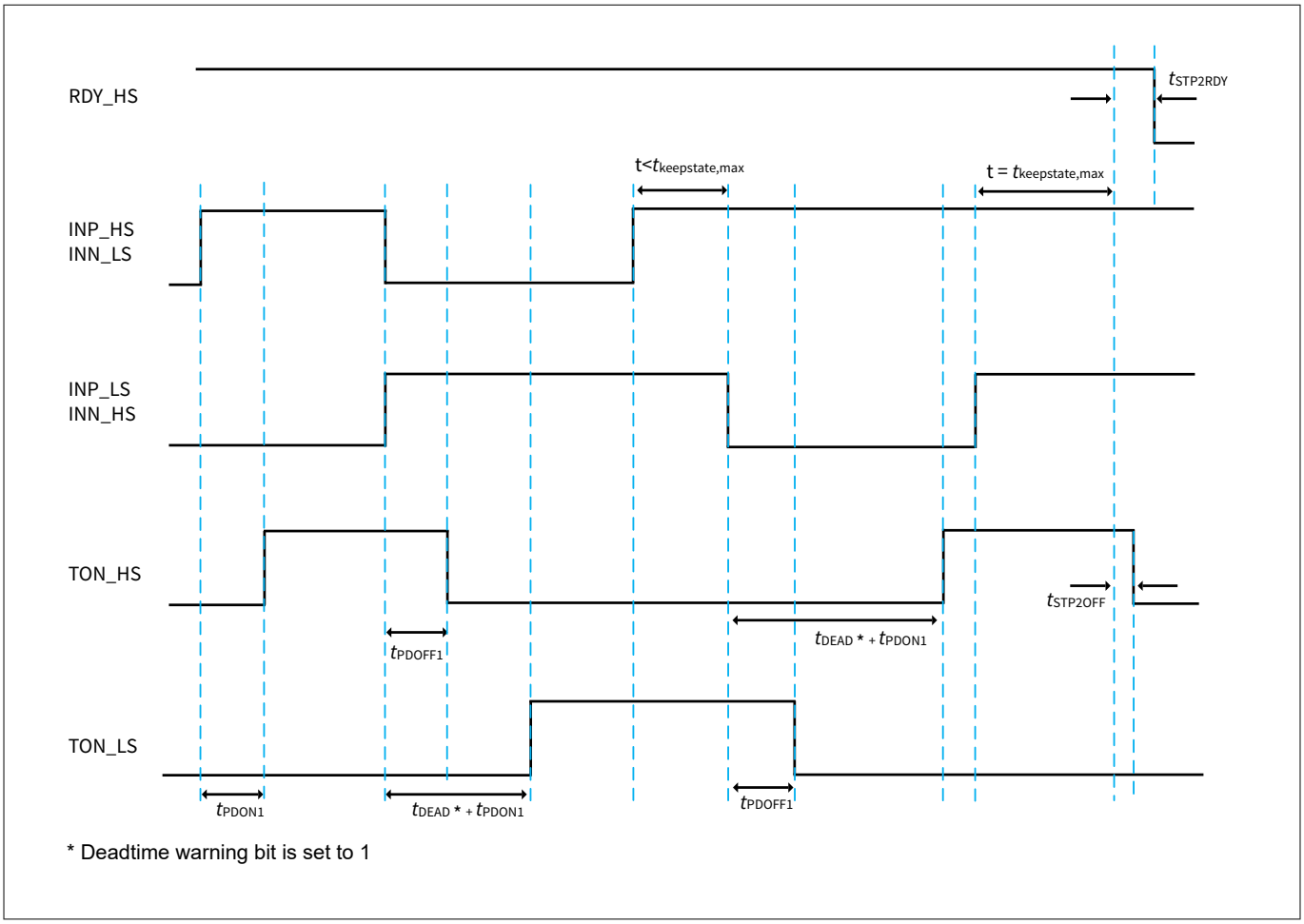

Figure 15 Shoot through protection timing diagram

11.2 Electrical characteristics STP

Table 15 Electrical characteristics STP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Dead time for shoot through protection	t_{DEAD3}	650	800	950	ns		PRQ-153
Keep state time limit	$t_{keepstate}$	3.3	3.5	3.7	µs		PRQ-598

(table continues...)

Table 15 (continued) Electrical characteristics STP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
STP keep error detection to notification time	$t_{STP2RDY}$	–	100	500	ns	VCC2 = typ., VEE2 = typ.	PRQ-723
STP keep error detection & reaction time	$t_{STP2OFF}$	–	100	500	ns	no C_{LOAD}, no R_{LOAD}, Start: $t_{keepstate}$ elapsed Stop: TON = V_{VCC2} - 1.5 V, VCC2 = typ., VEE2 = typ.	PRQ-724

12 Secondary Side input

The device offers the combined pin AIP/SASC on the secondary side to achieve two functionalities:

- Measuring analog system signals like temperature or voltages with an integrated current source
- Achieving the system safe state by pulling the output stage of the driver IC into static "high" condition

12.1 Analog-to-Digital Converter (ADC)

12.1.1 Functional description ADC

The device has an integrated 12 BIT Delta Sigma analog to digital converter.

The Delta-Sigma ADC can measure the following possible analog values inside the system:

- Measurement of NTC voltage when externally supplied by VCC2
- Measurement of on chip temperature diodes biased by internal current source
- Measurement of DC Link voltage when supplied from HV rail over resistor ladder.

The voltage signal VAIP is encoded and output as a PWM signal on the DATA pin on the primary side. The Total Unadjusted Error is the square sum of errors (INL, EROFF and ERGAIN).

The integrated ADC allows isolated temperature sensing by using an externally connected NTC.

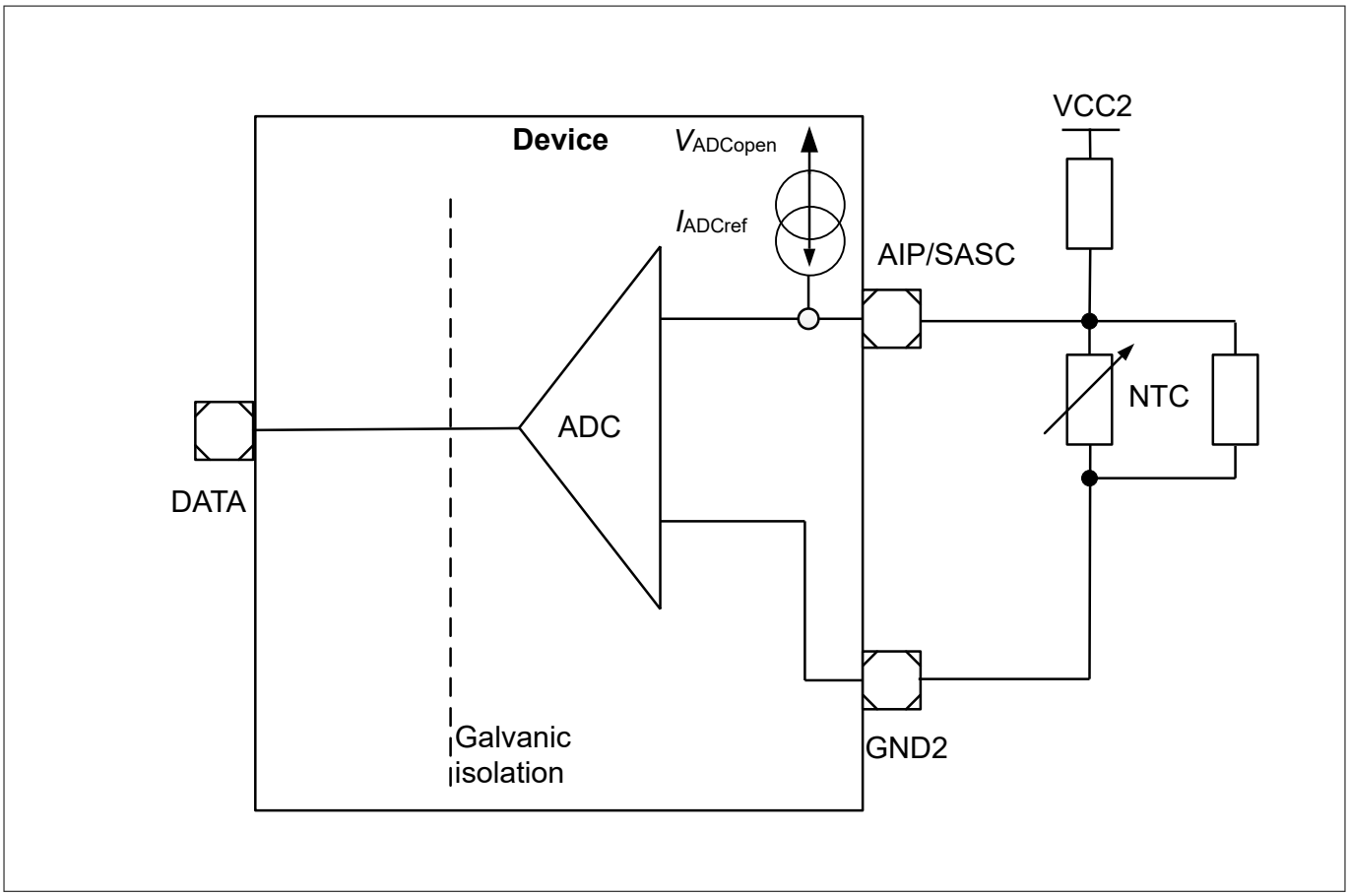

Figure 16 ADC application diagram with NTC.

The integrated ADC allows isolated temperature sensing. An internal current source I_{ADCref} is biasing an external thermal diode of the used power module.

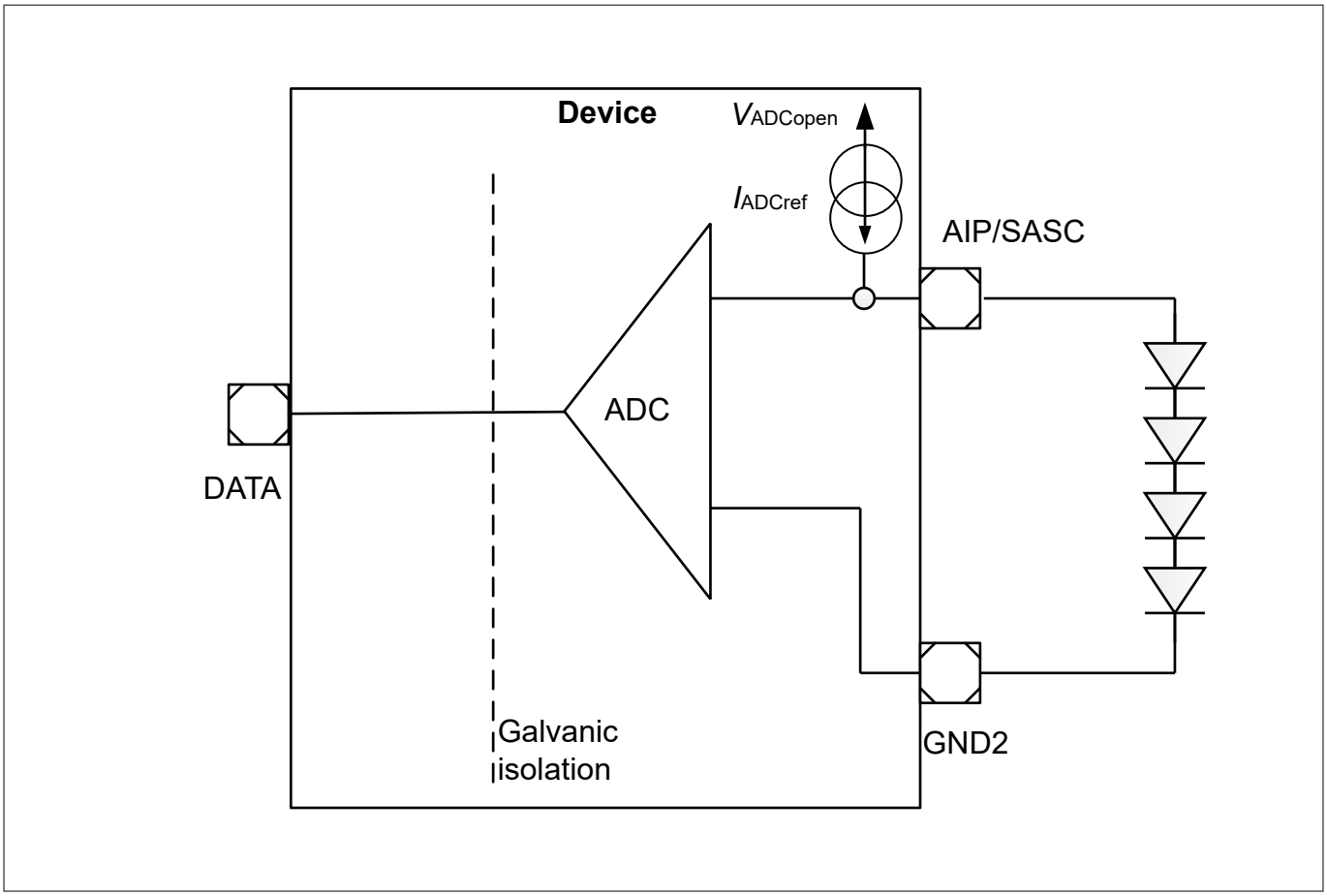

Figure 17 Temperature measurement diagram

The integrated ADC allows measuring the DC-link voltage by using an external resistor divider.

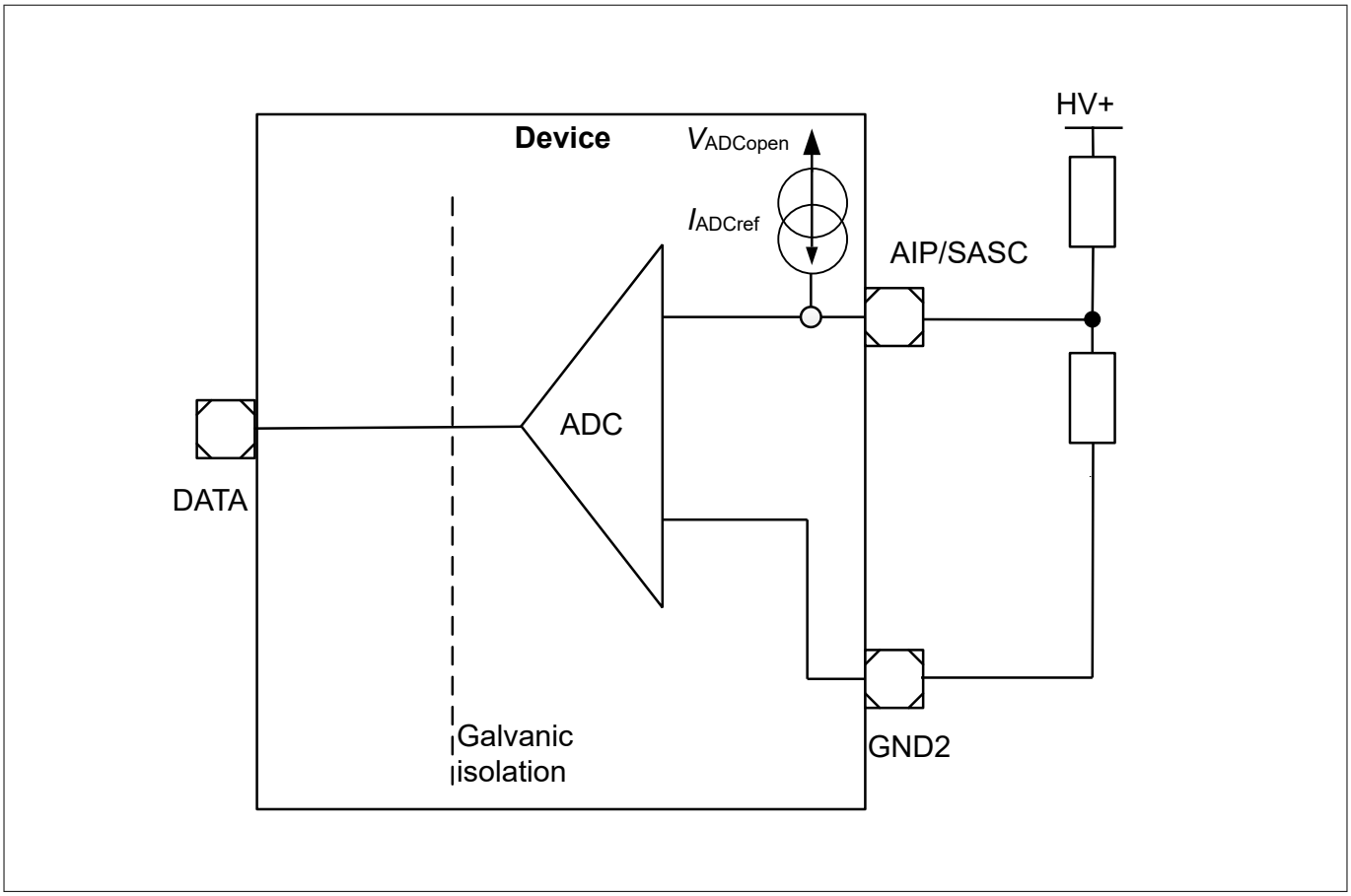

Figure 18 DC-link measurement diagram

***Note**: FS equals Full Scale Range*

12.1.2 Electrical characteristics ADC

Table 16 Electrical characteristics ADC

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC resolution	ADC_{res}	–	–	12	bit		PRQ-225
Ideal ADC input voltage full scale	V_{IADC}	–	3.5	–	V		PRQ-226
ADC pin open voltage	$V_{ADCopen}$	–	–	6.5	V	no load	PRQ-732
ADC Gain Error	ER_{GAIN}	-1.35	–	+1.35	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2 V	PRQ-227

(table continues...)

Table 16 (continued) Electrical characteristics ADC

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC Offset error	ER_{OFF}	-0.5	–	+0.35	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2 V	PRQ-739
ADC total error @trimming voltage	$TE_{@2V}$	-14	–	+21	mV	Refers to V_{IADC}, trimmed at V_{AIP} = 2 V	PRQ-228
ADC total error	TE	-35	–	+35	mV	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2 V	PRQ-740
ADC INL	INL	–	0.024	0.073	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2 V	PRQ-229
ADC DNL	DNL	–	0.007	0.025	%FS	Refers to V_{IADC}, valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2V	PRQ-230
ADC reference current @hot	I_{ADCref}	-205	-200	-195	µA	Valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2V, T_{amb} = 125°C	PRQ-231
ADC reference current @cold	I_{ADCref}	-206	-195	-186	µA	Valid for Input range V_{AIP} - V_{GND2} = 0.4 V...3.2 V, T_{amb} = -40°C	PRQ-232
ADC sample rate	f_{SAMPLE}	2.28	2.4	2.52	kHz	12 bit	PRQ-233

12.2 Secondary Active Short Circuit (SASC)

12.2.1 Functional description SASC

The device implements a secondary side ASC function which is driving TON = "high" in static condition.

Note: The SASC behavior for certain conditions/errors is stated in the table SASC Status at Failure Events/ Conditions.

In case SASC is active a warning Bit is set inside the diagnostic frame on DATA pin. If SASC is deactivated the warning bit is self-cleared after it was transmitted via the diagnostic frame once.

Table 17 TON/TOFF Status if SASC "high" at Failure Events

Condition/Error	TON/TOFF if SASC = "high"
Primary chip is not ready	TON ="high"
STP Keep Error Event	TON = "high"
UVLO1, OVLO2, UVLO3, OVLO3 Error Event	TON = "high"

(table continues...)

Table 17 (continued) TON/TOFF Status if SASC "high" at Failure Events

Life sign error	TON = "high"
OCP Error Event	Safe turn-off
Gate Monitoring Error Event	Safe turn-off
Output Stage Monitoring Error Event	Tristate
UVLO2, Sec. Internal Supervision Error Event	TON = "low"

In case the output stage is switched to "low" or to tristate due to an error the output stage can be reactivated via SASC:

- decrease the voltage below V_{SASCL} for at least t_{SASC}
- wait t_{SASC_retry}
- increase the voltage above V_{SASCH}

Note: The error event needs to disappear to reactivate SASC.

12.2.2 Electrical characteristics SASC

Table 18 Electrical characteristics SASC

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SASC ON delay	t_{SASC}	400	–	550	ns	$V_{SASC\_Overdrive}$ = 200 mV, TON = V_{VEE2} + 1.5 V, Slew Rate = 50 V/µs, C_{LOAD_TON} = no load, no resistive load	PRQ-238
SASC input voltage range	V_{SASC}	0	–	V_{VCC2}	V	Referenced to GND2	PRQ-239
SASC pin high input voltage	V_{SASCH}	8.6	9	-	V	$V_{VCC2} \geq V_{SASCOFF}$, referenced to GND2	PRQ-240
SASC pin low input voltage	V_{SASCL}	-	-	6.5	V	$V_{VCC2} \geq V_{SASCOFF}$, referenced to GND2	PRQ-241
SASC input current	$I_{SASCHcurrent}$	50	100	120	µA	V_{ASCH} = 15 V	PRQ-242
SASC minimum operating voltage	$V_{SASCOFF}$	V_{UVLO2H}	–	–	V	Referenced to GND2, $V_{SASC} = V_{VCC2}$	PRQ-244
Minimum SASC pulse width	$t_{SASCmin}$	150	–	–	ns		PRQ-246

(table continues...)

Table 18 (continued) Electrical characteristics SASC

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Reactivation time after error event during SASC	t_{SASC_retry}	29.4	31	32.6	µs		PRQ-672

13 DATA readout

13.1 Functional description DATA

The DATA output pin on the primary side is reflecting either the ADC result, the diagnostic frame 0 or the diagnostic frame 1 in an alternating scheme.

The output frame is defined by following scheme:

ADC frame - diagnostic frame 0 - ADC frame - diagnostic frame 1

This scheme is repeated independent from operation mode or error condition.

Exceptions:

- In case of Primary_Init mode the DATA output is pulled to "low".
- In case no valid ADC signal is transferred from secondary side to primary side the ADC frame is skipped.

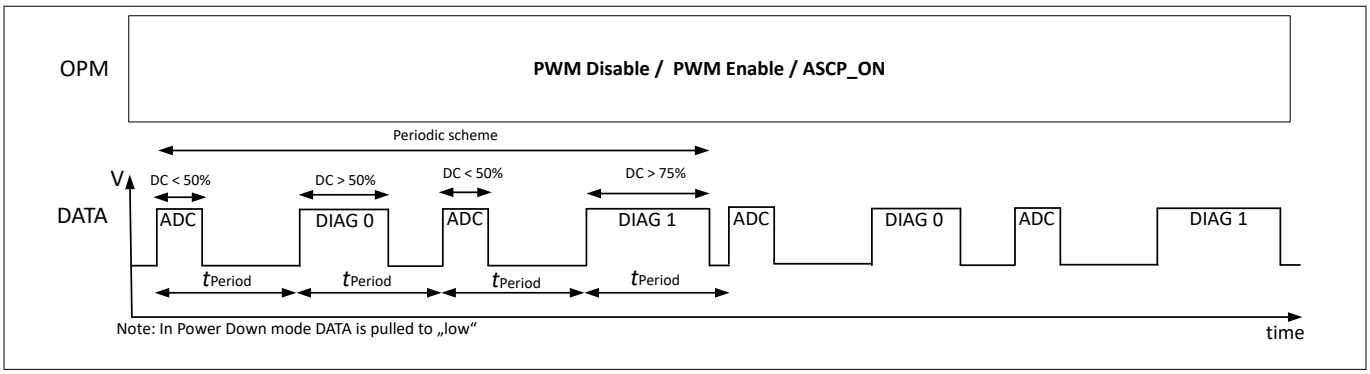

Figure 19 Alternating ADC and diagnosis readout at DATA

The 12 bit ADC DATA output is a pulse width modulated signal with an update rate with defined period of t_{Period}.

The duty cycle of 12 bit ADC output on DATA remains always in the range of D_{ADC} regardless of the ADC input.

The diagnostic functionality is split into two 13 BIT diagnostic frames.

Following diagnostic results are reported in diagnostic frame 0:

- No life sign established
- OVLO2 error
- UVLO2 error
- OVLO3 error
- UVLO3 error
- Bipolar detection warning
- SASC activation warning

Following diagnostic results are reported in diagnostic frame 1:

- Dead time warning
- STP keep error
- Output stage monitoring error
- Gate monitoring error
- Overcurrent protection error
- Overcurrent protection built-in-self-test warning
- SASC activation warning

The 13 bit diagnostic frame is pulse width modulated to a signal with a period of t_{Period}.

The duty cycle of the diagnostic frame on DATA pin always remains in the range of D_{Diag} regardless of the diagnostic status.

Note:

- *0% duty cycle means primary side is not ready. The DATA pin weak pull down to GND1 is active.*
- *100% duty cycle is not possible at DATA pin.*

Table 19 Diagnostic frame 0 readout at DATA pin

Bit_x	Description	Value	Duty-cycle
BIT0	0: reserved	1	0.01%
BIT 1	0: reserved	2	0.02%
BIT 2	0: reserved	4	0.05%
BIT 3	1: reserved	8	0.09%
BIT 4	1: No life sign established	16	0.20%
BIT 5	1: OVLO2 error	32	0.39%
BIT 6	1: UVLO2 error	64	0.78%
BIT 7	1: OVLO3 error	128	1.56%
BIT 8	1: UVLO3 error	256	3.13%
BIT 9	1: Bipolar detection warning	512	6.25%
BIT 10	1: SASC activation warning	1024	12.50%
BIT 11	0: Diagnosis frame 0	2048	25.00%
BIT 12	0: ADC 1: Diagnosis frame	4096	50.00%

Table 20 Diagnostic frame 1 readout at DATA pin

Bit_x	Description	Value	Duty-cycle
BIT0	0: reserved	1	0.01%
BIT 1	0: reserved	2	0.02%
BIT 2	0: reserved	4	0.05%
BIT 3	1: reserved	8	0.09%
BIT 4	1: Dead time warning	16	0.20%
BIT 5	1: STP keep error	32	0.39%
BIT 6	1: Output stage monitoring error	64	0.78%
BIT 7	1: Gate monitoring error	128	1.56%
BIT 8	1: Overcurrent protection error	256	3.13%
BIT 9	1: No Overcurrent protection BIST warning	512	6.25%
BIT 10	1: SASC activation warning	1024	12.50%
BIT 11	1: Diagnosis frame 1	2048	25.00%
BIT 12	0: ADC 1: Diagnosis frame	4096	50.00%

***Note**: In case the primary chip is not ready the duty cycle of diagnosis readout is internally pulled down to "low".*

The duty cycle for diagnostic readout of diagnosis frame 0 and diagnosis frame 1 can be calculated using the following formula:

$$DC = \frac{\sum_0^{12}(BIT_n \times 2^n)}{2^{13}}$$

Figure 20

13.2 Electrical characteristics DATA

Table 21 Electrical characteristics DATA

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ADC DATA duty cycle range	D_{ADC}	0.19	–	49.91	%	No life sign lost, no primary reset	PRQ-286
Diagnostic duty cycle range	D_{Diag}	50.1	–	99.9	%		PRQ-287
DATA period	t_{Period}	194.6	204.8	215	µs		PRQ-288
DATA output low level	$V_{DATA,output(low)}$	–	0	0.5	V	$V_{VCC1} \geq 3.0$ V, $\lvert I_{load} \rvert = 5$ mA	PRQ-290
DATA output high level	$V_{DATA,output(high)}$	V_{VCC1} - 0.5	V_{VCC1}	–	V	$V_{VCC1} \geq 3.0$ V, $\lvert I_{load} \rvert = 5$ mA	PRQ-291

14 Overcurrent Protection (OCP)

14.1 Functional description OCP protection

The device offers a short circuit protection pin. It monitors the voltage difference between OCP pin and GND2 in case TON = "high" after the OCP blanking time t_{OCPBT} is elapsed.

If the threshold level V_{OCP} is reached, it issues a safe turn off within $t_{OCP2SOFTOFF}$.

It changes its state into PWM Disable mode and signals the error by pulling NFLT to "low" within $t_{OCP2NFLT}$.

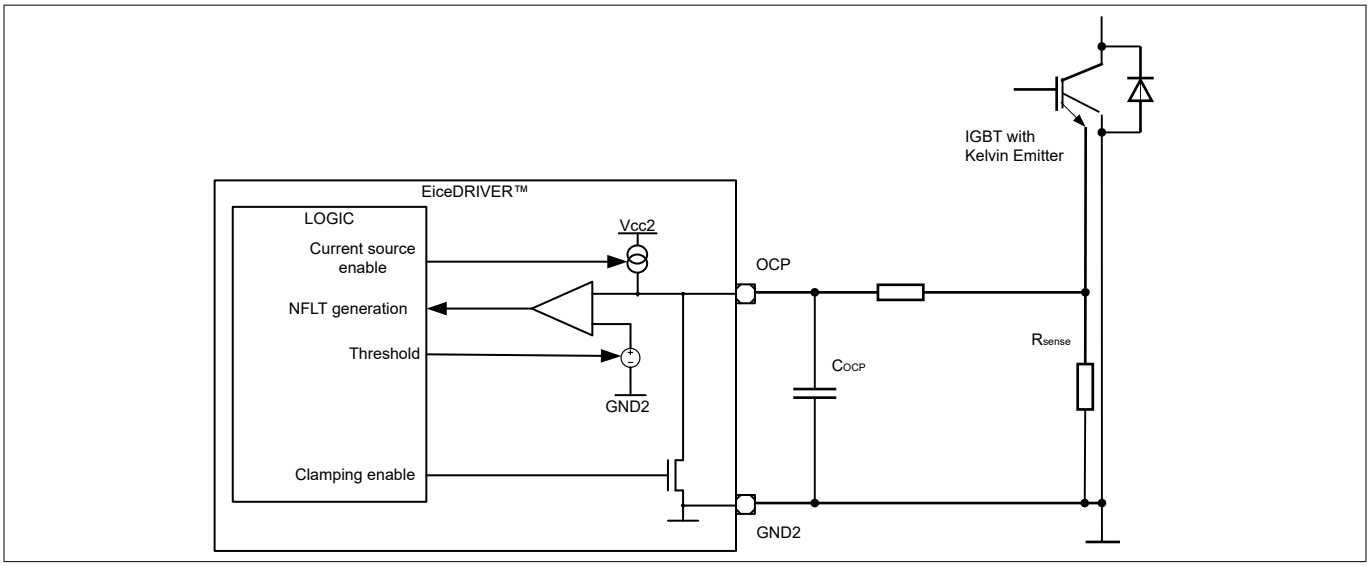

Figure 21 OCP application schematic

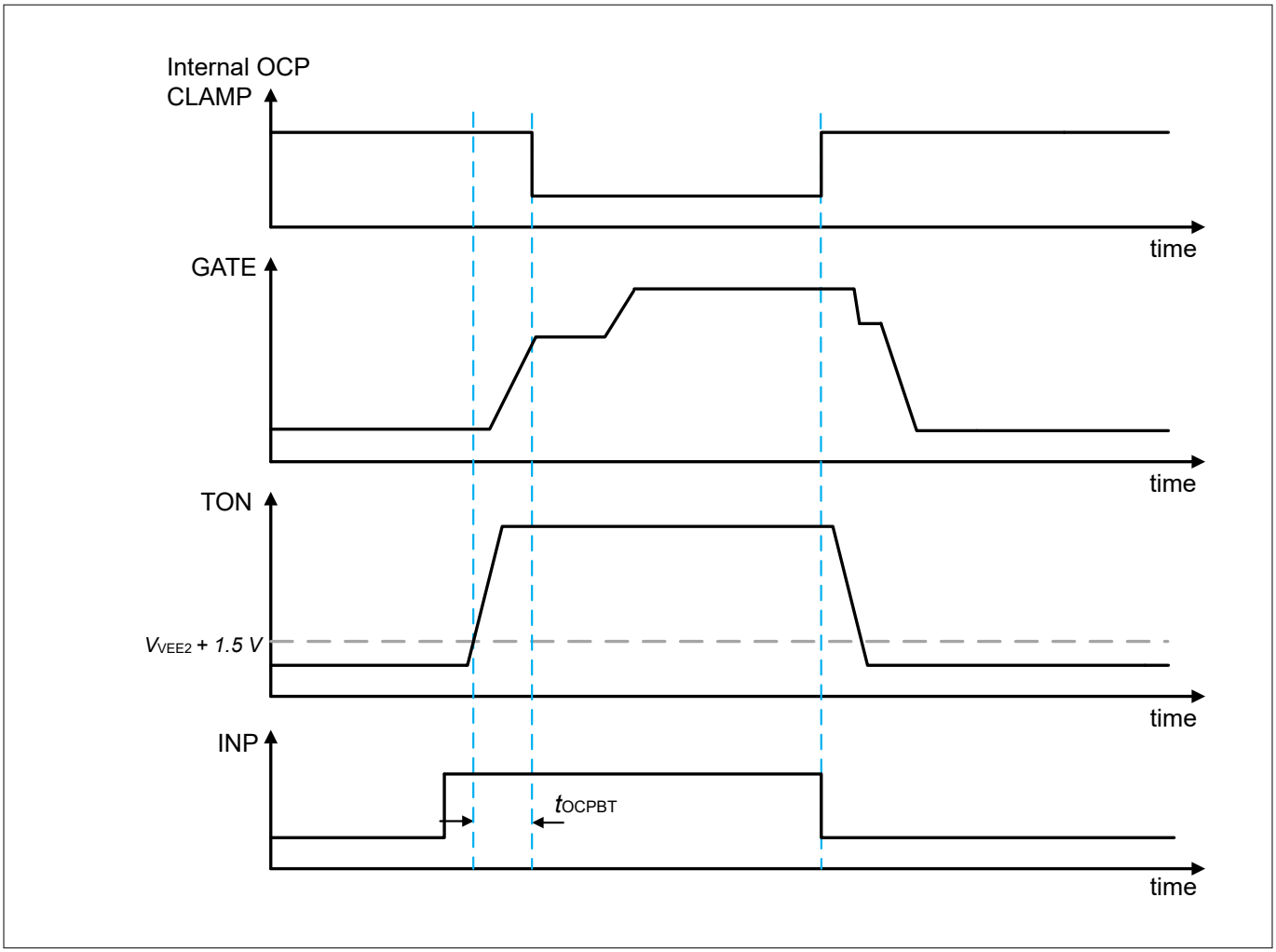

Figure 22 OCP blanking time

14.2 Functional description OCP BIST

The device has an built in self test to supervise the OCP functionality.

The OCP built in self test is executed whenever V_{VCC2} exceeds $V_{UVLO2Hx}$ after an UVLO2 was raised.

The OCP built in self test consists of two phases that need to succeed collectively.

In the first phase the pin connection to external components is checked, by deactivating the internal clamp for up to $t_{OCP\_BIST\_CLAMP}$ or until the internal threshold comparator is triggered.

The first phase succeeds when the internal threshold comparator is not triggered, indicating an intact connection of the pin to the external circuit.

In the second phase an artificial OCP event is generated once internally, in order to monitor the functionality of the threshold comparator.

Phase one and two of the OCP built in self test are processed internally for up to t_{OCP_BIST}.

The OCP BIST result is stored inside the No Overcurrent protection BIST warning bit, which is shown in the DATA diagnostics frame.

In case the OCP BIST succeeded without errors the No Overcurrent protection BIST warning bit is switched to "1".

This bit is latched and cannot be cleared via valid clear signal.

In case the OCP BIST did not succeed, the No Overcurrent protection BIST warning bit inside the DATA diagnostics frame stays "0".

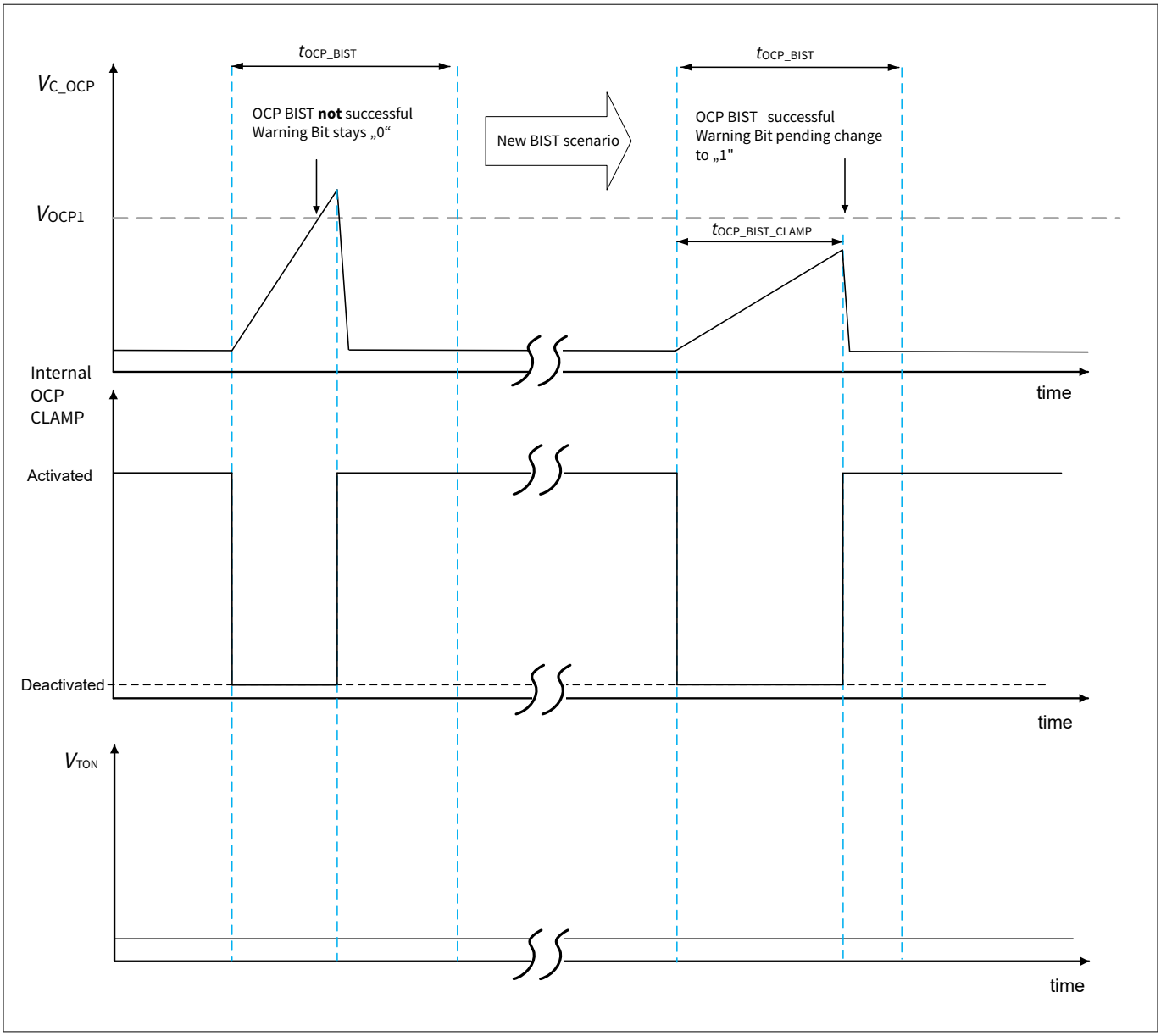

Figure 23 OCP BIST detailed timing diagram

14.3 Electrical characteristics OCP

Table 22 Electrical characteristics OCP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent error detection threshold	V_{OCP1}	970	1000	1040	mV	V_{OCP}-V_{GND2}	PRQ-132

(table continues...)

Table 22 (continued) Electrical characteristics OCP

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP current source	I_{OCPCS}	-550	-500	-450	µA		PRQ-134
OCP input voltage range	V_{OCP}	GND2	–	VCC2	V	referring to GND2	PRQ-135
OCP detection & reaction time	$t_{OCP2SOFTOFF}$	-	120	170	ns	$V_{OCP\_Overdrive}$ = 200 mV, slew rate = 100 mV/ns, TON = V_{VCC2} - 1.5 V, after OCP blanking time elapsed, $C_{LOAD\_TON/TOFF}$ = no load, no resistive load	PRQ-136
OCP blanking time	t_{OCPBT}	235	260	305	ns	From TON = V_{EE2} + 1.5V to release of clamping transistor	PRQ-137
OCP BIST timer	t_{OCP_BIST}	9.5	10	10.5	µs	Start: V_{VCC2} > $V_{UVLO2Hx}$ after device is powered-up and V_{VCC2} = 8 V	PRQ-667
OCP BIST clamp release timer	$t_{OCP\_BIST\_CLAMP}$	8	–	–	µs	Start: V_{VCC2} > $V_{UVLO2Hx}$ after device is powered-up and V_{VCC2} = 8 V Stop: OCP clamp activated	PRQ-722

15 Soft turn off

15.1 Functional description soft turn off

The soft turn off functionality ensures a safe turn off in case of an emergency to prevent high voltage overshoots on the power semiconductor.

The activation of the SOFTOFF pin is described as a safe turn off.

The safe turn off functionality is executed when following failures appear in the system and are recognized by the device :

- Overcurrent protection
- Gatemonitoring error

In case of an error, the safe turn off functionality is activated, TON and TOFF is tri-stated and the power semiconductor safe turn off is done using the SOFTOFF pin.

The safe turn off function via SOFTOFF is deactivated if V_{GATE} undershoots V_{CLAMP} .

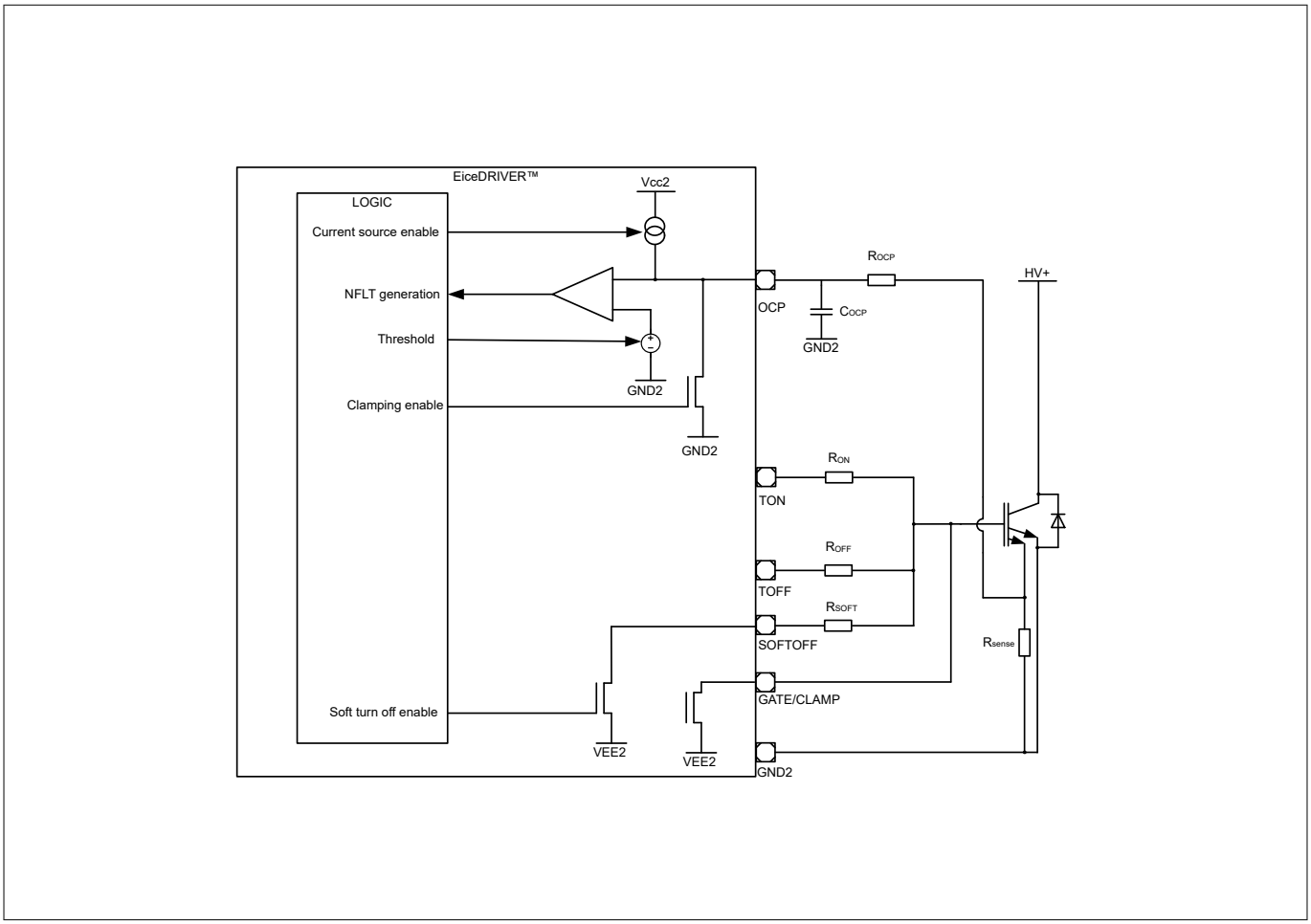

Figure 24 Softoff application schematic

The soft turn off is activated when *VOCP* is reached. The timing between exceeding *VOCP* and the voltage on SOFTOFF reached VCC2 - 1.5V is defined as $t_{OCP2SOFTOFF}$.

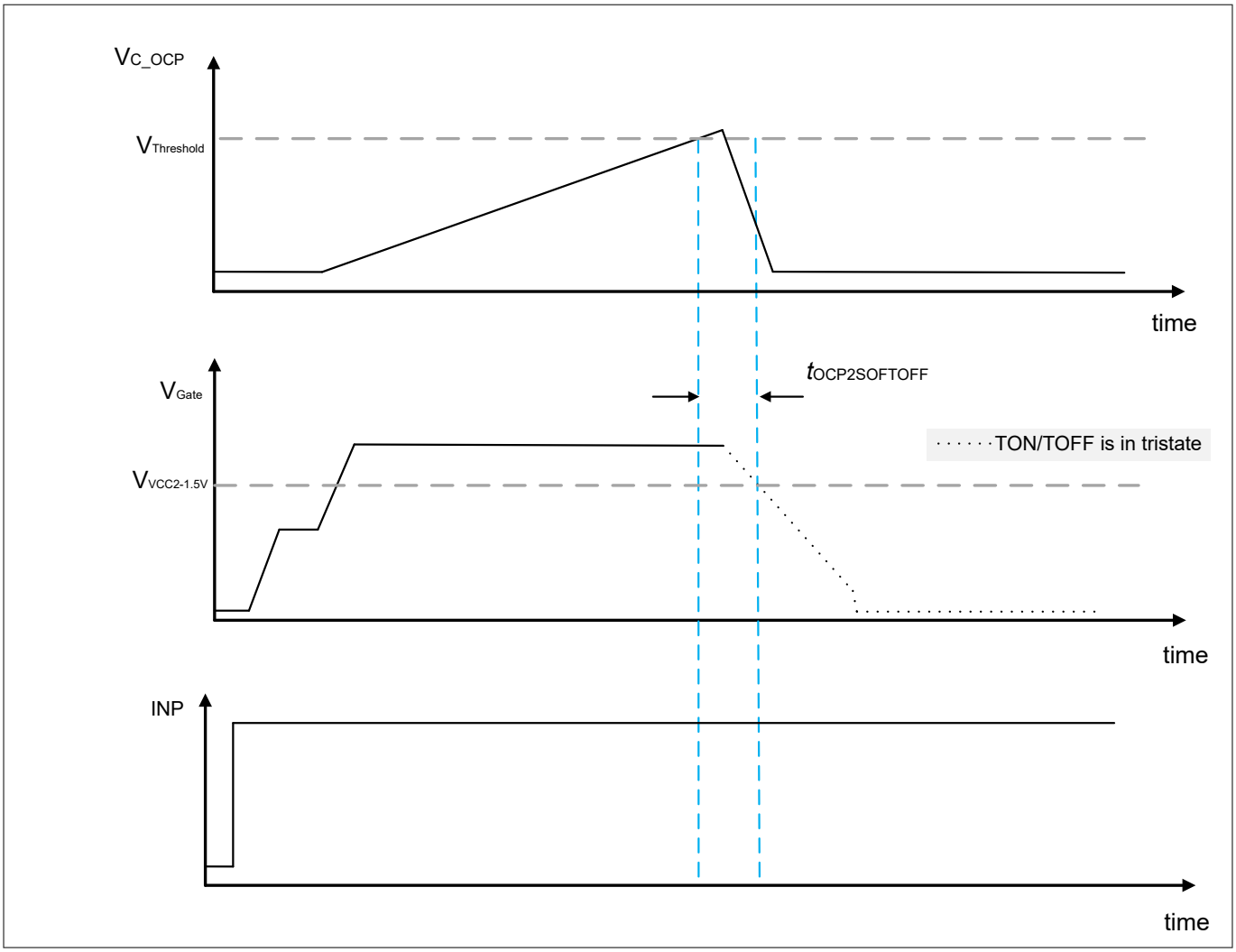

Figure 25 OCP to soft turn off diagram

15.2 Electrical characteristics soft turn off

Table 23 Electrical characteristics soft turn off

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Lowside Rdson	$R_{DSON\_SOFTOFF}$	–	1.5	3	Ω	$V_{INP} = V_{GND1}$, $V_{SI1} = V_{SI2} = V_{VCC1}$, $V_{TOFF} = V_{VEE2}$, $V_{TON} = V_{VEE2}$, $V_{CLAMP/GATE} = V_{VEE2}$, V_{VCC2} = 15 V, V_{VEE2} = -5 V, $V_{SOFTOFF} = V_{VEE2}$ + 0.2V	PRQ-544

(table continues...)

Table 23 (continued) Electrical characteristics soft turn off

T_J = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Soft turn off fall time	$t_{Fall-SOFTOFF}$	–	–	25	ns	no C_{LOAD}, no R_{LOAD} Start: SOFTOFF falling edge at $V_{SOFTOFF}$ = V_{VCC2} -1.5 V, Stop: SOFTOFF falling edge at $V_{SOFTOFF}$ = V_{VEE2} + 1.5 V, VCC2 = typ., VCC1 = typ., VEE2 = typ.	PRQ-652

16 Gate monitoring

The gate monitoring functionality checks the correct state of V_{GATE} at pin GATE/CLAMP against signal $V_{TON/TOFF}$ during t_{GMBT}. If a mismatch is detected the device issues a safe turn-off in less than t_{GM-DaR} and changes to PWM Disable mode and RDY is pulled to "low" within t_{RDY_GM}.

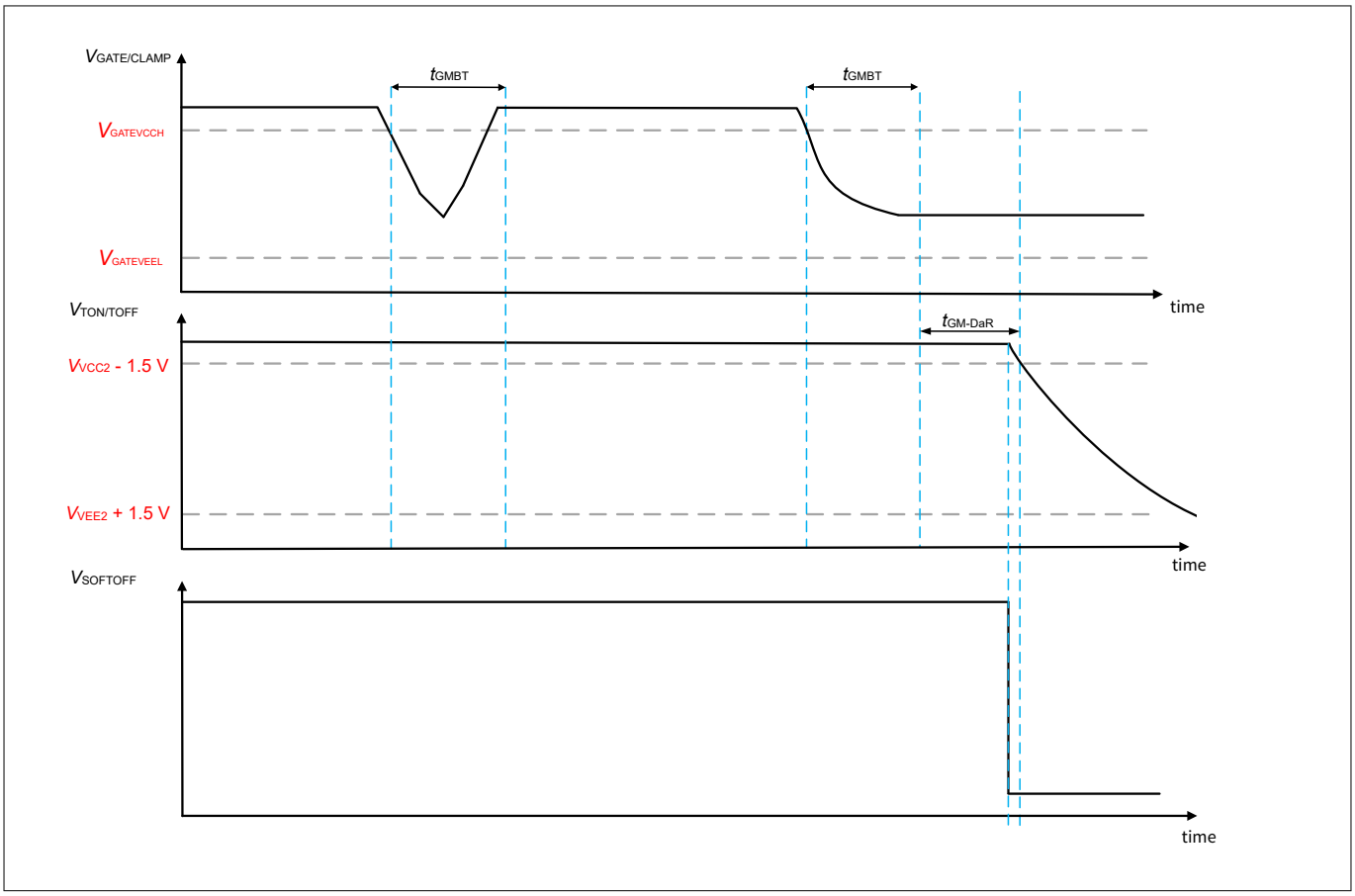

Figure 26 Static gate monitoring timing diagram

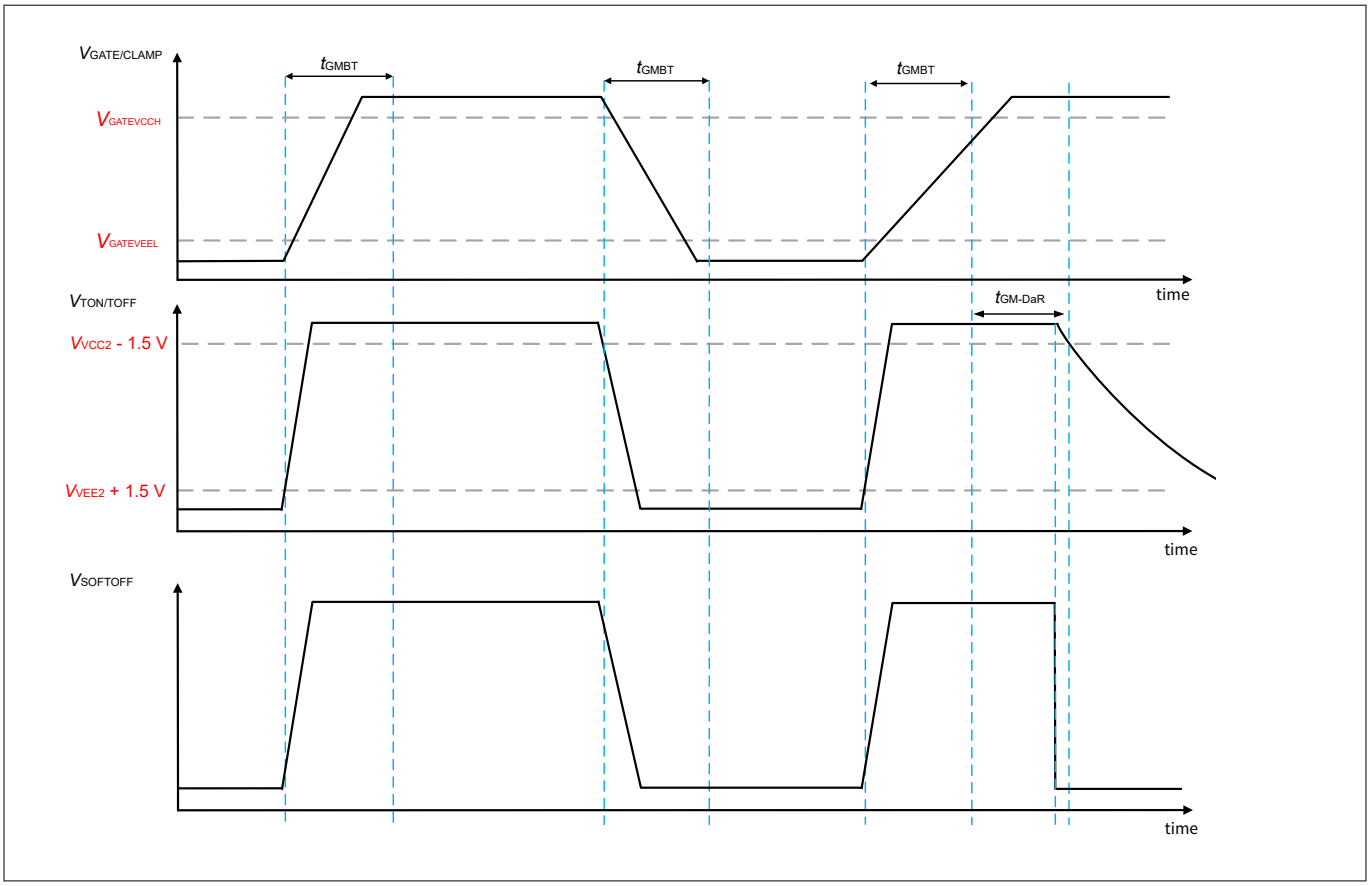

Figure 27 Dynamic gate monitoring timing diagram

16.1 Electrical characteristics gate monitoring

Table 24 Electrical characteristics gate monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring detection and reaction time	t_{GM-DaR}	200	350	560	ns	VCC2 = typ., VEE2 = typ.	PRQ-185
Gate monitoring detection and notification time	t_{RDY_GM}	–	1.5	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-186

(table continues...)

Table 24 (continued) Electrical characteristics gate monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate monitoring blanking time	t_{GMBT3}	6.99	7.7	8.4	µs	VEE2 = typ., VCC2 = typ.	PRQ-737
Gate monitoring VCC2 voltage threshold high level	$V_{GATEVCCH}$	V_{VCC2} - 2.3	V_{VCC2} - 2.1	V_{VCC2} - 1.9	V	t_{GMBT} is active	PRQ-199
Gate monitoring VCC2 voltage threshold low level	$V_{GATEVCCL}$	V_{VCC2} - 3.2	V_{VCC2} - 3	V_{VCC2} - 2.8	V	t_{GMBT} is active	PRQ-200
Gate monitoring VEE2 voltage threshold high level	$V_{GATEVEEH}$	V_{VEE2} + 2.8	V_{VEE2} + 3	V_{VEE2} + 3.2	V	t_{GMBT} is active	PRQ-201
Gate monitoring VEE2 voltage threshold low level	$V_{GATEVEEL}$	V_{VEE2} + 1.9	V_{VEE2} + 2.1	V_{VEE2} + 2.3	V	t_{GMBT} is active	PRQ-202

17 Output stage monitoring

The output stage monitoring function monitors if the measured TON/TOFF signal is following the input control signals within $t_{OSM-CPL}$.
If a mismatch is detected the device switches TON/TOFF into tri-state in less than $t_{OUTM-TRI}$ and changes to PWM Disable mode. RDY is pulled to "low" within t_{RDY_OSM}.

The TON/TOFF can be controlled from:

- The primary side PWM input INP and INN
- The primary side safety inputs SI1 and SI2
- The secondary side SASC input

In case the output stage monitoring functionality detects a failure it tri-states the output stage. After t_{OSM_retry} the tri-state of TON/TOFF is released and the device switches the output stage to "low". In case another output stage monitoring error is detected the t_{OSM_retry} timer starts again.

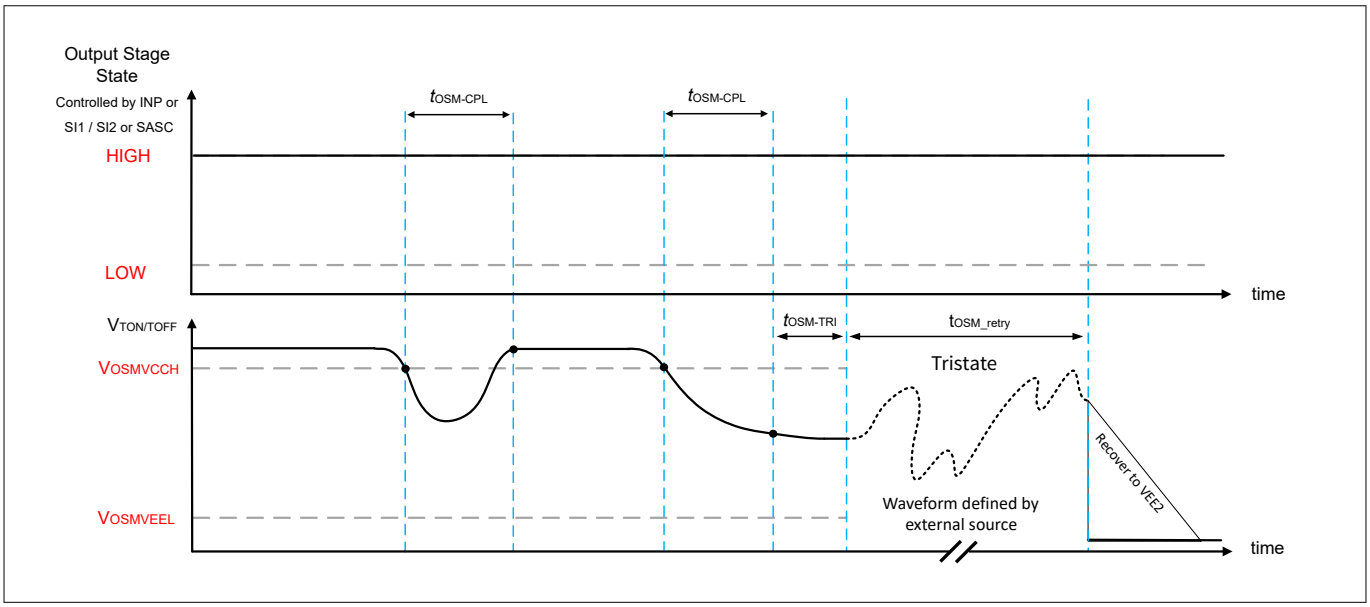

Figure 28 Static output stage monitoring timing diagram

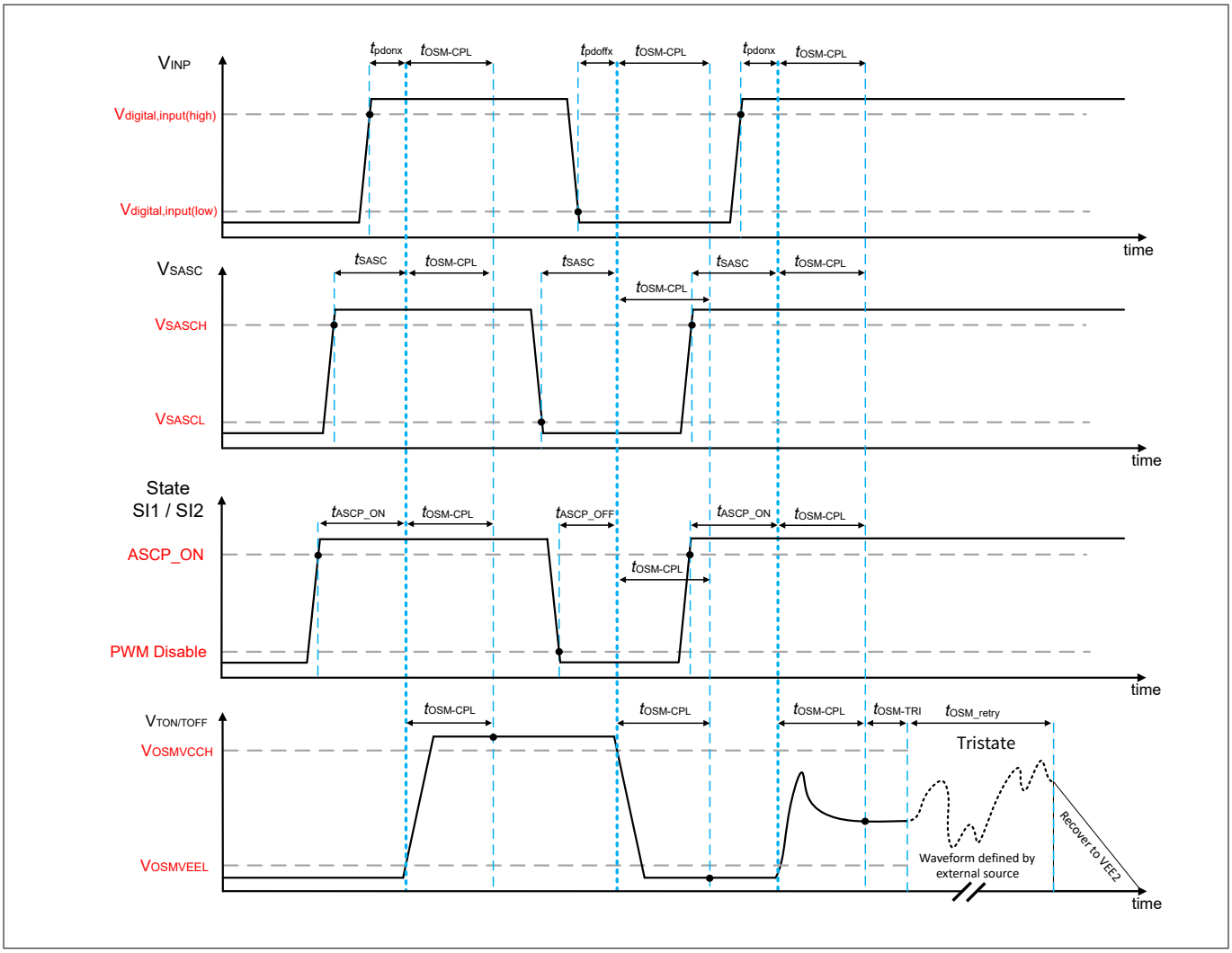

Figure 29 Dynamic output stage monitoring

17.1 Electrical characteristics output stage monitoring

Table 25 Electrical characteristics output stage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output stage monitoring detection to tri-state time	$t_{OSM-TRI}$	200	350	1000	ns	VCC2 = typ., VEE2 = typ.	PRQ-204

(table continues...)

Table 25 (continued) Electrical characteristics output stage monitoring

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output stage monitoring detection and notification time	t_{RDY_OSM}	–	1.5	2.5	µs	VCC2 = typ., VEE2 = typ.	PRQ-205
Output stage monitoring compliance time	$t_{OSM-CPL}$	600	950	1200	ns	VEE2 = typ., VCC2 = typ.	PRQ-208
Output stage monitoring retry time	t_{OSM_retry}	195	205	215	µs	VEE2 = typ., VCC2 = typ.	PRQ-211
Output stage monitoring VCC2 voltage threshold high level	$V_{OSMVCCH}$	V_{VCC2} - 2.3	V_{VCC2} - 2.1	V_{VCC2} - 1.9	V	$t_{OSM-CPL}$ is active	PRQ-212
Output stage monitoring VCC2 voltage threshold low level	$V_{OSMVCCL}$	V_{VCC2} - 3.2	V_{VCC2} - 3	V_{VCC2} - 2.8	V	$t_{OSM-CPL}$ is active	PRQ-213
Output stage monitoring VEE2 voltage threshold high level	$V_{OSMVEEH}$	V_{VEE2} + 2.8	V_{VEE2} + 3	V_{VEE2} + 3.2	V	$t_{OSM-CPL}$ is active	PRQ-214
Output stage monitoring VEE2 voltage threshold low level	$V_{OSMVEEL}$	V_{VEE2} + 1.9	V_{VEE2} + 2.1	V_{VEE2} + 2.3	V	$t_{OSM-CPL}$ is active	PRQ-215

18 Active Miller clamp

The internal clamping structure to VEE2 is activated if the voltage on GATE/CLAMP crosses V_{CLAMP} during turn-off sequence.

The internal clamping structure to VEE2 is deactivated if the INP signal is switched to "high".

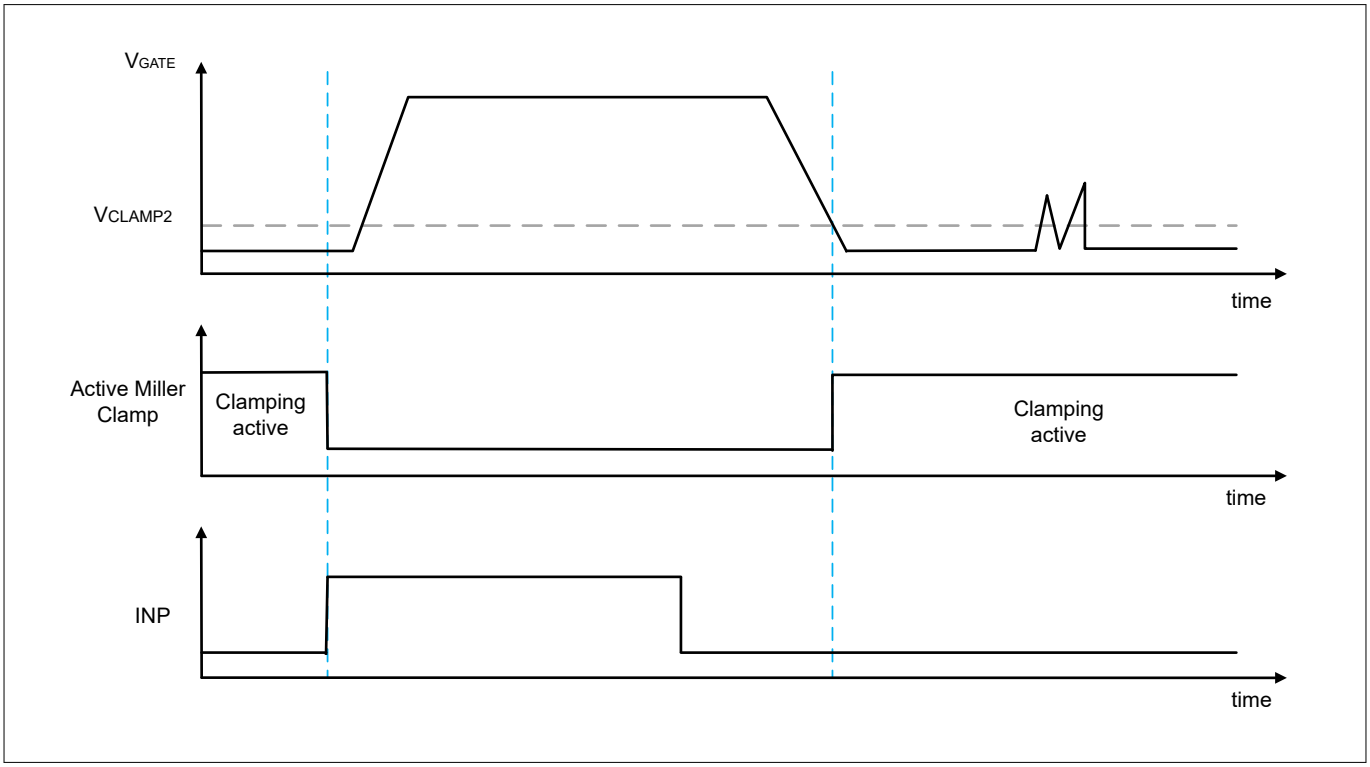

Figure 30 Active Miller clamp timing diagram.

***Note**: In a half bridge configuration the switched off power switch tends to dynamically turn on during the turn on phase of the opposite power switch. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore, in many applications the use of a negative supply voltage can be avoided.*

18.1 Electrical characteristics Active Miller clamp

Table 26 Electrical characteristics Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level clamp peak current	I_{CLAMPL}	3	4	–	A	INP = V_{GND1}, INN = V_{GND1}, SI1 = SI2 = V_{VCC1}, TOFF = falling edge to V_{VEE2}, VCC2 = 15 V, VEE2 = -5 V, C_{LOAD}= 1 µF	PRQ-217
CLAMP/GATE voltage	$V_{CLAMP/GATE}$	V_{VEE2}	–	V_{VCC2}	V	Referenced to GND2, no load	PRQ-218

(table continues...)

Table 26 (continued) Electrical characteristics Active Miller clamp

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CLAMP threshold voltage	V_{CLAMP2}	V_{VEE2} + 1.9	V_{VEE2} + 2.1	V_{VEE2} + 2.3	V	Voltage is related to GND2	PRQ-585
CLAMP RDSON	$R_{DSON-CLAMP}$	0.1	–	0.5	Ω	Voltage drop $V_{GATE/CLAMP}$ - V_{VEE2} < 1 V	PRQ-219

19 Passive clamping

If the secondary chip is not supplied, the pin GATE/CLAMP is passively clamped to VEE2.

19.1 Electrical characteristics passive clamping

Table 27 Electrical characteristics passive clamping

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GATE passive clamping voltage (ICLAMP = 10 mA)	V_{PCLPG1}	–	–	V_{VEE2} + 2 V	V	Secondary chip not supplied (VCC2 floating, VEE2 = 0 V), I_{Clamp} = 10 mA	PRQ-221

20 Short circuit clamping

The short circuit clamping diodes ensure in case of a short circuit that the voltage on GATE will not exceed $V_{VCC2} + V_{fSC}$.

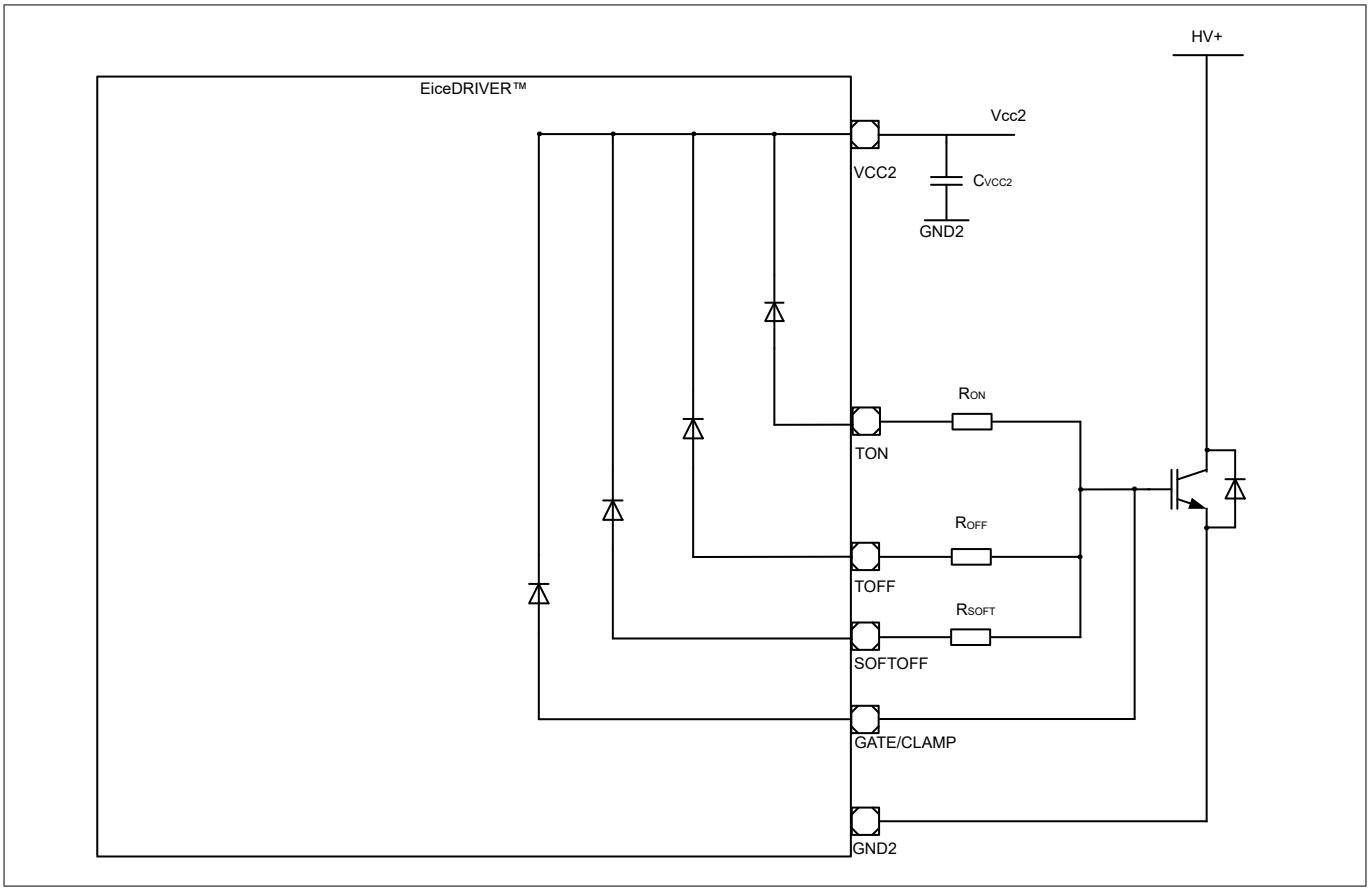

Figure 31 Internal short circuit clamping diodes

20.1 Electrical characteristics short circuit clamping

Table 28 Electrical characteristics short circuit clamping

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Short circuit clamping voltage	V_{fSC}	–	–	2	V	Current in GATE/CLAMP / TON / TOFF / SOFTOFF = 2 A, t_{max} = 3 µs	PRQ-596

21 Ready (RDY)

The RDY pin reports whether the device is ready. It needs to be connected to an external pull-up resistor.
All RDY-related errors are described in the Functional description of RDY error.
In case the primary die is not supplied RDY Pin is pulled to GND1 with an internal passive clamping transistor.

21.1 Electrical characteristics RDY

Table 29 Electrical characteristics RDY

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).
Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDY open drain output low level	$V_{RDY(low)}$	–	–	0.1	V	$V_{VCC1} \geq 3.0$ V, I_{load} = 500µA	PRQ-252
RDY output low passive clamping	$V_{RDYCLAMP}$	–	0.5	1	V	$I_{RDYCLAMP}$ = 500 µA, V_{CC1} = floating, all I/O = floating	PRQ-253
Power up timing primary	t_{PUprim}	–	100	1500	µs	Time from UVLO1 release to device operable, secondary chip running	PRQ-254
Power up timing secondary	t_{PUsec}	–	100	1500	µs	Time from UVLO2 release to device operable, primary chip running	PRQ-255

22 Fault (NFLT)

22.1 Functional description NFLT

NFLT reports short circuit events. The pin is active "low".

If the device switches into safe turn off of the output stage due to an OCP event, it goes to PWM Disable mode and signals the event on pin NFLT by changing NFLT to "low". The $t_{OCP2NFLT}$ time is defining the time from the detection of an OCP event until the notification on NFLT.

The device keeps the fault signal available unless a clear event takes place.

22.2 Electrical characteristics NFLT

Table 30 Electrical characteristics NFLT

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Voltage supply inputs (V_{VCC1}, V_{VCC2} and V_{VEE2}) are within the functional range (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OCP event detection to NFLT activation	$t_{OCP2NFLT}$	–	1.2	2.3	µs	$V_{OCP\_Overdrive}$= +/-200 mV, slew rate = 100 mV/ns, NFLT = 90%, R_{PU_NFLT} = 1 kΩ	PRQ-260
NFLT open drain output low level	V_{NFLT}	–	–	0.5	V	V_{VCC1} ≥ 3.0 V; $\|I_{NFLT}\|$ = 5 mA	PRQ-262

23 Application information

The following figure describes how the IC is used in its environment.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

- Please contact Infineon for additional supportive documentation.
- For further information you may contact http://www.infineon.com/

Note: This figure is a simplified example of an application circuit. The function must be verified in the application.

The external component values are specified as typical values in a typical application. Deviation of the nominal values are specified as min or max values, if applicable. Unless otherwise specified the deviation for external components are:

- Resistor: ±10 %
- Capacitor: -50 % ... +30 %

Table 31 Electrical characteristics external components

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Decoupling capacitance (between VCC1 and GND1)	C_{VCC1}	0.55	1.1	–	µF	Total capacitance refers to 1 µF capacitance + 0.1 µF close to the device. Max value depends on t_{RP1}.	PRQ-292
INP resistance	R_{INP}	–	1	–	kΩ	Value must fit to application	PRQ-296
INN resistance	R_{INN}	–	1	–	kΩ	Value must fit to application	PRQ-621
DATA resistance	R_{DATA}	–	1	–	kΩ	Value must fit to application	PRQ-622
Pull-up resistance	R_{pullup}	–	10	–	kΩ	Min value depends on I_{OUTx_MAX}.	PRQ-295
Safety input resistor	R_{SI}	–	1	–	kΩ		PRQ-300
Decoupling capacitance (between VCC2 and GND2)	C_{VCC2}	–	11	–	µF	Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Values depend on external C_{LOAD}.	PRQ-293

(table continues...)

Table 31 (continued) Electrical characteristics external components

T_J = -40°C to 150°C; all voltages with respect to ground, pos. current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Decoupling capacitance (between VEE2 and GND2)	C_{VEE2}	–	11	–	µF	Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Values depend on external C_{LOAD}.	PRQ-294
OCP filter resistance	R_{OCP}	–	10	–	Ω	Depends on required response time.	PRQ-301
OCP filter capacitance	C_{OCP}	–	10	–	pF	Depends on required response time	PRQ-302
Gate ON resistor	R_{ON}	1	3	–	Ω		PRQ-303
Gate OFF resistor	R_{OFF}	1	3	–	Ω	Min resistor value required according to max output current in functional range. Max value limited by gate monitoring feature.	PRQ-304
SOFTOFF resistor	$R_{SOFTOFF}$	5	20	–	Ω	Value need to fit to application conditions	PRQ-626
ADC Filter resistance	R_{ADC}	–	10	–	Ω	Optional component. Value must fit to application	PRQ-623
ADC filter	C_{ADC}	–	100	–	pF	Optional component. Value must fit to application	PRQ-625

23.1 Typical application example

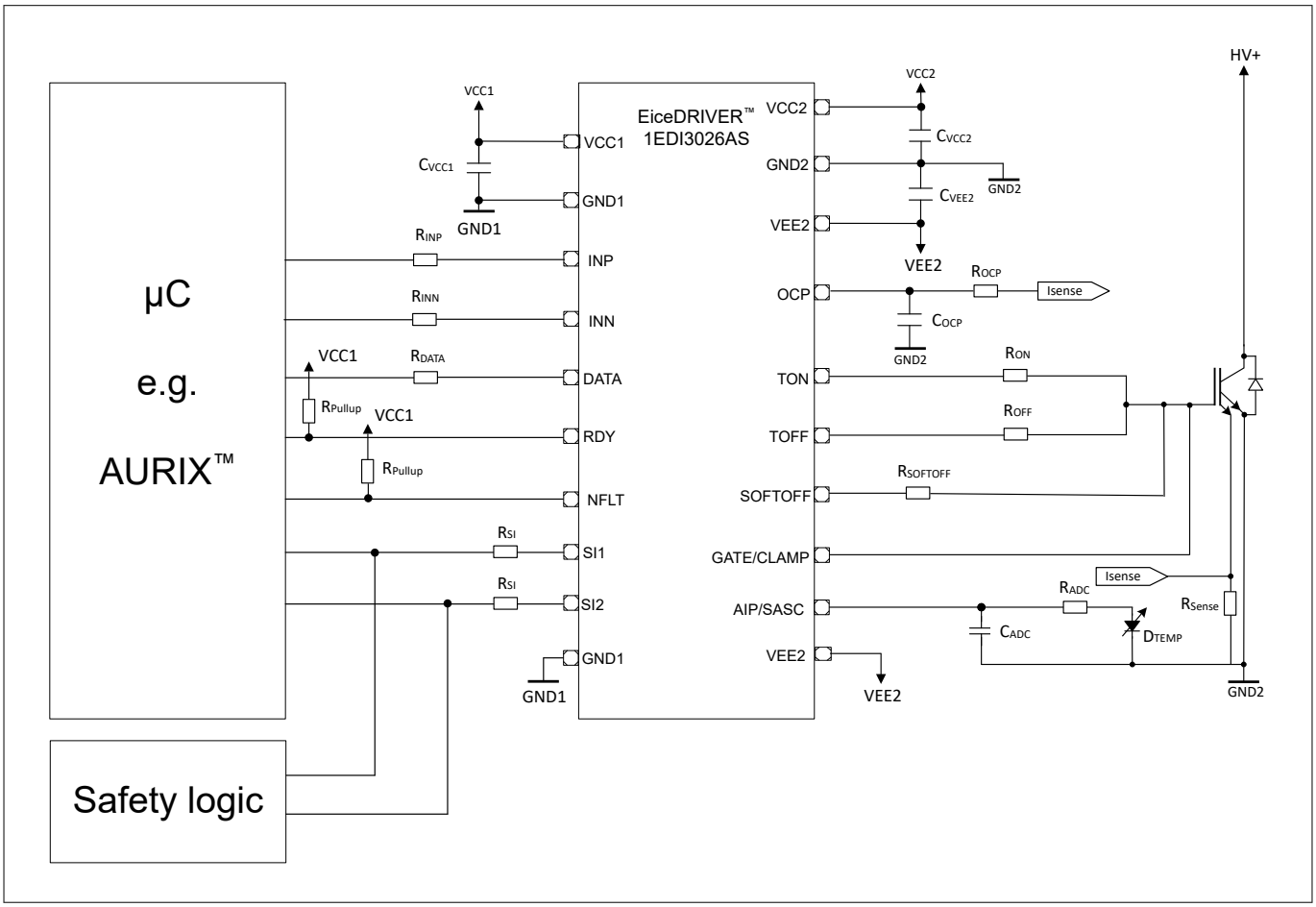

Figure 32 Typical application schematic

24 Package information

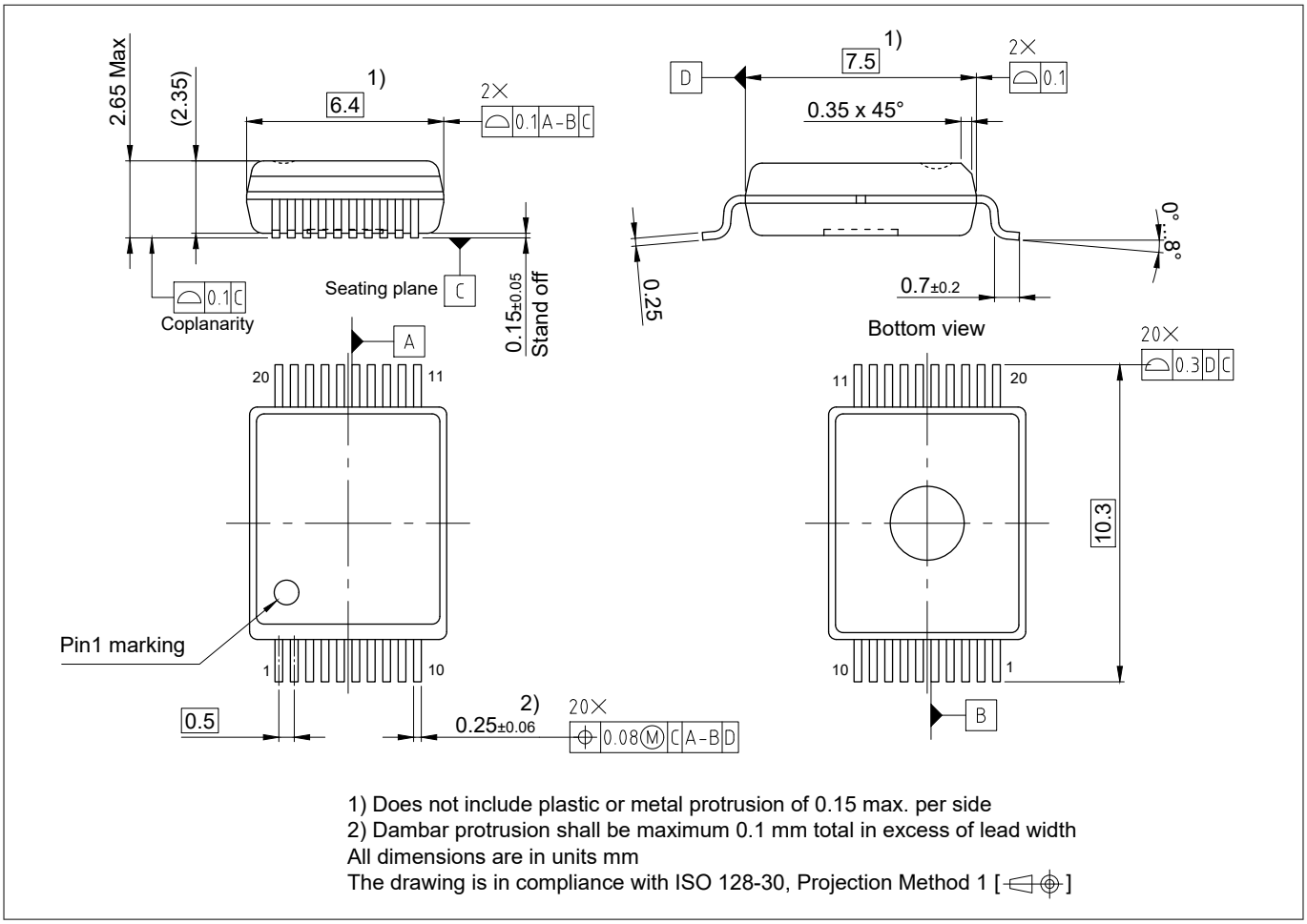

Figure 33 PG-DSO-20

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

25 Revision history

Revision	Date	Changes
1.0	2024-06-20	Datasheet created

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