EiceDRIVER™ 2EDL803X

120 V boot, 3 A / 4 A, junction-isolated high-side and low-side gate driver IC

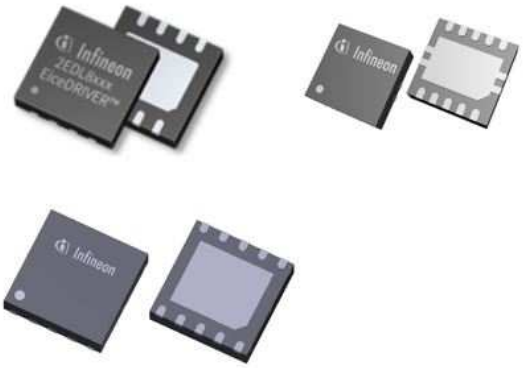
Datasheet

Features

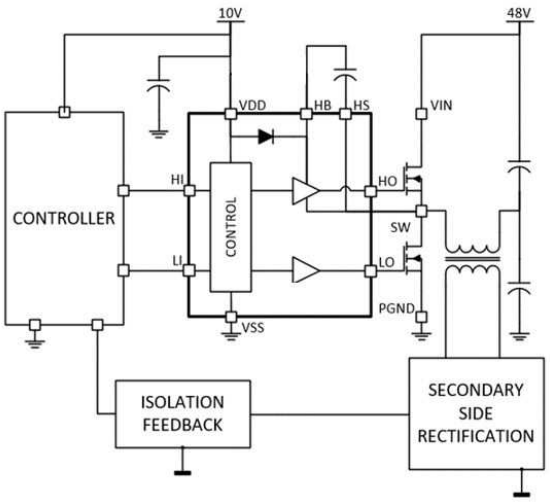
- Level-shift high-side low-side dual channel driver
- Independent high-side and low-side TTL logic inputs
- 3 A & 4 A source / 6 A sink output current capability
- 120 V absolute maximum boot voltage
- Integrated bootstrap diode
- -10 V to 20 V input pin capability for increased robustness
- -5 A output pin reverse current capability
- -12 V absolute maximum negative voltage on HS
- 8 V to 17 V supply voltage operating range
- UVLO for both high-side and low-side driver
- Fast propagation delay (< 35 ns)
- 2 ns typical delay matching
- Enable / disable functionality in SON10 (3 x 3) package
- Offered in SON8 (4x4), SON10 (4x4) and SON10 (3x3) package
- Specified from -40°C to 125°C operating junction temperature range

Potential applications

- Telecom/Datacom half and full bridge power converters
- Current-fed push-pull converters
- Buck converters
- Two-switch forward converters
- Active clamp forward converters
- Class D amplifiers
- DC motor drives



Typical application diagram



Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2EDL803x is designed to drive both high-side and low-side MOSFETs in a half-bridge configuration. The floating high-side driver is capable of driving a high-side MOSFET operating up to 120 V bootstrap voltage. Version 4 provides full 4 A current capability, while version 3 provides 3 A. The high-side bias voltage is generated using a bootstrap technique using an integrated bootstrap diode. The inputs of the driver are TTL logic compatible and can withstand input common mode swing from -10 V up to 20 V. Independent inputs allow controlling high- and low-side domains independently. Undervoltage lockout (UVLO) on both high- and low-side supplies forces the corresponding outputs low in case of insufficient supply. The 2EDL803x is available in SON-8 pins 4 mm x 4 mm, SON-10 pins 4 mm x 4 mm and SON-10 pins 3 mm x 3 mm package.

Table 1 Device information

Part number	Package	Body size
2EDL803X-G4B	PG-VDSON-8-5	4 mm x 4 mm
2EDL803X-G3C	PG-VSON-10-4	3 mm x 3 mm
2EDL803X-G4C	PG-VDSON-10-2	4 mm x 4 mm

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1 Package information

1.1 Ordering information

Base part number	Package type	Standard pack		Orderable part number	Marking code
		Form	Quantity		
2EDL8034-G4B	PG-VDSON-8-5	Tape and reel	5000	2EDL8034G4BXTMA1	2ED 8034G4B
2EDL8033-G4B				2EDL8033G4BXTMA1	2ED 8033G4B
2EDL8034-G3C	PG-VSON-10-4	Tape and reel	4000	2EDL8034G3CXTMA1	2EDL8 034G3
2EDL8033-G3C				2EDL8033G3CXTMA1	2EDL8 033G3
2EDL8034-G4C	PG-VDSON-10-2	Tape and reel	5000	2EDL8034G4CXTMA1	2ED 8034G4C
2EDL8033-G4C				2EDL8033G4CXTMA1	2ED 8033G4C

1.2 Pin configuration

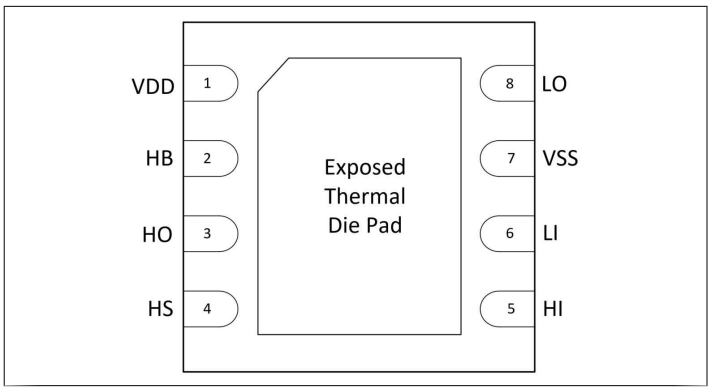

Figure 1 **VDSON-8 4 mm x 4 mm, Top transparent view**

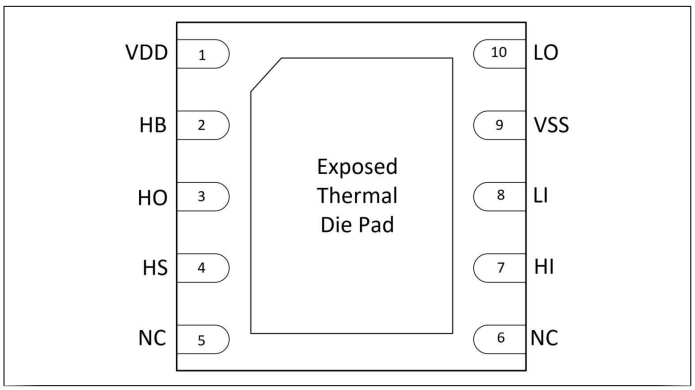

Figure 2 **VDSON-10 4 mm x 4 mm, Top transparent view**

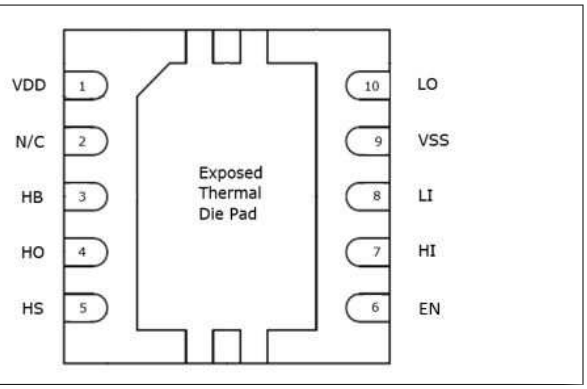

Figure 3 **VSON-10 3 mm x 3 mm, Top transparent view**

1.3 Pin description

Pin name	VDSON-8 pin #	VSON-10 pin #	VDSON-10 pin #	Function
VDD	1	1	1	Gate drive supply
HB	2	3	2	High-side gate driver bootstrap rail
HO	3	4	3	High-side gate driver source and sink current output
HS	4	5	4	High-side FET source connection
HI	5	7	7	High-side driver control input
LI	6	8	8	Low-side driver control input
VSS	7	9	9	Ground return
LO	8	10	10	Low-side gate driver source and sink current output
EN	–	6	–	Enable input. When this pin is high or left-open, it enables the driver. If pulled low, it disables the driver. Pulling the EN pin to VDD is recommended for high-noise system if EN pin is not needed.
NC	–	2	5,6	Not connected

2 General product characteristics

2.1 Absolute maximum ratings

Table 3

Stresses above the values listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply input voltage	V_{DD}	-0.3	–	20	V	
High side supply voltage	V_{HB-HS}	-0.3	–	20	V	Referenced to V_{HS}
High side bootstrap voltage	V_{HB}	-0.3	–	120	V	1)
Phase voltage	V_{HS}	-1	–	V_{HB} + 0.3	V	
Phase voltage (repetitive pulse)	V_{HS}	-12		V_{HB} + 0.3	V	< 100 ns 2)
HI and LI input voltage	V_{HI}, V_{LI}	-10	–	20	V	
EN input voltage	V_{EN}	-10	–	20	V	
Output voltage on LO	V_{LO}	-0.3	–	V_{DD}+0.3	V	
Output voltage on LO (repetitive pulse)	V_{LO}	-2	–	V_{DD}+0.3	V	< 100 ns 2)
Output voltage on HO	V_{HO}	V_{HS}-0.3	–	V_{HB}+0.3	V	
Output voltage on HO (repetitive pulse)	V_{HO}	V_{HS}-2	–	V_{HB}+0.3		< 100 ns 2)
Peak reverse current on LO and HO	I_{OR}	–	–	5	A	2) 3)

(table continues...)

Table 3 (continued)

Stresses above the values listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Operating junction temperature	T_J	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	°C	

1) Verified with VDD supplied within the recommended operating voltage range.
2) Not subject to production test. Verified by design/characterization.
3) For < 500 ns pulses.

2.2 ESD ratings

Description	Symbol	Value	Unit
Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001	ESD_{HBM}	±2000	V
Charged Device Model sensitivity as per ANSI/ESDA/JEDEC JS-002	ESD_{CDM}	±1000	V

2.3 Recommended operating conditions

Table 4

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply input voltage	V_{DD}	8	12	17	V	
High side supply voltage	V_{HB-HS}	8	12	17	V	Referenced to V_{HS}.
High side bootstrap voltage	V_{HB}	V_{HS} + 8	–	V_{HS} + 17	V	
Phase voltage	V_{HS}	-1	–	100	V	
Phase voltage (repetitive pulse)	V_{HS}	-12	–	100	V	< 100 ns
HI and LI Input voltage	V_{HI}, V_{LI}	0	–	V_{DD}+0.3	V	

(table continues...)

Table 4 (continued)

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
EN input voltage	V_{EN}	0	–	V_{DD}+0.3	V	
Output voltage on LO	V_{LO}	0	–	17	V	
Output voltage on HO	V_{HO-HS}	0	–	17	V	Referenced to V_{HS}
HS slew rate	$HS_{dV/dT}$	–	–	50	V/ns	
Operating junction temperature	T_J	-40	–	125	°C	

2.4 Thermal mechanical characteristics

Table 5 Thermal resistance

Symbol	Description	VDSON-8	VSON-10	VDSON-10	UNIT	Conditions
R_{thJC}	Junction-to-case thermal resistance	4.6	4.7	4.6	°C/W	Bottom
R_{thJC}	Junction-to-case thermal resistance	37	39.3	38.4	°C/W	Top
R_{thJA}	junction-to-ambient	57	61.4	57.5	°C/W	Device soldered on PCB [1)]

1) Device on 76.2 mm x 114.3 mm x 1.5 mm board (JEDEC 2s2p) with 6 cm^2 copper area for drain connection. PCB vertical in still air.

2.5 Electrical characteristics

Table 6

Unless otherwise specified: V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current						
VDD quiescent current	I_{VDD}	–	290	380	uA	V_{LI} and V_{HI} = 0 V

(table continues...)

Table 6 (continued)

Unless otherwise specified: $V_{DD} = V_{HB} = 12$ V, $V_{HS} = V_{SS} = 0$ V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD operating current	I_{VDDO}	–	2.4	3.5	mA	$F_{sw} = 500$ kHz, $C_{load} = 0$ nF
HB quiescent current	I_{HB}	–	185	250	uA	V_{LI} and $V_{HI} = 0$ V
HB operating current	I_{HBO}	–	2.0	3.5	mA	$F_{sw} = 500$ kHz, $C_{load} = 0$ nF
HB to VSS leakage current	I_{HBS}	–	–	2	uA	$V_{DD} = V_{LI} = V_{HI} = 0$ V, $V_{HS} = V_{HB} = 100$ V
Input						
Input voltage rising threshold	V_{IR}	1.8	2.4	2.9	V	LI and HI Input voltage rising threshold
Input voltage falling threshold	V_{IF}	1.0	1.5	2.1	V	LI and HI Input voltage falling threshold
Input voltage hysteresis	V_{IH}	–	0.9	–	V	
Input pull down resistance	R_{IN}	100	200	300	kΩ	V_{LI} and $V_{HI} \leq 4$ V
Enable						
Enable input rising threshold	V_{EN}	1.5	2.3	2.8	V	
Enable input falling threshold	V_{DIS}	0.6	1	1.3	V	
Enable input voltage hysteresis	V_{ENHYS}	–	1.3	–	V	
Enable pull up current	I_{EN}	–	8	10	uA	$V_{EN} \leq 4$ V
Time to enable the driver	T_{EN}	–	25	40	ns	$V_{EN} = 2.8$ V
Time to disable the driver	T_{DIS}	–	29	45	ns	$V_{EN} = 0$ V
Undervoltage lockout (UVLO)						
VDD UVLO rising threshold	V_{DDR}	6.8	7.3	7.8	V	
VDD UVLO falling threshold	V_{DDF}	6.2	6.7	7.2	V	

(table continues...)

Table 6 (continued)

Unless otherwise specified: V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD UVLO threshold hysteresis	V_{DDH}	–	0.6	–	V	
VHB-HS UVLO rising threshold	V_{HBR}	5.8	6.3	6.8	V	Referenced to V_{HS}
VHB-HS UVLO falling threshold	V_{HBF}	5.2	5.7	6.2	V	Referenced to V_{HS}
HB-HS UVLO threshold hysteresis	V_{HBH}	–	0.6	–	V	
Bootstrap diode						
Dynamic resistance	R_D	2	4.2	6.5	Ω	I_{VDD-HB} = 100 mA, I_{VDD-HB} = 80 mA
Low current forward voltage	V_{FL}	0.2	0.5	0.8	V	I_{VDD-HB} = 100 uA
High current forward voltage	V_{FH}	1.2	1.4	1.6	V	I_{VDD-HB} = 100 mA
Reverse recovery time	T_{rr}	–	10	–	ns	I_F = 20 mA, I_{RR} = 500 mA, T_C = 25°C[1)]
Low-side gate driver						
High level output voltage	V_{LOH}	0.05	0.1	0.20	V	I_O = -100 mA , V_{LOH} = V_{DD} - V_{LO}, 2EDL8034
High level output voltage	V_{LOH}	0.07	0.12	0.25	V	I_O = -100 mA , V_{LOH} = V_{DD} - V_{LO}, 2EDL8033
Low level output voltage	V_{LOL}	0.03	0.05	0.1	V	I_O = 100 mA
Peak pull-up current	I_{PUL}	–	4	–	A	V_{LO} = 0 V[1)] , 2EDL8034
Peak pull-up current	I_{PUL}	–	3	–	A	V_{LO} = 0 V[1)] , 2EDL8033
Peak pull-down current	I_{PDL}	–	6	–	A	V_{LO} = 12 V[1)]
High-side gate driver						
High level output voltage	V_{HOH}	0.05	0.1	0.2	V	I_O = -100 mA , V_{HOH} = V_{HB} - V_{HO}, 2EDL8034

(table continues...)

Table 6 (continued)

Unless otherwise specified: V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output voltage	V_{HOH}	0.07	0.12	0.25	V	I_O = -100 mA , V_{HOH} = V_{HB} - V_{HO}, 2EDL8033
Low level output voltage	V_{HOL}	0.03	0.05	0.1	V	I_O = 100 mA
Peak pull-up current	I_{PUH}	–	4	–	A	V_{HO} = 0 V[1)] , 2EDL8034
Peak pull-up current	I_{PUH}	–	3	–	A	V_{HO} = 0 V[1)] , 2EDL8033
Peak pull-down current	I_{PDH}	–	6	–	A	V_{HO} = 12 V[1)]

1) Not subject to production test. Verified by design/characterization.

2.6 Switching characteristics

Table 7

Unless otherwise specified: V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Propagation delays						
Rising propagation delay	T_{DR}	–	33	50	ns	C_{load} = 0 , 50 %-50 %[1)]
Falling propagation delay	T_{DF}	–	33	50	ns	C_{load} = 0, 50 %-50 %[2)]
Delay matching						
Delay matching ON	T_{DMON}	–	2	6	ns	between LO rising and HO falling
Delay matching OFF	T_{DMOFF}	–	2	6	ns	between LO falling and HO rising
Output rise and fall time						
LO, HO rise time	T_R	–	4.4	–	ns	C_{load} = 1 nF, 10 % - 90 %[3)] , 2EDL8034
LO, HO rise time	T_R	–	4.6	–	ns	C_{load} = 1 nF, 10 %-90 %[3)] , 2EDL8033

(table continues...)

Table 7 (continued)

Unless otherwise specified: V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LO, HO rise time	T_{R1}	–	131	–	ns	C_{load} = 100 nF, 25 %-75 %[3], 2EDL8034
LO, HO rise time	T_{R1}	–	195	–	ns	C_{load} = 100 nF, 25 %-75 %[3], 2EDL8033
LO, HO fall time	T_F	–	3.3	–	ns	C_{Load} = 1 nF, 10 %-90 %[3]
LO, HO fall time	T_{F1}	–	106	–	ns	C_{LOAD} = 100 nF, 25 %-75 %[3]
Miscellaneous						
Minimum input pulse width that changes the output	T_{PW}	–	–	40	ns	

1) Rising propagation delay from LI to LO and from HI to HO.
2) Falling propagation delay from LI to LO and from HI to HO.
3) Not subject to production test. Verified by design/characterization.

3 Timing diagrams

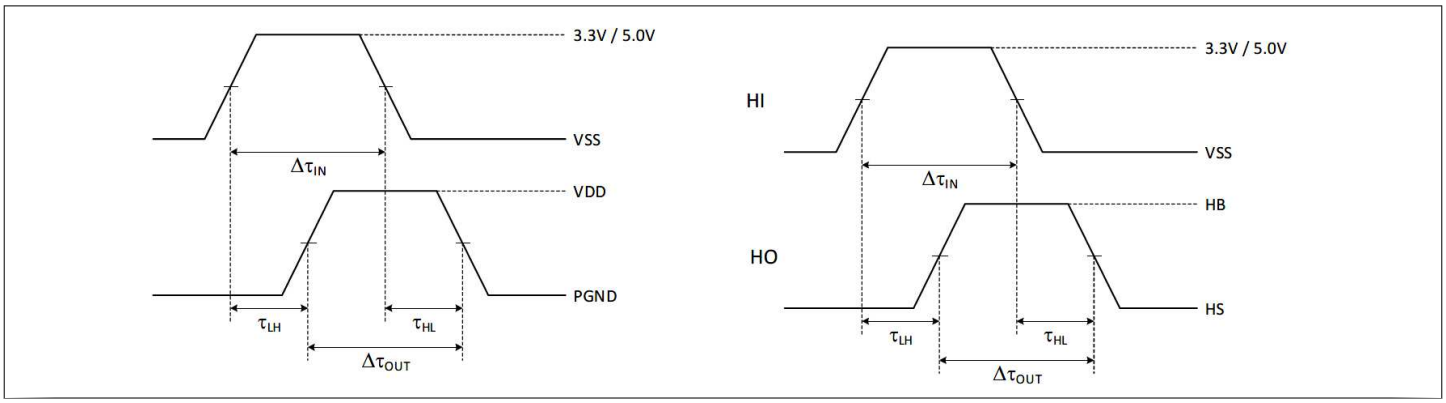

Figure 4 Propagation delay

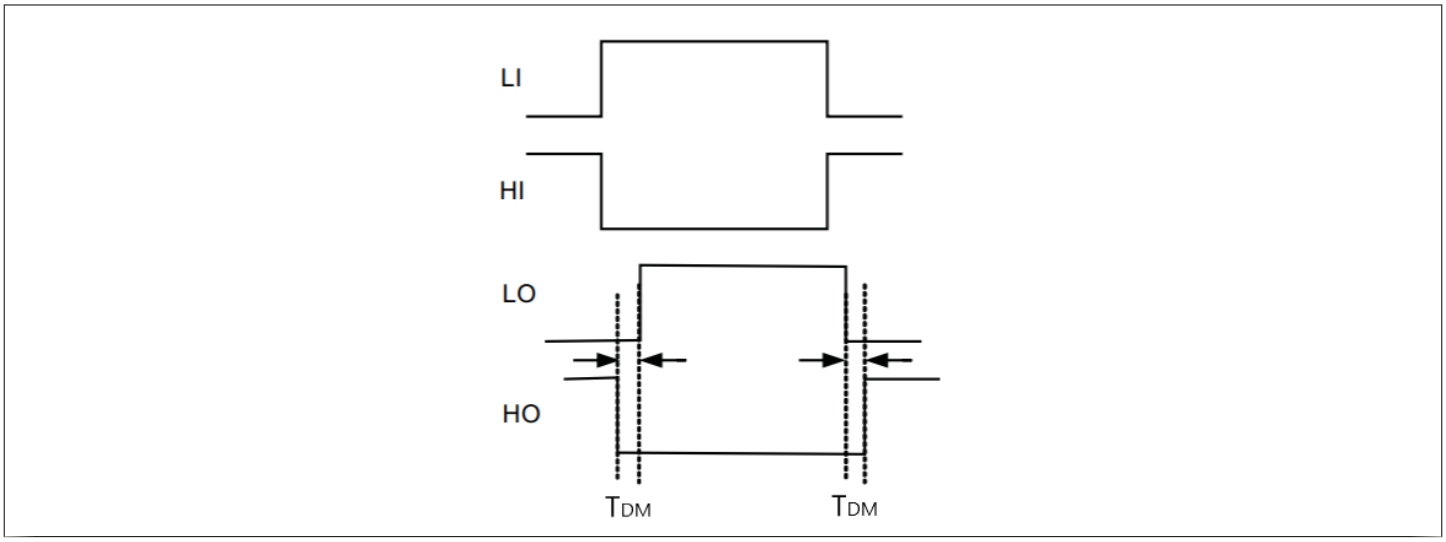

Figure 5 Delay matching

4 Typical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = 12$ V, $V_{HS} = V_{SS} = 0$ V, $T_C = 25$°C and no load on the outputs.

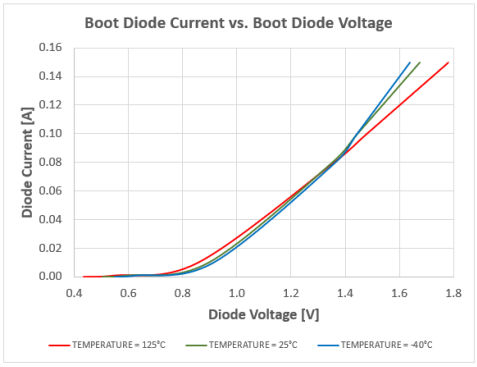

Figure 6 Diode current vs. diode voltage

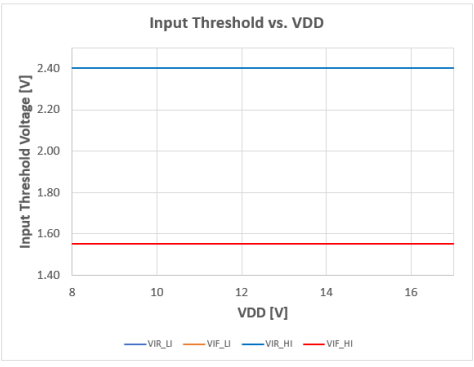

Figure 7 Input threshold vs. VDD

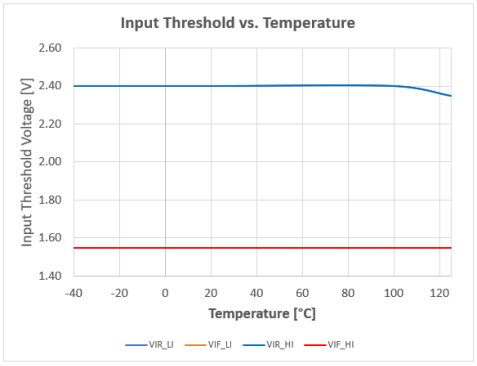

Figure 8 Input threshold vs. temperature

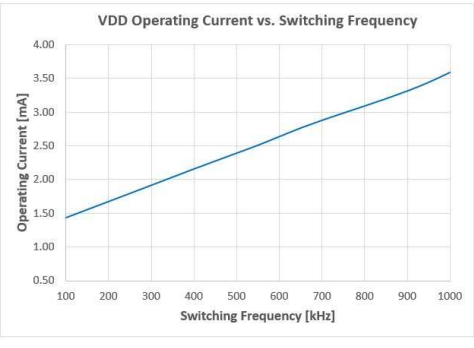

Figure 9 VDD operating current vs. switching frequency

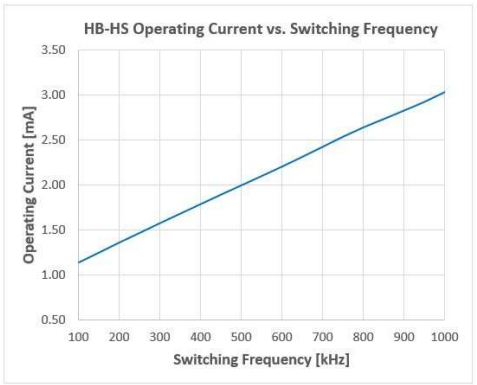

Figure 10 HB operating current vs. switching frequency

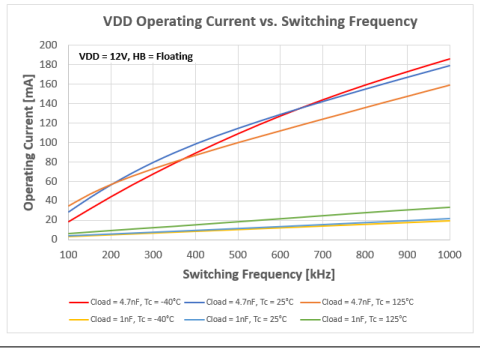

Figure 11 VDD operating current vs. switching frequency

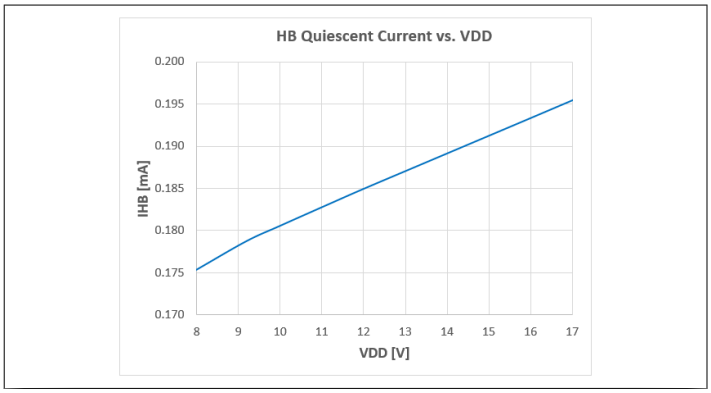

Figure 12 HB quiescent current vs. VDD

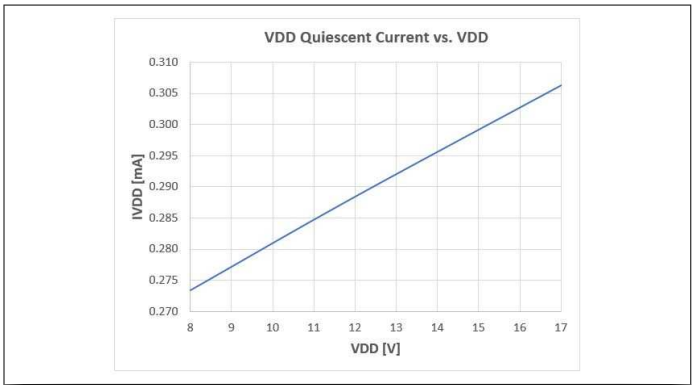

Figure 13 VDD quiescent current vs. VDD

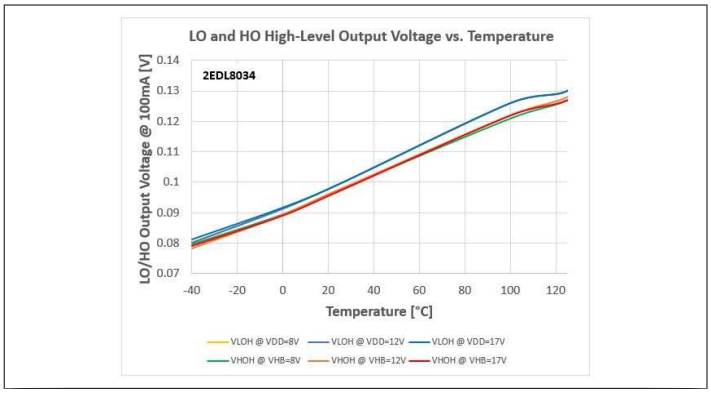

Figure 14 LO/HO high-level output voltage vs. temperature

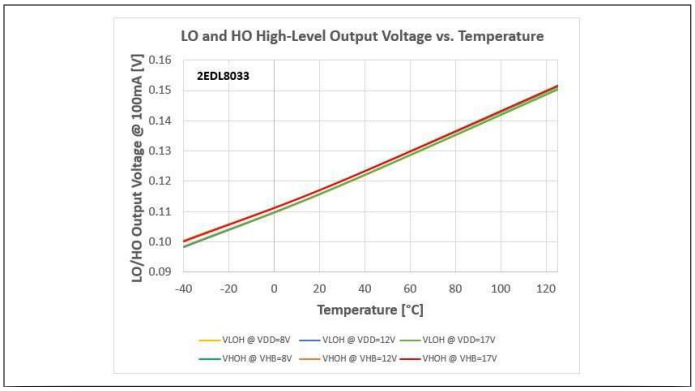

Figure 15 LO/HO high-level output voltage vs. temperature

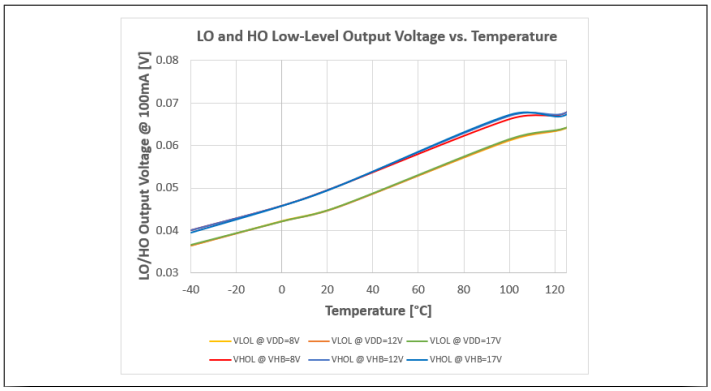

Figure 16 LO/HO low-level output voltage vs. temperature

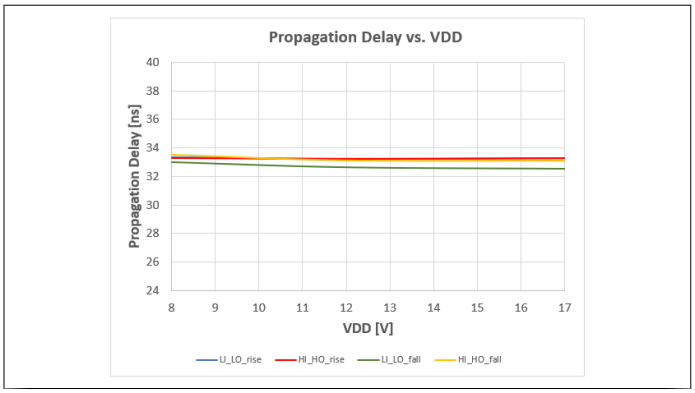

Figure 17 Propagation delay vs. VDD

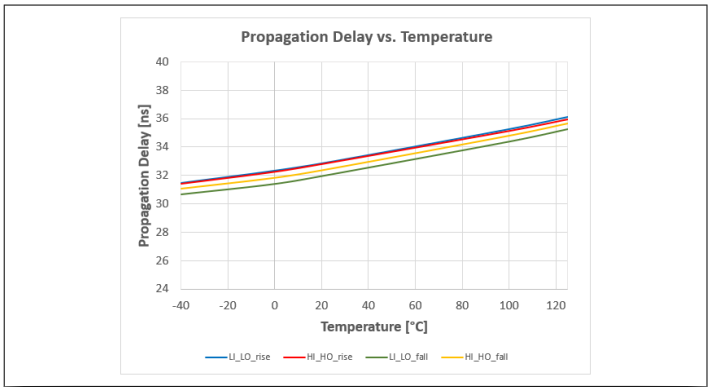

Figure 18 Propagation delay vs. temperature

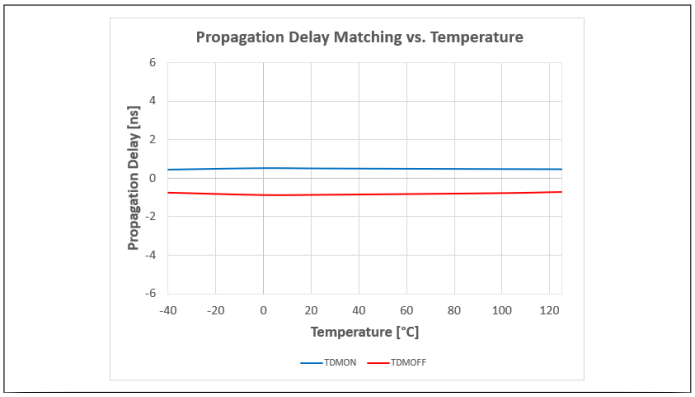

Figure 19 Propagation delay matching vs. temperature

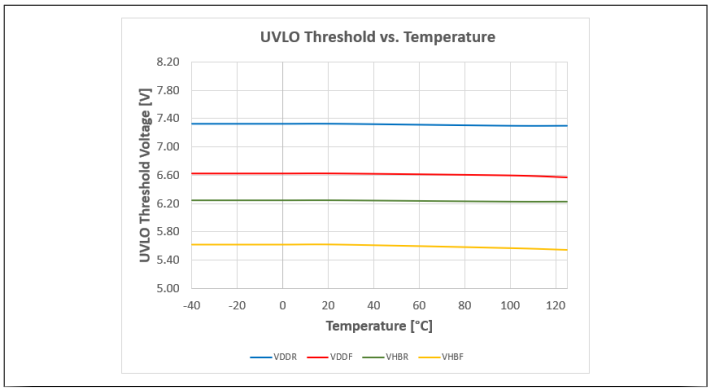

Figure 20 UVLO threshold vs. temperature

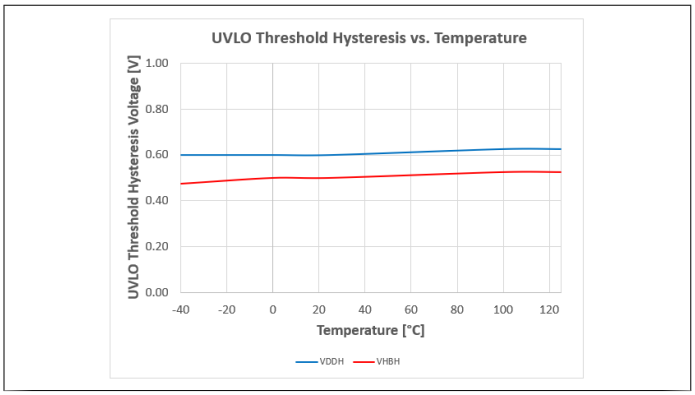

Figure 21 UVLO threshold hysteresis vs. temperature

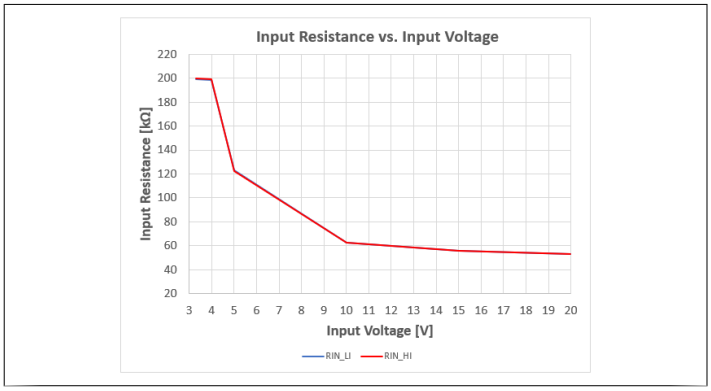

Figure 22 Input impedance vs. input voltage

5 Product information

5.1 Block diagram

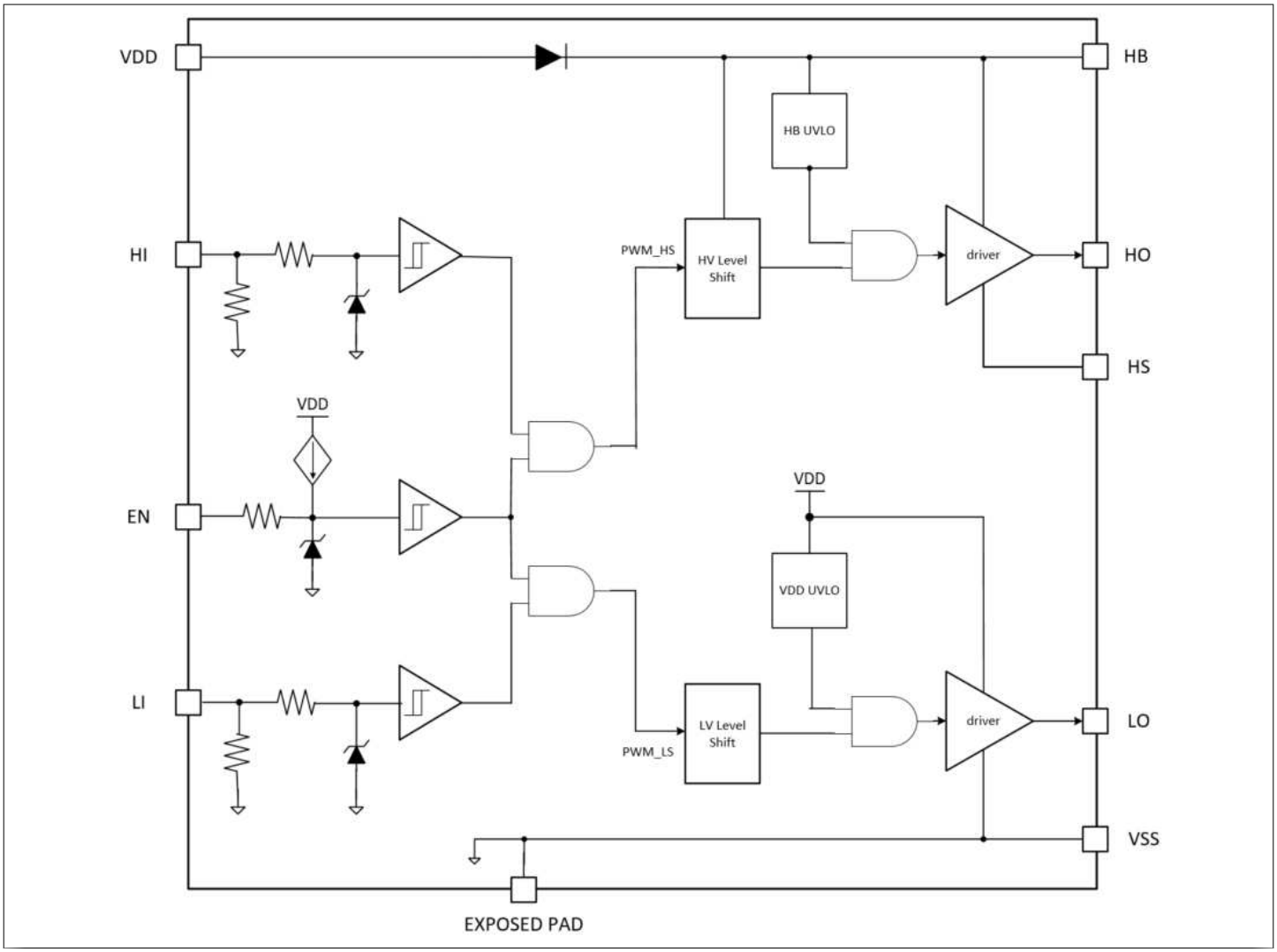

Figure 23

5.2 Functional description

The device is a level-shifted 2-channel driver designed to support topologies with high-side and low-side configurations. The high side is level shifted by the combination of an on-chip 120 V rated bootstrap diode and an external bootstrap capacitor. The device provides 3 A and 4 A peak source current capability and a strong 6 A sink current capability for both high-side and low-side drivers. This allows driving large power MOSFETs with minimum or optimized switching losses during the transition through the MOSFET's miller plateau.

2EDL803x's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are independently controlled and matched to typical 2 ns between the turn on and turn off of each other.

The switching node (HS pin) is able to handle negative voltages down to –12 V which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductances and stray capacitances.

UVLO circuits are provided for both the high-side and low-side drivers. UVLO protects the system by forcing the output low when the supply voltage is lower than the specified threshold.

The following sections describe the key functionalities.

5.2.1 Supply voltage

The absolute maximum supply voltage is 20 V. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 7.3 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

5.2.2 Input stage

The input pull-down resistance has a value of 200 kΩ typical when the HI and LI input voltage is ≤ 4 V. When it is above 4 V, the effective input resistance is lower because of the activation of the 5 V clamp as shown in the input stage diagram below. At an input voltage of 10 V, the effective input resistance is at 46 kΩ typical.

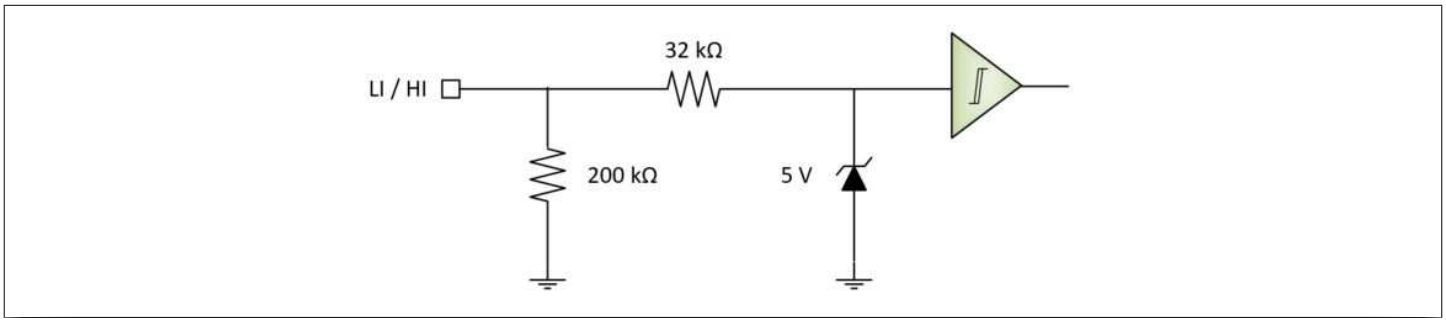

Figure 24 Input stage diagram

2EDL803X device responds to the two inputs signals (HI and LI) independently according to Table 8.

Table 8 2EDL803X truth table

EN	LI	HI	LO	HO
L	L	L	L	L
	H	L	L	L
	L	H	L	L
	H	H	L	L
H	L	L	L	L
	H	L	H	L
	L	H	L	H
	H	H	H	H

5.2.3 Enable

2EDL803X in SON10 (3 mm x 3 mm) package has an enable (EN) pin which enables or disables the output of the driver. The outputs are active when the voltage at the EN pin is above the rising threshold and are disabled when the EN pin voltage falls below the falling threshold. The EN input stage has built-in hysteresis for enhanced noise immunity. An internal pull-up current source connects the EN pin to VDD thus leaving the EN pin floating enables the output. If the EN pin is not actively controlled, it is recommended to pull up this pin to VDD especially for high-noise system. Externally pulling the EN pin to ground disables the output.

5.2.4 Driver outputs

The strong 3 A and 4 A source and 6 A sink current capability of both, the low-side and high-side output, allows for faster switching of the power MOSFETs thus leading to lower switching losses. The ultra-low pull down resistances, typically 0.5 Ω for both outputs, keep the gate of the power MOSFETs down during fast transient events thus avoiding

dv/dt induced turn on. The output stage can sustain negative transient pulse up to -2 V for 100 ns. The output stage is implemented using a PMOS for the pull-up and NMOS for the pull-down in a totem-pole configuration.

5.2.5 Undervoltage lockout (UVLO)

The UVLO function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus it can be ensured that the power MOSFET is not switched on if the driving voltage is too low to completely switch on the device, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 7.3 V with 0.6 V hysteresis for supply voltage (V_{DD}) and 6.3 V with 0.6 V hysteresis for high-side boot voltage (V_{HB-HS}).

5.2.6 Minimum input pulse width

The device responds to input level according to the truth table in input control section as long as the logic signal complies with the minimum pulse width requirement. Signal pulse longer than the minimum allowable input pulse width yields valid output. Any output in response to shorter pulses or glitches should be disregarded and filtered out by the user. Under all allowable operation above input minimum pulse width of 40 ns, the output behaves one to one to the input with minimal pulse width distortion.

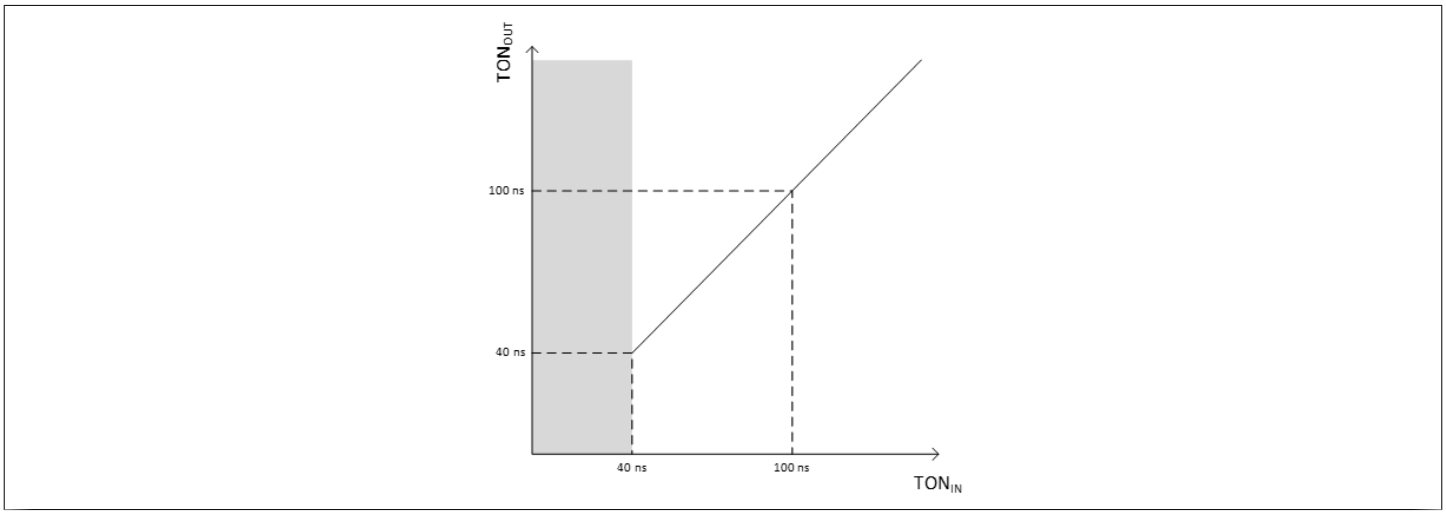

Figure 25 Minimum pulse width input-output on-time transfer function

6 Application information

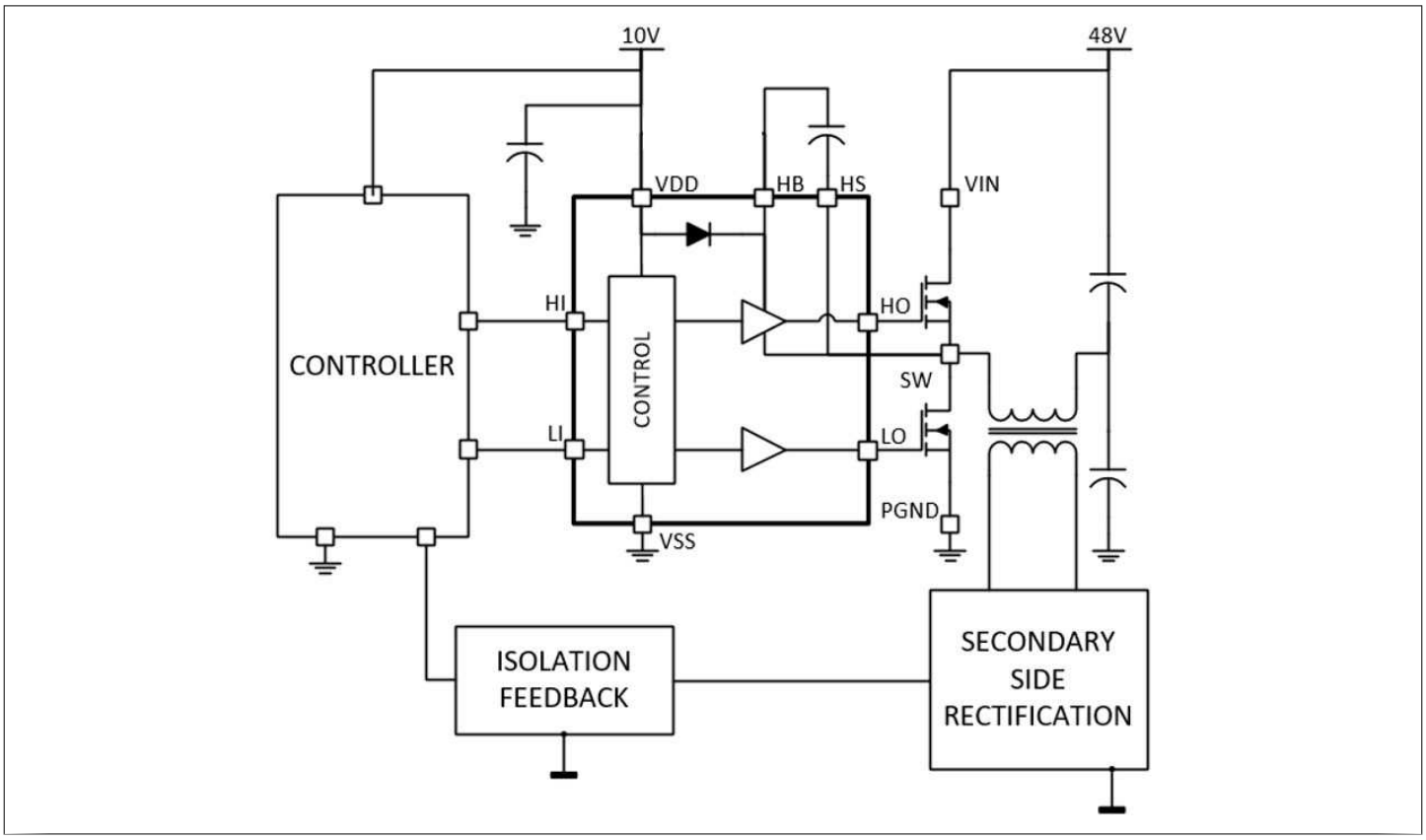

Figure 26 Typical application - primary side half-bridge

6.1 Design guidelines

In a half-bridge configurations, a high-side bias that is referenced to the switch node is needed in order to drive the gate of the high-side MOSFET. One of the most common solutions due to its simplicity and low cost is the usage of a bootstrap circuit consisting of a diode (internal to the driver) and a capacitor as seen in Figure 27. However, this method imposes limitation on the power converter's duty cycle due to the requirement of recharging the bootstrap capacitor. This limitation can be mitigated through the proper selection of the bootstrap components.

The bootstrap circuit operation is defined by two main periods:

Charging period: When the low-side MOSFET (Q2) is ON and the high-side MOSFET (Q1) is OFF, the switch node/HS pin is pulled to ground creating a charging path for the bootstrap capacitor (*C*boot) through the *V*dd bypass capacitor (*C*Vdd) and the internal bootstrap diode. For high dV/dt application, it is recommended to use an extrenal bootstrap diode.

Discharging period: When the low-side MOSFET (Q2) is turned OFF and the high-side MOSFET (Q1) starts conducting, the switch node/HS pin is pulled to the high voltage *V*in thus the internal bootstrap diode gets reverse biased. The bootstrap capacitor (*C*boot) will then discharge some of its stored charges to the gate of the high-side MOSFET as well as to other contributing factors such as the MOSFET's gate-source leakage current, floating section quiescent current, floating section leakage current and the internal bootstrap diode reverse bias leakage current.

Typical waveform for the voltage across *C*boot as a function of time is shown in Figure 28 where the various contributions have been distinguished. The voltage across *C*boot increases during the charging period and then it drops with a high negative dV/dt as it charges the gate of the high-side MOSFET (Q1). After this, the *C*boot voltage continues to drop but with a much lower slope because only the high-side bias current and some leakage current is discharing the *C*boot during this phase.

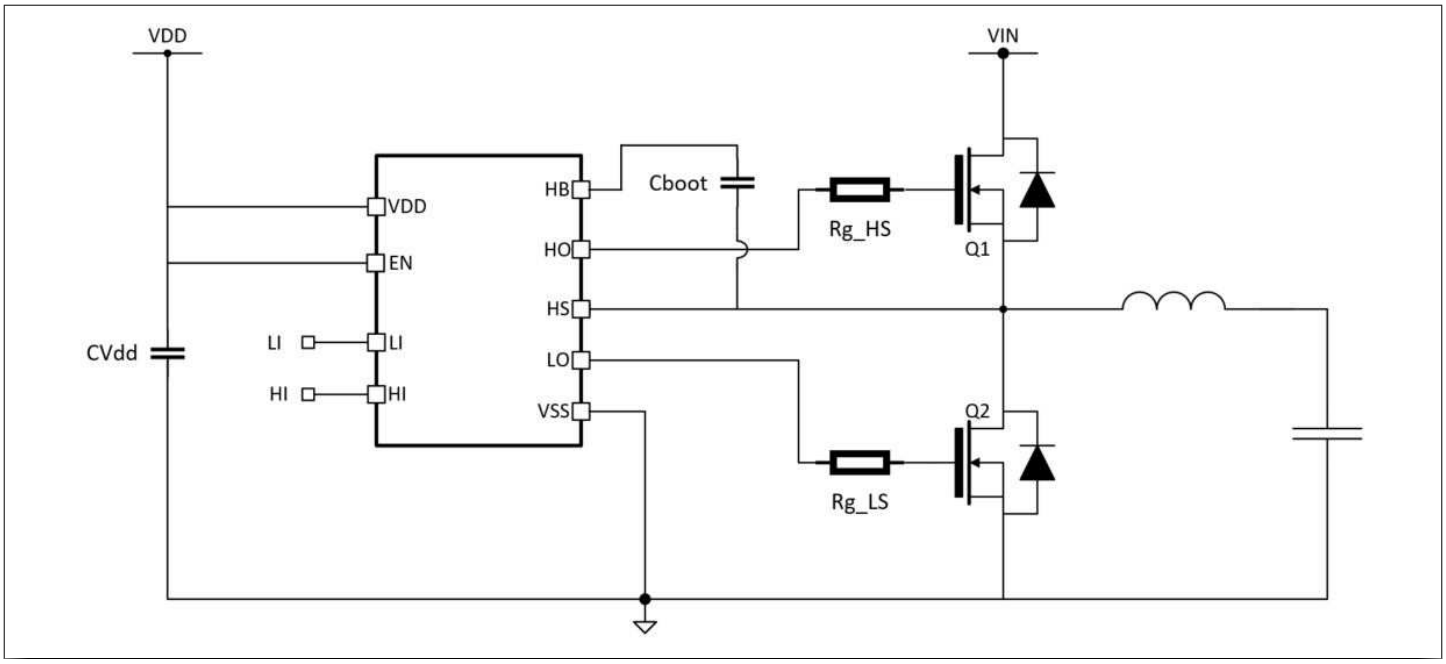

Figure 27 Gate drive circuitry using 2EDL803X to drive MOSFETs in a half-bridge configuration

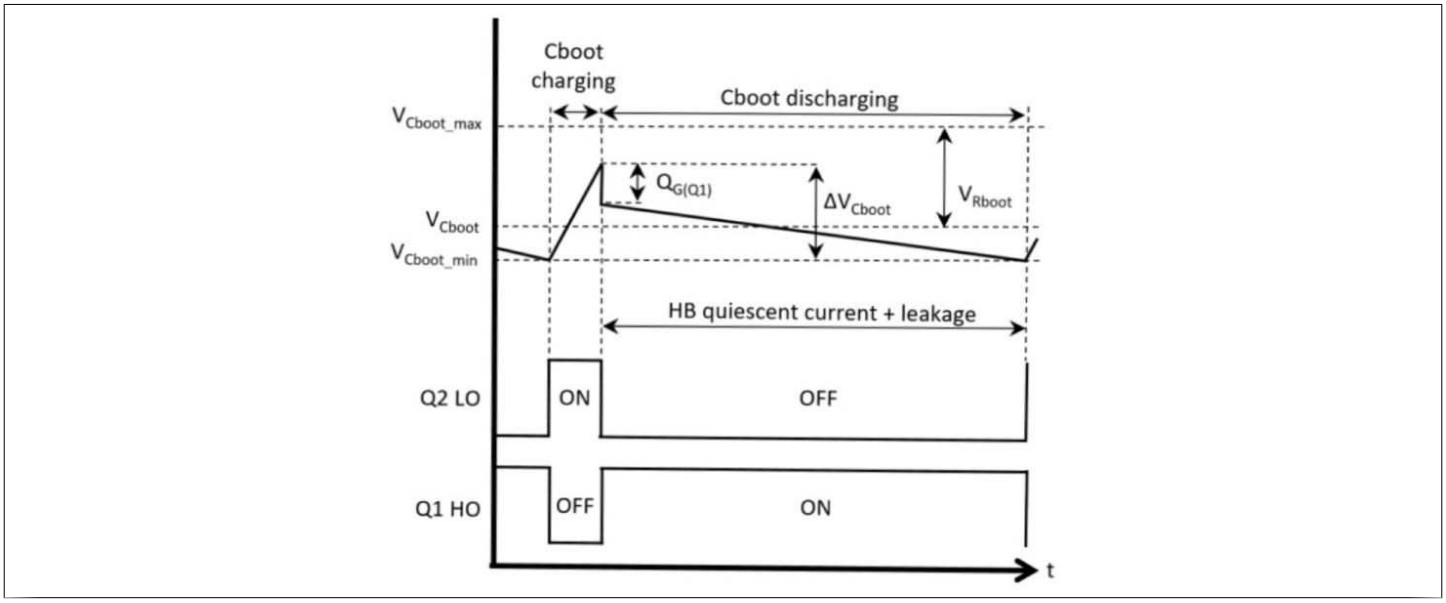

Figure 28 Typical C_{boot} waveform

6.1.1 Selection of bootstrap capacitor

The bootstrap capacitor provides the necessary charge to drive the high-side MOSFET and thus it needs to be sized in such a way that the maximum voltage drop across this capacitor does not fall below the high-side UVLO threshold during transient and normal operations. First, determine the maximum allowable voltage drop (ΔV_{Cboot_max}) when the high-side MOSFET (Q1) is on which is given by the following formula:

$$\Delta V_{Cboot\_max} = V_{dd} - V_F - V_{HBR} - V_{HBH}$$

Equation 1

Where:

V_{dd} = Gate driver supply voltage
V_F = Bootstrap diode forward voltage drop
V_{HBR} = HB UVLO rising threshold
V_{HBH} = HB UVLO threshold hysteresis

Next, determine the total charge (Q_T) that must be delivered by the bootstrap capacitor at maximum duty cycle. As mentioned, there are several factors that contribute to the discharge of the bootstrap capacitor such as the Q1's total gate charge, Q1's gate-source leakage current, HB quiescent current, HB leakage current, bootstrap diode reverse bias leakage current and bootstrap capacitor leakage current (if using an electrolytic capacitor). For sake of simplicity, only Q1's total gate charge and HB quiescent and leakage current are considered as the other sources of leakage are negligible in comparison.

$$Q_T = Q_G + \frac{I_{HB}}{F_{sw}} + I_{HBS} \times \frac{D_{max}}{F_{sw}}$$

Equation 2

Where:
Q_G = High-side MOSFET (Q1) total gate charge
I_{HB} = HB maximum quiescent current
I_{HBS} = HB to VSS leakage current
D_{max} = Maximum duty cycle
F_{sw} = Switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{boot\_min} \geq \frac{Q_T}{\Delta V_{Cboot\_max}}$$

Equation 3

6.1.2 Selection of VDD bypass capacitor

The V_{dd} bypass capacitor provides the charge for the bootstrap capacitor during the charging period. As a rule of thumb, the V_{dd} bypass capacitor should be sized to be at least 10~20 times larger than the bootstrap capacitor. This equates to a voltage ripple of 5 ~ 10 % in the V_{dd} capacitor. It should be placed as close as possible to the VDD and VSS pins of the gate driver.

$$C_{Vdd} \geq 10 \sim 20 \times C_{boot}$$

Equation 4

6.1.3 Selection of bootstrap resistor

The bootstrap resistor limits the current in the bootstrap diode during start-up when the bootstrap capacitor is initially completely discharged. The peak current through this resistor is given by:

$$I_{Pk\_Rboot} = \frac{V_{dd} - V_F}{R_{boot}}$$

Equation 5

The bootstrap resistor together with the bootstrap capacitor introduces a time constant and should be sized appropriately to achieve the desired start-up time. For this calculation, it is assumed that the bootstrap capacitor is fully charged after 4 time constant. With this, R_{boot} can be calculated using the following formula:

$$R_{boot} \leq \frac{t_{min}}{4 \times C_{boot}}$$

Equation 6

Where:

t_{min} = Minimum on time of the low-side MOSFET (Q2)

6.1.4 Selection of external bootstrap diode

For high dV/dT applications, an external bootstrap diode is recommended to be in parallel with the internal bootstrap diode. A fast recovery or schottky diode with low forward voltage drop is recommended in order to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current from Equation (5) during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{in}) with enough derating.

6.1.5 Selection of gate resistor

The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver providing an external way to control the switching speed of the MOSFET for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot –through protection etc. The following formulas show the effect of the external gate resistor to the output current capability of the gate driver.

$$I_{HSRC} = \frac{V_{dd} - V_F}{R_{PUH} + R_{G\_HS} + R_{G\_int}}$$

Equation 7

$$I_{HSNK} = \frac{V_{dd} - V_F}{R_{PDH} + R_{G\_HS} + R_{G\_int}}$$

Equation 8

$$I_{LSRC} = \frac{V_{dd}}{R_{PUL} + R_{G\_LS} + R_{G\_int}}$$

Equation 9

$$I_{LSNK} = \frac{V_{dd}}{R_{PDL} + R_{G\_LS} + R_{G\_int}}$$

Equation 10

Where:

I_{HSRC} = High-side peak source current
I_{HSNK} = High-side peak sink current
I_{LSRC} = Low-side peak source current
I_{LSNK} = Low-side peak sink current
R_{PUH} = High-side pull-up resistance
R_{PDH} = High-side pull-down resistance
R_{PUL} = Low-side pull-up resistance
R_{PDL} = Low-side pull-down resistance
V_{dd} = Gate driver supply voltage
V_F = Bootstrap diode forward voltage drop
R_{G_HS} = High-side external gate resistance
R_{G_LS} = Low-side external gate resistance
R_{G_int} = MOSFET internal gate resistance

6.2 PCB Layout guidelines

To maximize the performance of EiceDRIVER™ 2EDL803X, the following are some recommendations for optimizing the PCB layout:

- Use a low-ESR decoupling capacitors on VDD-GND and HB-HS and placed it as close as possible to the VDD-GND and HB-HS pins of the driver
- An option for a series boot resistor is recommended to control the high-side MOSFET slew rate and therefore the low-side MOSFET overshoot. The boot loop path including the VDD capacitor, boot diode, boot series resistor and boot capacitor should be as small as possible
- It is recommended to have an external boot diode placement for high dv/dt application.
- Placement for gate resistor is also recommended to control the switching speed of the MOSFET. Both the gate resistor and the MOSFET should be placed as close as possible to the driver in order to minimize the gate loop inductance.
- Use copper plane underneath the exposed GND pad of the driver and connect it to buried copper plane(s) with multiple thermal vias for better heat dissipation into the PCB.
- Connection to the HS pin of the driver from the high-side MOSFET source and low-side MOSFET drain should be as short and wide as possible and avoid connecting it directly through the high switching current path.
- LO and HO traces should be as short and wide as possible
- Avoid letting the LI and HI signal trace to come close to high dV/dT traces which might induce significant noise.

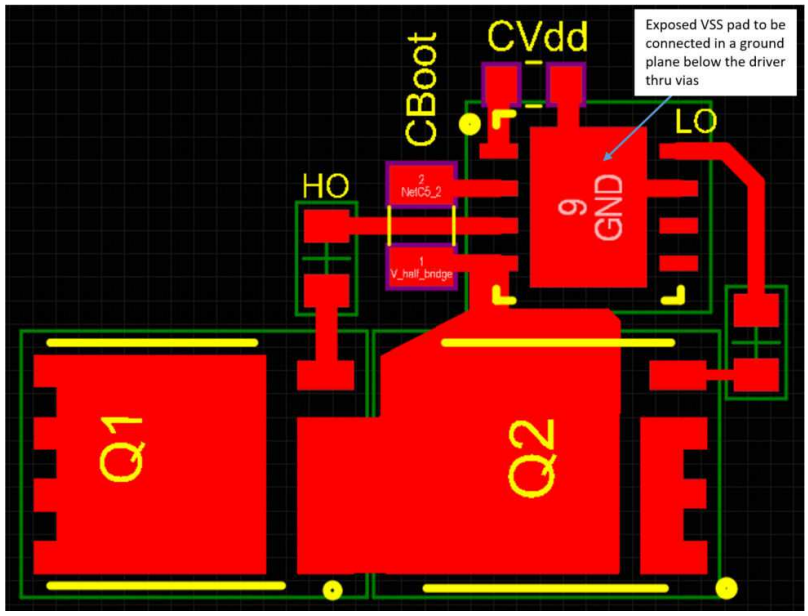

Figure 29 2EDL803X Layout example

7 Outline dimensions

For further information on package types, recommendation for board assembly, please go to:
www.infineon.com\packages

7.1 PG-VDSON-8-5

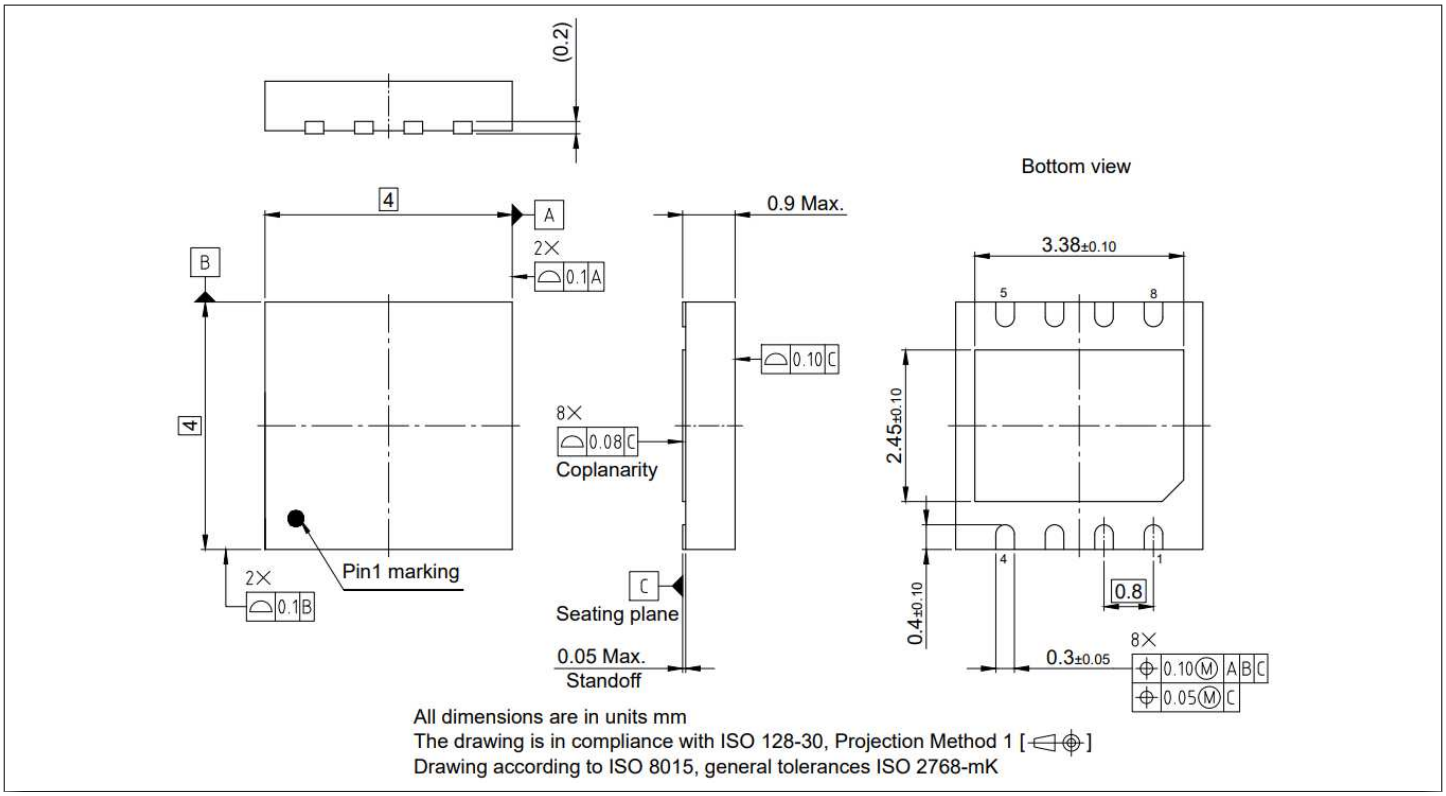

Figure 30 PG-VDSON-8-5 outline dimensions

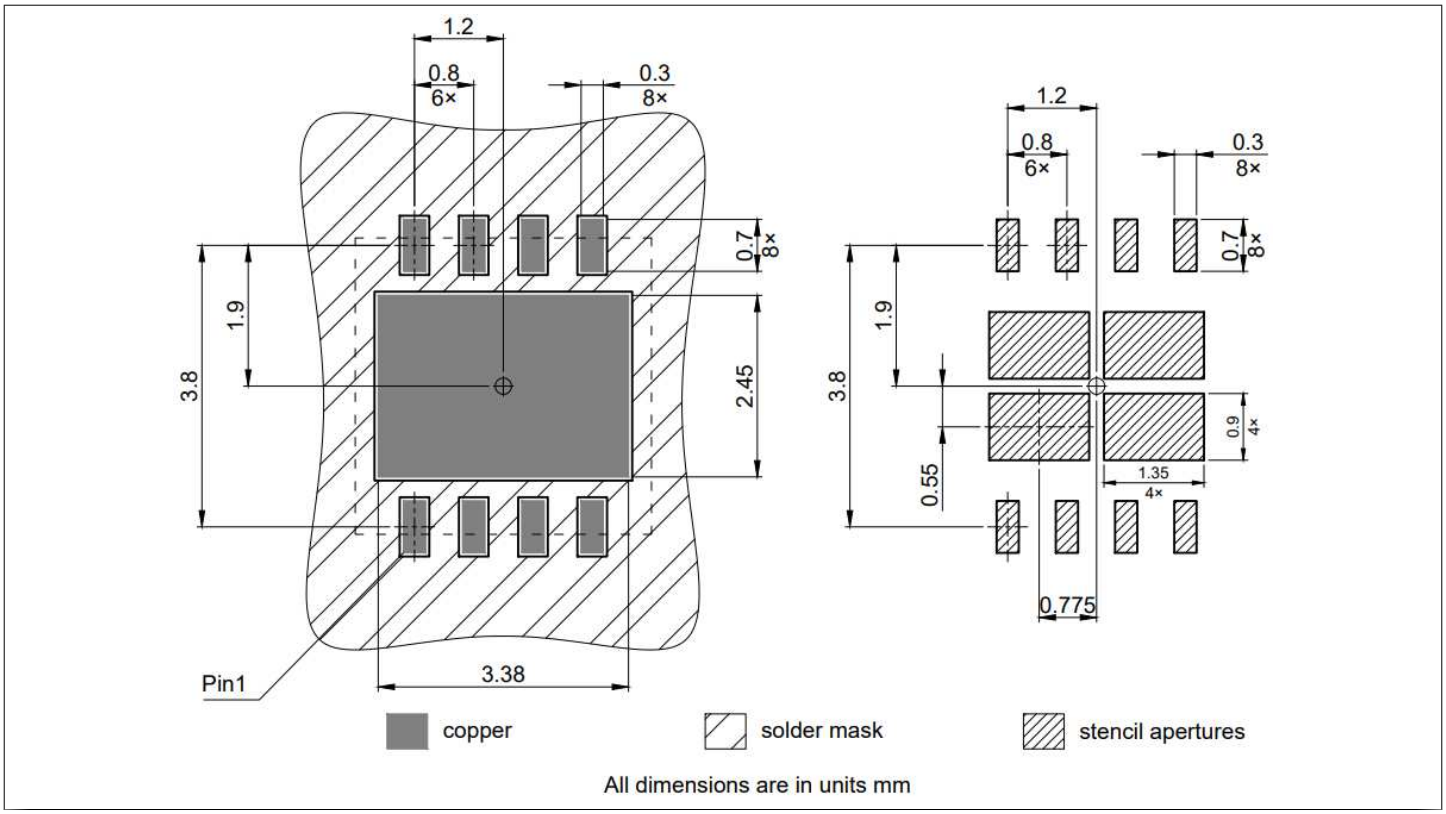

Figure 31 PG-VDSON-8-5 footprint dimensions

7.2 PG-VSON-10-4

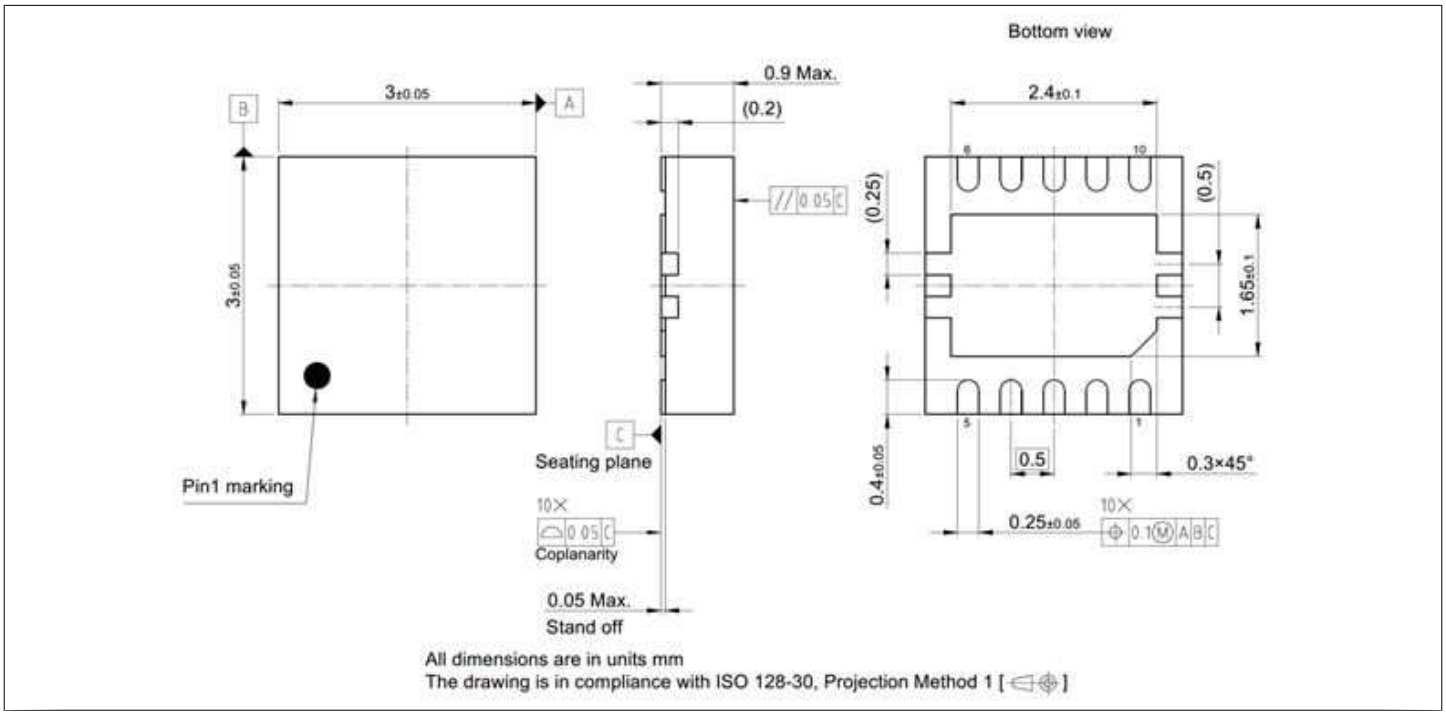

Figure 32 PG-VSON-10-4 outline dimensions

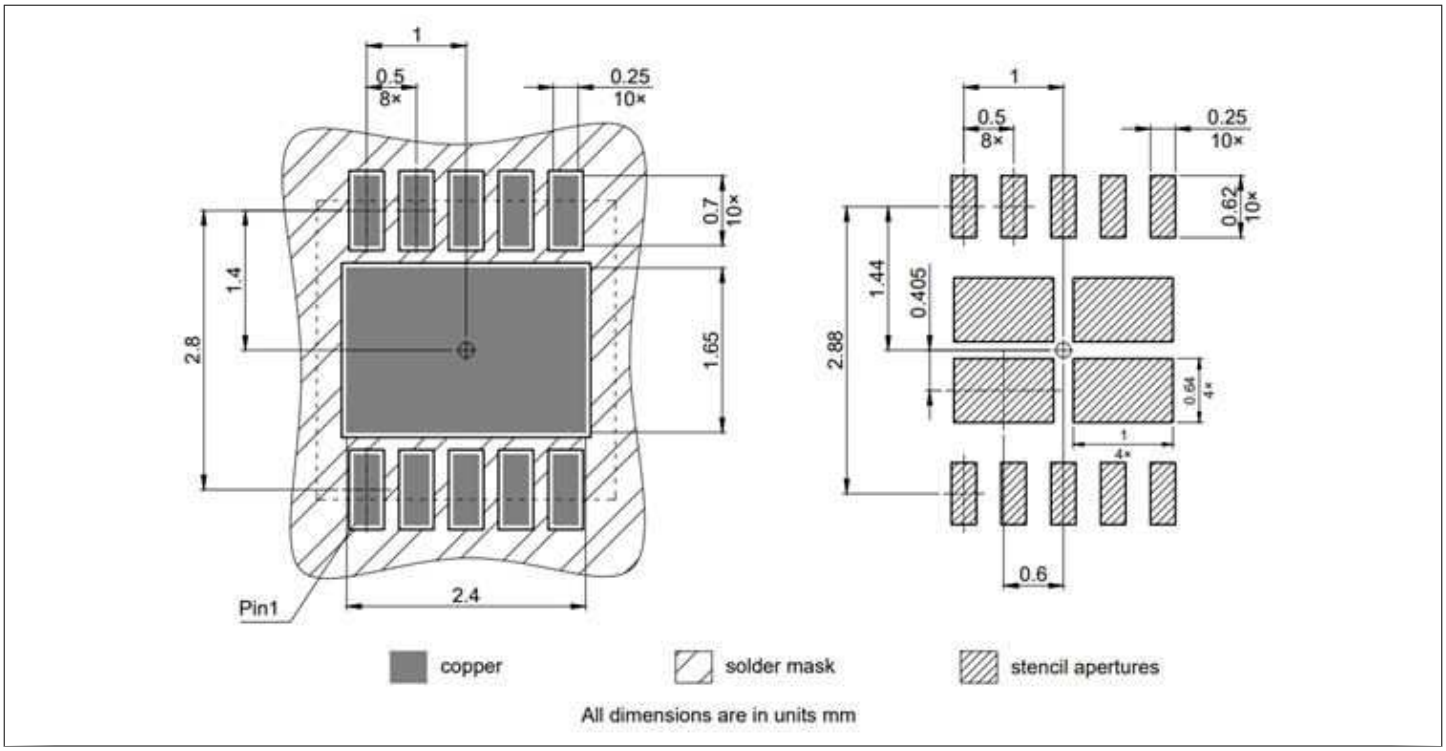

Figure 33 PG-VSON-10-4 footprint dimensions

7.3 PG-VDSON-10-2

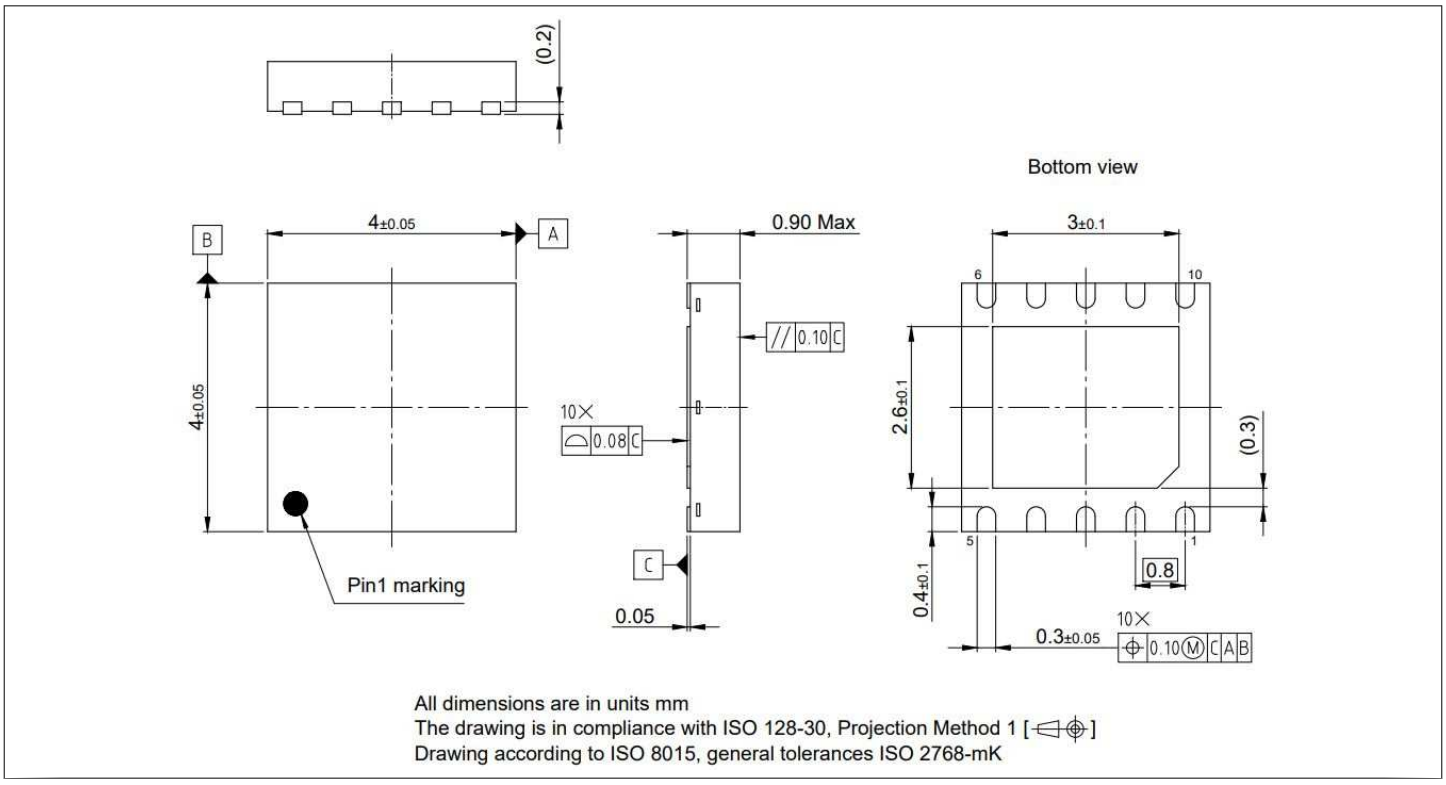

Figure 34 PG-VDSON-10-2 Outline dimensions

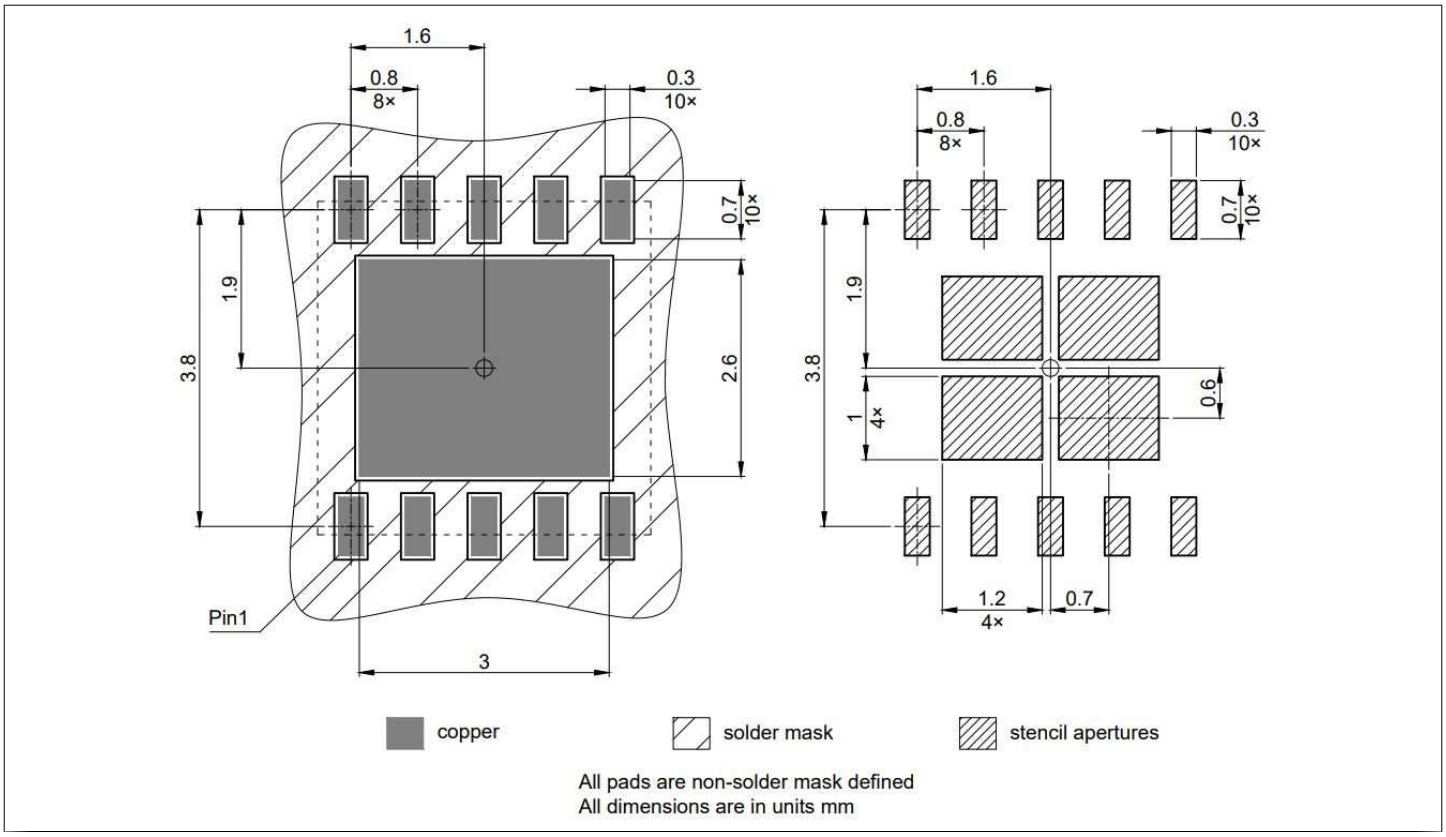

Figure 35 PG-VDSON-10-2 Footprint dimensions

8 Tape and reel

8.1 PG-VDSON-8-5

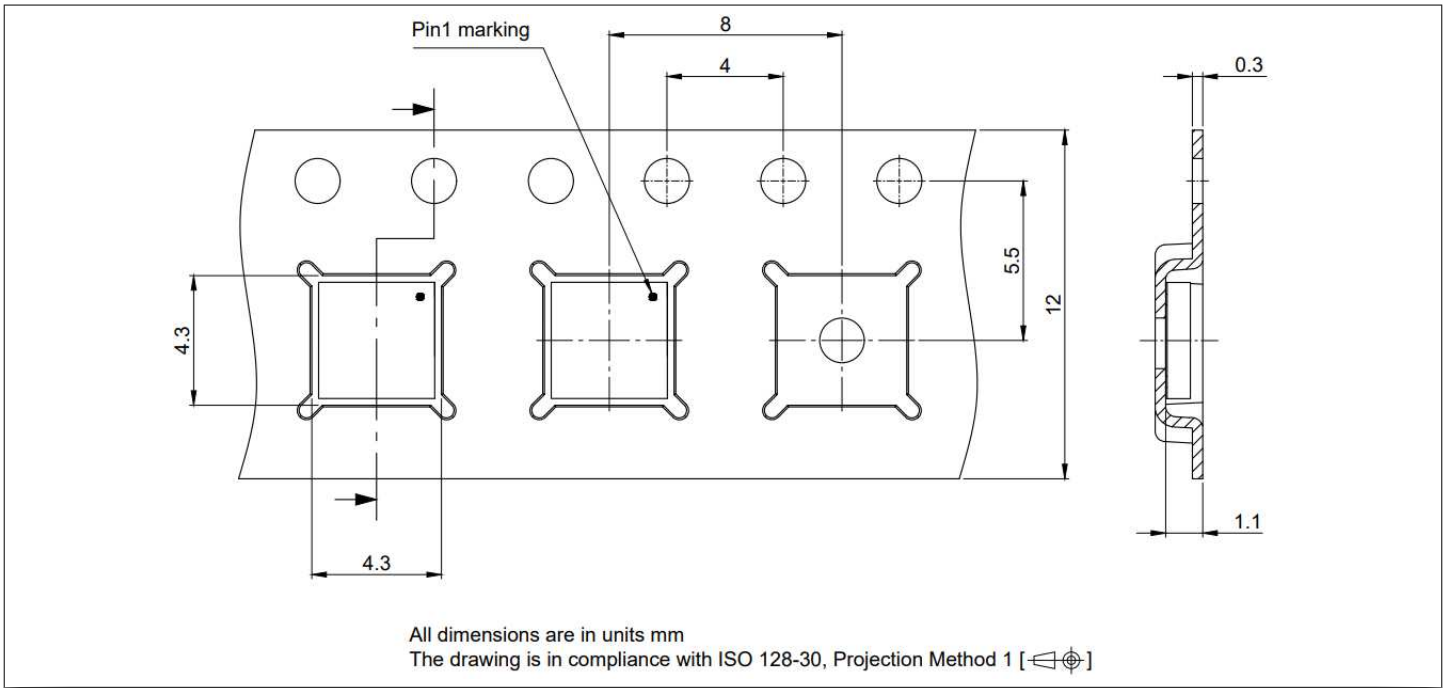

Figure 36 PG-VDSON-8-5 tape and reel

8.2 PG-VSON-10-4

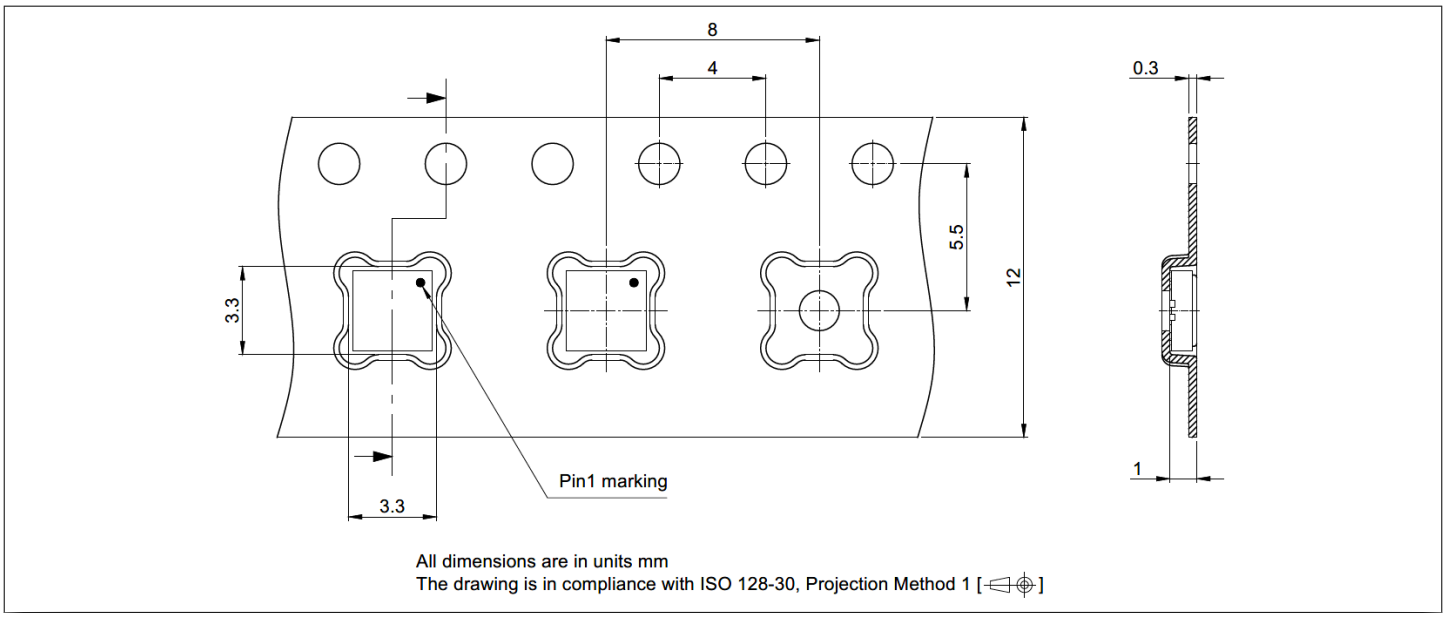

Figure 37 PG-VSON-10-4 tape and reel

8.3 PG-VDSON-10-2

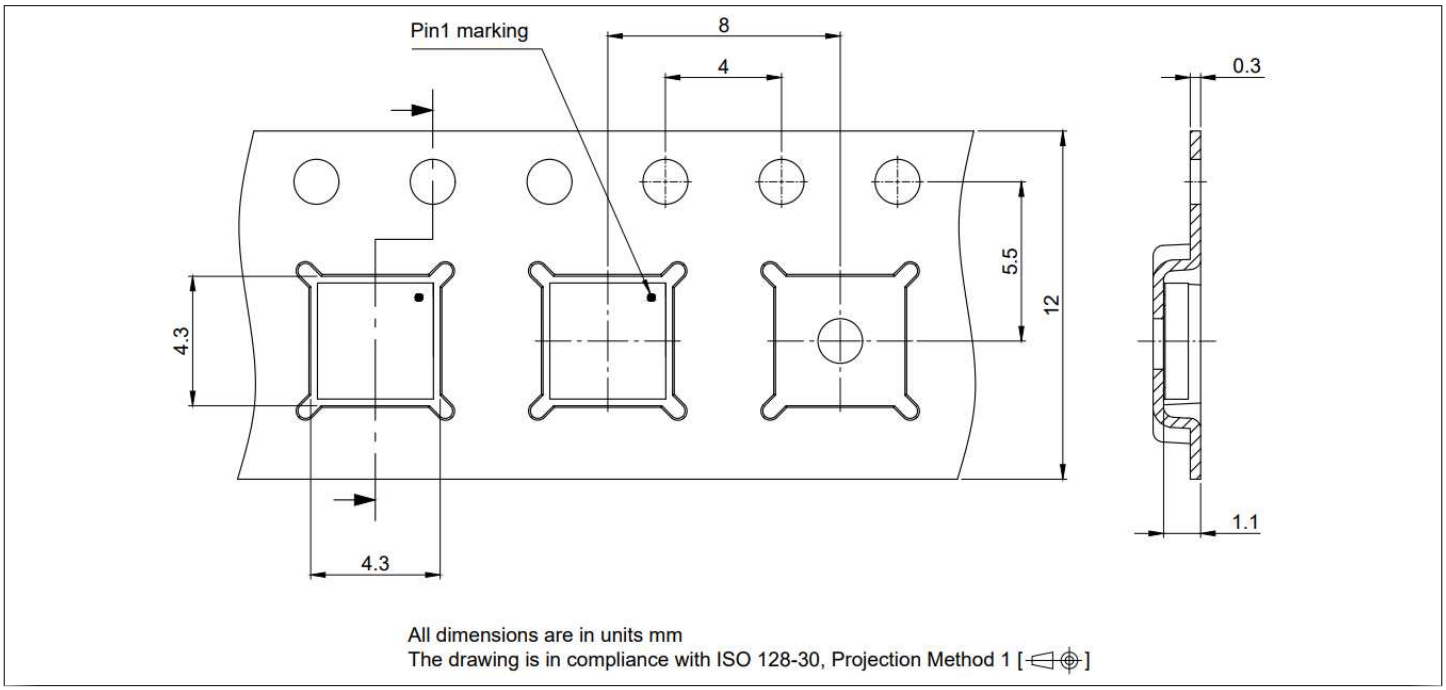

Figure 38 PG-VDSON-10-2 tape and reel

Revision History

2EDL803x

Revision: 2023-04-21, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2023-03-22	Release of final version
2.1	2023-04-21	Modified the EN pin description in the pin and functional description section.

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