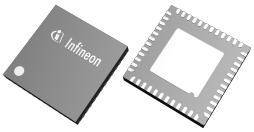
MOTIX™ three-phase smart gate driver

Features



- Three-phase smart gate driver
  - 5.5 V to 70 V recommended operating voltage
  - 1.5 A sink / 1.5 A source peak gate driver currents, with SPI programmable independent high-side/low-side slew rate control
  - Programmable driving voltage (7 V, 10 V, 12 V, 15 V)
  - Support 1PWM, 3PWM or 6PWM inputs up to 200 kHz
- 600 mA synchronous buck converter, 300 mA LDO (3.3 V or 5 V), and dual charge pumps
- Three current sense amplifiers with adjustable gain and offset, for shunt resistor or R_{DSON} sensing
- ADC for signal monitoring
- Protections with VDS sensors, OCPs, UVLOs, OVLOs, OTW, OTS, watchdog timers, locked rotor detection, and so on
- Thermally enhanced 48-pin VQFN package

Potential applications

- Battery powered power tools and gardening tools
- Robotic lawn mowers
- Electric bicycles
- Robotics, RC toys, consumer drones and multicopters
- Pumps and fans
- Other three-phase BLDC and PMSM motors

Product validation

Fully qualified according to JEDEC for industrial applications.

Description

6EDL7151 is a gate driver IC for three-phase BLDC or PMSM motor drive applications. It provides three half-bridge drivers, each capable of driving a high-side and low-side N-type MOSFET.

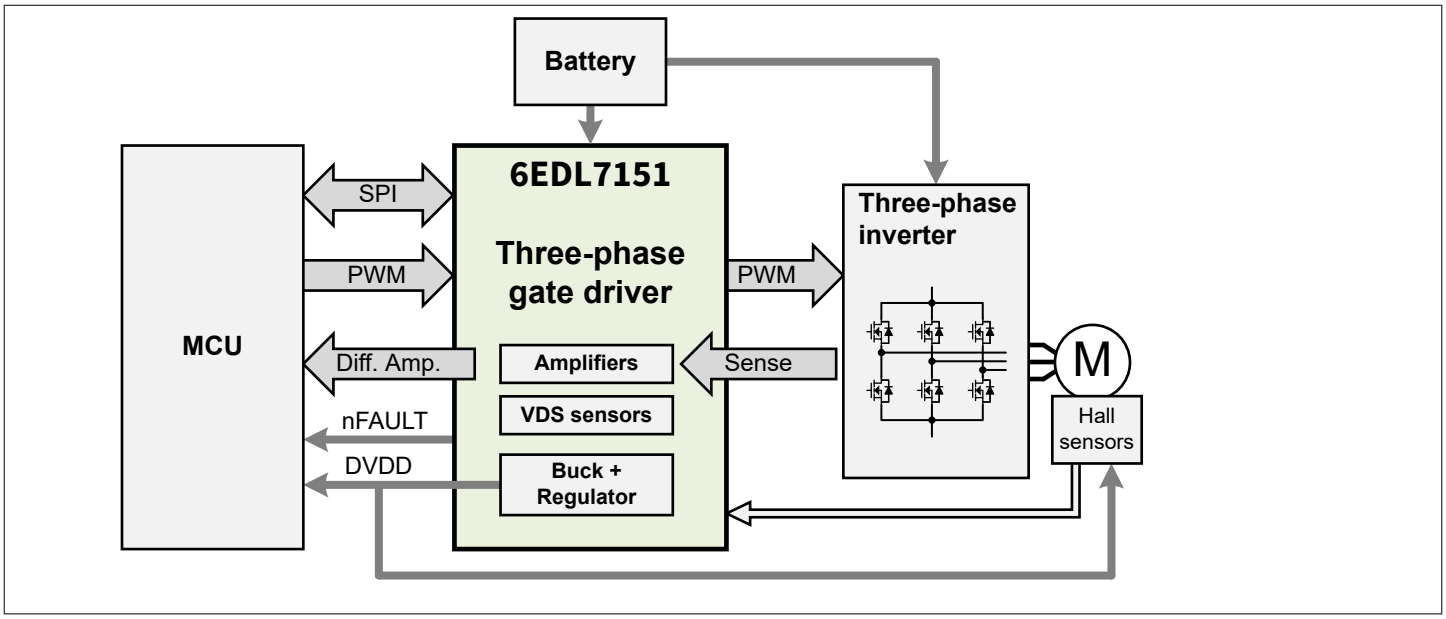
The gate driver is also provided with programmable dead time delays for preventing current shoot through between high-side and low-side switches in normal operation. Separate charge pumps for low- and high-side gate drivers support 100% duty cycle and low voltage supply operation. Supplies for the gate drivers are programmable to one of the following levels: 7 V, 10 V, 12 V or 15 V. Additionally, the slew rate of the driving signal can be programmed with fine granularity to reduce EMI emissions.

An integrated synchronous buck converter provides an efficient supply of current to the rest of the system. However, power tool systems require high precision current measurements, involving a very precise ADC reference voltage. For that purpose, 6EDL7151 uses a linear voltage regulator (up to 300 mA), powered by the buck converter to supply the MCU and other sensitive components in the system. With this advanced power supply architecture, not only the best possible signal quality is achieved, but also the power efficiency is optimized at any input and output condition.

6EDL7151 includes three current sense amplifiers for accurate current measurements that support bidirectional low-side current sensing with programmable gain. R_{DSON} sensing is supported through the internal connection of the phase nodes to the current sense amplifier inputs. Temperature compensation if needed shall be provided by the user application. Outputs of current sense amplifiers support both 3.3 V and 5 V allowing most commercial controllers to be compatible. Low noise, low settling times and high accuracy are the main features of the integrated operational amplifiers. An internal buffer can be used to offset the sense amplifier outputs for optimizing the dynamic range.

The device provides numerous protection features such as highly programmable VDS sensors for inverter MOSFET protection, external brake with programmable braking response, overcurrent protection (OCP) on current sense amplifiers, overcurrent protection (OCP) for buck converter and DVDD linear regulator, undervoltage lockouts (UVLO) for internal and external supplies, overvoltage fault (OVLO) reporting for buck converter and DVDD linear regulator, overtemperature warning and shutdown (OTW and OTS) with independent supply system temperature sensor, and programmable watchdog timers. These features are to monitor the power supply voltages, system parameters, as well as V_{DS} voltages of external power MOSFETs to improve the application robustness during adverse conditions. The failure behavior, threshold voltages, and filter times of the supervisions of the device are adjustable via SPI. Monitored aspects include inverter currents, gate drive voltages and currents, device temperature, and rotor locked. When a fault occurs, the device stops driving and pulls the nFAULT pin low, to prevent system damage or other possible malfunction. This signal can be connected to a microcontroller to inform the processor that a fault has

happened. The microcontroller can request more information on the fault via SPI commands. The integrated SPI interface can be used to configure 6EDL7151 for the application. The SPI provides both detailed fault reporting and flexible parameter settings such as gain of the current sense amplifiers, slew rate control of the gate drivers, various protection features or gate driver voltage.



Product name	Package	Body size	Pin pitch
6EDL7151	PG-VQFN-48-78	7 mm x 7 mm	0.5 mm

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1 Pin configuration and functionality

1.1 Pin configuration

In Figure 1, the pinout of the 6EDL7151 is presented.

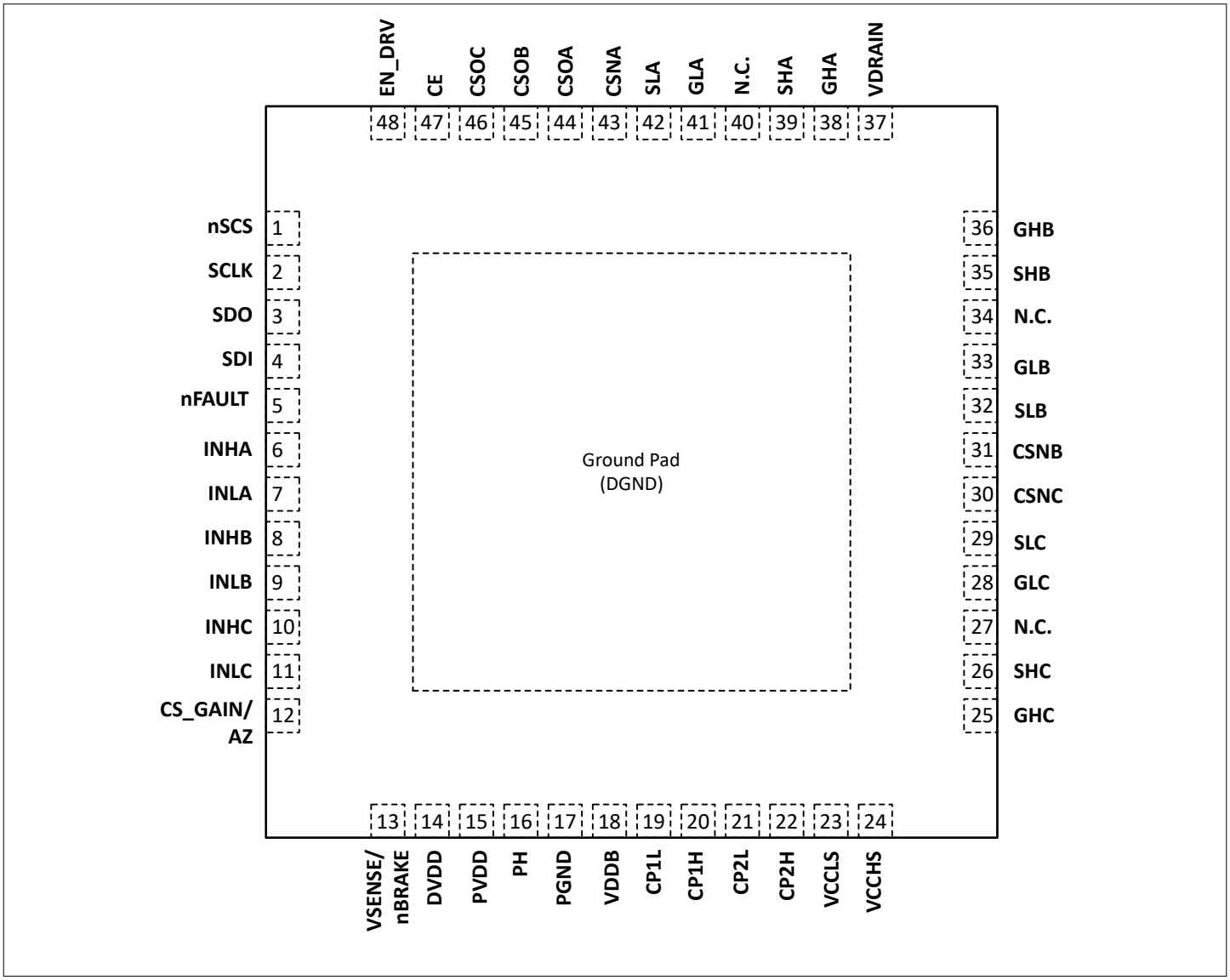

Figure 1 Pin configuration

1.2 Pin definitions and functions

Table 1 describes the characteristics and functionalities assigned to different pins of the 6EDL7151 device.
I: Input, O: Output, IO: Input and/or Output, D: Digital, A: Analog, AD: Analog and/or Digital, P: Power, G: Ground.

Table 1 Pin definition

Pin No.	Pin name	IO	Type	Description
1	nSCS	I	D	Chip select for SPI. Active low.
2	SCLK	I	D	SPI clock signal.

(table continues...)

Table 1 (continued) Pin definition

Pin No.	Pin name	IO	Type	Description
3	SDO	O	D	SPI data output signal.
4	SDI	I	D	SPI data input signal.
5	nFAULT	O	D	When low indicates that a fault has occurred; open drain. Connect external pull-up to MCU power supply.
6	INHA	I	D	PWM input signal for channel A high-side. PWM input for 1PWM modes. Connect to DGND if not used.
7	INLA	I	D	PWM input signal for channel A low-side. Input of Hall sensor A in 1PWM modes. Connect to DGND if not used.
8	INHB	I	D	PWM input signal for channel B high-side. Connect to DGND if not used.
9	INLB	I	D	PWM input signal for channel B low-side. Input of Hall sensor B in 1PWM modes. Connect to DGND if not used.
10	INHC	I	D	PWM input signal for channel C high-side. DIR signal for 1PWM modes. Connect to DGND if not used.
11	INLC	I	D	PWM input signal for channel C low-side. Input of Hall sensor C in 1PWM modes. Connect to DGND if not used.
12	CS_GAIN/ AZ	I	A	Analog programming for the current sense amplifier gain. Dual function as auto-zero: input to control the external auto-zero function.
13	VSENSE/ nBRAKE	I	A/D	Analog programming of DVDD output voltage during start-up. Connect a pull-down resistor R_{SENSE} to select DVDD voltage: $R_{SENSE} \leq 3.3\ k\Omega$ => DVDD = 3.3 V $R_{SENSE} \geq 10\ k\Omega$ => DVDD = 5 V After start-up, the pin is in nBRAKE mode: used for motor braking. Active low.
14	DVDD	–	P	Supply for external MCU, Hall sensors, and so on. Voltage is generated by an integrated linear regulator and defined by VSENSE pin or SPI.
15	PVDD	–	P	Power supply of the device.
16	PH	–	P	Buck phase node voltage. Connect to output inductor.
17	PGND	–	G	Power ground used for buck converter, charge pumps, and gate drivers.
18	VDDB	–	P	Buck output voltage. Connect capacitor between VDDB and PGND.
19	CP1L	–	P	Bottom connection of the charge pump flying capacitor 1.
20	CP1H	–	P	Top connection of the charge pump flying capacitor 1.
21	CP2L	–	P	Bottom connection of the charge pump flying capacitor 2.
22	CP2H	–	P	Top connection of the charge pump flying capacitor 2.

(table continues...)

Table 1 (continued) Pin definition

Pin No.	Pin name	IO	Type	Description
23	VCCLS	–	P	Output of low-side charge pump. Connect a capacitor from VCCLS to PGND.
24	VCCHS	–	P	Output of high-side charge pump. Connect a capacitor from VCCHS to PVDD or PGND.
25	GHC	O	A	High-side gate driving signal for phase C. Not connected or connected to PVDD if not used.
26	SHC	IO	A	High-side source connection (phase node) for phase C. Positive input of current sense amplifier C for R_{DSON} sensing. Not connected if not used.
27	N.C.	–	–	Not connected.
28	GLC	O	A	Low-side gate driving signal for phase C. Not connected if not used
29	SLC	IO	A	Low-side source connection for phase C. Positive input of current sense amplifier C for shunt resistor sensing. Short to PGND if not used.
30	CSNC	I	A	Current sense amplifier negative input for phase C. Short to PGND or DGND if not used.
31	CSNB	I	A	Current sense amplifier negative input for phase B. Short to PGND or DGND if not used
32	SLB	IO	A	Low-side source connection for phase B. Positive input of current sense amplifier B for shunt resistor sensing. Short to PGND if not used.
33	GLB	O	A	Low-side gate driving signal for phase B. Not connected if not used.
34	N.C.	–	–	Not connected.
35	SHB	IO	A	High-side source connection (phase node) for phase B. Positive input of current sense amplifier B for R_{DSON} sensing. Not connected if not used.
36	GHB	O	A	High-side gate driving signal for phase B. Not connected or connected to PVDD if not used.
37	VDRAIN	I	A	High-side drain, the common sense pin for high-side VDS sensors
38	GHA	O	A	High-side gate driving signal for phase A. Not connected or connected to PVDD if not used.
39	SHA	IO	A	High-side source connection (phase node) for phase A. Positive input of current sense amplifier A for R_{DSON} sensing. Not connected if not used.
40	N.C.	–	–	Not connected.
41	GLA	O	A	Low-side gate driving signal for phase A. Not connected if not used.

(table continues...)

Table 1 (continued) Pin definition

Pin No.	Pin name	IO	Type	Description
42	SLA	IO	A	Low-side source connection for phase A Positive input of current sense amplifier A for shunt resistor sensing. Short to PGND if not used.
43	CSNA	I	A	Current sense amplifier negative input for phase A. Short to PGND or DGND if not used.
44	CSOA	O	A	Current sense amplifier output for phase A. Not connected if not used.
45	CSOB	O	A	Current sense amplifier output for phase B. Not connected if not used.
46	CSOC	O	A	Current sense amplifier output for phase C. Not connected if not used.
47	CE	I	A	Chip enable. Starts up the device upon the rising edge.
48	EN_DRV	I	D	Enables the gate driver section and internal circuitry based on the configuration. Can be configured as a watchdog clock. Internal pull-down.
–	Ground pad	–	G	Ground connection for digital section. Solder to PCB (Printed circuit board).

2 Block diagram

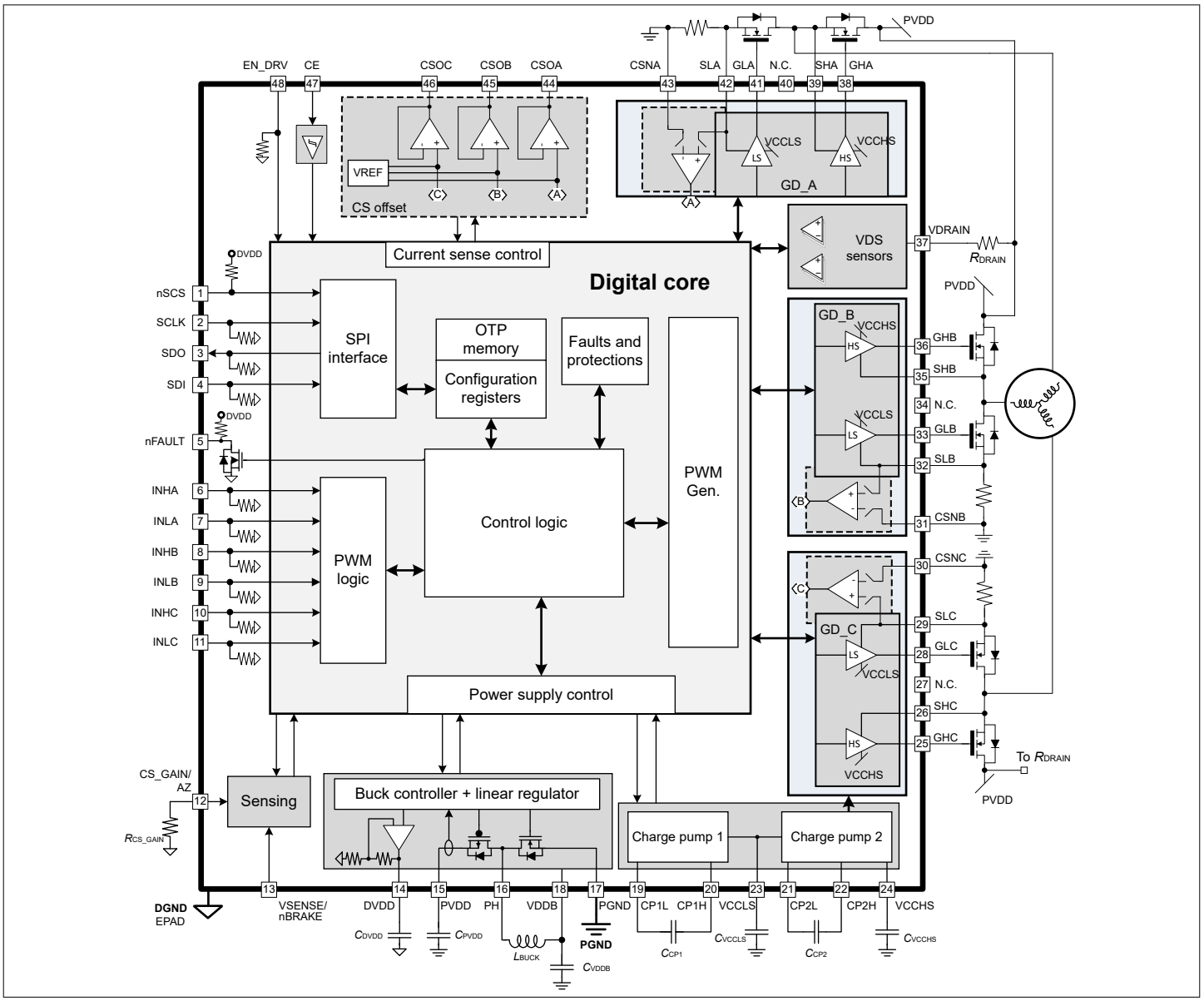

Figure 2 Block diagram

3 Functional description

3.1 PWM modes

6EDL7151 offers four different PWM modes and a subvariant to address different MCU needs. The first mode is 6PWM and drives the gate driver in a classic way by using six PWM signals from the MCU. 6EDL7151 implements additionally three other modes, where it applies intelligence to simplify the PWM generation on the microcontroller side. Together with integrated protection features it results in a highly robust and faster development for drive applications. An intelligent dead time unit ensures that no shoot-through happens at any condition. A highly configurable braking mode provides a safe reaction to motor or system events.

6EDL7151 supports the following PWM modes that can be selected via the bitfield PWM_MODE:

1. 6PWM
2. 3PWM
3. 1PWM and commutation pattern
4. 1PWM with Hall sensor commutation
5. 1PWM with Hall sensor commutation and alternating recirculation

The following subsections provide further details for each of these PWM modes and sub-modes.

***Note**:* *It is possible to use only one or two phases instead of all three phases, for example in a full bridge configuration. For such cases, it is recommended to keep INHx and INLx signals of the unused phases shorted to DGND and the corresponding GHx, GLx, SHx and SLx signals open.*

3.1.1 PWM with six independent inputs - 6PWM

If PWM_MODE is set to b000, then 6EDL7151 is configured for six independent PWM inputs. In this mode, the microcontroller (MCU) provides three pairs of complementary PWM signals with dead time between high-side and low-side PWM. For safety reasons, a minimum dead time is observed by 6EDL7151 to prevent strong shoot-through conditions.

VSENSE/nBRAKE pin can be used to brake the motor in a controlled manner. See Chapter 3.1.6 for more information on PWM braking modes.

Table 2 shows the truth table for 6PWM mode while Figure 3 shows a system diagram for this mode.

Table 2 Truth table for 6PWM mode

INHx	INLx	VSENSE/nBRAKE	GHx	GLx	SHx
1	1	1	LOW	LOW	High-Z
1	0	1	HIGH	LOW	HIGH
0	1	1	LOW	HIGH	LOW
0	0	1	LOW	LOW	High-Z
X	X	0	Brake cfg.	Brake cfg.	Brake cfg.

***Note**:* *X means any level.*

***Note**:* *The brake function can be configured to switch on all low-side MOSFETs, all high-side MOSFETs, alternate between these two options, or set all outputs to high-Z.*

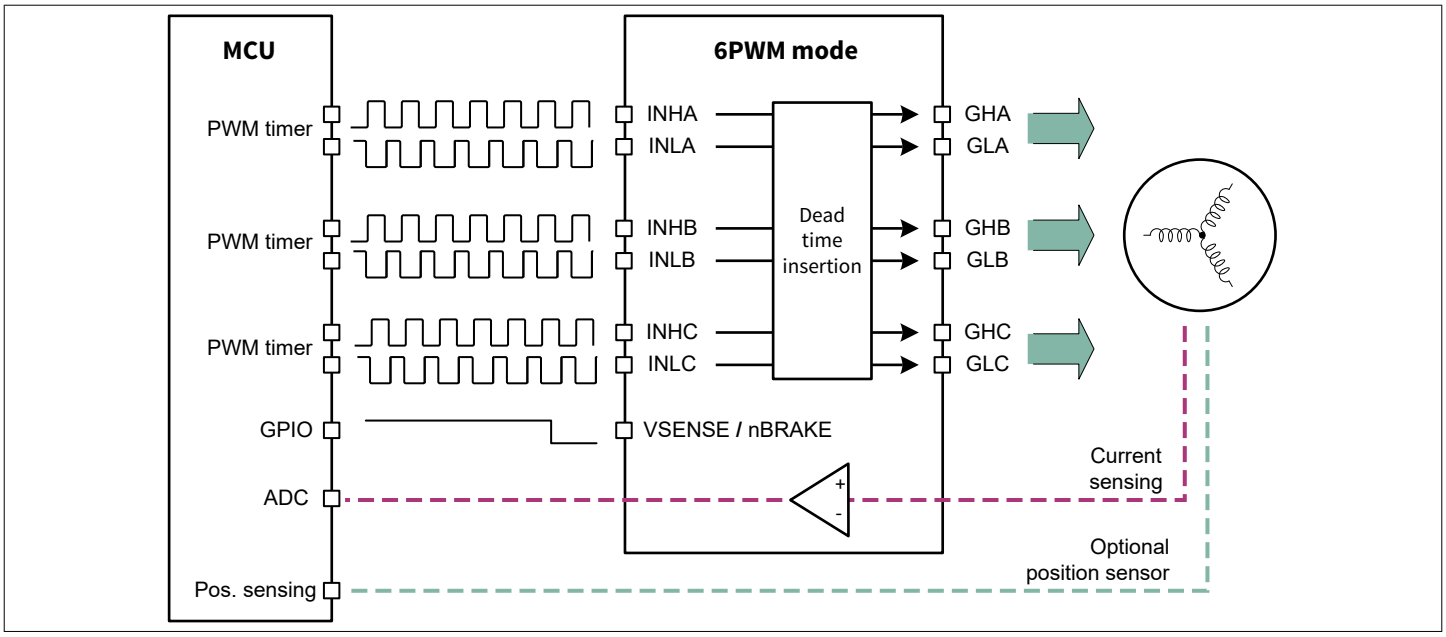

Figure 3 6PWM mode scheme

3.1.2 PWM with three independent inputs - 3PWM

The 6EDL7151 can be configured to 3PWM mode by setting the PWM_MODE bitfield to b001. In such a case, only one input PWM signal (high-side) per phase is necessary. The 6EDL7151 automatically generates the low-side signals according to Table 3 and inserts a configurable dead time. The dead time is independently programmable for high to low (fall of phase node voltage) and low to high (rise of phase voltage) transitions through the bitfields DT_RISE and DT_FALL.

INLx signals can be ignored in this mode.

The VSENSE/nBRAKE pin may be used for braking the motor. See Chapter 3.1.6 for more information on braking modes. Figure 4 depicts a system diagram for this PWM mode.

Table 3 Truth table for 3PWM mode

INHx	INLx	VSENSE/nBRAKE	GHx	GLx	SHx
1	0	1	HIGH	LOW	HIGH
0	0	1	LOW	HIGH	LOW
X	1	1	LOW	LOW	High-Z
X	X	0	Brake cfg.	Brake cfg.	Brake cfg.

***Note**: X means any level.*

***Note**: The brake function can be configured to switch on all low-side MOSFETs, all high-side MOSFETs, alternate between these two options, or set all outputs to high-Z.*

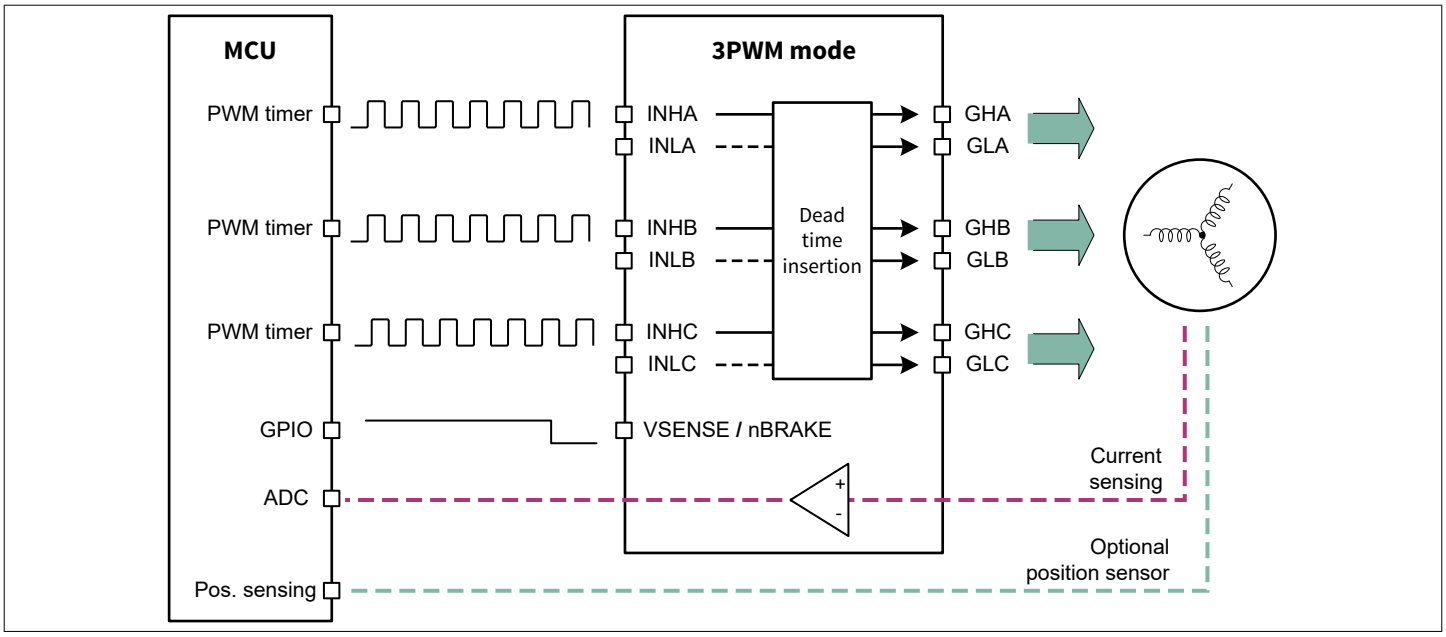

Figure 4 3PWM mode scheme

3.1.3 PWM with one input and commutation pattern - 1PWM

When PWM_MODE is set to b010, 6EDL7151 is configured to 1PWM mode. In this case, the duty cycle and frequency of signal INHA is used to determine the duty cycle (or amplitude) and the frequency of the PWM outputs generated by 6EDL7151. The rest of the inputs are captured to decide the commutation pattern or state of the outputs. INHC signal can be used to implement 12-step trapezoidal commutation (also called block commutation). Dead time is automatically inserted according to programmed values in the bitfields DT_RISE and DT_FALL.

Figure 5 shows a system diagram of 1PWM mode.

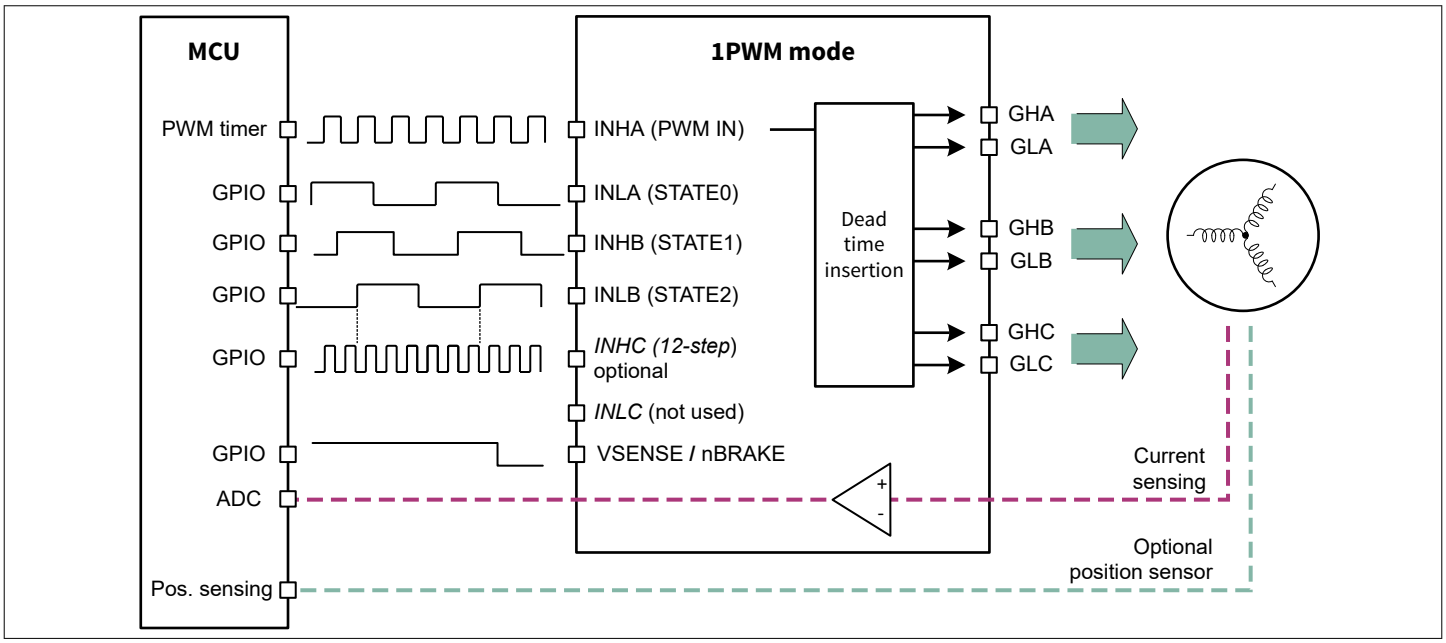

Figure 5 1PWM mode scheme

Additionally, the user has the option to select between two main commutation schemes programmable via the register bitfield PWM_FREEW_CFG:

- **Diode freewheeling** - bitfield PWM_FREEW_CFG = b1: In this case, the freewheeling current flows through the low-side MOSFET body diodes. The truth table for this mode is shown in Table 4.
- **Active freewheeling** - bitfield PWM_FREEW_CFG = b0: In this case, the low-side MOSFETs are switched synchronously to reduce conduction losses on the body diode conduction. The truth table for this mode is shown in Table 5.

Table 4 Truth table for 1PWM mode with diode freewheeling

State	INLA, INHB, INLB,	INHC	VSENSE/ nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
AB	011	0	1	PWM	LOW	LOW	HIGH	LOW	LOW	HIGH	LOW	-
AB_CB	*010*	*1*	*1*	*PWM*	*LOW*	*LOW*	*HIGH*	*PWM*	*LOW*	*HIGH*	*LOW*	*HIGH*
CB	010	0	1	LOW	LOW	LOW	HIGH	PWM	LOW	-	LOW	HIGH
CB_CA	*110*	*1*	*1*	*LOW*	*HIGH*	*LOW*	*HIGH*	*PWM*	*LOW*	*LOW*	*LOW*	*HIGH*
CA	110	0	1	LOW	HIGH	LOW	LOW	PWM	LOW	LOW	-	HIGH
CA_BA	*100*	*1*	*1*	*LOW*	*HIGH*	*PWM*	*LOW*	*PWM*	*LOW*	*LOW*	*HIGH*	*HIGH*
BA	100	0	1	LOW	HIGH	PWM	LOW	LOW	LOW	LOW	HIGH	-
BA_BC	*101*	*1*	*1*	*LOW*	*HIGH*	*PWM*	*LOW*	*LOW*	*HIGH*	*LOW*	*HIGH*	*LOW*
BC	101	0	1	LOW	LOW	PWM	LOW	LOW	HIGH	-	HIGH	LOW
BC_AC	*001*	*1*	*1*	*PWM*	*LOW*	*PWM*	*LOW*	*LOW*	*HIGH*	*HIGH*	*HIGH*	*LOW*
AC	001	0	1	PWM	LOW	LOW	LOW	LOW	HIGH	HIGH	-	LOW
AC_AB	*011*	*1*	*1*	*PWM*	*LOW*	*LOW*	*HIGH*	*LOW*	*HIGH*	*HIGH*	*LOW*	*LOW*
Align	111	X	1	PWM	LOW	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Stop	000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
Brake	XXX	X	0	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.

***Note**: X means any level.*

***Note**: SHx HIGH means that the SHx pin is switching between GND and the DC bus voltage or battery voltage according to PWM signals. '-' represents a floating state, meaning both high-side and low-side MOSFETs are OFF.*

***Note**: The brake function can be configured to switch on all low-side MOSFETs, all high-side MOSFETs, alternate between these two options or set all outputs to high-Z.*

Table 5 Truth table for 1PWM mode with active freewheeling

State	INLA, INHB, INLB,	INHC	VSENSE/ nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
AB	011	0	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-

(table continues...)

Table 5 (continued) Truth table for 1PWM mode with active freewheeling

State	INLA, INHB, INLB,	INHC	VSENSE/ nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
AB_CB	*010*	*1*	*1*	PWM	!PWM	LOW	HIGH	PWM	!PWM	HIGH	LOW	HIGH
CB	010	0	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
CB_CA	*110*	*1*	*1*	LOW	HIGH	LOW	HIGH	PWM	!PWM	LOW	LOW	HIGH
CA	110	0	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
CA_BA	*100*	*1*	*1*	LOW	HIGH	PWM	!PWM	PWM	!PWM	LOW	HIGH	HIGH
BA	100	0	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
BA_BC	*101*	*1*	*1*	LOW	HIGH	PWM	!PWM	LOW	HIGH	LOW	HIGH	LOW
BC	101	0	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
BC_AC	*001*	*1*	*1*	PWM	!PWM	PWM	!PWM	LOW	HIGH	HIGH	HIGH	LOW
AC	001	0	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
AC_AB	*011*	*1*	*1*	PWM	!PWM	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Align	111	X	1	PWM	!PWM	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Stop	000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
Brake	XXX	X	0	Brake cfg.	Brake cfg	Brake cfg	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.

***Note**: X means any level.*

***Note**: SHx HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. '-' is floating state, meaning both high-side and low-side MOSFETs are OFF.*

***Note**: The brake function can be configured to switch on all low-side MOSFETs, all high-side MOSFETs, alternate between these two options or set all outputs to high-Z.*

3.1.3.1 12-step trapezoidal commutation

Input INHC can be optionally used to create a 12-step trapezoidal commutation. This method energizes two or three phases at the same time in contrast to a typical 6-step trapezoidal commutation where only two phases are energized at any time. In the 12-step trapezoidal commutation, torque ripple is improved and the angle created between stator and rotor flux vectors can be controlled within 30º (electrical angle, the same below) accuracy instead of 60º in 6-step trapezoidal commutation. This method improves motor efficiency and torque ripple, however it requires additional position information. This information can be processed by a microcontroller to produce the signals INHA, INLA, INHB, INLB and INHC according to Table 4 or Table 5. As can be seen, from a system perspective, the INHC signal must toggle at every 30º rotation.

In case the INHC signal is not toggled, the device applies the commutation as shown in to Table 4 or Table 5.

As an example, if INHC is left low, a classic 6-step trapezoidal commutation pattern are produced. In case INHC is pulled high, the pattern shows a 30º advance with respect to a standard 6-step trapezoidal commutation. The user can use these variants or toggle the INHC pin every 30º of rotation to create a 12-step commutation pattern.

VSENSE/nBRAKE pin can be used for braking the motor. See Chapter 3.1.6 for more information on braking modes. Below is a summary of inputs and output functionalities:

- INHA - PWM input, defines PWM output duty cycle and frequency
- INLA, INHB, INLB - Provide timing for modulation pattern changes
- INHC - Signalizes 12-step commutation by toggling every 30º, otherwise keep it low (or high) for 6-step commutation
- INLC - This input is ignored in this mode. It is recommended to pull it low
- VSENSE/ nBRAKE signal - When active, 6EDL7151 forces the motor to brake
- GHA, GLA, GHB, GLB, GHC, GLC - Complementary PWM output signals

Table 4 shows the possible states for 1PWM mode with diode freewheeling while Table 5 for active freewheeling.

3.1.4 PWM with one input and commutation with Hall sensor inputs - 1PWM with Hall sensors

6EDL7151 integrates three Hall comparators (Chapter 3.8) to detect the pattern of movement in the motor. This can be used for rotor-locked detection but can also be utilized to drive the PWM commutation pattern automatically allowing a simplified PWM pattern in the MCU. This will enable cost sensitive applications where a low-end controller or some type of simpler circuitry is used basically to create a clock signal for INHA input.

To enable this mode, the PWM_MODE bitfield needs to be configured to value b011. The truth table presented in Table 6 dictates the commutation pattern. In this mode, 6EDL7151 together with Hall sensor inputs decides the switching pattern of the PWM output signals. The duty cycle and frequency of the output signals is determined by INHA duty cycle and frequency. Dead time is inserted automatically according to programmed values in DT_RISE and DT_FALL.

Figure 6 shows a schematic diagram of 1PWM mode with Hall sensors.

In a similar way as in Chapter 3.1.3, the user has the option to select between two main commutation schemes programmable via the bitfield PWM_FREEW_CFG in the PWM_CFG register: diode and active freewheeling. No truth table is shown for diode mode. This can be constructed by substituting “!PWM” cells in Table 6 with “LOW”.

Similarly to other PWM modes, VSENSE/nBRAKE pin can be used for braking the motor. See Chapter 3.1.6 for more information on braking modes.

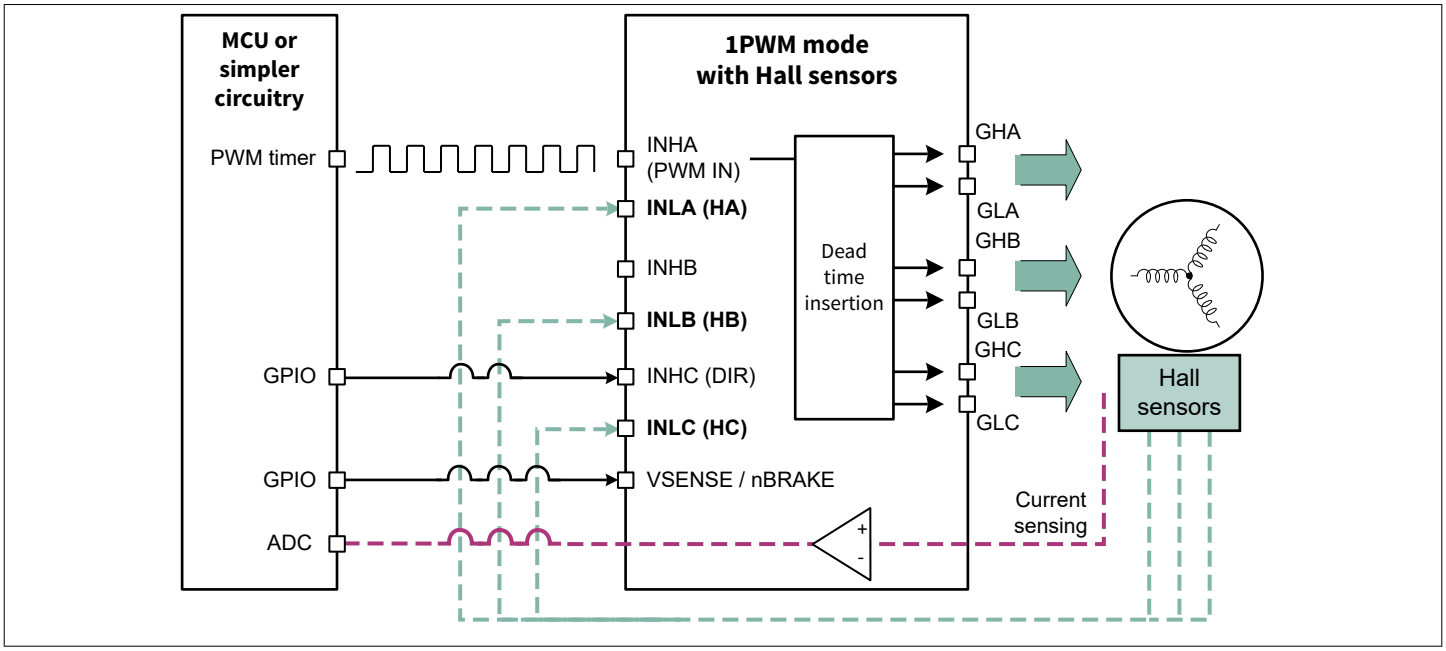

Figure 6 1PWM mode with Hall sensors, self-controlled pattern switching

Table 6 Truth table for 1PWM with Hall sensors, active freewheeling

INLx [A,B,C]	INHC (DIR)	VSENSE / nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
101	1	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
100	1	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
110	1	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
010	1	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
011	1	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
001	1	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
101	0	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
100	0	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
110	0	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
010	0	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
011	0	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
001	0	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
XXX	X	0	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.
111 (Forbidden state)	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
000 (Forbidden state)	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-

***Note**: X means any level. XXX means any other combination on inputs not shown.*

***Note**: SHx HIGH means that the SHx pin is switching between GND and the DC bus voltage or battery voltage. '-' represents a floating state, meaning both high-side and low-side MOSFETs are OFF.*

***Note**: For diode freewheeling mode, substitute "!PWM" cells with "LOW".*

***Note**: The brake function can be configured to switch on all low-side MOSFETs, all high-side MOSFETs, alternate between these two options or set all outputs to high-Z.*

Below are the signal functionality for 1PWM mode with Hall sensors:

- INHA - PWM input, defines the duty cycle and frequency of PWM output signals
- INLA, INLB, INLC - Hall sensor inputs (HA, HB, HC) define the PWM output pattern depending on motor position
- VSENSE/nBRAKE signal - when active, 6EDL7151 forces a brake event
- INHC - Direction (DIR) control. Provided by an MCU to define the direction of motor rotation
- GHA, GLA, GHB, GLB, GHC, GLC - PWM output signals for high-side and low-side

A schematic representation of the commutation states is presented in Figure 7.

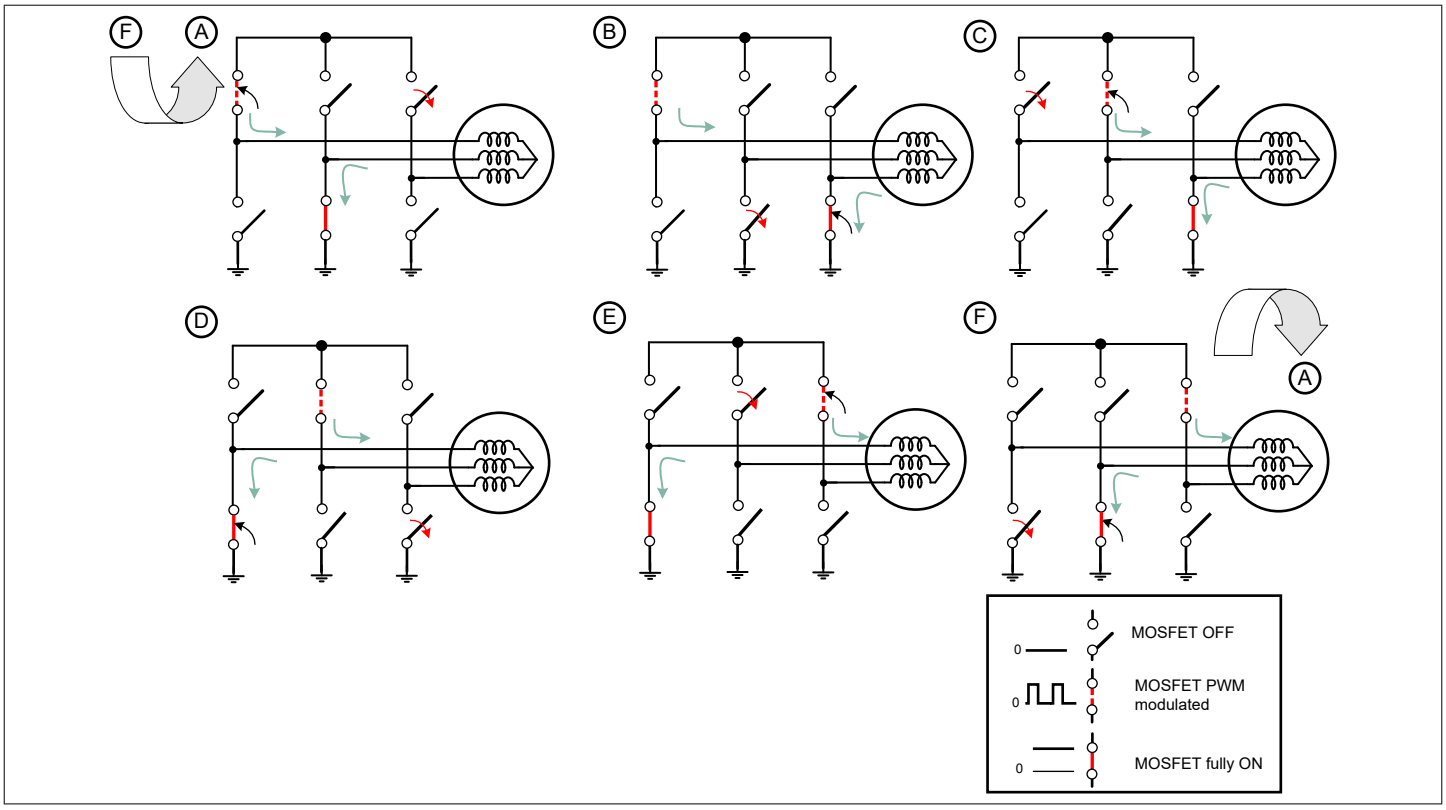

Figure 7 **6-state switching overview, diode freewheeling mode is represented here for simplification, single direction considered**

3.1.5 PWM with one input and commutation with Hall sensor inputs and alternating recirculation - 1PWM with Hall sensors and alternating recirculation

Thermal management in power tools systems is a key factor for achieving higher power densities. A more advance thermal management may allow smaller heat sink components or a smaller PCB area. This PWM mode focuses on distributing the MOSFET stress more evenly between all MOSFETs in the inverter. This concept alternates the recirculation of the freewheeling current between high-side and low-side MOSFETs. This is achieved by extending the truth table shown in Table 6 into Table 7.

On the first rotation (electrical), the inverter recirculates the current through the high-side MOSFETS (PWM modulated MOSFET) and the low-side MOSFET are always ON. In the second electrical rotation, the low-side MOSFETs recirculates the freewheeling current (PWM modulated MOSFET), and therefore, the high-side is the one fully ON. This cycle repeats in further rotations. A graphical representation for the switching states is presented in Figure 8. In this figure, states A to F represent high-side modulation while states G to L represent the low-side modulation. The state machine returns to state A after state L, starting over again the cycle.

PWM_FREEW_CFG configures this mode as well either as diode or active freewheeling. No truth table is shown for the diode mode. This can be constructed by substituting the “!PWM” cells with LOW in Table 7.

Table 7 Truth table for 1PWM mode with Hall sensors, active freewheeling and alternating recirculation

INLx [A,B,C]	VSENSE / nBRAKE	Fully ON	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
INHC (DIR) = 1											
101	1	Low-side	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
100	1	Low-side	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
110	1	Low-side	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
010	1	Low-side	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
011	1	Low-side	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
001	1	Low-side	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
101	1	High-side	HIGH	LOW	LOW	LOW	!PWM	PWM	HIGH	-	LOW
100	1	High-side	LOW	LOW	HIGH	LOW	!PWM	PWM	-	HIGH	LOW
110	1	High-side	!PWM	PWM	HIGH	LOW	LOW	LOW	LOW	HIGH	-
010	1	High-side	!PWM	PWM	LOW	LOW	HIGH	LOW	LOW	-	HIGH

(table continues...)

Table 7 (continued) Truth table for 1PWM mode with Hall sensors, active freewheeling and alternating recirculation

INLx [A,B,C]	VSENSE / nBRAKE	Fully ON	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
011	1	High-side	LOW	LOW	!PWM	PWM	HIGH	LOW	-	LOW	HIGH
001	1	High-side	HIGH	LOW	!PWM	PWM	LOW	LOW	HIGH	LOW	-
INHC (DIR) = 0											
101	1	Low-side	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
100	1	Low-side	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
110	1	Low-side	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
010	1	Low-side	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
011	1	Low-side	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
001	1	Low-side	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
101	1	High-side	!PWM	PWM	LOW	LOW	HIGH	LOW	LOW	-	HIGH
100	1	High-side	LOW	LOW	!PWM	PWM	HIGH	LOW	-	LOW	HIGH
110	1	High-side	HIGH	LOW	!PWM	PWM	LOW	LOW	HIGH	LOW	-
010	1	High-side	HIGH	LOW	LOW	LOW	!PWM	PWM	HIGH	-	LOW
011	1	High-side	LOW	LOW	HIGH	LOW	!PWM	PWM	-	HIGH	LOW
001	1	High-side	!PWM	PWM	HIGH	LOW	LOW	LOW	LOW	HIGH	-
XXX	0	X	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.
111 (Forbidden state)	1	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
000 (Forbidden state)	1	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-

***Note**: X means any level.*

***Note**: SHx HIGH means that the SHx pin is switching between GND and the DC bus voltage or battery voltage. '-' represents a floating state, meaning both high-side and low-side MOSFETs are OFF.*

***Note**: For diode freewheeling mode, substitute "!PWM" cells with "LOW".*

***Note**: The brake function can be configured to switch on all low-side MOSFETs, all high-side MOSFETs, alternate between these two options or set all outputs to high-Z.*

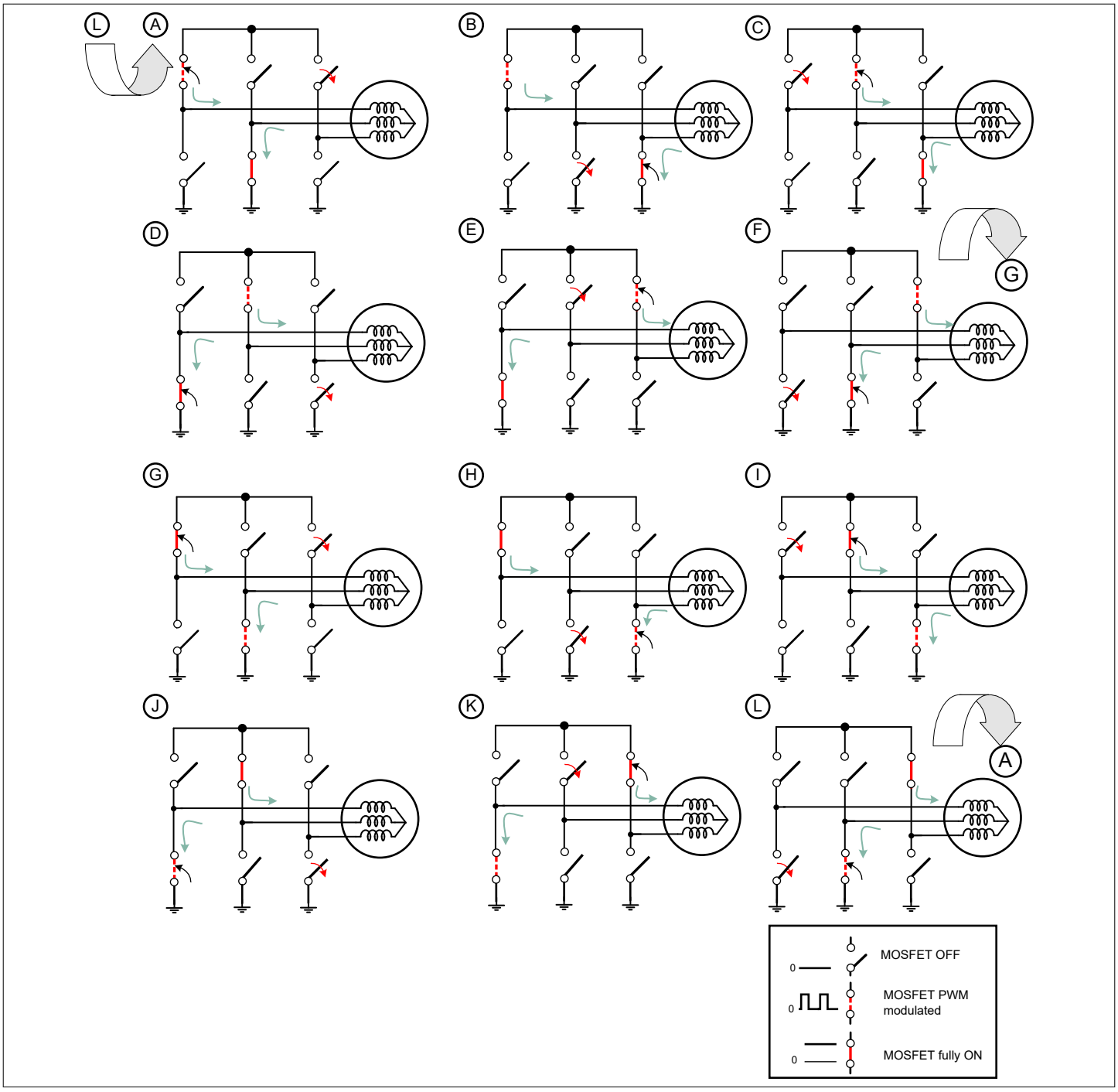

Figure 8 **12-state switching overview for alternating recirculation. Six new states are included (G to L) compared to other 1PWM modes, diode freewheeling mode is represented here for simplification, single direction considered**

3.1.6 PWM braking modes

In all the PWM modes presented previously, the device can go into a controlled braking mode. This braking mode drives the PWM signals in a way that the motor goes to a safe state in a controlled manner. This is of critical importance for some power tool applications where a sudden or uncontrolled braking may destroy elements of the tool or become a hazard to the user. The following events can trigger the braking action in 6EDL7151:

- Pull-low pin VSENSE/nBRAKE
- Programmable overcurrent protection (OCP) fault on current sense amplifiers
- Programmable watchdog timer fault

Of the above, the pin VSENSE/nBRAKE is the only one that can be actively used by, for example, a microcontroller to start a braking event. The other two are the reactions to fault detections.

Pin VSENSE/ nBRAKE shall be high for normal operation of the motor. However, as soon as a low level is detected in it, the gate driver logic activates high-side MOSFETs or low-side MOSFETs, therefore braking the motor actively.

The 6EDL7151 braking circuitry can be configured as illustrated in Figure 9 in the following modes by programming the bitfield BRAKE_CFG in the register PWM_CFG:

- **High-side braking mode**: upon a braking event, all high-side MOSFETs are activated and all low-side MOSFETs are switched off.
- **Low-side braking mode**: upon a braking event, all low-side MOSFETs are activated and all high-side MOSFETs are switched off.
- **Alternate braking mode**: upon every new braking event, the system alternates between high-side braking and low-side braking. With alternate braking, stresses on the MOSFETs are distributed equally, therefore improving the system robustness.
- **Non-power braking mode** - high impedance (high-Z) outputs: upon a braking event all switches are forced to high-Z mode. Currents present in motor windings are recirculate through MOSFET body diodes or other available structures in the inverter. This mode is recommended if a MOSFET short occurs in the inverter.

The system microcontroller (MCU) can modify the brake-related bitfields during the run time of the system to adapt to specific conditions.

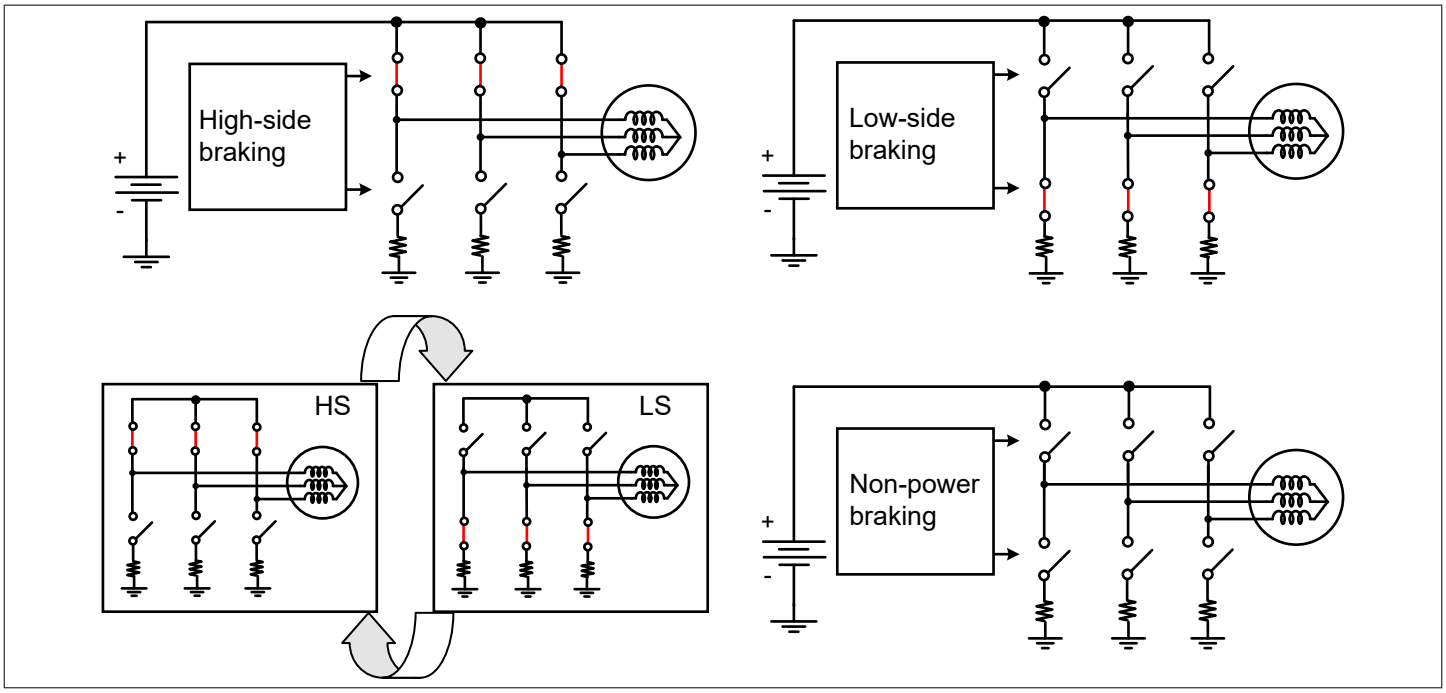

Figure 9 System overview for PWM braking modes

Before the braking action starts, the 6EDL7151 prepares the inverter as fast as possible for a safe braking. Depending on the inverter state at the moment of the braking request, the device needs to switch off some MOSFETs and insert dead times. For example, the braking signal arrives when phase A is high-side switched-off and low-side switched-on, and assuming a high-side braking configuration, then the 6EDL7151 immediately switches off the low-side MOSFET, inserting the configured dead time, and finally switch on the high-side MOSFET of phase A with the rest of high-side MOSFETs.

3.1.7 Dead time insertion

The PWM unit in the 6EDL7151 automatically inserts a dead time between complementary signals (GHx and GLx). The DT_RISE bitfield defines the dead time period for the rising transition (of phase node voltage) while DT_FALL independently defines the dead time for the falling transition. A minimum dead time (see Table 21 for values and conditions) is always observed to prevent a strong shoot-through condition.

Figure 10 shows a detailed timing diagram of 1PWM modes dead time insertion including the timing definitions. A propagation time (t_{PROP_HS} and t_{PROP_LS}) elapses between the input signal and the actual gate driver output signals. These timing definitions are applicable to all other PWM modes.

Dead time and slew rate control features are designed in a safe way so that a change in slew rate updates in a synchronous manner to the PWM switching. This eliminates the possible shoot-through during the possible update of the slew rate during operation due to misalignment of timings.

***Note**:* *Current sense amplifier OCP and VDS sensors can be used to detect the excessive current in the system. Nevertheless, the application software must ensure that dead time is sufficient for the slew rate configuration and the MOSFETs selection.*

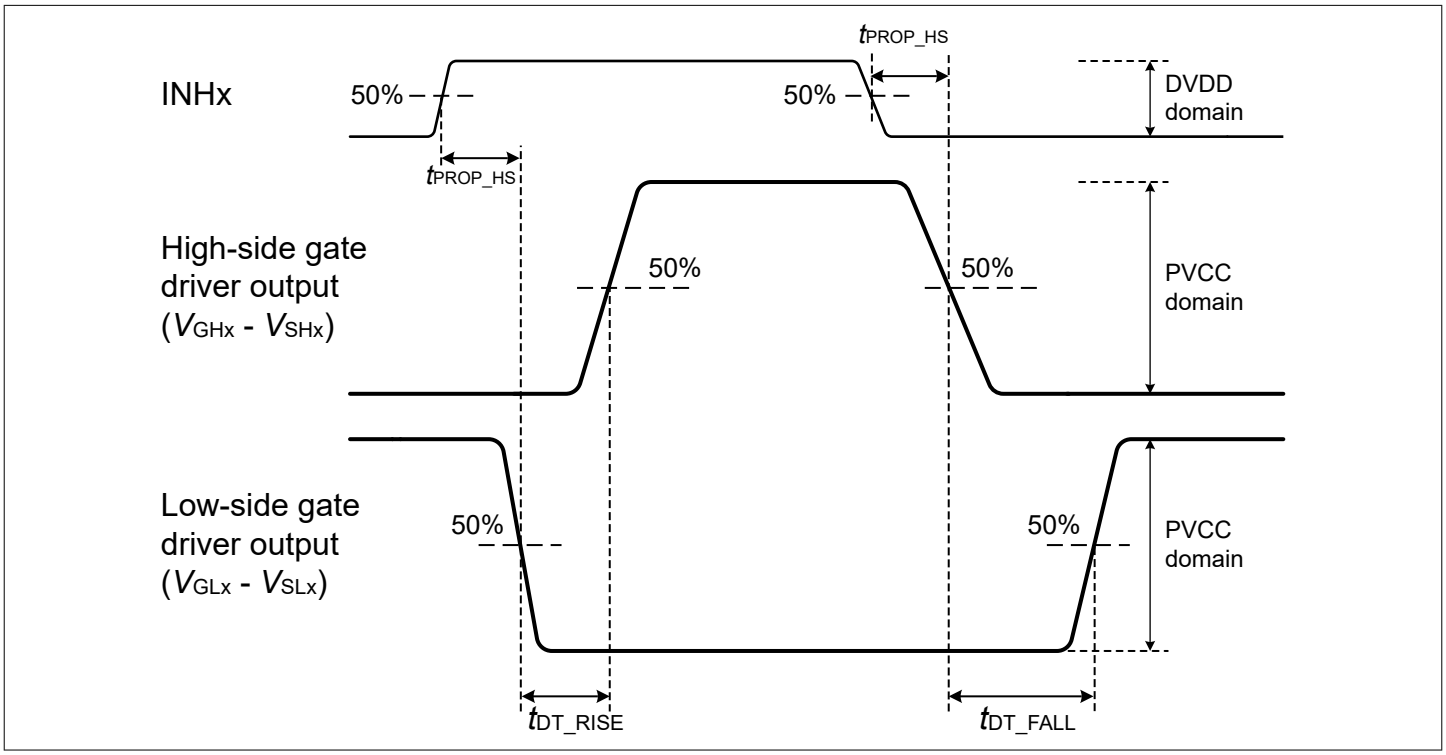

Figure 10 Dead time insertion timing diagram in 1PWM modes

3.2 Three-phase gate driver

The 6EDL7151 three-phase gate driver is a floating driver for a three-phase two-level inverter. It is capable to drive with a configurable slew rate and driving voltage with up to 1.5 A of both sourcing and sinking peak currents. Configurations and settings are shared by all three half-bridge drivers. Programmable charge pumps supply the gate drivers ensuring a 100% duty cycle and configurable driving voltage for maximum optimization of the gate driver. Numerous protections are included to ensure safe operation of the gate driver system under stress conditions, including improved phase node (V_{SHx}) tolerance to negative voltage spikes (see Table 17). This section describes the following features of the integrated three-phase gate driver:

- Gate driver architecture
- Slew rate control
- Gate driver voltage programmability

3.2.1 Gate driver architecture

Three identical pairs of gate drivers are integrated to the device. High-side and low-side drivers are designed with the same architecture. However, supply domains for both sections are designed differently. Precise charge pumps are utilized to supply both drivers, VCCLS to the low-side gate drivers, and VCCHS to the high-side gate drivers. An overview of the general architecture is shown in Figure 11.

The low-side section of the gate driver is supplied by VCCLS. When the device is under normal operation, VCCLS is “PVCC” volts above ground and PVCC voltage is programmable via the SPI registers and defines the gate driving voltage for the inverter power MOSFETs. The VCCLS voltage is generated by the low-side charge pump from VDDB voltage - the integrated buck converter output voltage. An external “flying” capacitor C_{CP1} is required for the charge pump to work properly.

The high-side section of the gate driver is supplied by VCCHS, a separate charge pump that generates “PVCC” volts above PVDD for proper bias of the high-side MOSFET drivers. Similarly to the low-side section, a “flying” capacitor C_{CP2} is necessary for proper operation of the charge pump, and PVCC voltage is programmable via the same SPI register.

Additional "tank" capacitors C_{VCCLS} and C_{VCCHS} are required for VCCLS and VCCHS pins respectively. These and other required components' recommended values are shown in Table 22.

The selection of those capacitors will have impacts in different parameters in the charge pump, including the voltage ripple in VCCLS and VCCHS, as well as the start-up time or the maximum current the gate drivers can supply.

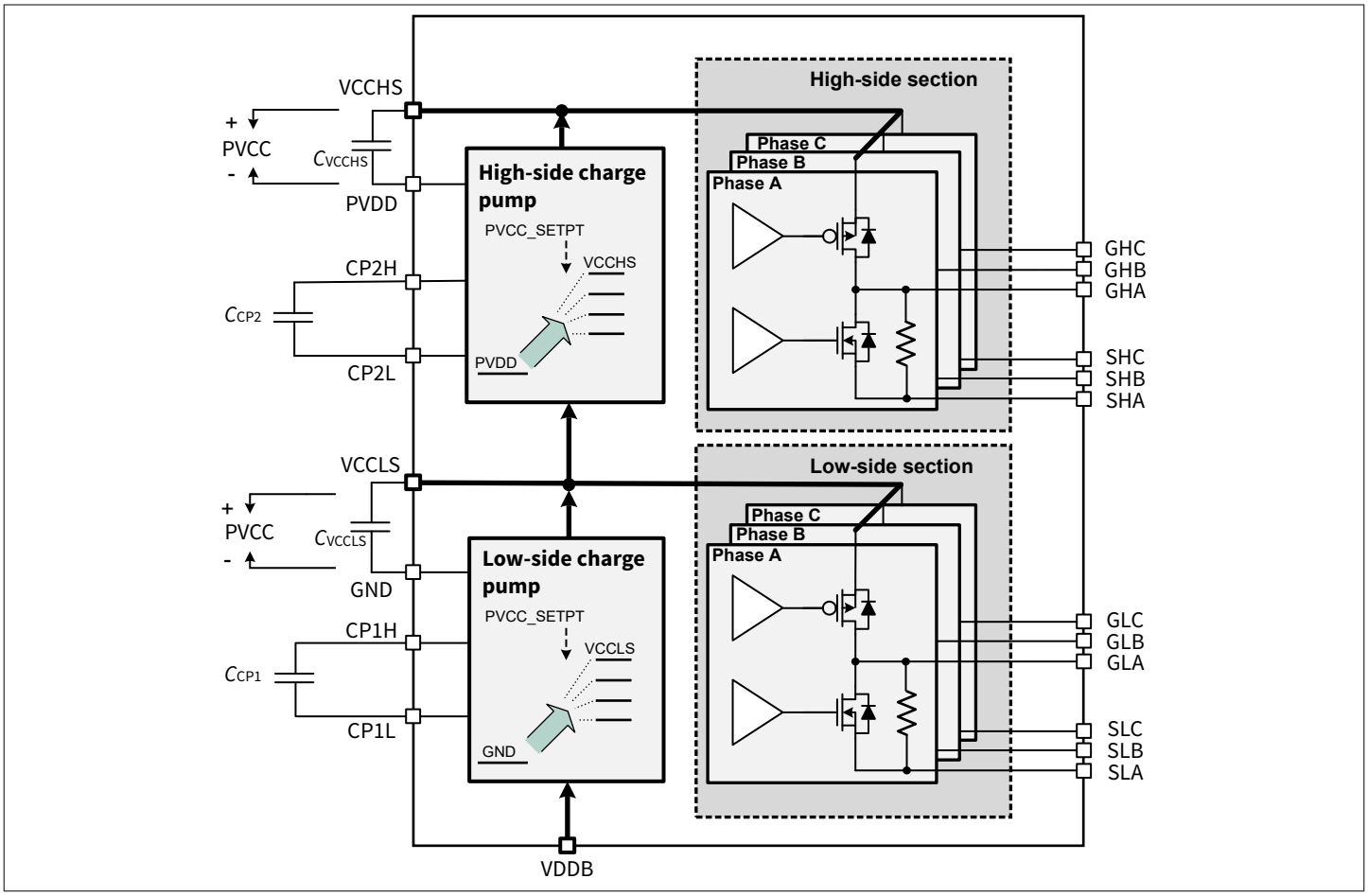

Figure 11 Gate driver architecture overview

3.2.2 Slew rate control

Control of MOSFET V_{DS} rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors like:

- Switching losses
- Dead time optimization
- V_{DS} ringing with possible avalanche event in MOSFETs. Avalanche is a critical factor in MOSFETs that can lead to device destruction or reliability issues
- EMI design and optimizations

- Control of negative spike in SHx pins
- Possible snubber design (MOSFET snubber or bridge bypass capacitors)

6EDL7151 is capable of adjusting the slew rate of the MOSFET switching (V_{DS}). Slew rate control functionality controls independently the rise (low to high) and fall (high to low) slew rates of the drain-to-source voltage by adjusting the gate current applied to MOSFET gate.

***Note**:* *R_g resistors might be used, however, the user must consider the voltage drop on the resistor when driving the MOSFET with the constant current provided by 6EDL7151.*

3.2.2.1 Slew rate control parameters and usage

The user can configure the gate driver current and timings with the following parameters via the SPI-accessible registers:

- I_{HS_SRC} - bitfield IHS_SRC: gate driver current value for switching ON high-side MOSFETs
- I_{HS_SINK} - bitfield IHS_SINK: gate driver current value for switching OFF high-side MOSFETs
- I_{LS_SRC} - bitfield ILS_SRC: gate driver current value for switching ON low-side MOSFETs
- I_{LS_SINK} - bitfield ILS_SINK: gate driver current value for switching OFF low-side MOSFETs
- I_{PRE_SRC} - bitfield I_PRE_SRC: precharge gate driver current value for switching ON both high-side and low-side MOSFETs. Needs to be enabled via the bitfield I_PRE_SRC_DIS, otherwise precharge is set to maximum current
- I_{PRE_SINK} - bitfield I_PRE_SINK: pre-discharge gate driver current value for switching OFF both high-side and low-side MOSFETs. Needs to be enabled via the bitfield I_PRE_SNK_DIS, otherwise pre-discharge is set to maximum current.
- T_{DRIVE1} - bitfield TDRIVE1: amount of time that I_{PRE_SRC} is applied. Shared configuration between high-side and low-side drivers.
- T_{DRIVE2} - bitfield TDRIVE2: amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high-side and low-side drivers.
- T_{DRIVE3} - bitfield TDRIVE3: amount of time that I_{PRE_SINK} is applied. Shared configuration between high-side and low-side drivers.
- T_{DRIVE4} - bitfield TDRIVE4: amount of time that I_{HS_SINK} and I_{LS_SINK} are applied. Shared configuration between high-side and low-side drivers.

A possible configuration is graphically presented in Figure 12. This represents a 6PWM mode in which the microcontroller inserts a specific dead time between the INHx and INLx signals. The driving scheme is applicable to other PWM modes. Propagation delays are not depicted for simplification of the diagram (see Figure 10 for details on propagation delay).

Once the gate is commanded to apply a change to the output, the gate driver applies a constant current defined by the user programmable value I_{PRE_SRC} for a time defined by T_{DRIVE1}. After T_{DRIVE1} period, the MOSFET gate voltage should ideally have reached the threshold voltage ($V_{GS(th)}$). After T_{DRIVE1}, the gate driver applies the next gate current configuration for a period defined by T_{DRIVE2}. The current applied in this period is decisive to determine both dI/dt and dV/dt of the MOSFETs as it charges the Q_{sw} of the MOSFETs. The user can alternatively decide to reduce this period to cover only Q_{gd} portion, therefore controlling dI/dt region with the T_{DRIVE1} period for independent control. To ensure proper fine-tuning, the 6EDL7151 offers separate configuration registers for the high-side and low-side (I_{HS_SRC} and I_{LS_SRC} respectively) for this second period.

Once the T_{DRIVE2} period is elapsed, the gate driver applies full current (1.5 A) to ensure the fastest turn on of the MOSFET. This fully charges the MOSFET gate ($Q_{od} = Q_g - Q_{sw} - Q_{g(th)}$) till the programmed PVCC value.

A similar process takes place in the discharge of the MOSFET.

***Note**:* *Considering that slew rate variations affect the actual dead time value, the user must select dead time accordingly.*

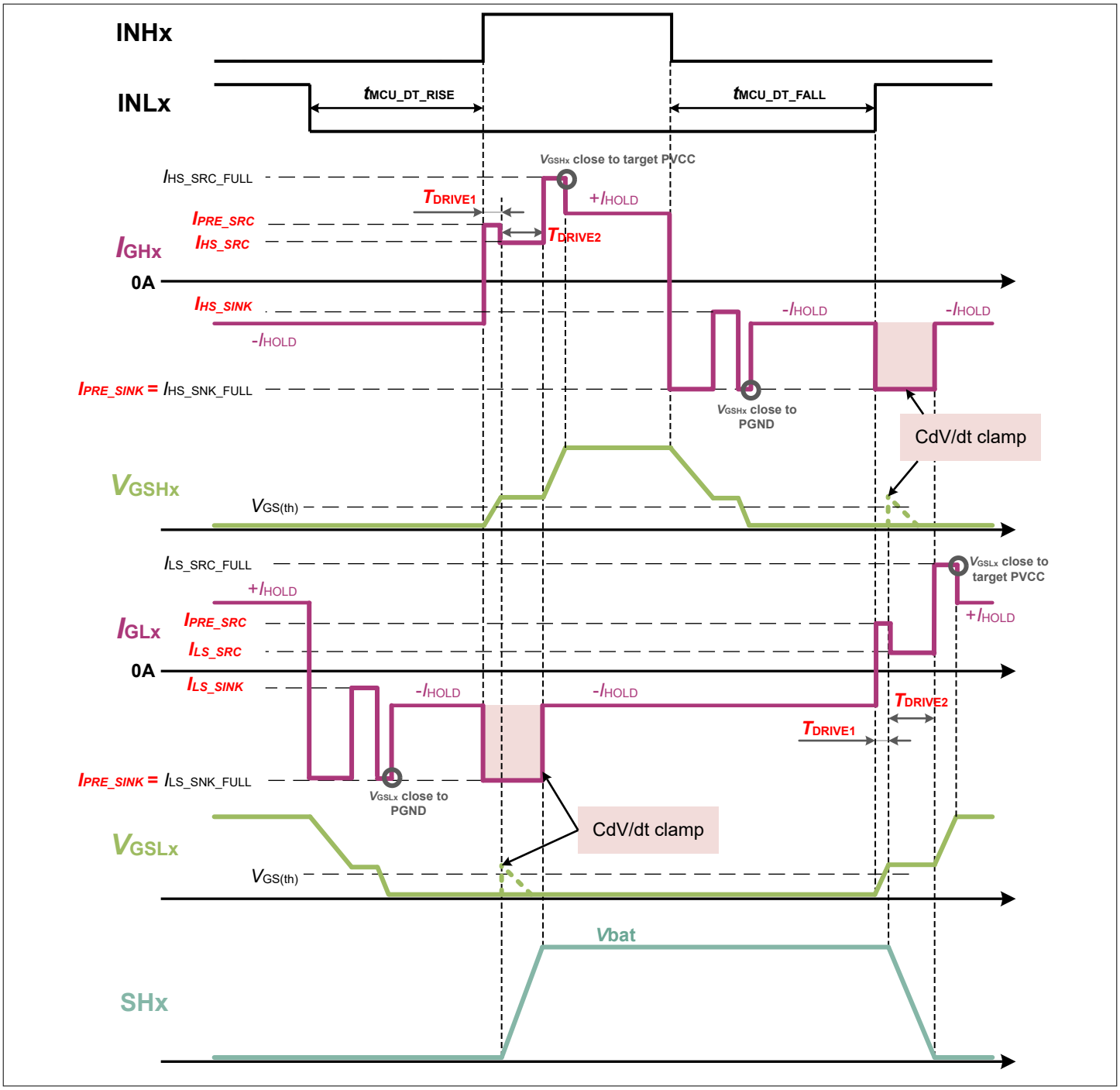

Figure 12 CdV/dt clamp waveforms

3.2.2.2 Gate driver clamping: CdV/dt suppressor

In motor drive applications using a three-phase inverter, it is known that during the turn-on of one MOSFET of the half bridge (high-side or low-side), the complementary MOSFET gate voltage is influenced resulting in a self-turn-on effect possibly creating a shoot-through situation. This is especially critical in the following case: to suppress CdV/dt in a complementary MOSFET, the slew rate controller applies the strongest pull-down current to hold tight the gate to the source when the other MOSFET starts switching.

***Note**: It is expected that V_{GS} still rises, but the strong gate driver setting should help mitigate the risk of $V_{GS(th)}$ crossing.*

The device activates the strong pull-down during both T_{DRIVE1} and T_{DRIVE2} of the complementary signal.

- If T_{DRIVE1} = 0, the start of the strong pull-down is triggered by T_{DRIVE2} start and last for T_{DRIVE2} period.
- If T_{DRIVE2} = 0, the start of the strong pull-down is triggered by T_{DRIVE1} start and last for T_{DRIVE1} period.
- If T_{DRIVE1} = T_{DRIVE2} = 0, the gate driver is activated with 1.5 A current. In this case the suppressor/clamp is not activated.

***Note**:* *If a user wants to use the device as 'slew rate control disabled', he must set T_{DRIVE1} different from 0 and T_{DRIVE2} = 0 to achieve the 1.5 A always setting.*

IDRIVE_PRE_CFG controls the usage of this feature via the bitfield I_CLAMP_DIS. The clamping or suppressor concept is described in Figure 12.

***Note**:* *The current consumption in VCCLS and VCCHS pins can increase when the clamping feature is enabled.*

3.2.2.3 VGS comparators

The gate driver module integrates gate to source comparators as well. These are used to detect when the V_{GS} signal is almost at the target value, that is, $V_{GSx} \geq$ PVCC - $V_{GS\_CMP\_TH}$ during the switching on and $V_{GSx} \leq V_{GS\_CMP\_TH}$ during the switching off. When any of these happen, the comparator trips and sets the gate current to I_{HOLD} value. This is to reduce the power consumption and the impact of the self-turn-on effect, for example, when the high-side MOSFET is turning on while the low-side MOSFET is off. In this case, the hold current for the low-side MOSFET holds the gate of the MOSFET to the source with I_{HOLD} strength. In Figure 13 I_{HOLD} is shown and depending on the V_{GS} value, and will be applied sooner or later. In Figure 14 the thresholds for activating I_{HOLD} current are shown.

The comparator integrates a deglitching stage to prevent the noise to activate the comparator erroneously during noisy events. The deglitching time is defined by $t_{VGS\_CMP\_DEGLITCH}$.

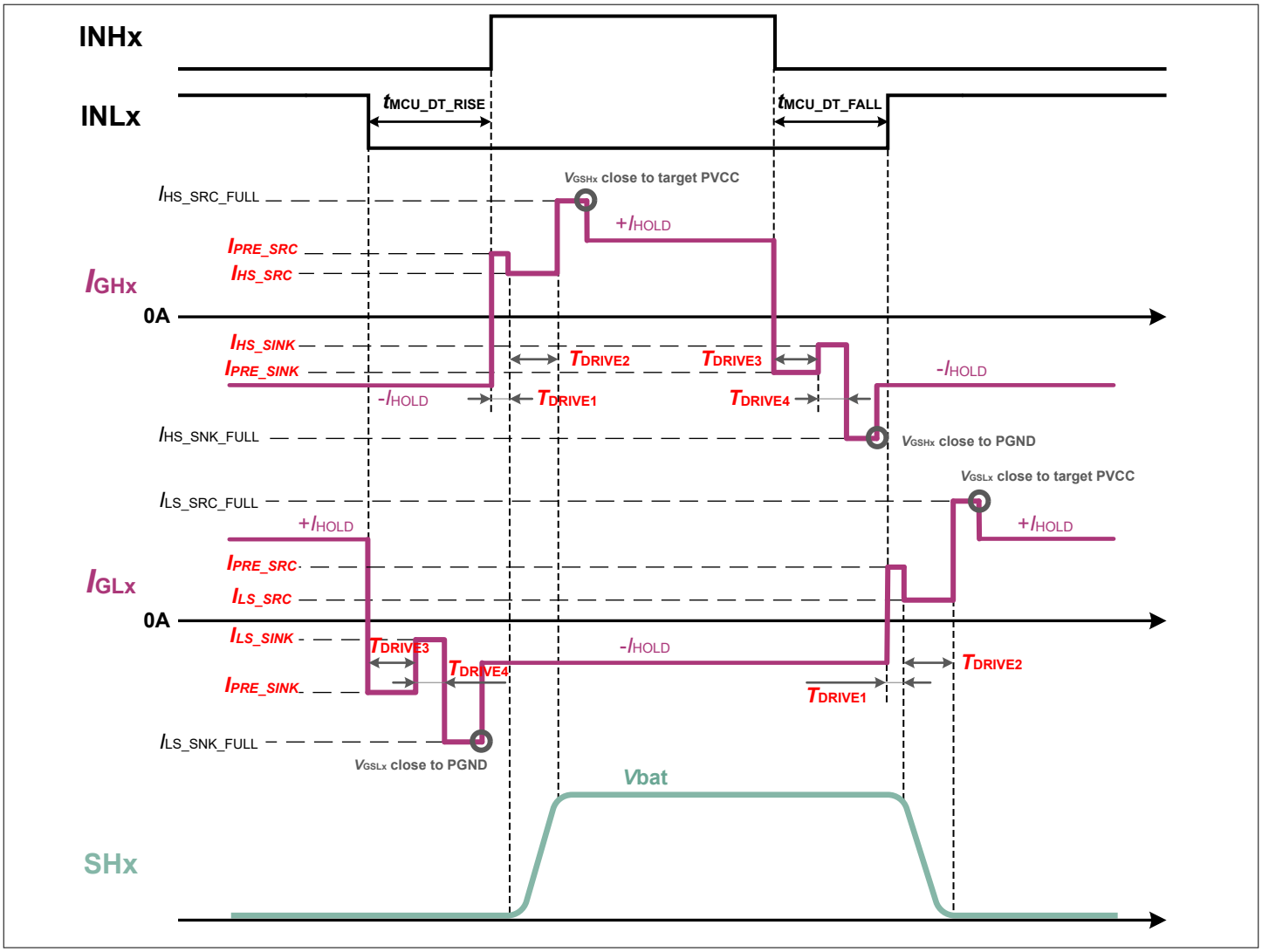

Figure 13 Slew rate control timing for a complete switching cycle on a 6PWM mode, dead time inserted by MCU and propagation delays (INxy->Gxy) not considered for simplification. Parameters in red refer to programmable values

Figure 14 shows details of the charging and discharging transitions for a high-side MOSFET. Similar applies to a low-side MOSFET. The different gate charge areas of the MOSFET are shown. As a result of the flexible timing structure and the high T_{DRIVEx} resolution, the user has full control of the gate current applied during critical charge areas like Q_{sw} which is the key parameter controlling the MOSFET V_{DS} slew rate. This at the same time can be done while maintaining fast charging of other areas like Q_{od} which typically is relatively large compared to Q_{sw} and therefore, as it does not affect neither dV/dt nor dI/dt, can be accelerated by increasing gate current. Additionally, the precharge area ($Q_{g(th)}$), depending on the particular MOSFET, can benefit from a larger gate current than the one applied to the Q_{sw} region where maximum control is required. Using the precharge current configuration, higher gate currents can be selected for $Q_{g(th)}$ reducing importantly the precharge timing, which otherwise could have needed several hundreds of ns to reach to $V_{GS(th)}$.

The precharge current can be selected from 17 different values. 16 defined by $I_{PRE\_SRC/SINK}$ and additionally 1.5 A, which is the maximum peak current capability of the gate driver. In case of large MOSFETs, $Q_{g(th)}$ during turn-on or Q_{od} during turn-off, might benefit from using the whole gate driver capability. To enable the full strength during the precharge area, the bitfields I_PRE_SNK_DIS and I_PRE_SRC_DIS have to be set in the register IDRIVE_PRE_CFG.

***Note**: When transitioning from one current setting to another, the user can experience some transition period until new current value is up and stable. During this period, the current might become lower than programmed for a brief period before reaching the target value.*

***Note**: When the gate to source voltage is getting close to the target voltage, either PVCC when charging or PGND when discharging, the gate driver is not able to fully maintain the target I_G current. This effect deviates from the ideal behavior shown before and can follow similar behavior to the dashed lines in Figure 14. This is independent from the I_{HOLD} values described before.*

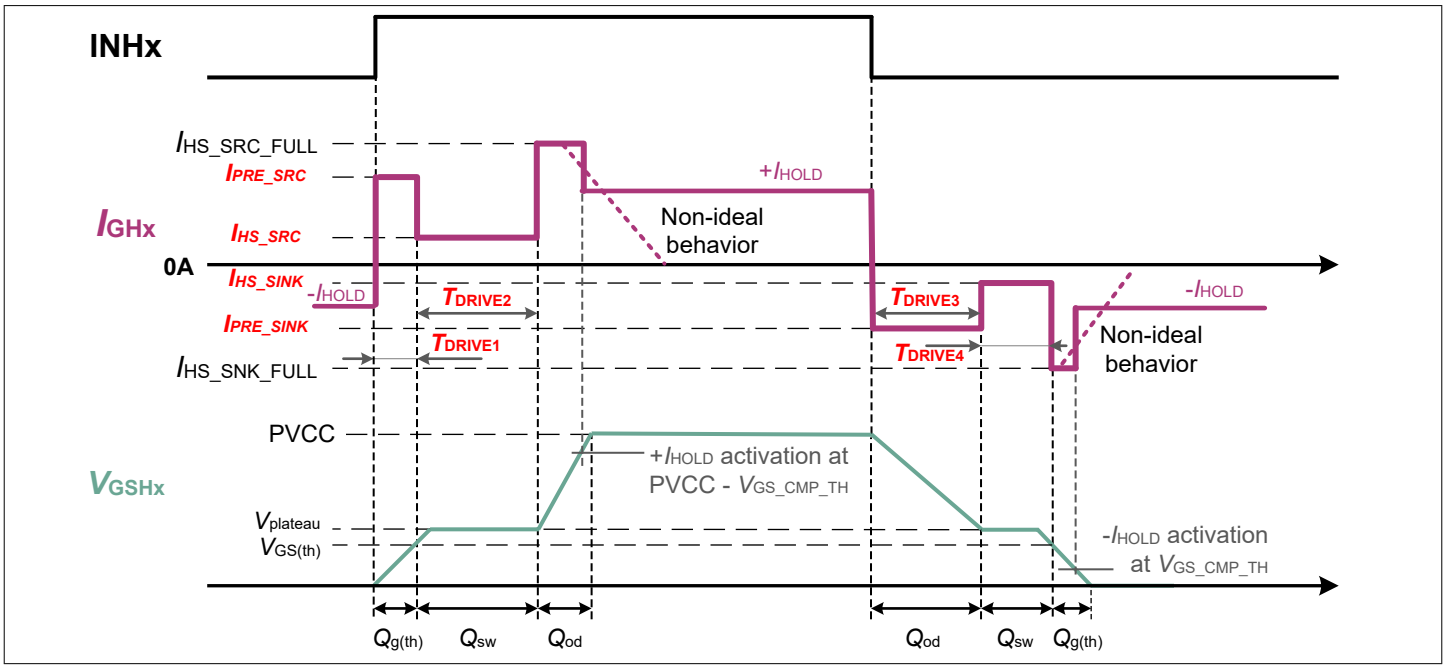

Figure 14 Detail of MOSFET gate charge during the charging and discharging transitions

In cases where $Q_{g(th)}$ is too small to apply a larger current than the one used for slew rate control, the user can set T_{DRIVE2} to value 0. This results in the gate driver start driving the MOSFETs with T_{DRIVE1} and once the period is elapsed it applies 1.5 A ignoring the T_{DRIVE2} configuration. This ensures optimal settings for both large and small MOSFETs and the right fit for different technologies like OptiMOS™ or StrongIRFET™. Similarly, T_{DRIVE2}, T_{DRIVE3} and/or T_{DRIVE4} can be set to 0 resulting in those configurations being skipped.

Figure 15 shows an example of this behavior where T_{DRIVE2} = 0 while other T_{DRIVEx} settings are different from zero.

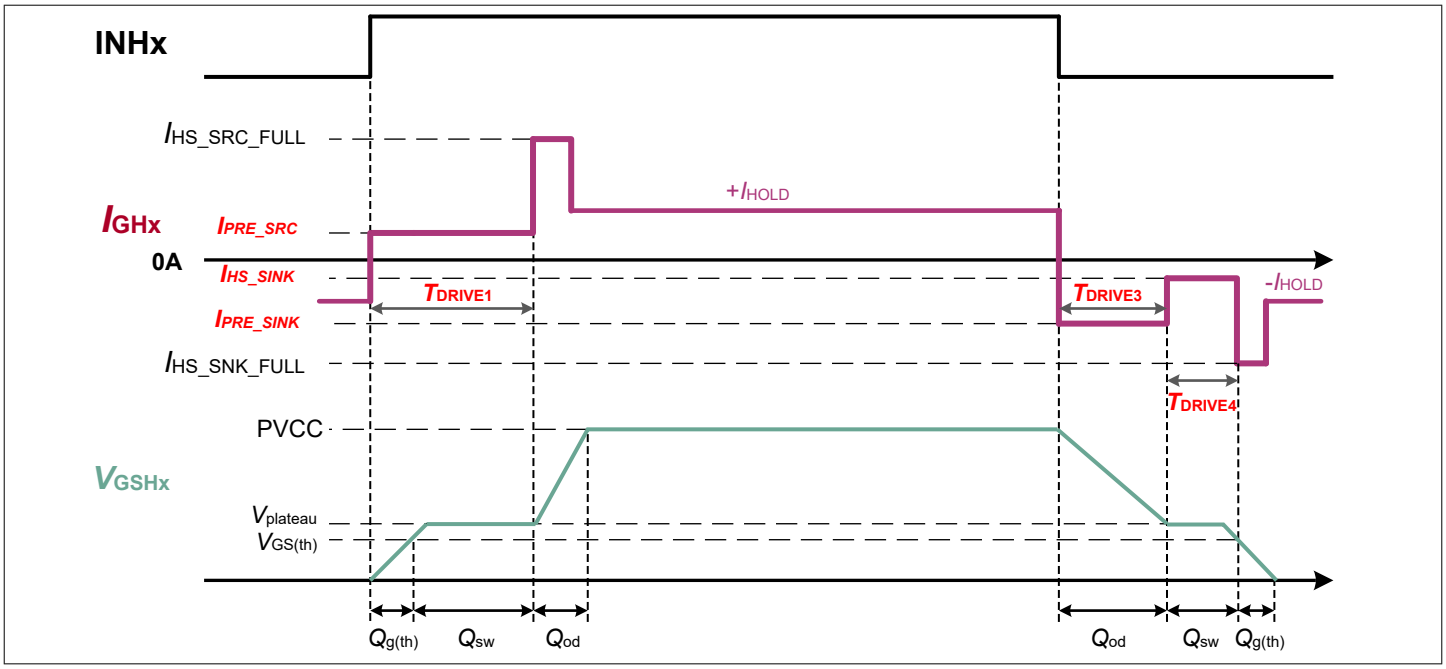

Figure 15 Detail of MOSFET gate charge during the charging and discharging transitions. T_{DRIVE2} = 0 as example

3.2.3 Gate driver voltage programmability

Different drives systems might benefit from different MOSFET technologies. An example is the common usage of logic level MOSFET versus standard or normal level MOSFETs, which show a higher threshold voltage ($V_{GS(th)}$). For the same gate to source voltage, a logic level MOSFET presents a lower R_{DSON} value than a normal level MOSFET.

Increasing the driving voltage helps to reduce the R_{DSON} of the MOSFET channel during the conduction, which is shown in Figure 16. As a result, it reduces the conduction losses of the system. However, rising the driving voltage increases the switching time (both rise and fall), leading to higher switching losses. The user must choose the right driving voltage depending on the system conditions.

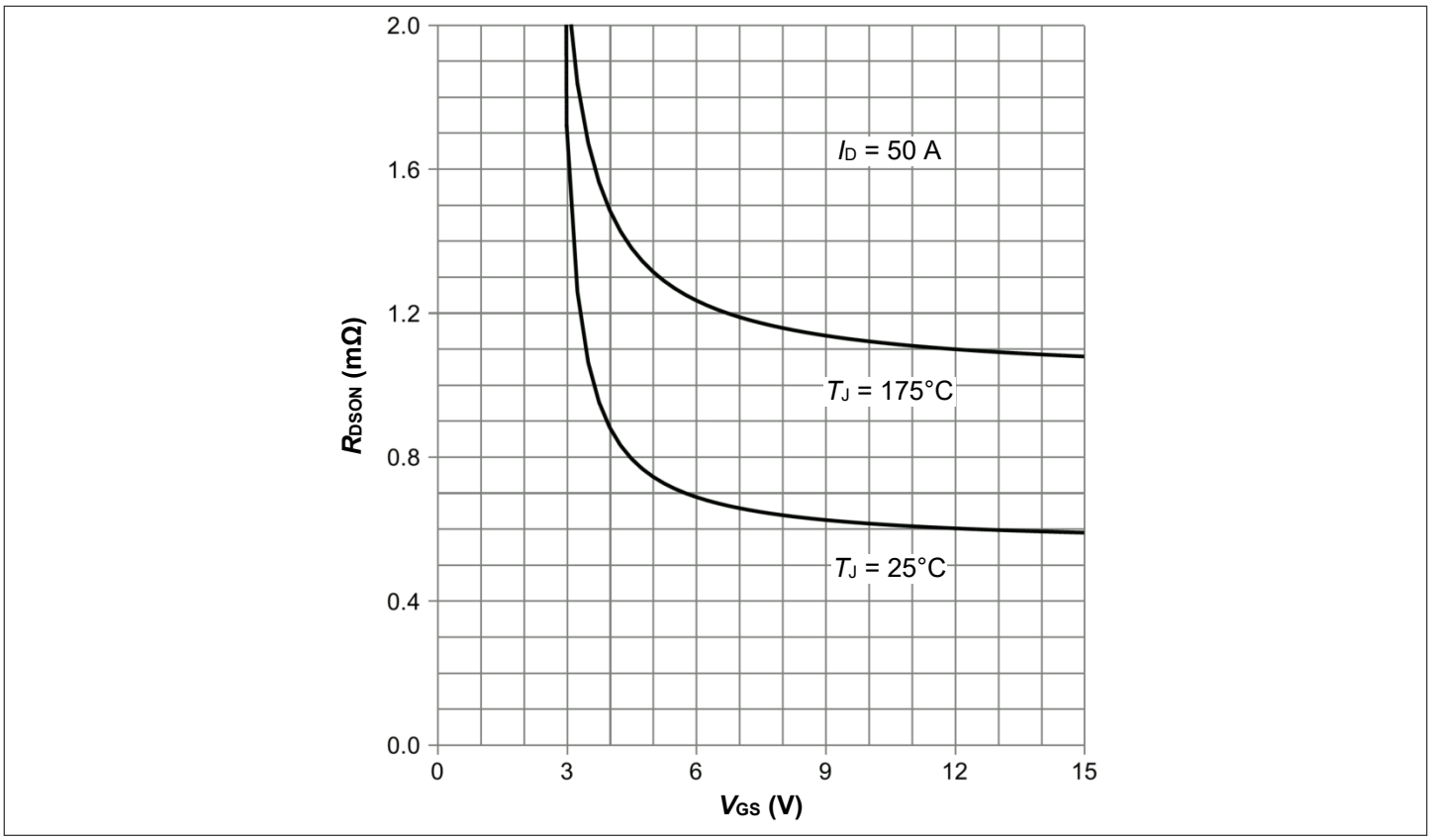

Figure 16 Typical R_{DSON} versus V_{GS} characteristic in MOSFETs. Higher V_{GS} voltage reduces the R_{DSON} of the MOSFET

The 6EDL7151 allows designers to adjust the MOSFET driving voltage (PVCC voltage) via the SPI registers. The same value PVCC applies to both high-side and low-side side charge pumps with four possible values: 7 V, 10 V, 12 V, and 15 V. This is done via the bitfield PVCC_SETPT.

***Note**: It is expected that the high-side charge pump produces a slightly lower voltage due to internal circuitry (diode). See Chapter 4.6.*

Figure 17 shows ideal examples of how supply the voltage of the driver and slew rate control can play a role together in an ideal turn on of a low-side MOSFET. Section A of the figure shows how to set the slew rate of V_{GS} of the MOSFET by programming different current values (in this case I_{LS_SRC}). Section B shows the case in which, provided a fixed gate driver current I_{LS_SRC}, PVCC is varied.

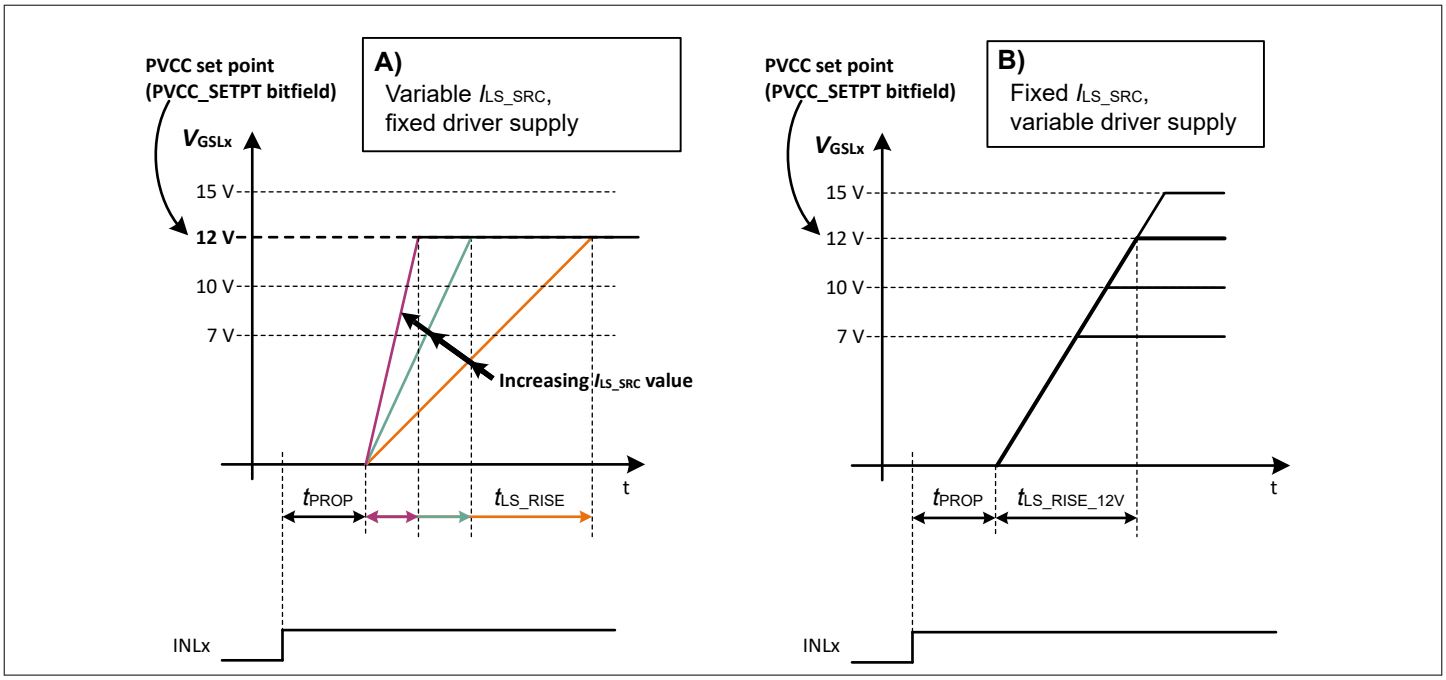

Figure 17 Gate driver slew rate configurability in an ideal low-side MOSFET switching, A) given a fixed supply voltage (PVCC = 12 V), variable I_{LS_SRC}, B) Fixing the charging current, changes in PVCC produce different rise times

3.3 Charge pump configuration

The user can adjust the charge pump operations depending on the specific needs. The following sections describe these configurations.

3.3.1 Charge pump clock frequency selection

Charge pumps are based on switched capacitor circuits that work at a given switching frequency. 6EDL7151 offers the possibility to choose four different clock frequencies via SPI programming of the bitfield CP_CLK_CFG in the register CP_CFG. Both flying capacitors and tank capacitors of the charge pumps must be chosen according to this configuration and both affect the start-up time of VCCLS and VCCHS rails as well as the possible voltage ripple of those pins.

3.3.2 Charge pump clock spread spectrum feature

When the charge pump clock spread spectrum is enabled, it artificially introduces a frequency variation (see Table 21 for values) into the charge pump clock signal. The frequency at which the charge pump operates varies between those limits, reducing the emission intensity on the target frequency value by distributing that energy over a wider range of frequencies.

3.3.3 Charge pump precharge for VCCLS

Precharge of the charge pump VCCLS is a feature that, if enabled via the SPI register, precharges the VCCLS rail right below the buck converter output voltage (VDDB) before the EN_DRV pin is activated. This precharge takes place only the first time after a power-up (CE cycle) sequence.

In this case, when EN_DRV is activated to enable the driver stage, the charge pump needs to ramp up the voltage in C_{VCCLS} from the existing precharge voltage until the PVCC selected value, therefore reducing considerably the start-up time for the charge pump when compared to the default situation in which C_{VCCLS} needs to be charged the whole PVCC voltage.

To enable the precharge of VCCLS, the bitfield CP_PRECHARGE_EN in the register SUPPLY_CFG must be set.

3.3.4 Charge pump tuning

The start-up time for the charge pumps, defined as the time that the VCCLS voltage requires to reach the target programmed voltage (PVCC set point), depends on several factors:

- Target voltage programmed via the PVCC_SETPT bitfield. The higher the PVCC voltage, the longer the start-up time
- Charge pump clock frequency: higher clock frequency results in shorter start-up time
- Charge pump tank capacitors (C_{VCCLS} and C_{VCCHS}): using VCCLS as example, a smaller value of C_{VCCLS} results in:
  - Higher VCCLS ripple
  - Shorter start-up time
- Charge pump flying capacitors (C_{CP1} and C_{CP1}): smaller capacitors lead to longer start-up time.

The selection of those parameters have an impact as well in the VCCLS and VCCHS voltage ripple. If a short start-up time is not a design target, it is recommended to increase the C_{VCCLS} value to reduce the ripple and to improve the load transients. For a given C_{VCCLS} value, the selection of flying capacitor C_{CP1} also impacts the ripple in VCCLS and start-up time.

If start-up time needs to be optimized, the charge pump precharge feature is recommended. This is explained in Chapter 3.3.3.

The start-up behavior of the charge pumps and the rest of power supply is shown in detail in Chapter 3.12.

3.3.5 Charge pump and gate driver protections

The gate drivers have the following protections:

- VCCLS UVLO
- VCCHS UVLO
- Floating gate driver pull-down
- Dead time insertion, this is explained in Chapter 3.1.7

3.3.5.1 VCCLS undervoltage lockout (VCCLS UVLO)

The UVLO prevents the gate driver from propagating PWM signals if the drive voltage is not above the UVLO threshold as specified in Table 21.

During start-up, the charge pump voltage VCCLS ramps up until the UVLO rising threshold is crossed and release the UVLO status, allowing the PWM signals to propagate to gate driver outputs.

In case of overload of the VCCLS rail beyond the specified maximum load of the charge pump, the VCCLS drops. Eventually, the VCCLS voltage can cross the VCCLS UVLO falling threshold leading to the VCCLS UVLO fault. Refer to Table 12 for more information on the VCCLS UVLO fault handling. As a result of the VCCLS UVLO, the nFAULT pin is pulled down so the microcontroller in the system can decide how to proceed.

3.3.5.2 VCCHS undervoltage lockout (VCCHS UVLO)

Similarly to VCCLS, a UVLO mechanism is integrated for the VCCHS voltage rail. The UVLO rising and falling thresholds can be found in Table 21.

During start-up, the charge pump voltage VCCHS ramps up until the UVLO rising threshold is crossed and release the UVLO status, allowing the PWM to propagate. In case of overload of VCCHS rail beyond the specified maximum load of the charge pump, the VCCHS voltage starts dropping. VCCHS voltage can then cross the VCCHS UVLO falling threshold leading to the VCCHS UVLO fault. Refer to Table 12 for more information on the VCCHS UVLO fault handling. As a result of the VCCHS UVLO, the nFAULT pin is pulled down so the microcontroller in the system can decide how to proceed.

3.3.5.3 Floating gate strong pull-down

MOSFETs in an inverter can be exposed to non-zero gate voltage levels when the controllers or gate drivers are off. Sometimes those voltages are enough to activate or partially activate the MOSFETs leading to system failure or destruction, for example, a high-side MOSFET and a low-side MOSFET in an inverter leg activate at the same time. To stop such behavior, it is common to assemble weak pull down resistors (in the order of 100 kΩ) between gate and

source of the MOSFET. When the gate driver is off, the gate is pulled down to the source to prevent any turn-on or partial turn-on. As it is weak pull-down, this does not have much impact when the gate driver is active and driving MOSFETs normally. These external R_{GS} resistors however require a good amount of PCB area and need to be placed in a location where the power layout needs to be optimized with no compromises.

To address this, the 6EDL7151 gate driver integrates a floating gate strong pull-down mechanism that includes both a passive and an active pull-down, as shown in Figure 18.

- Weak pull-down: A weak pull-down ($R_{GS\_PD\_WEAK}$) is always connected between gate and source of each gate driver output. This ensures a weak pull-down during states where the gate driver is off, either because EN_DRV is turned off or because the device is fully off (CE off). This mechanism is similar to the one described above (R_{GS}).
- Strong pull-down: Additionally, during those gate driver off periods, if the external gate to source voltage increases for any reason as mentioned, an extra-pull down, much stronger ($R_{GS\_PD\_STRONG}$) is activated, ensuring a tight pull-down and hindering any possible partial turn-on.

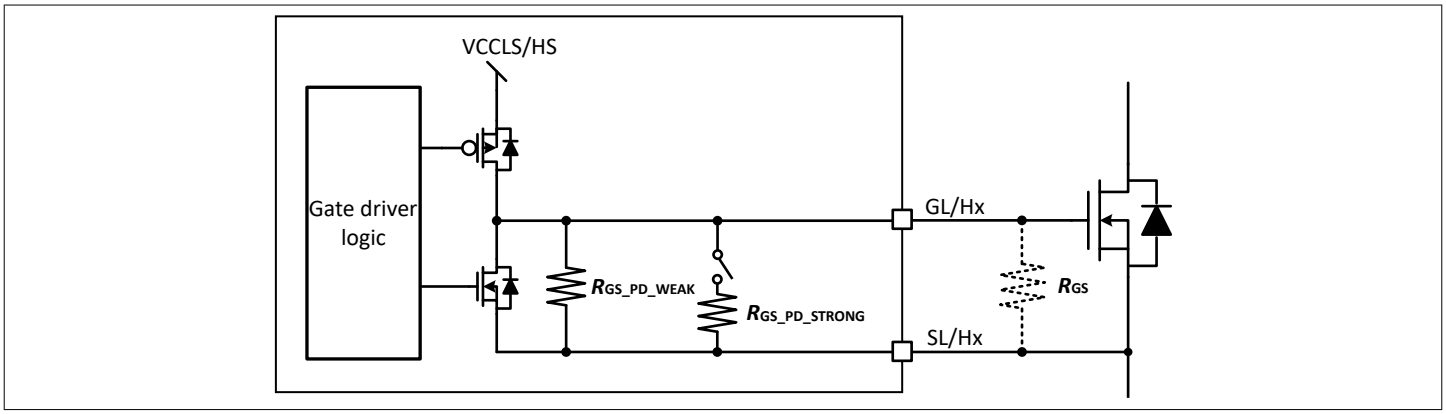

Figure 18 Floating gate driver pull down resistors. Strong pull down activates when gate driver is off and gate to source voltage increases

3.4 Power supply system

The device embeds an advanced power supply system comprised of:

- Synchronous buck converter including both power switches
- DVDD linear voltage regulator programmable to output 3.3 V or 5 V
- Charge pump for low-side gate driver (described in Chapter 3.2)
- Charge pump for high-side gate driver (described in Chapter 3.2)

The 6EDL7151 has been designed for the lowest BOM (Bill of materials). The synchronous buck converter does not require external components like diodes, voltage dividers, or bootstrap capacitors yet at the same time reduces the low-side conduction losses as it utilizes a NMOS instead of a diode.

The overall goal of the buck converter is to support the rest of the power supply system. With the help of an external inductor L_{BUCK} and capacitor C_{VDDB}, it supplies both (high-side and low-side) charge pumps and the integrated DVDD voltage regulator. This architecture increases the efficiency of the device greatly compared to an only linear regulator system, yet maintains a very compact system solution. Furthermore, it allows working at a high supply voltage rating (PVDD).

DVDD linear voltage regulator is integrated to provide accurate and stable voltage to other external components either at 3.3 V or 5 V. In Figure 19, a schematic diagram of the complete power converter architecture and interconnections is shown.

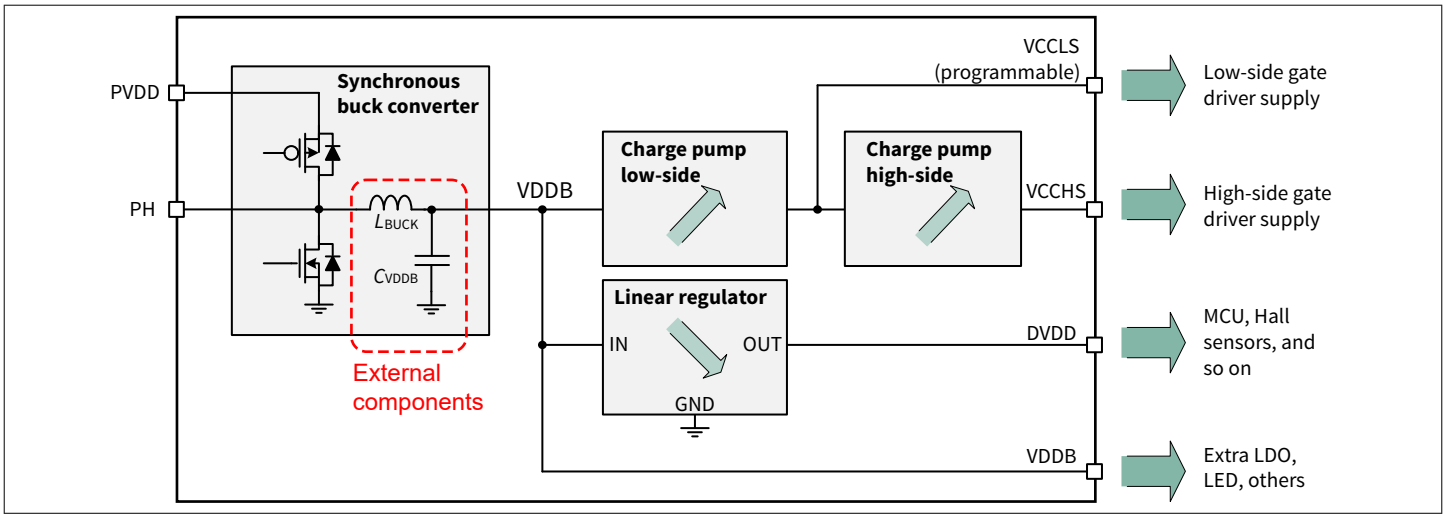

Figure 19 Block diagram of power converter architecture

Designers can use VDDB pin to supply external components as long as the current limits of the buck converter, including charge pumps and linear regulator, are not exceeded. Nevertheless, overcurrent protections (OCP) are implemented for both buck converter and the linear regulator, preventing any damage to the device when overloading VDDB pin. Additional overtemperature protections (OTS and OTW) are integrated to ensure that the device is under correct thermal conditions at any time.

3.4.1 Synchronous buck converter

Although integrated in the same package, the synchronous buck converter is designed completely independent of the rest of the gate driver circuitry. This makes the supply system robust against gate driver failures. As an example, the buck converter and linear regulator still operate even if a failure occurs in the gate driver section (for example, VCCLS UVLO), ensuring right operation of a microcontroller and other circuits supplied by the buck converter or LDO integrated for example.

The control method utilized is Adaptive Constant ‘ON’ Time (ACOT). In contrast to a pure constant ON time control method, ACOT allows ON time variations during transitions to avoid large frequency jumps. Together with feedforward techniques, the buck converter can operate with reduced switching frequency.

Two different switching frequencies (500 kHz and 1 MHz) can be selected from the BK_FREQ bitfield via SPI for the buck converter. The recommended values of the inductor and capacitor for each configuration are provided in Table 22 of Chapter 5.1.

***Note**: It is recommended to only modify the buck converter frequency via OTP.*

A detailed figure of both synchronous buck converter and linear voltage regulator circuits is depicted in Figure 20.

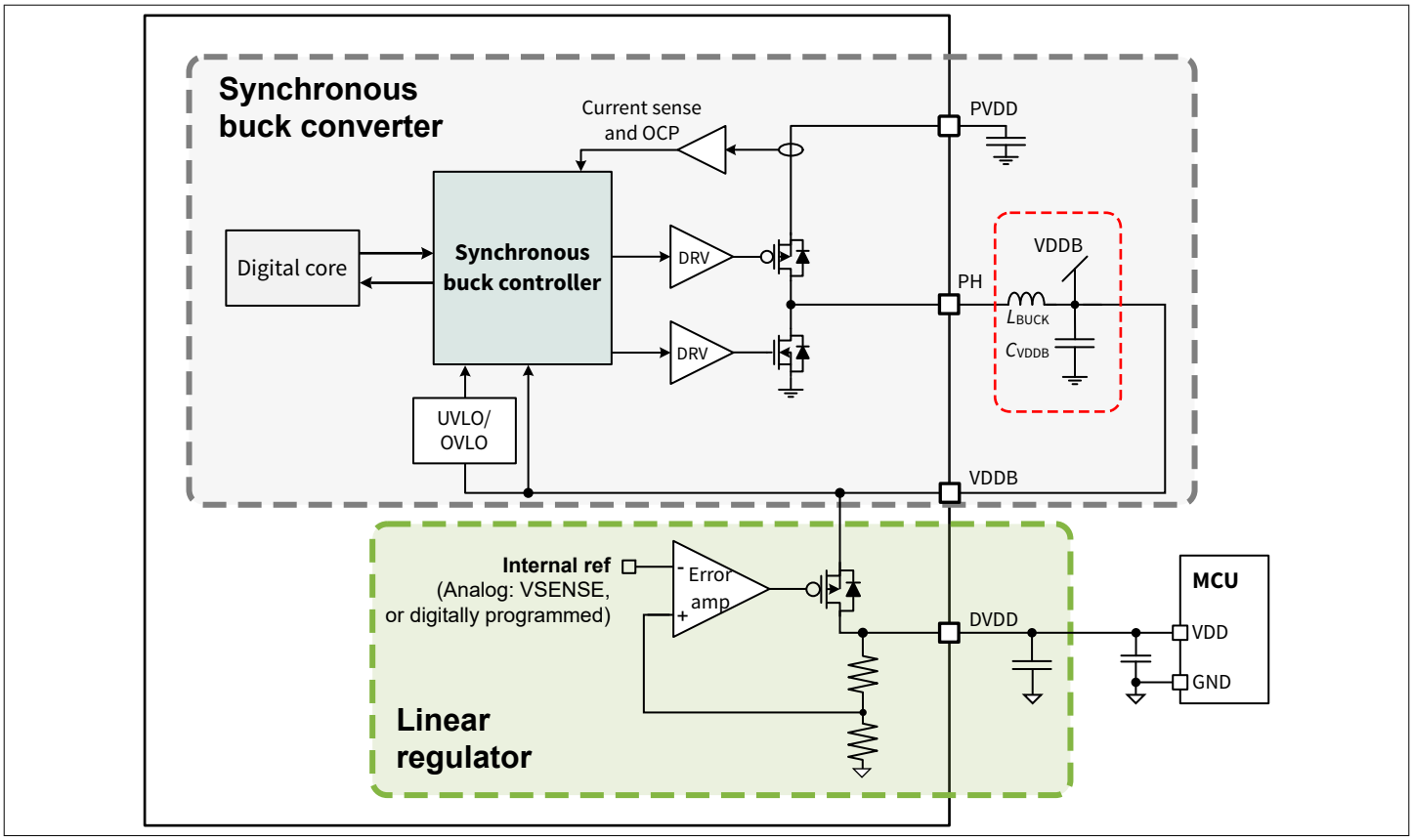

Figure 20 Details of integrated synchronous buck converter and linear regulator

3.4.1.1 Buck converter output voltage dependency on PVCC_SETPT

An important feature of the buck converter is the ability to adjust the VDDB target value automatically depending on the PVCC (target gate driver voltage), which is configured by the user via SPI commands. This is done to optimize the power losses in the device. For example, if the driving voltage PVCC is 7 V, then the target voltage of the buck converter is set to 6.5 V automatically. In this case, the charge pumps still have enough room to reach PVCC = 7 V on a 'doubler' configuration. The relationship between VDDB and PVCC is shown in Table 8.

Table 8 Buck converter output target voltage versus PVCC_SETPT setting

PVCC_SETPT bitfield	PVCC target voltage (V)	VDDB (V)
b11	7	6.5
b10	10	7
b00	12	8
b01	15	8

Another important factor to consider in the synchronous buck converter output target voltage is PVDD or supply voltage. If 6EDL7151 is supplied with a relative low voltage then $VDDB_{NOM\_LV}$ rating applies (see Table 21). In such situation the buck converter operates in open loop with the duty cycle saturation limit given by D_{BUCK_MAX} (see Table 21). If buck converter loading increases in that situation or PVDD voltage reduces further, the VDDB voltage drops. On the lower end, VDDB UVLO falling threshold protects from lower limits.

Therefore, depending on PVDD voltage, it is possible that VDDB cannot reach the target voltage, limiting as a consequence the actual PVCC voltage, which even in a doubler configuration might not be sufficient. The approximate possible PVCC voltage (= VCCLS) in the doubler configuration is given by the following equation:

$$PVCC_{max} \approx min(PVCC \quad target \quad voltage, 2 * VDDB - 1 \quad V) \tag{1}$$

As an example, if PVDD = 7.5 V, VDDB ≈ 6.5 V (limited by low PVDD voltage), if PVCC_SETPT targets 15 V, the doubler on the charge pump is able to reach maximum of approximately 2 * VDDB - 1 V ≈ 12 V. If PVDD rises to 12 V, then the VCCLS is able to regulate to 15 V as this value is below/equal to the value = 2 * VDDB (8 V) - 1 V = 15 V.

See Chapter 4.6 for more details on relationship between VCCLS, VCCHS and PVDD.

3.4.1.2 Synchronous buck converter protections

The following protections are implemented to ensure correct operation of the buck converter:

- **Output undervoltage lockout (UVLO)**: See Table 21 for specific values.
- **Output overvoltage lockout (OVLO)**: See Table 21 for specific values. If the value is reached the buck converter switches off, both high-side and low-side MOSFETs interrupting any further energy transfer to the output.
- **Overcurrent protection (OCP)** cycle by cycle: given a situation in which the current increases till the OCP level (see Table 21 for details), the buck converter controller truncates the high-side FET PWM signal until the next PWM period starts. The low-side FET is driven accordingly after insertion of a dead time.

Once the OCP event takes place, a counter starts counting for each consecutive period that the peak current is reached. After 16 periods, the buck OCP fault is triggered and the nFAULT pin (see Table 12) is set low to inform the MCU that it can proceed with correcting actions. The buck converter continues operations in current limitation to ensure the MCU is supplied. If the OCP does not trigger for three consecutive PWM periods, the counter resets and does not trigger the buck OCP fault. If the buck OCP fault is activated, then the bitfield BK_OCP_FLT in the register FAULT_ST is set.

3.4.2 DVDD linear regulator

The integrated linear regulator generating DVDD can be set to provide either 3.3 V or 5 V by means of an external resistor R_{SENSE} as described in Table 21 or alternatively via bitfield DVDD_SETPT. The selected DVDD value can be read via SPI in the bitfield DVDD_ST in the register FUNCT_ST.

DVDD linear regulator can be used as well to provide an offset to the current sense amplifiers integrated, allowing negative current measurements. See Chapter 3.5.4 for more details. The linear regulator is soft started during ramp-up of the device as depicted in Figure 45 after a delay time $t_{DVDD\_TON\_DELAY}$ after the buck converter has reached its UVLO level ($V_{VDDB\_UVLO\_R}$) and analog programming of CS_GAIN/AZ and VSENSE/nBRAKE are finished. The DVDD ramp-up timing can be configured by the bitfield DVDD_SFTSTRT via SPI.

A schematic view of the DVDD linear regulator and the interaction with the buck converter is presented in Figure 20.

DVDD voltage can be used to supply a microcontroller (MCU) and additional elements in the circuit like Hall sensors, LEDs, and so on.

3.4.2.1 DVDD linear regulator OCP

DVDD has an OCP mechanism and can be configured between four different levels by writing register the DVDD_OCP_CFG. If the OCP for DVDD is reached, a fault is reported on the nFAULT pin. The DVDD OCP works in two different stages as shown in Figure 21:

1. **Pre-warning mode at 66% of selected OCP level**: The nFAULT pin is pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching 100% level, the operation continues normally releasing the nFAULT pin. The pre-warning allows some extra time for the microcontroller to make a decision on how to react to the possible DVDD OCP event.
2. **Current limiting mode at 100% of selected OCP level**: If current increases beyond the configured OCP level, the DVDD regulator starts limiting the output current. This causes a DVDD voltage drop, eventually resulting in a DVDD UVLO fault if the DVDD UVLO threshold is crossed. As a result of this limitation, possible shorts on the DVDD rail do not affect the rest of the system, keeping other components safe.

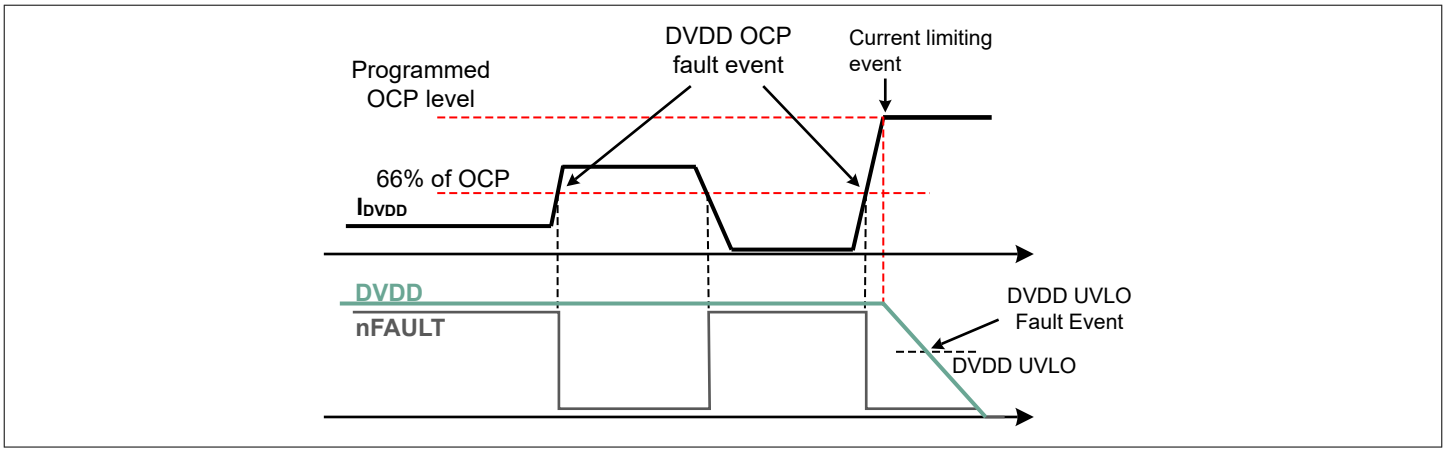

Figure 21 DVDD OCP behavior including pre-warning and current limiting modes

***Note**: The OCP in DVDD is suppressed during ramp up of the device to avoid that initial charge of DVDD decoupling capacitors (eventually large capacitors) triggers the OCP fault.*

Overtemperature faults (OTS and OTW) provide an additional level of protection. These will trip if too high temperature is developed in the device, for example, when the DVDD linear regulator or the buck converter outputs excessive load current.

3.5 Current sense amplifiers

The device integrates three current sense amplifiers that can be used to measure the current in the power inverter via shunt resistors. Single, dual and triple shunts measurements are supported as shown in Figure 22.

The CS_EN bitfield enables each current sense amplifier individually. Gain and offset are generated internally and programmable.

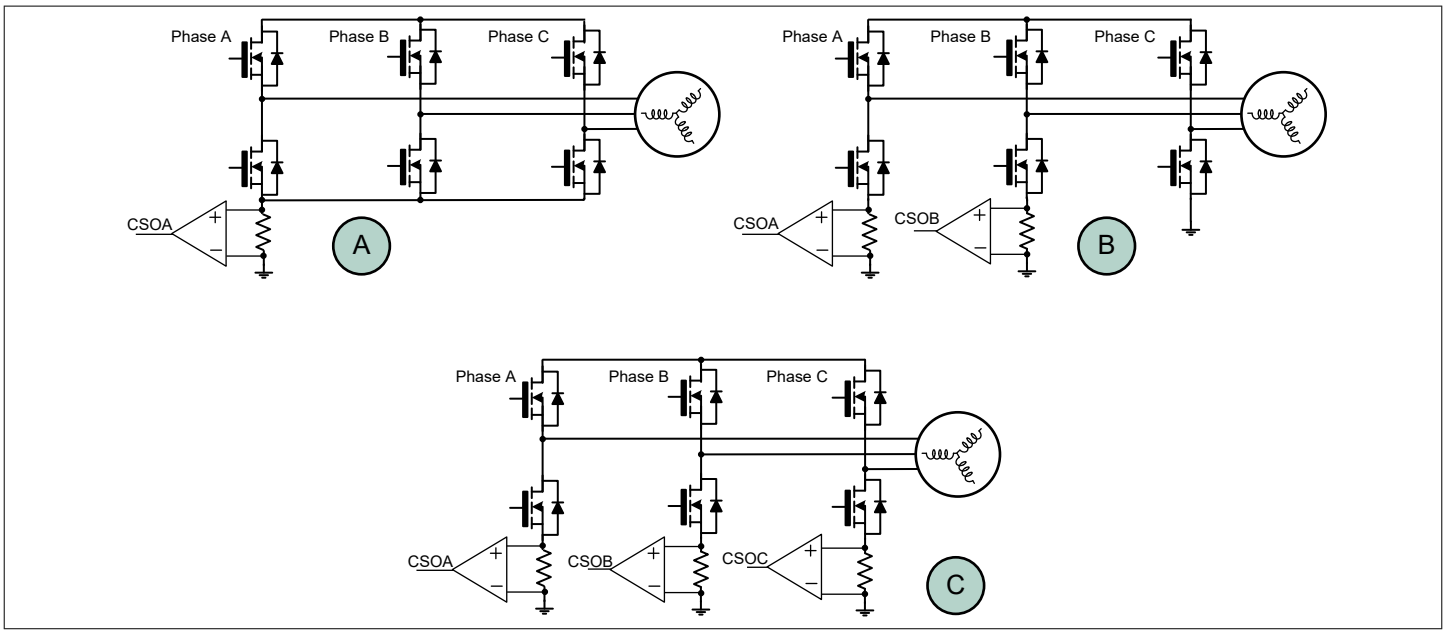

Figure 22 Single (A), dual (B) and triple (C) shunt current sensing configurations

The current sense amplifier block contains the following subblocks explained in detail in this section:

- **Current sense amplifier**: Connected to an external shunt resistor or internally to the SHx and SLx pins for R_{DSON} sensing configuration. This module amplifies the shunt voltage or the low-side V_{DS} voltage to a more appropriate voltage level for a microcontroller ADC. It allows as well blanking the signal synchronized to PWM transitions, during periods when the noise is disturbing the measurement.

- **Output buffer**: Allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to four different values either by programming the internally generated level. With this implementation, negative current in shunt resistors can be measured. Additionally, it permits to optimize the controller ADC dynamic range according to the system conditions.
- **Positive over-current comparator**: Used for detecting the overcurrent condition on the motor winding for positive shunt voltage. This comparator can be used to apply PWM truncation in block or trapezoidal commutation schemes, limiting the motor current to the configured OCP threshold.
- **Negative over-current comparator**: Used for detecting the over-current condition on motor winding for negative shunt currents.
- **OCP Digital-to-Analog Converter (DAC)**: Used for programming the threshold of the overcurrent comparators. One for positive level and a second one for negative level. The programming of DAC levels is shared among all three different OCP comparators.

Current sense amplifiers are automatically “auto-zero”. This happens during operation and ensures the best accuracy of measurements during the lifetime of the device. Additionally, the 6EDL7151 includes a DC calibration mode for the current sense amplifiers that can be used to calculate the residual offset when the shunt current is known to be zero, for example, because there is no PWM yet propagated to the MOSFETs. A microcontroller firmware can remove this initial offset value from future measurements to improve accuracy.

Figure 23 shows these blocks and their interconnections.

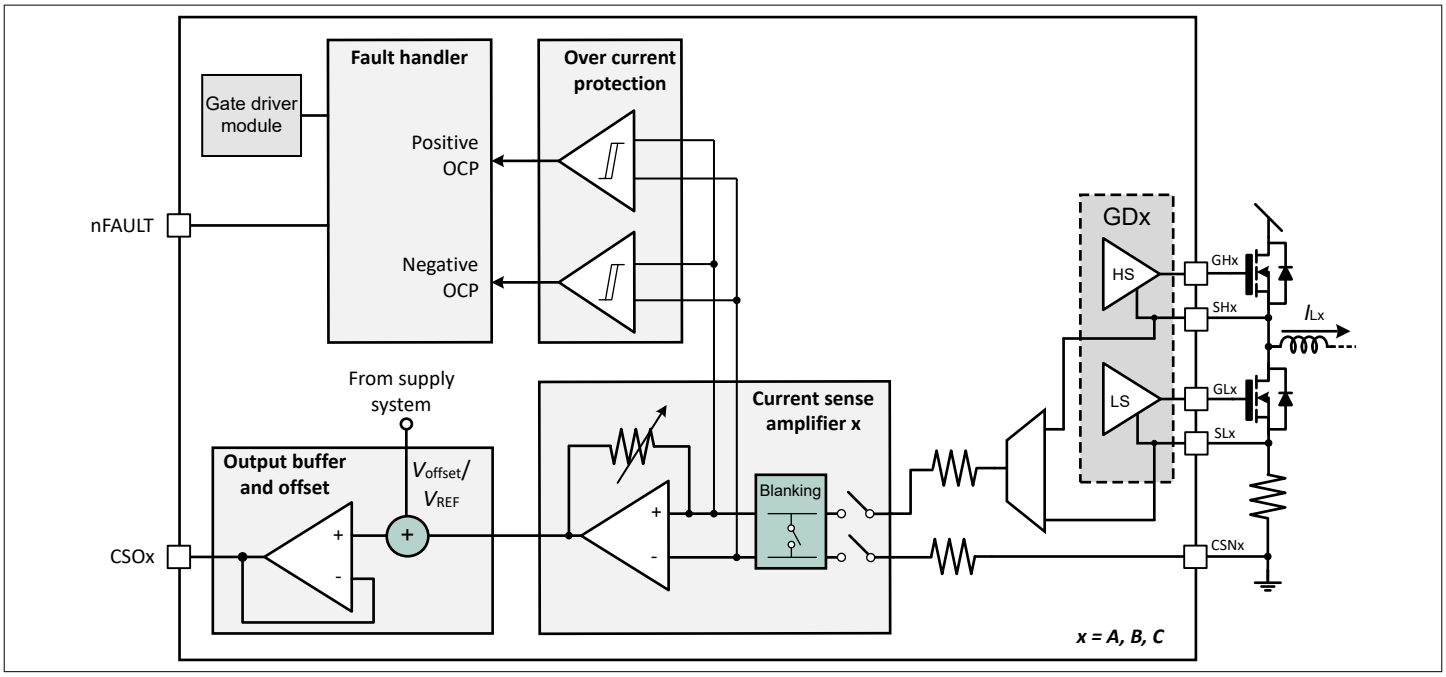

Figure 23 Current sense amplifier simplified block diagram

***Note**: It is recommended to disable the current sense amplifiers that are not used.*

3.5.1 RDSON sensing and shunt resistor sensing modes

Current sense amplifiers in the 6EDL7151 can be configured as shunt resistor sensing, or R_{DSON} sensing where the ‘ON’ resistance of the MOSFETs is used as shunt in a ‘lossless’ measurement approach. In R_{DSON} sensing mode, the 6EDL7151 connects the drain of the low-side MOSFET to the positive input of the current sense amplifier. The negative input is connected to the source as shown in Figure 24. This is in contrast to the shunt resistor sensing mode shown in Figure 25, where the positive input of the current sense amplifier is connected to the source of the low-side MOSFET. Internal series resistors help to filter possible noise before the amplification takes place. Depending on the circuit and board design, a small filtering capacitor between SLx and CSNx pins can help clean up the current signal.

***Note**: R_{DSON} sensing mode is only possible in three-phase current sensing (configuration C in Figure 22 with all amplifiers in RDSON sensing mode and shunt resistors removed).*

***Note**: In R_{DSON} sensing mode, the CSAMP (current sense amplifier) is forced to be CS_TMODE = b00, meaning the current sense amplifiers outputs are active when the GLx signal is high (GL ON mode). If the CS_TMODE bitfield is written with a value different from b00, the configuration is ignored by the internal logic.*

***Note**: Temperature compensation for the R_{DSON} measurement, if required, must happen at the MCU.*

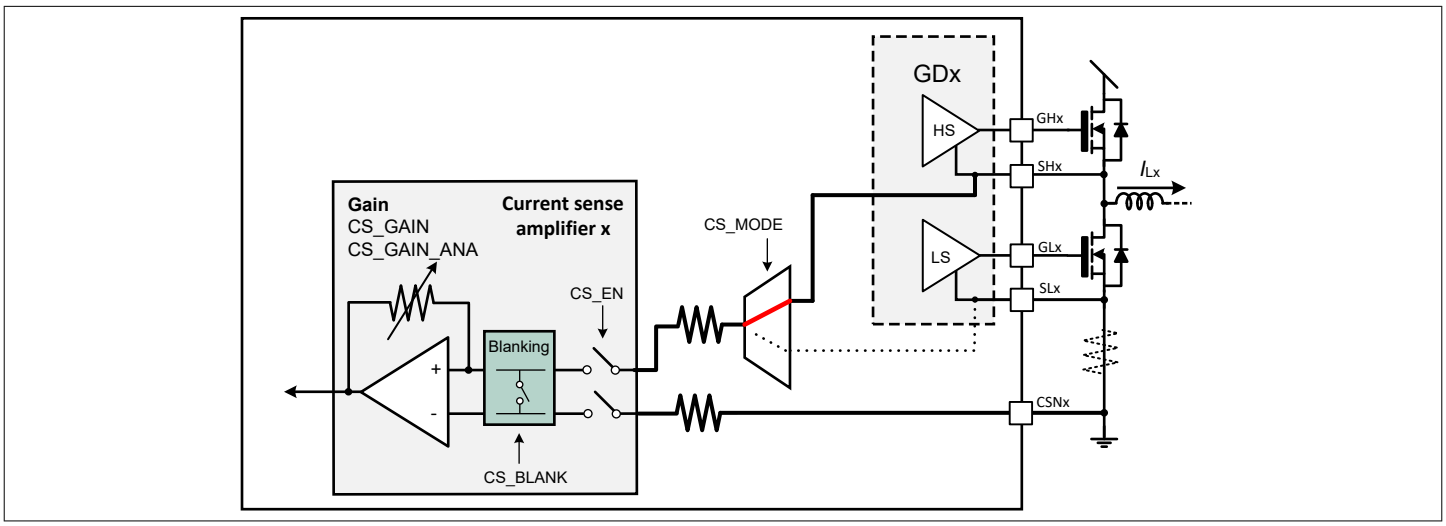

Figure 24 System diagram of a low-side R_{DSON} sensing configuration

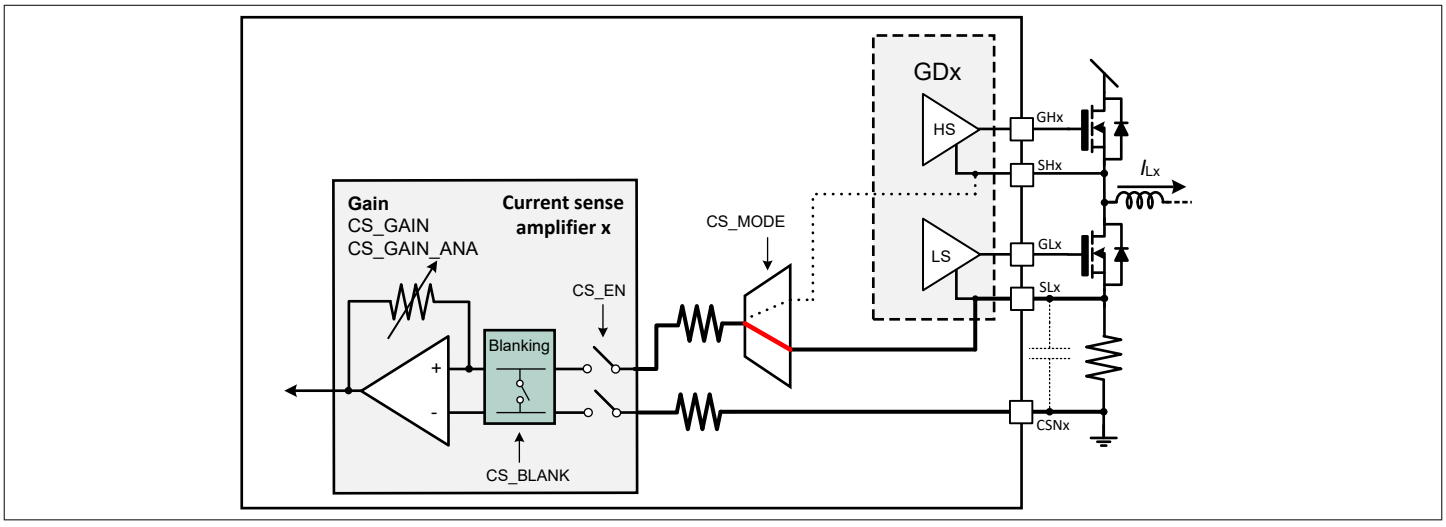

Figure 25 System diagram of shunt resistor sensing configuration

3.5.2 Current sense amplifier timing mode

Often in drives applications, the current is sampled via leg shunts. In this case, the voltage in the shunt that needs to be amplified appears only when the low-side MOSFET is turned on. In other cases, it might be useful to propagate the signal continuously. The 6EDL7151 supports four different modes of operation of the current sense amplifiers regarding when the output pin CSOx is connected to the amplifier stage. These four modes are:

- **Always OFF**: Current sense amplifier output is disabled. This is achieved by disabling the amplifier via the bitfield CS_EN in the register CSAMP_CFG.

- **GL ON**: In this mode, the CSOx pin is connected to the amplifier only when the same leg or phase GLx signal is active. In single shunt mode, CSOx is connected according to the OR'ing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSOx are dedicated to that GLx signal. This mode is forced if R_{DSON} sensing is selected to prevent any possible overvoltage damage in the internal circuitry. To enable this mode, the amplifier must be enabled via the CS_EN bitfield and the timing mode selected via write to the CS_TMODE bitfield in the register SENSOR_CFG.
- **GH OFF**: Similarly to GL ON, this mode connects the CSOx outputs during GL ON period, but extends that the connection to the dead times both rising and falling so it is more than GL ON. In some cases like during diode recirculation current, the diode might carry a current that can be useful, especially in cases where the PWM pulses are very narrow. Same as GL ON, single shunt will logic OR the GLx activations and three shunt modes are activate according to each GLx signal only. To enable this mode, the amplifier must be enabled via the CS_EN bitfield and the timing mode selected via write to the CS_TMODE bitfield.
- **Always ON**: This mode continuously connects the activated amplifier CSOx signals to the amplifier independently of PWM signals. To enable this mode, the amplifier must be enabled via the CS_EN bitfield and the mode selected via write to the CS_TMODE bitfield.

Figure 26 shows a comparison of the current sense amplifier working in both modes GL ON and GH OFF for a half bridge example with a shunt resistor sensing configuration with three active amplifiers. GH OFF can potentially propagate current information when the diode recirculates current. Auto-zero occurs on one GHx rising edge.

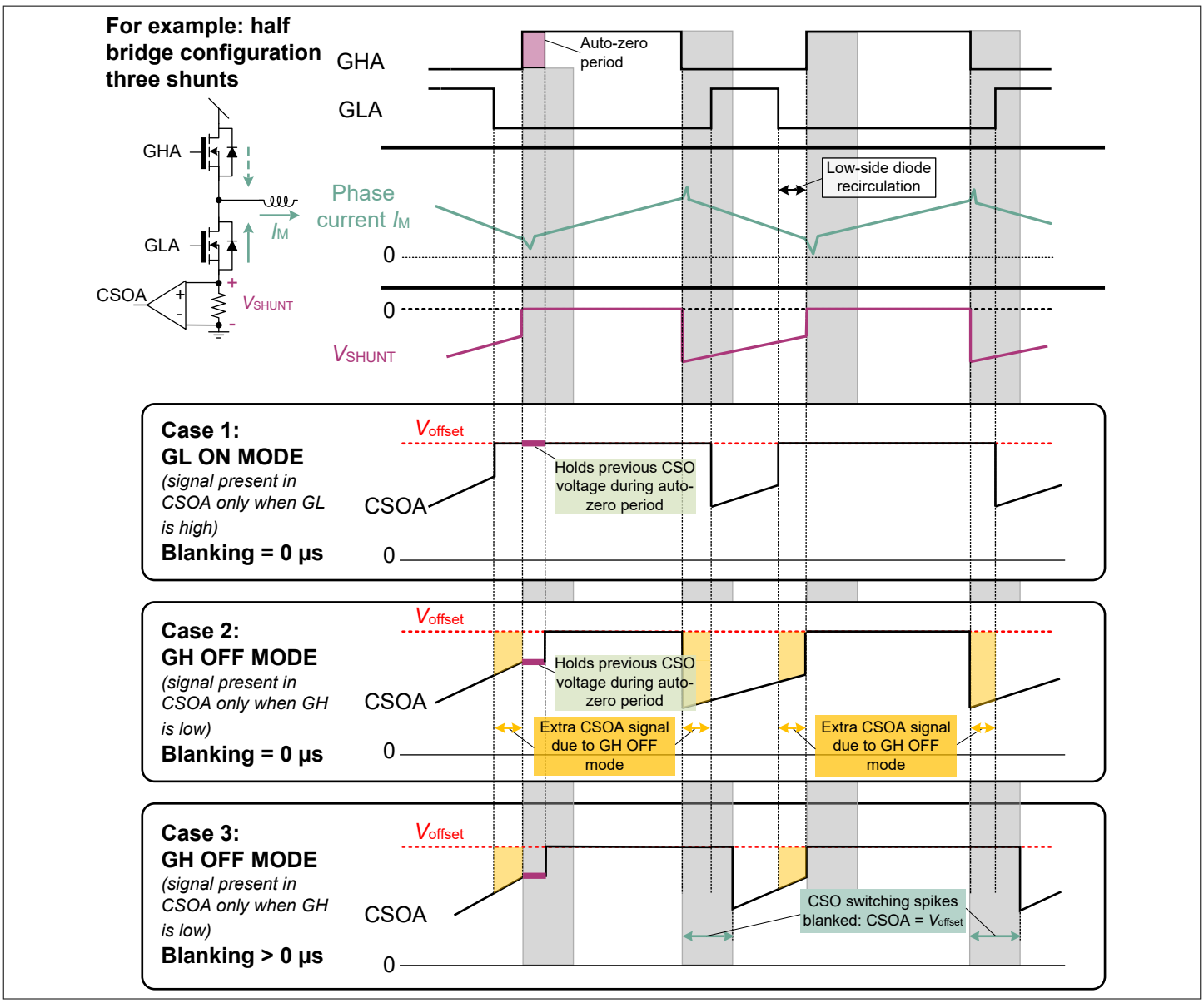

Figure 26 Current sense amplifier ideal timing mode example

3.5.3 Current sense amplifier blanking time

A programmable blanking period can be configured in the current sense amplifiers and the goal to prevent propagating a distorted signal to the microcontroller ADCs during MOSFET switching transitions. Since both voltages at SHx and SLx pins (or CSNx) are subject to ringing due to the switching activities, the blanking module disconnects the inputs for a configurable blanking time (t_{CS_BLANK}). This action occurs in synchronicity with the GHx signal (rising and falling edges) driving the external MOSFETs.

During the blanking time, the pin CSOx shows a V_{offset} voltage until the programmed blanking time period expires and inputs are connected again to the current sense amplifier.

Two examples are shown in Figure 27:

Example A) represents a trapezoidal commutation scheme with one shunt similar to the one in Figure 73. In such a case, the high-side of one phase (phase B) is switching, while the low-side of another phase (phase A) is always ON, allowing the current to flow through the motor windings. As the low-side MOSFET of phase A is ON for 120° of rotation, the current sense amplifier is amplifying the shunt voltage continuously except blanking and recirculation periods. These blanking periods correspond to both high-side rising and falling edges (ORing to all phases applied). In this case, the voltage across the shunt is positive.

Example B) corresponds to a generic half bridge configuration (for example, a synchronous buck converter). In this case, when the high-side is turned on, the current in the inductor increases in the complementary cycle when the high-side switches off and the low-side turns on after dead time, the current flows through the low-side and starts decreasing. During the low-side conduction, the current sense amplifier generates the output as shown, which is proportional to the voltage across the shunt, in this case, the voltage is negative.

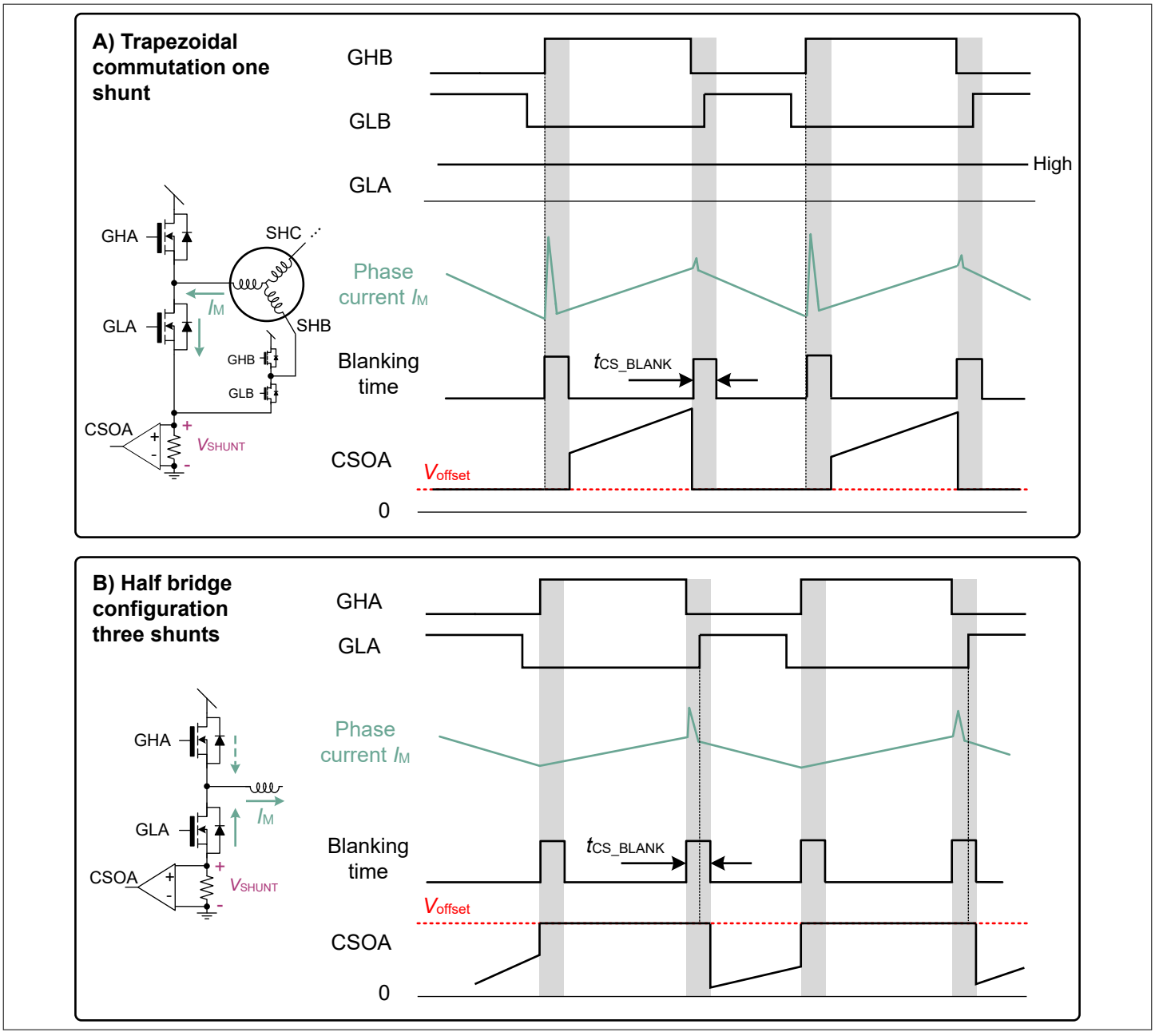

Figure 27 **Timing diagram of a current measurement utilizing blanking time feature for suppressing current spikes during MOSFET switching**

3.5.4 Current sense amplifier offset generation

The internal linear regulator DVDD is used for the offset generation for all integrated current sense amplifiers. The DVDD voltage is scaled down to different programmable values to adjust the desired offset voltage levels. The bitfield CS_REF_CFG controls this scaling factor.

Some microcontrollers generate internally the reference for an integrated ADC out of the supply voltage. In this way, the microcontroller can accurately measure in a ratio-metric way the output of the current sense amplifiers, increasing noise immunity. Figure 28 shows a block diagram representing this implementation.

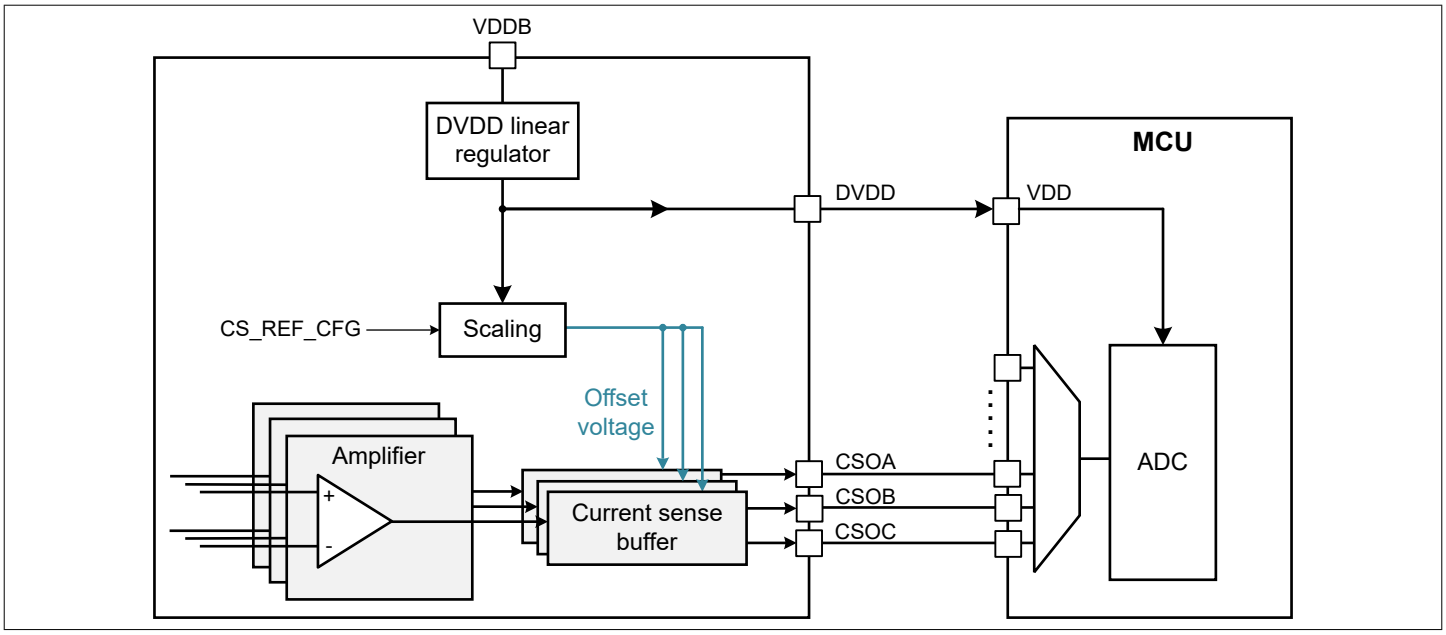

Figure 28 Current sense amplifier offset generation block diagram

3.5.5 Current sense amplifier OCP

Two overcurrent comparators are integrated for monitoring the current in both positive and negative direction with an extensive level of programmability. Figure 29 shows a schematic diagram of this implementation. Both comparators monitor the current flowing through the shunt. The triggering level is independent from the gain setting of the current sense amplifiers and is defined as the voltage across the shunt. The comparator features a hysteresis ($V_{CS\_OC\_HYS}$) for consistent operation.

Positive and negative triggering levels for the comparator are set with two independent Digital to Analog Converters (DAC). These DACs are programmed via the bitfields CS_OCP_PTHR for positive overcurrent protection and CS_OCP_NTHR for negative overcurrent protection. For possible threshold levels, see the registers description in Chapter 3.16.

The output of the comparators can be deglitched by programming the register CS_OCP_DEGLITCH before reaching the fault handler, where the fault is processed (see Chapter 3.14) and eventually pulls down the nFAULT pin reporting a fault to the microcontroller or other circuitry.

Alternatively, the comparator output propagates to the PWM modules. PWM truncation can be enabled via the bitfield CS_TRUNC_DIS. If PWM truncation is activated, the PWM module immediately interrupts the PWM signal without having to wait for the microcontroller to make such decision when the OCP level is reached. This ensures the fastest reaction to the OCP event. PWM truncation is detailed in Chapter 3.5.5.4.

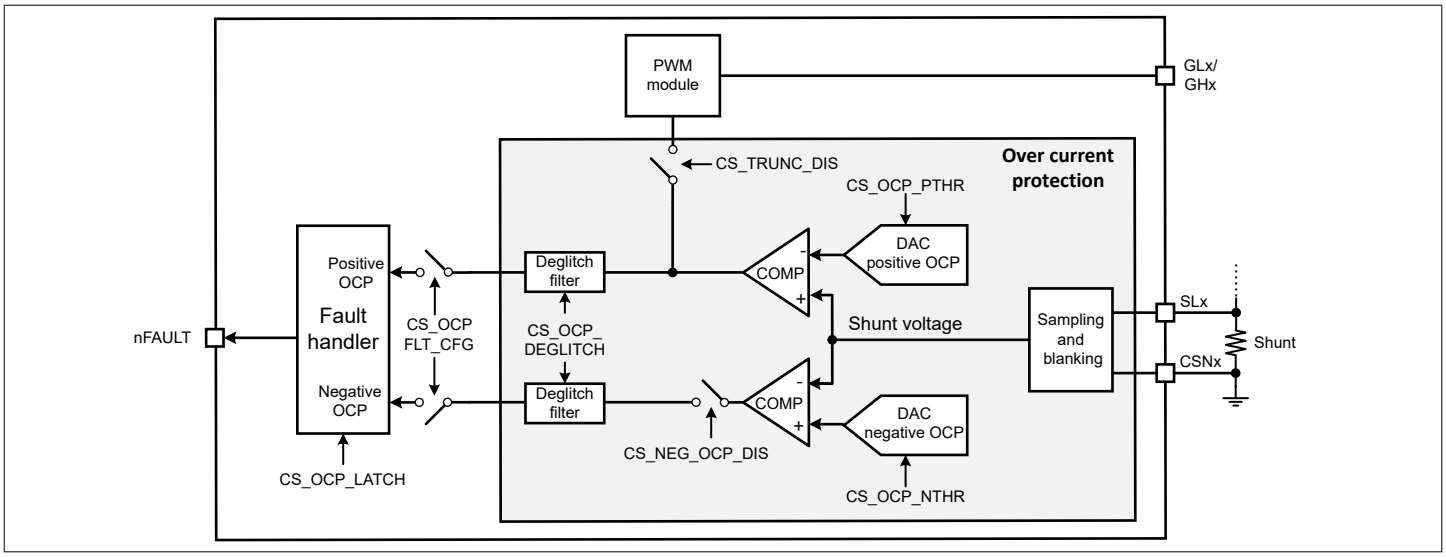

Figure 29 Current sense amplifier protections schematic block diagram

3.5.5.1 OCP use cases

The reaction to an OCP event is programmable via SPI. The following scenarios may be useful for different applications:

- **Apply PWM truncation** immediately after OCP event and report on the nFAULT pin after the OCP event - deglitching is disabled if PWM truncation is enabled. This is useful in trapezoidal control schemes.
- **Disable reporting and keep PWM truncation**. This can be useful during events where the reporting function to the microcontroller might not be necessary. This is useful in trapezoidal control schemes.
- **Trigger a configurable brake action** upon OCP event. If PWM truncation is not desired, the brake event can be configured to, for example, brake the motor by shorting all low-side MOSFETs. By using the deglitch function, the possible noise in the analog signal can be filter out to avoid false trip of the OCP. This configuration can be useful for FOC (Field Oriented Control) schemes given the flexibility. Braking is explained in more detail in Chapter 3.1.6 and Chapter 3.14.
- **Disable OCP protection**, keep both nFAULT reporting and PWM truncation. In this case, OCP is ignored. This might be useful for transition states or stop procedures as well.

These configurations can be adjusted also during active state of the device. It is also possible to select whether the OCP fault trips on a single event or more and whether is latched or not via the bitfield CS_OCP_LATCH.

3.5.5.2 OCP fault reporting

OCP fault can be reported to the MCU via nFAULT pin pulling low. CS_OCPFLT_CFG in the register CSAMP_CFG allows the user to set a target number of consecutive events (PWM cycles with current above OCP threshold) that triggers the OCP fault. This means the user can configure the device to wait for several PWM periods before declaring a fault and therefore be more conservative. Three options are possible: no fault, trigger immediately (that is, trigger on all events) or trigger on a number of counts (8 or 16). The logic for the counting mode works as follows:

1. Every time that an OCP event occurs, a counter increments. All three phases have dedicated counters.
2. If any counter (ORing) reaches the target value configured in CS_OCPFLT_CFG, then the fault is asserted and the nFAULT pin is pulled low.
3. If before reaching the target value, the OCP event does not occur for three consecutive PWM cycles, the counter is reset to value 0, starting over next time an OCP event takes place.

3.5.5.3 OCP fault latching

The OCP fault can be configured as latched or non-latched via the bitfield CS_OCP_LATCH. This defines how the fault is cleared via a register write. If configured as latched:

- and in counting mode (8 or 16): fault cannot be cleared until there is one whole PWM period without fault.
- and in immediate or on all events mode: fault can be cleared only after the fault condition is released.

If not latched, the fault can be cleared any time. If conditions is still present after clear, the fault is set again after the clear event. Independently of the latch configuration, the status register shows that the fault happened.

3.5.5.4 PWM truncation

PWM truncation is a method to intrinsically limit the current flowing into the motor by switching off the PWM signal immediately after the OCP detection. In this way, the GHx signals (all three) are pulled down automatically when the configured peak current level is reached. Low-side remains unaffected until the next PWM cycle when the motor current increases again. This happens in a PWM cycle by cycle base. An example of PWM truncation is depicted in detail in Figure 30.

***Note**: Truncation always occurs on high-side except for 1PWM mode with alternate recirculation, where the truncation occurs in low-side during high-side recirculation periods and on high-side during low-side recirculation periods.*

PWM truncation takes place upon OCP event in all phases if it is enabled. For example, if the protection is triggered in current sense amplifier A, then PWM signals in phases A, B and C are truncated. This enables the single shunt systems to utilize any of the current sense amplifiers.

Blanking is applied to truncation logic on both rising and falling edge of high-side as described in Figure 27, with the bitfield CS_BLANK for blanking time configuration. Blanking from all phases are OR'ed and prevent any mistriggering of the PWM truncation during the blanking time selected by the user.

If PWM truncation is enabled, the deglitching filter is automatically disabled, which means the nFAULT pin signalizes simply that a PWM truncation has occurred.

***Note**: Depending on the PWM modulation utilized, PWM truncation might not provide the desired results. In modulation schemes where it is possible more than one phase are energizing the motor at a given time like SVM FOC (Space Vector Modulated Field Oriented Control), it is recommended to disable truncation and use OCP fault instead.*

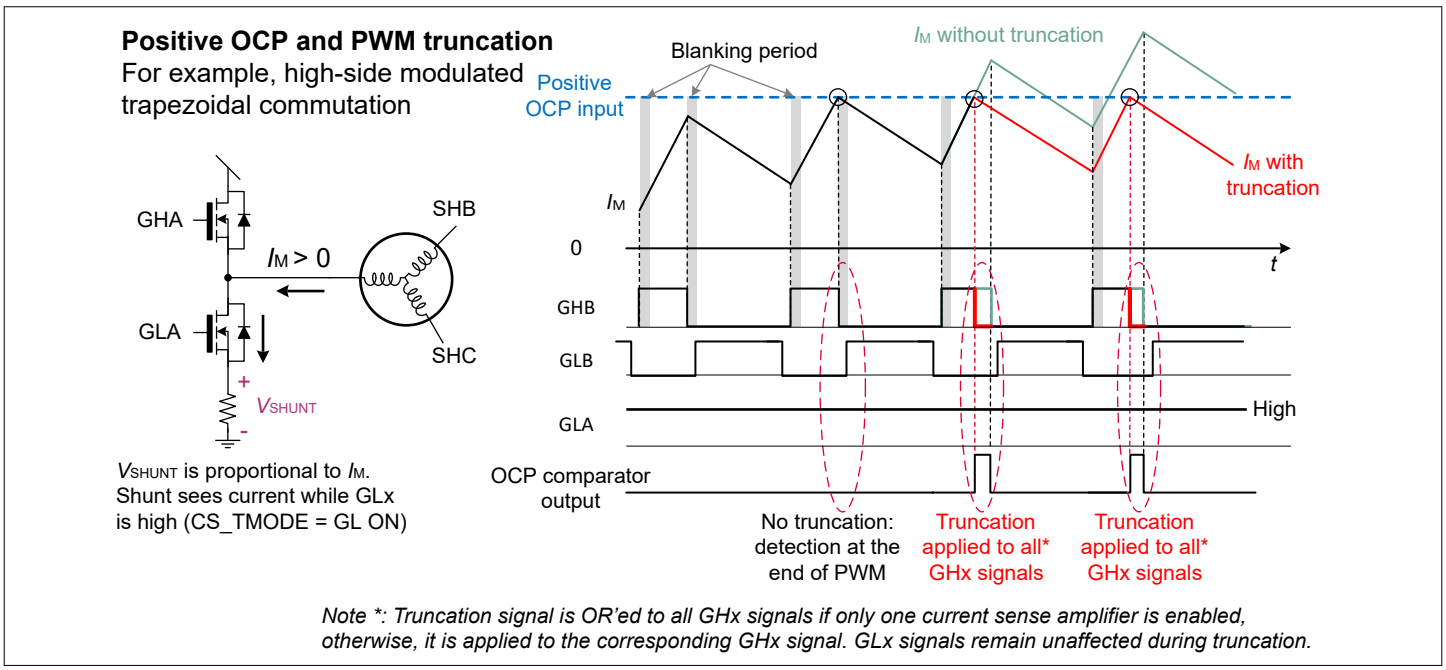

Figure 30 Positive OCP PWM truncation example

3.5.6 Current sense amplifier gain selection

Gain of the current sense amplifiers can be programmed digitally via the bitfield CS_GAIN to one of the following values: 4, 8, 12, 16, 20, 24, 32 and 64. Alternatively, the gain can be selected by connecting an external resistor R_{CS_GAIN} from CS_GAIN/AZ pin to ground. To enable analog programming of the current sense amplifier via an external resistor, the user must ensure the bitfield CS_GAIN_ANA is set accordingly. The value of R_{CS_GAIN} is evaluated during start-up of the device (see Chapter 3.10.3). Table 9 provides the resistor values and register settings for gain selection by analog and digital programming.

Table 9 Programming of current sense amplifier gain

Gain value	Digital programming	Analog programming
	CS_GAIN (Hexadecimal)	R_{CS_GAIN} (kΩ)
4	0x0	0
8	0x1	1.5
12	0x2	3.0
16	0x3	4.7
20	0x4	6.2
24	0x5	7.5
32	0x6	9.1
64	0x7	11

***Note**: For analog programming, resistors are recommended to be 1% tolerance or lower.*

The actual value of the current sense amplifier gain can be read via the bitfield CS_GAIN_ST of the register FUNCT_ST.

3.5.7 Current sense amplifier DC calibration

The 6EDL7151 features a calibration method for the current sense amplifiers. This helps, for example, to eliminate any unwanted offset in the output of the amplifiers before starting motor operation.

The activation of the DC calibration mode via the bitfield CS_EN_DCCAL configuration (only during active state when EN_DRV is high) will short the inputs of the amplifiers. Once the DC calibration is enabled, the output on the CSOx pins then can be measured by precise ADC channels in an MCU to record any possible offset in the amplifiers. The excess voltage in the CSOx pin can be subtracted in the MCU from the future measurements, for example, by software means. It is recommended to perform DC calibration before the PWM is started, when the current in the shunts, is known to be zero.

Once the offset value is captured, the MCU should set the CS_EN_DCCAL bitfield back to b0 to end the calibration process and reconnect the operation amplifier to the input pins. After that the PWM signals can start-up.

***Note**: Auto-zero, if enabled, is executed every 100 µs instead of 200 µs during DC calibration.*

3.5.8 Current sense amplifier auto-zero

Current sense amplifiers tend to accumulate offset during operation if they are not corrected. This can be due to the temperature or aging effects. The auto-zero feature of the current sense amplifiers provides an automatic way of compensating any possible drifts in the amplifiers. Internally the amplifier shorts the inputs to correct any possible offset excess for a t_{AUTO_ZERO} period of time. CSOx pin holds the voltage before the auto-zero start during the auto-zero period.

The auto-zero feature can be disabled via the bitfield CS_AZ_CFG in the register CSAMP_CFG2.

3.5.8.1 Internal auto-zero

If configured as internally triggered or internal synchronization via the bitfield CS_AZ_CFG, the auto-zero period starts with the GHx (x depends on the activated current sense amplifier A, B or C) signal rising edge after at least 100 µs from last auto-zero period. The synchronized start of auto-zero period is chosen to interfere minimum possible with the shunt resistor sensing. Details of signals behavior example can be seen in Figure 26 or Figure 31. The auto-zero occurs upon next GHx rising edge after the timer has reached 100 µs.

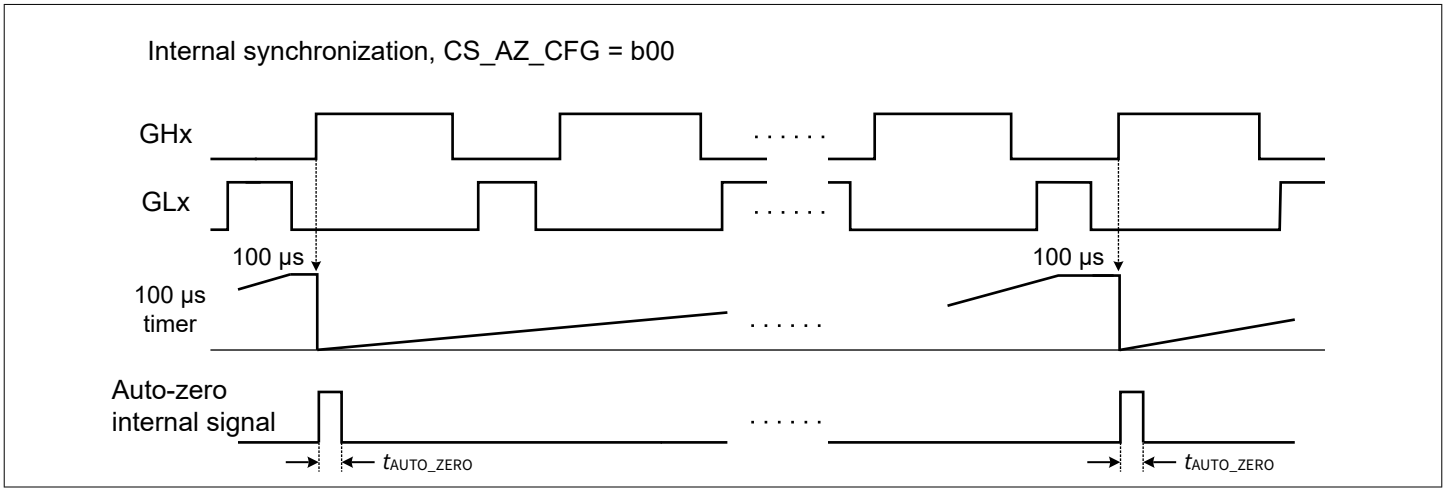

Figure 31 Auto-zero operating with internally synchronization with GHx signals

During start-up, the auto-zero function automatically activates to ensure that the amplifiers are optimized before the active state is entered. This happens during the charge pump start-up, which is from EN_DRV turn on until charge pump UVLOs are released.

If no GHx rising edge happens for a given time ($t_{AUTO\_ZERO\_CYCLE}$), for example if the low-side is fully turned on for a long period in a 6-step commutation, then an internal watchdog forces an auto-zero compensation. Auto-zero continues during standby state.

***Note**: When the auto-zero period finishes and the CSOx returns to normal, it is expected to see a minor voltage glitch. This can be blanked or filtered out, for example, at the signal path prior to the ADC conversion.*

3.5.8.2 External auto-zero synchronization via CS_GAIN/AZ pin

The user can enable external synchronization of the auto-zero function by writing the bitfield CS_AZ_CFG. In this case, the internal synchronization with GHx signals is disabled and the falling edge of the pin CS_GAIN/AZ becomes the trigger for auto-zero correction period. This is depicted in Figure 32. The CS_GAIN/AZ pin falling edge triggers the auto-zero correction period.

If externally triggered, the microcontroller in the system can decide when to execute the auto-zero correction according to the particular current sense method. As a result of this feature, the auto-zero effect can be moved, for example, far from the ADC sampling in the microcontroller, so it can benefit from the auto-zero corrections but still be able to sample without the interference of the auto-zero process.

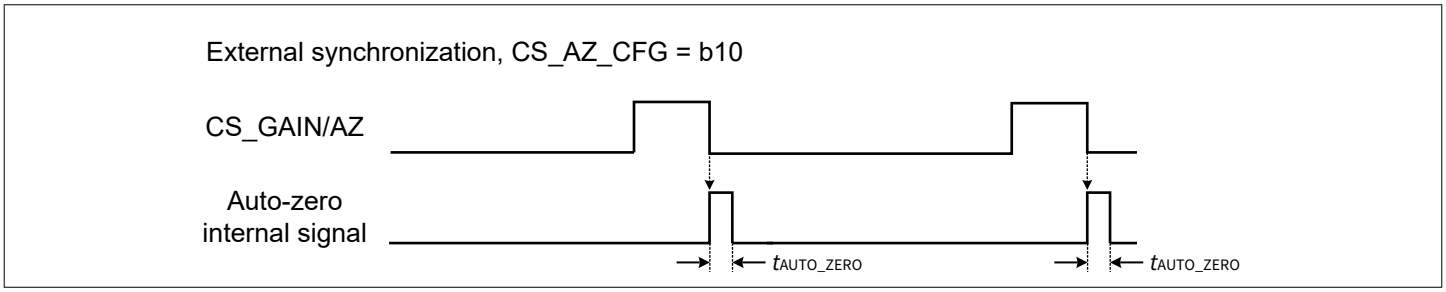

Figure 32 Auto-zero functionality with external synchronization

3.5.8.3 External auto-zero synchronization via CS_GAIN/AZ pin with enhanced sensing

6EDL7151 allows it to stop the clock (clock gating) of the charge pump modules according to CS_GAIN/AZ pin state. If this feature is activated by the bitfield CS_AZ_CFG, the charge pump clock is gated from the rising edge of the CS_GAIN/AZ pin until the end of the auto-zero period, and the clock starts after the falling edge of the same pin. The effect of the clock gating is the reduction of possible switching noises that can couple into sensitive PCB signals like CSOx or other ADC measured voltages to the system MCU or other sampling circuits.

The auto-zero with external synchronization and charge pump clock gating is shown in Figure 33. The charge pump clock is gated to reduce the switching noise coupling during the periods when sensitive measurements are performed in the system, one example is the ADC sampling period in an MCU.

***Note**: During clock gating period, the charge pump stops operation. As a result, the VCCLS and VCCHS rails stops regulation and can drop below their regulated voltages. In most cases, the VCCLS and VCCHS capacitors maintain enough voltage to keep driving the MOSFETs efficiently. The user must check that the operating range and electrical characteristics in Chapter 4 are respected. UVLO protection on both VCCLS and VCCHS is provided in the event of a fault, protecting the inverter.*

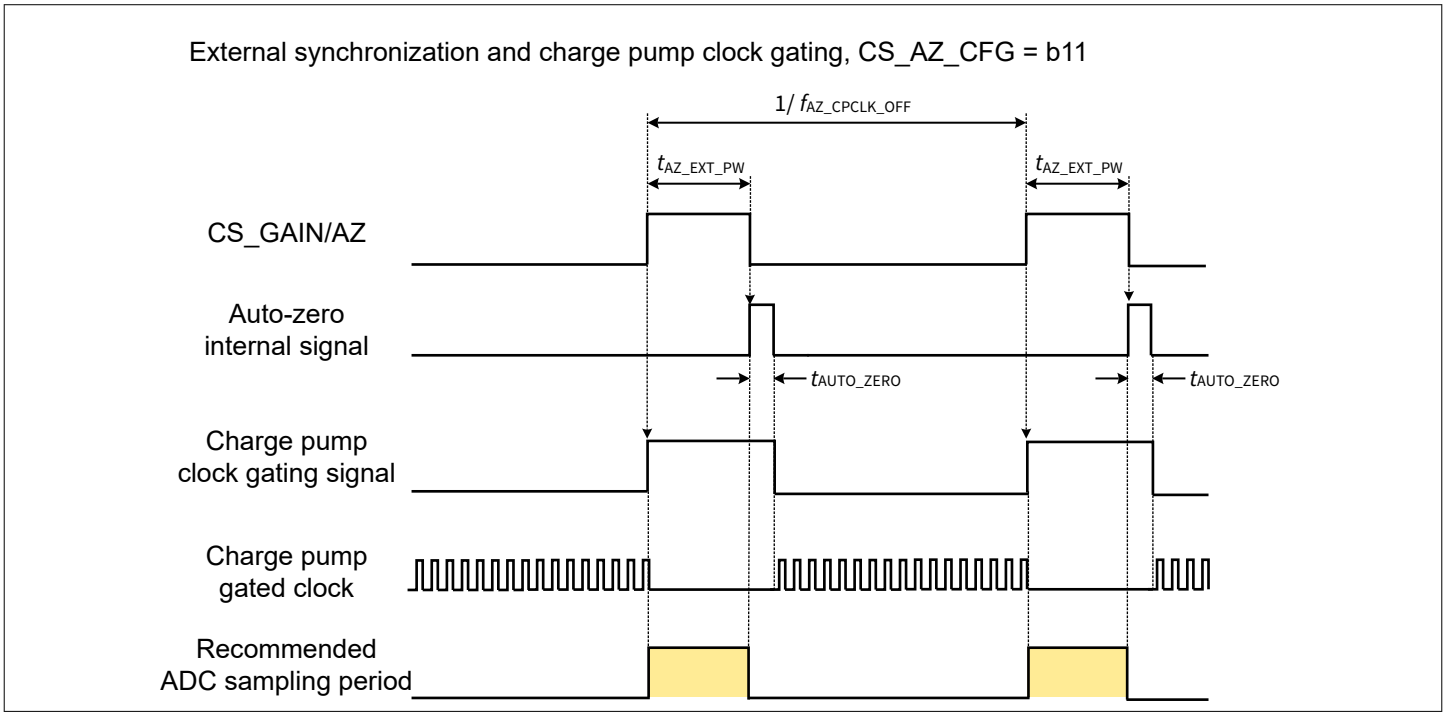

Figure 33 Signal diagram for the enhanced sensing mode using external synchronization of auto-zero function

3.6 VDS sensor system

VDS sensors provide the possibility to monitor the status of the external MOSFETs and detect potential fault conditions. One VDS sensor is provided for each MOSFET in a three-phase inverter, three for high-side MOSFETs and three for low-side MOSFETs. The sensors use the drain (VDRAIN pin for high-side MOSFETs and SHx pins for low-side MOSFETs) and source (SHx pins for high-side MOSFETs and SLx pins for low-side MOSFETs) terminals as inputs for the six VDS sensors. Programmable thresholds, independent for high-side (VDS_HS_TH) and low-side (VDS_LS_TH) MOSFETs, allow customized detection levels for different operating conditions. A blanking circuit is present as well to disable the VDS sensors during a programmable time (t_{VDS_BLANK}) when the MOSFETs are expected to switch from battery voltage to ground or vice versa. Finally, to avoid wrong triggering due to noise, a deglitching filter (VDS_FILTER) is also configurable via the SPI register.

Figure 34, Figure 35 and Figure 36 show the block diagram of the VDS sensor module in the 6EDL7151.

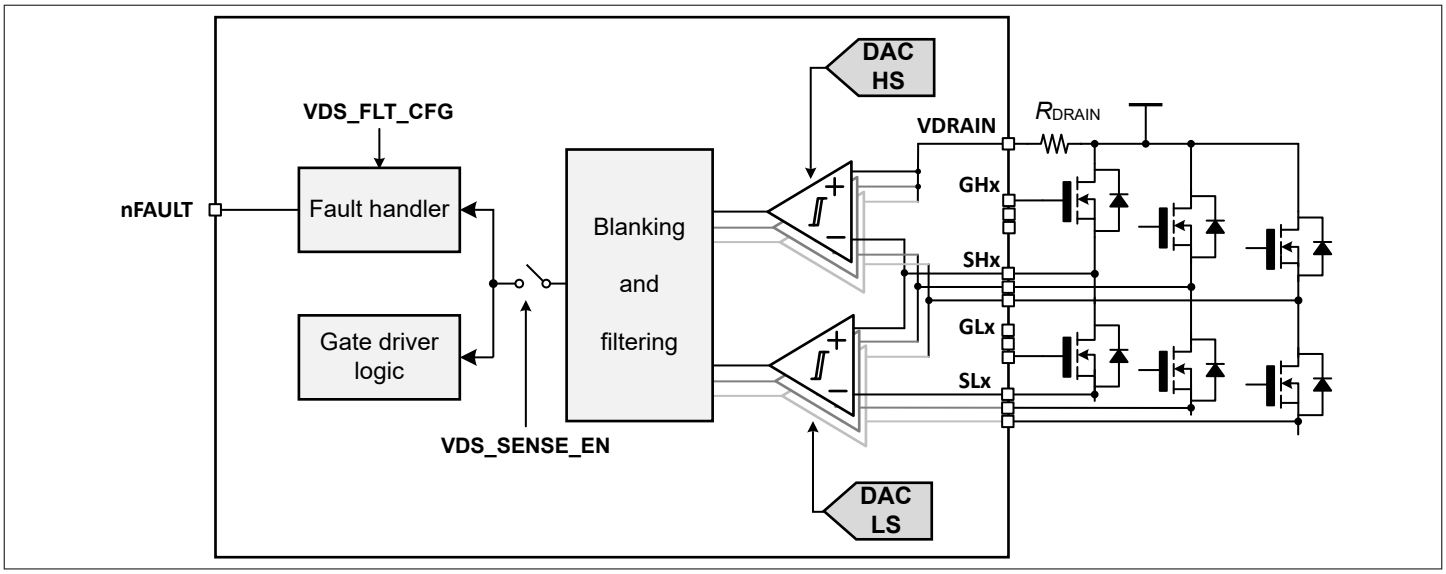

Figure 34 VDS sensor block diagram

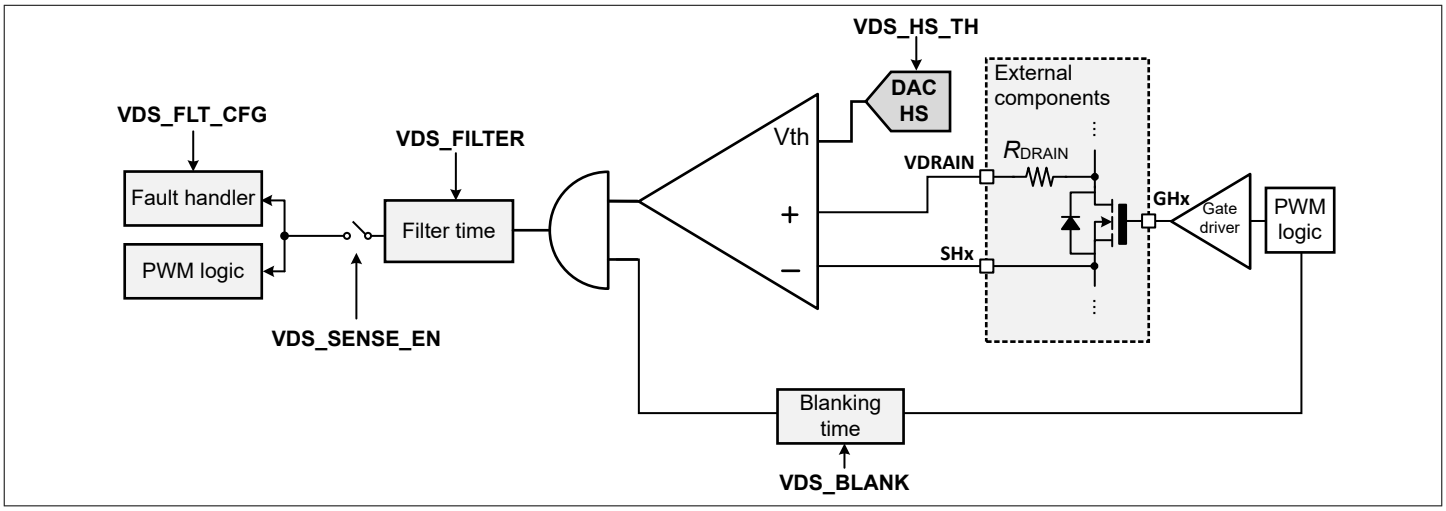

Figure 35 Block diagram of high-side VDS sensor including gate driver logic

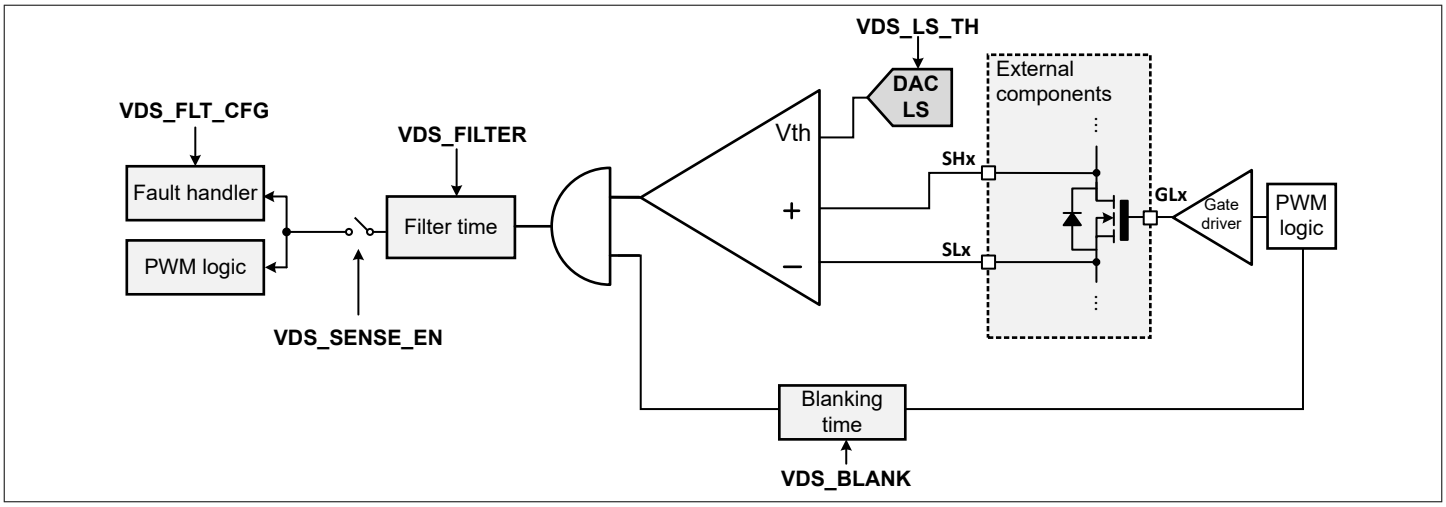

Figure 36 Block diagram of low-side VDS sensor including gate driver logic

Figure 37 shows the ideal behavior of one half bridge switching event. The MCU drives pins INHx and INLx for turning on and off the corresponding external MOSFETs according to the programmed PWM mode.

The VDS sensor of a MOSFET is enabled only when that MOSFET is activated. The VDS sensor for that MOSFET is switched off during the turn off periods of the MOSFET.

During the MOSFET switching, the inverter phase node (SHx) transitions from ground to battery voltage and vice versa. This period needs to be blanked to ensure these transitions are not detected as an overcurrent condition by the VDS sensor. A configurable blanking period is available via SPI programming to configure the period that is ignored from the start of Gxy signal activation. Only after the blanking time is elapsed, the inputs are compared with the programmed threshold to detect a fault condition.

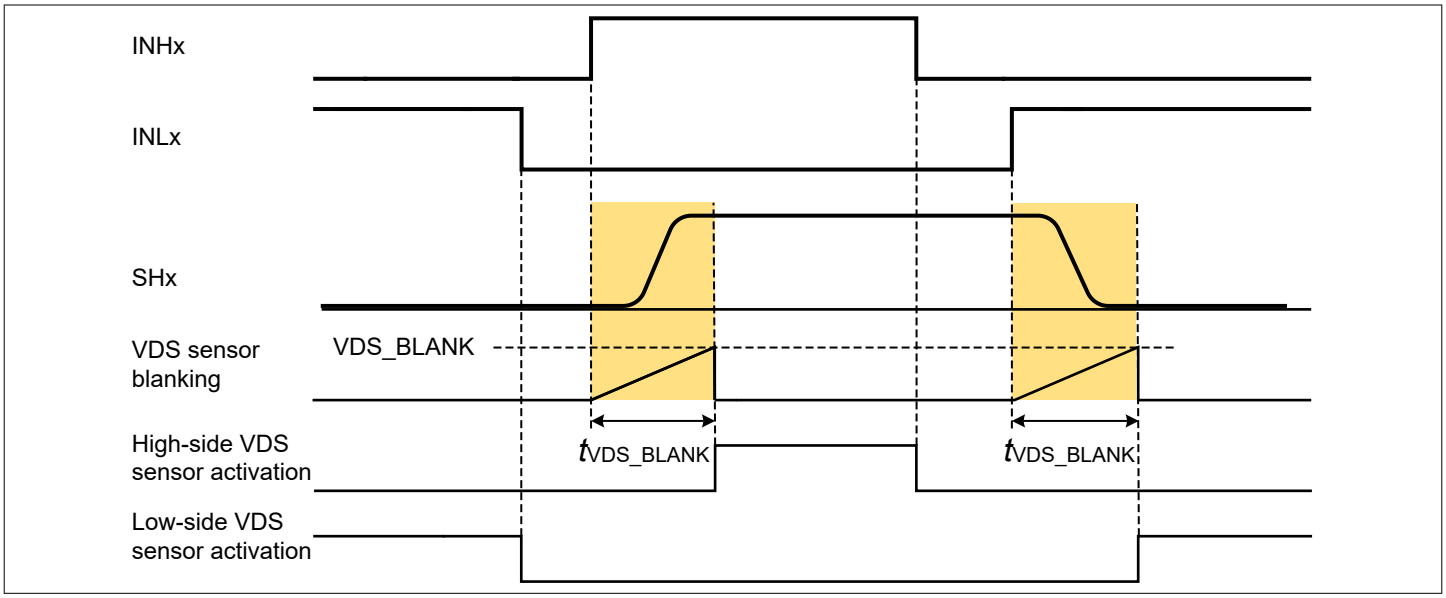

Figure 37 VDS sensor blanking behavior and operation waveforms

Once the VDS sensor is activated, the drain to source voltage is monitored and compared against a programmable value, $V_{VDS\_HS\_TH}$ for high-side and $V_{VDS\_LS\_TH}$ for low-side. When the comparator activates for longer than t_{VDS_FILTER} time (SPI configurable), the VDS fault is triggered, stopping the inverter operation and reporting to the nFAULT pin. The filter function deglitches the OCP functions and prevent noises, glitches or too short overcurrent events being detected as faults. The filter functionality is shown in Figure 38.

A microcontroller can check for the detected VDS faults by polling the status register or by monitoring the nFAULT pin, while the report behavior of the faults is configurable via the bitfield VDS_FLT_CFG. Status bits are available for each of the six VDS sensors. These faults are latched and operation can be resumed only if the MCU clears the fault or if there is a power cycle. For more details of VDS fault handling, see Chapter 3.14.

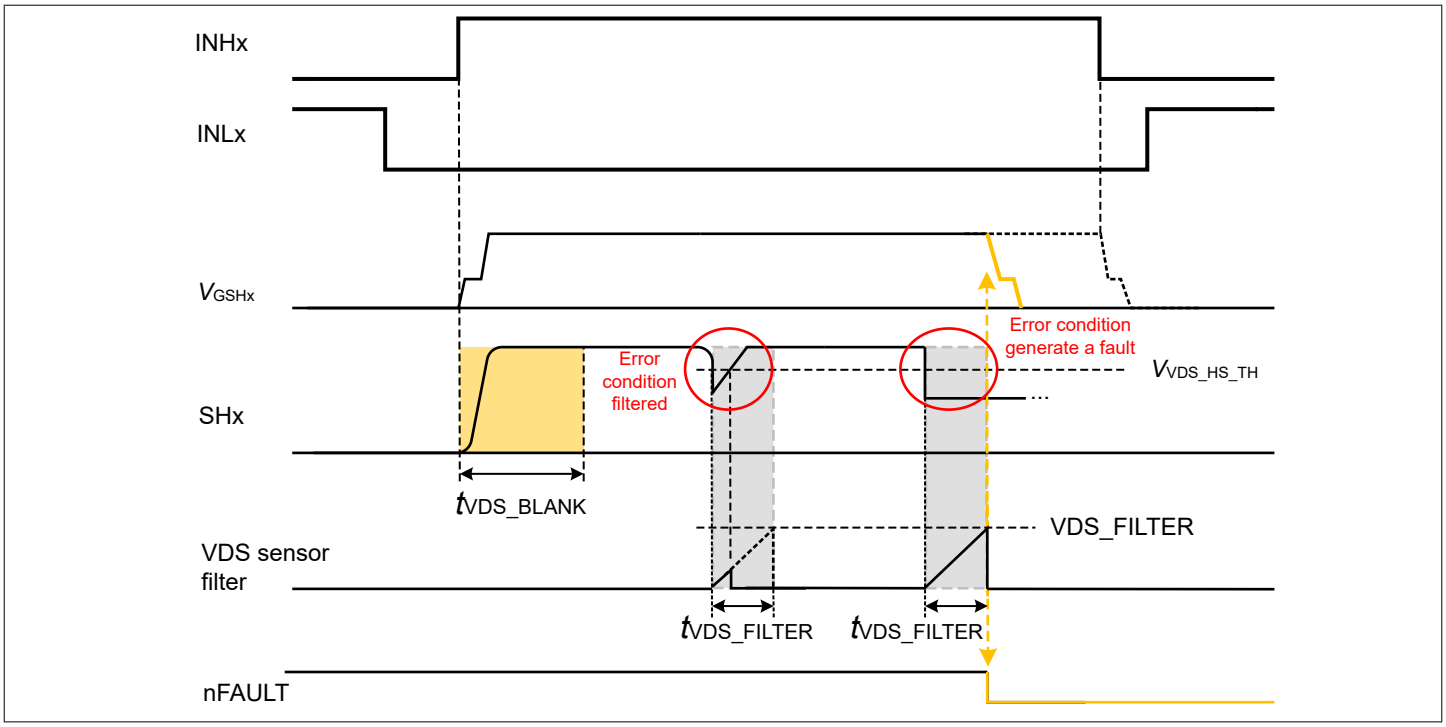

Figure 38 VDS sensor filter behavior

3.7 VDS sensor OFF state diagnostics mode

VDS sensors can be activated also during standby mode (EN_DRV pin is low). This can be used for OFF state diagnostics, which is activated by writing to the bitfield VDS_OFF_DIAG_EN in the SENSOR_CFG register. In this case, the VDS sensors are activated according to the input PWM signals (INHx and INLx) and blanking time as described before, but it does not activate the gate driver outputs. This means if INHA is high, then the VDS sensor for high-side MOSFET A is activated. However, the gate driver stage does not output any signal in the GHA pin. For this example, the drain to source voltage of the high-side MOSFET A is compared against the programmed $V_{VDS\_HS\_TH}$ value and report the status to the VDS high-side A sensor status bitfield VDS_HSA_ST of the register FUNCT_ST.

***Note**: The detected faults in OFF state diagnostics won't be reported via nFAULT pins but only via register reporting.*

***Note**: OFF state diagnostics must be used with 6PWM mode only.*

***Note**: To activate the OFF state diagnostics mode of VDS sensors, it is suggested first to pull low EN_DRV pin, write VDS_SENSE_EN and VDS_OFF_DIAG_EN bitfields to enable the VDS sensors and OFF state diagnostics mode, then pull high EN_DRV pin.*

Table 10 summarizes the expected behavior of the VDS sensors, CSAMP, and gate driver outputs for the combinations of VDS_OFF_DIAG_EN and EN_DRV.

Table 10 OFF state diagnostics truth table

VDS_OFF_DIAG_EN	EN_DRV	VDS sensors	CSAMP	Gate driver outputs	Description
1	0	OFF	OFF	Disabled, High-Z	–
1	1	ON	OFF	Disabled, High-Z	OFF state diagnostics mode. Charge pumps are enabled

(table continues...)

Table 10 (continued) OFF state diagnostics truth table

VDS_OFF_DIAG_EN	EN_DRV	VDS sensors	CSAMP	Gate driver outputs	Description
0	0	OFF	OFF	Disabled, High-Z	–
0	1	ON or OFF (user choice)	ON	Enabled, follow PWM inputs	Normal operation. Charge pumps are enabled

Figure 39 shows a timing example of different signals during the activation of the OFF state diagnostics mode.

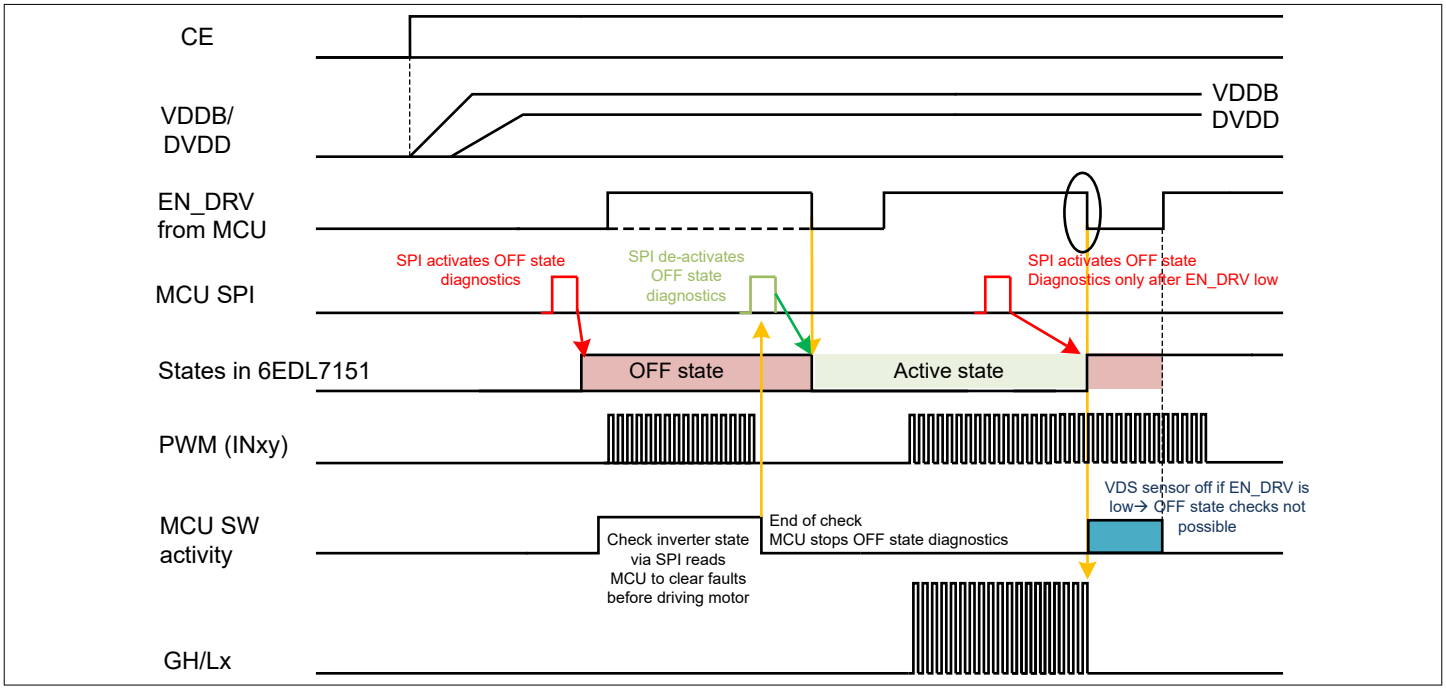

Figure 39 OFF state diagnostics mode waveforms - VDS sensors need to activate with EN_DRV low during OFF state period

3.8 Hall comparators

6EDL7151 has three identical channels of Hall comparators and the Hall sensor inputs are capable of interfacing with digital Hall sensors with open-drain outputs. Each Hall sensor should be connected to one of the INLx digital pins. Hall comparators are designed to be used for 1PWM mode with Hall sensors as described in Chapter 3.1.4 as well as for locked rotor detection functionality described in Chapter 3.9.3.

The Hall inputs are digitally deglitched so that those inputs ignore any extra Hall transitions for a configurable period of time. This is selected in the bitfield HALL_DEGLITCH that can be accessed via the SPI commands. It prevents the PWM noise from being coupled into the Hall inputs, which may result in erroneous commutation. The polarity of the Hall sensor inputs can be read in the bitfield HALLIN_ST of the register FUNCT_ST by an MCU at any time.

The integrated DVDD linear regulator can be used to supply the Hall sensors either with 3.3 V or 5 V according to the programming. In this case, the Hall sensors are not powered by the DVDD rail but by another power supply, and the DVDD supply is disabled for any reason due to IDLE or OFF mode ($V_{CE} < V_{CE\_TH\_F}$), the Hall inputs should not be driven by external voltages. In addition, they should be powered-up before starting the motor, otherwise an invalid Hall state may cause malfunction in the motor operation.

3.9 Watchdog timers

6EDL7151 integrates three independent watchdog timers that are SPI configurable. These protection features are used to ensure the correct functionality of different modules inside and outside the device, for example, to ensure that a microcontroller is having a correct behavior by serving or ‘kicking’ the 6EDL7151 watchdog. To configure

watchdog timers in 6EDL7151, the two registers WD_CFG and WD_CFG2 are available. The three independent watchdog timers are:

- Buck converter watchdog
- General purpose watchdog
- Rotor locked watchdog

Each watchdog timer core unit includes a digital timer (watchdog timer). A source signal is connected to that timer, which resets whenever a toggle occurs on the signal. Otherwise the timer keeps counting up. If the watchdog timer limit is reached without a reset input, then a fault takes place and action is performed according to Table 12.

The reaction to a watchdog fault is programmable to the following actions:

- Reporting to status register only
- Reporting to status register and the nFAULT pin
- Trigger a configurable braking event
- Select whether watchdog fault is latched or not

An example of a watchdog operation is presented in Figure 40. In this example, a generic signal 'WD input' is resetting the counter periodically (for example when reading the status register or toggling EN_DRV at the proper frequency). If the input signal stops toggling, the watchdog timer expires after the watchdog period resulting in a watchdog fault.

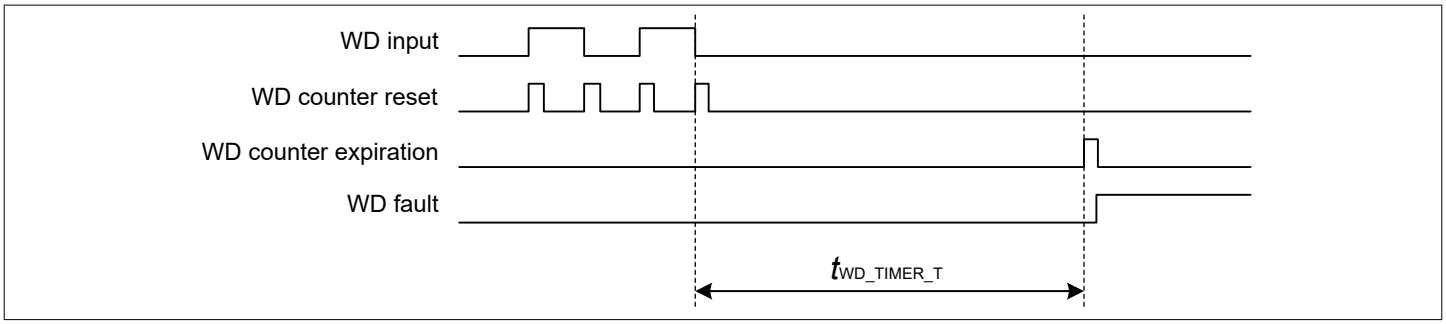

Figure 40 Watchdog operation diagram

3.9.1 Buck converter watchdog timer

During the device start-up, the buck converter watchdog monitors the VDDB UVLO signal. When UVLO of VDDB is asserted, the watchdog is cleared. If UVLO of VDDB is not asserted within the watchdog period ($t_{WD\_BUCK\_T}$), the system stops (STOP state in the state machine is described in Chapter 3.13) and stays disabled until a power cycle takes place. This watchdog can be used for a safe start-up debugging. To enable this feature, the bitfield WD_BK_DIS of the register WD_CFG2 needs to be cleared.

3.9.2 General purpose watchdog timer

This watchdog timer can be configured to use different general purpose inputs (timer reset signal) via the bitfield WD_INSEL. Possible inputs are:

1. **EN_DRV**: Coded in EN_DRV, a clock signal can be utilized as watchdog timer clock input. The watchdog measure that the frequency and duty cycle of this signal are correct. The proper frequency works as a watchdog 'kick', see Chapter 3.10.1. It requires enabling the watchdog via WD_EN and an input selection via WD_INSEL. After a fault occurs, clearing of the fault must be done only after two periods (500 Hz). The EN_DRV watchdog period is fixed and not programmable.
2. **DVDD start-up**: During start-up, if this input is selected, the watchdog is cleared upon a DVDD UVLO signal assertion. If DVDD has not reached the correct value before the watchdog period, the DVDD regulator retries to start. The number of attempts to restart the DVDD regulator when the start-up fails can be configured in WD_DVDD_RSTRT_ATT. Additionally, the time between restarts attempts is set in the bitfield WD_DVDD_RSTRT_DLY.

3. **Charge pumps start-up**: Similarly, the start-up time of the charge pumps (both VCCLS and VCCHS) can be monitored. The UVLO signal of both, VCCLS and VCCHS, clear the watchdog, otherwise, a fault is reported. To select this input, the bitfield in WD_INSEL has to be set accordingly.
4. **Status register SPI read action**: In this configuration, the watchdog resets every time the FAULT_ST status register is read via an SPI command. In this way, it checks that the MCU is active and the SPI communication is working adequately.

The general-purpose watchdog timer needs to be enabled via the WD_EN bitfield. The watchdog period is programmed in WD_TIMER_T except for EN_DRV as watchdog input.

3.9.2.1 Brake on general purpose watchdog fault

The general purpose watchdog timer can be configured to trigger a brake event when the comparator trips. This is activated in the bitfield WD_BRAKE and is only possible to the condition when either the ‘EN_DRV pin’ or the ‘Status register read’ is chosen as input. The brake event can be configured to either brake the motor by shorting all high-side MOSFETs, all low-side MOSFETs, alternate between those options, or set all MOSFETs to high-Z. This is configured in the bitfield BRAKE_CFG in the PWM_CFG register. For more details, refer to Chapter 3.1.6 and Chapter 3.14.

3.9.3 Locked rotor protection watchdog timer

6EDL7151 provides a locked or stalled rotor protection function by integrating a dedicated watchdog timer. The rotor locked watchdog timer inputs are the three Hall sensor signals (INLA, INLB and INLC). Therefore, this protection is only possible when using Hall sensor based on control schemes or 1PWM modes.

Locked or stalled rotor can occur in the event of a mechanical malfunction or excessive load torque that causes the motor to stop rotating while enabled. The locked rotor function can be enabled by setting the bitfield WD_RLOCK_EN to b1. A locked rotor condition is detected if the Hall pattern is maintained for t_{LOCK} period. The t_{LOCK} time is configured via SPI (bitfield WD_RLOCK_T).

In order to increase robustness, an especial case of rotor locked detection is implemented. In some cases, the motor stalls in a position in which the Hall sensors can still provide a cyclic or repeated toggling. In some cases vibration or bending of the motor can cause this effect, in other cases, the Hall sensors get stalled close to the magnets. 6EDL7151 detects this condition as rotor locked. An example of such Hall sensor inputs sequence that would report a fault is the following:

100, 101, 100, 101, 100, 101, …..

As soon as the locked rotor condition is detected, the device sets the bitfields WD_FLT and RLOCK_FLT of the FAULT_ST register to b1. Upon detection of locked rotor condition the device enters high impedance state (high-Z). Additionally, the nFAULT pin is pulled down. An MCU can read this signal and request a status update to the device or execute other corrective actions.

3.9.3.1 Hall sensor malfunction

In case of an Hall sensor failure, the rotor locked protection can help to bring the motor to a safe state. The malfunction of two or three Hall sensors causes a rotor lock fault in 6EDL7151. However, a single Hall sensor failure cannot be detected as malfunction and does not trigger a fault.

The rotor locked condition can be reset by toggling EN_DRV (switch off and on again).

3.9.3.2 Situation of PWM signals on hold

If the PWM input signals generated by the controller stop switching while the rotor locked protection is enabled, 6EDL7151 recognizes the subsequent motor stop as a failure and triggers the rotor locked protection after t_{LOCK} period. In case this behavior is not desired, the user code in the controller that stops the PWM switching must be preceded by an SPI command to disable the rotor locked protection.

3.10 Multi-function pins

3.10.1 EN_DRV pin

The pin EN_DRV has two different functionalities that can work simultaneously:

1. Enable pin: to start the charge pump operation and finally enable gate drivers and current sense amplifiers when pulled high: $V_{EN\_DRV} > V_{EN\_DRV\_TH}$ (see Table 21).
2. Watchdog clock input: this clock signal can be generated by the microcontroller in the system and permits 6EDL7151 to detect whether the microcontroller is generating the correct signal, and therefore to detect if the controller is working properly or not (for example software failure), increasing robustness of the whole system. In case the clock signal is not present or the period of this clock is outside of 10% of the expected value (see Table 21), the watchdog of 6EDL7151 will react with a pre-programmed action (more details in Chapter 3.9).

If both functions are used simultaneously, the microcontroller can use two GPIOs, one for EN_DRV (GPIO) and the other for the clock generation (GPIO or PWM signal, for example). The analog summation of those two signals is decoded inside 6EDL7151. Figure 41 describes the connections and electrical signals in such a configuration.

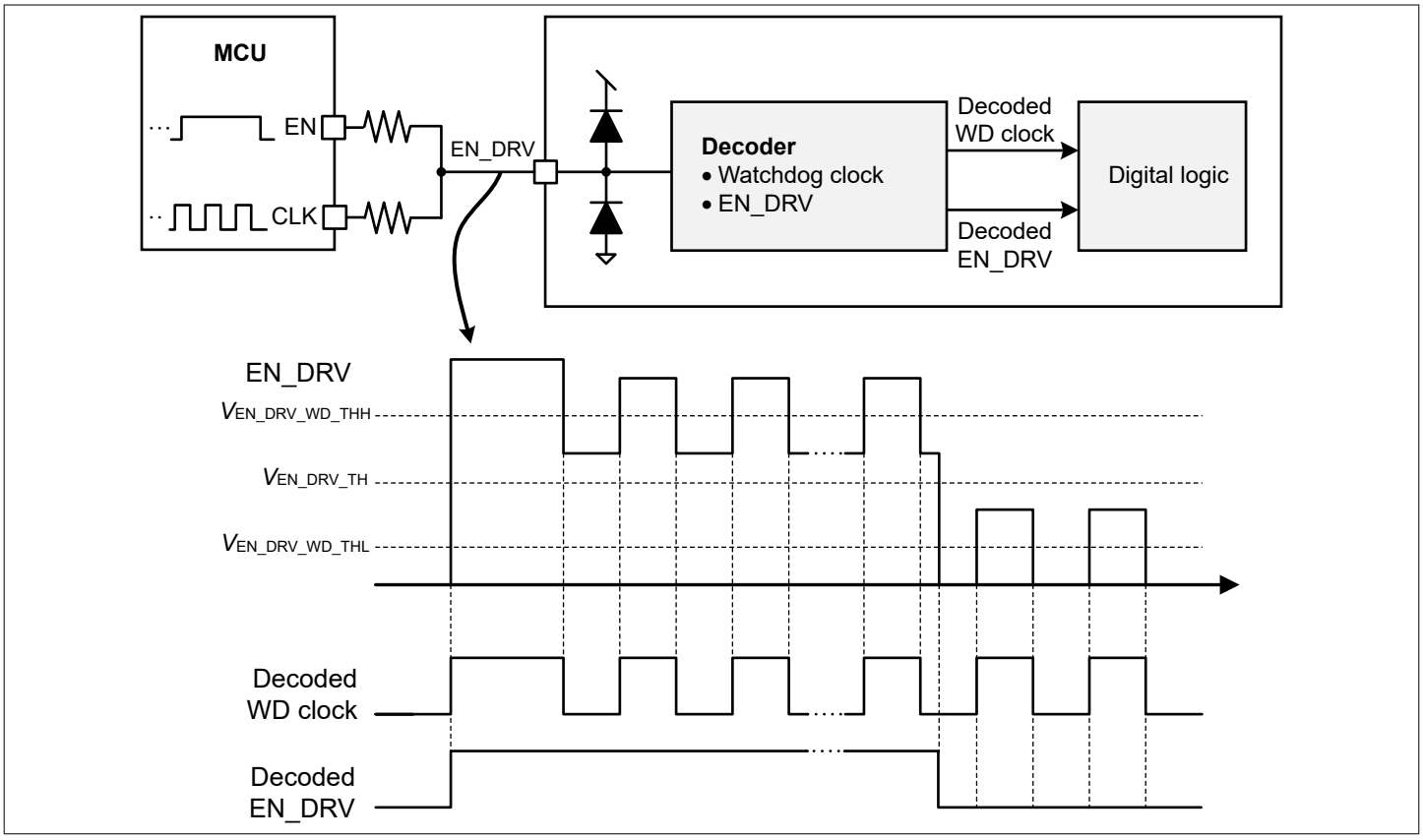

Figure 41 Usage of EN_DRV pin for both enabling gate driver and decoding of watchdog clock signal

3.10.2 VSENSE/nBRAKE pin

Pin VSENSE/nBRAKE supports two different functionalities:

1. VSENSE function: During start-up, the 6EDL7151 reads the resistor value connected to pin VSENSE/nBRAKE. Depending on the reading, the 6EDL7151 selects the DVDD set point to either 3.3 V or 5 V. After that, the device will start-up the DVDD linear regulator with the target DVDD set point.
2. nBRAKE function: During normal operation (after DVDD UVLO is released), the pin is an input (with active low logic) that can be pulled down, for example, by the MCU to initiate a brake event, bringing the motor to standstill in a controlled way. Usually the pin is high so that the PWM signals propagate to the gate driver outputs normally.

3.10.3 CS_GAIN/AZ pin

CS_GAIN/AZ pin implements two different functionalities:

1. CS_GAIN function: during start-up, a resistor R_{CS_GAIN} connected to this pin is read leading to the analog programming of the current sense amplifier gain. This is explained in detail in Chapter 3.5.6.
2. AZ function: during normal operation, the pin can be used as an input to enable the external auto-zero functionality described in Chapter 3.5.8.

In order not to affect the analog programming of the current sense amplifiers gain via the external resistor, the MCU is recommended to be connected to the CS_GAIN pin with a series diode, so that when DVDD is still not at the final target value, the MCU output circuitry does not load the CS_GAIN pin leading to a wrong programming of the amplifier's gain. This proposed circuit is shown in Figure 42. If digital programming of the current sense amplifier gain is desired, R_{CS_GAIN} is not needed and the diode can be excluded from the circuit as well.

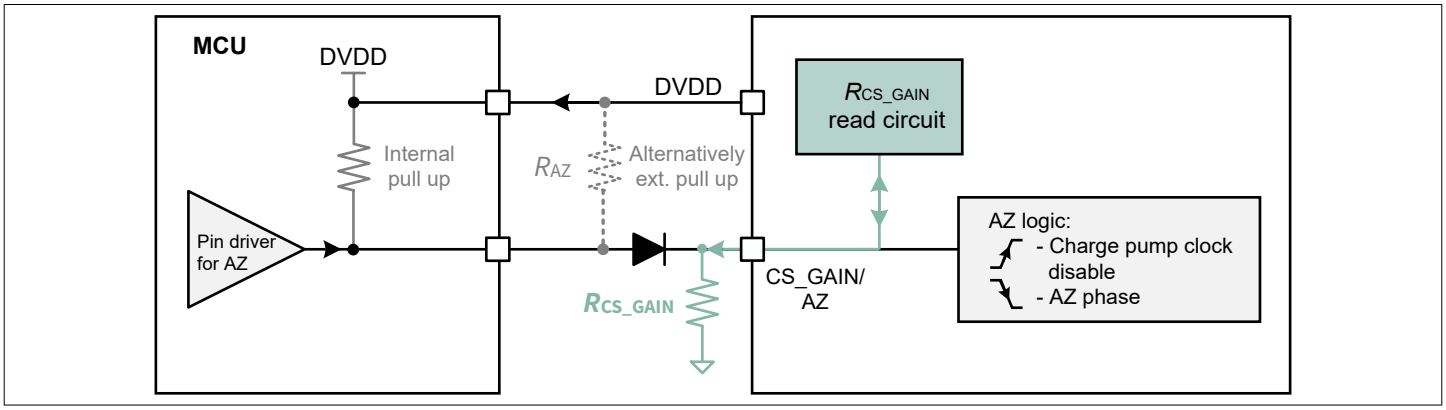

Figure 42 CS_GAIN/AZ multi-function pin usage example

***Note**: The internal pull up in the MCU side depends on the specific microcontroller. Some microcontrollers might not offer enough pull up capability and an external pull up resistor might be required as shown.*

3.11 ADC module

The 6EDL7151 integrates an ADC (analog to digital converter) based on the SAR architecture with 7-bit resolution. This ADC can be used to do redundant measurements to those executed in the MCU or to measure gate driver related voltages. The MCU can request the ADC results of these internal measurements via an SPI reading of the result registers. The ADC can measure the following inputs during active mode:

- Automatically in ADC conversion sequence:
  - On die temperature sensor (see Chapter 3.11.2)
  - PVDD: supply voltage
  - VCCLS: low-side gate driver supply
  - VCCHS: high-side gate driver supply
- Other (on demand) conversion inputs selected via the bitfield ADC_OD_INSEL:
  - $I_{DIGITAL}$: device digital section current consumption
  - DVDD: linear regulator output voltage
  - VDDB: buck converter output voltage

Those ADC inputs are continuously converted in sequence. After each conversion is finished, the result of the conversion can be processed through integrated digital filters, which are moving average filters with configurable number of samples. PVDD uses a dedicated filter (ADC_FILT_CFG_PVDD) while the rest share a second filter (ADC_FILT_CFG). The complete architecture of the ADC module is depicted in Figure 43.

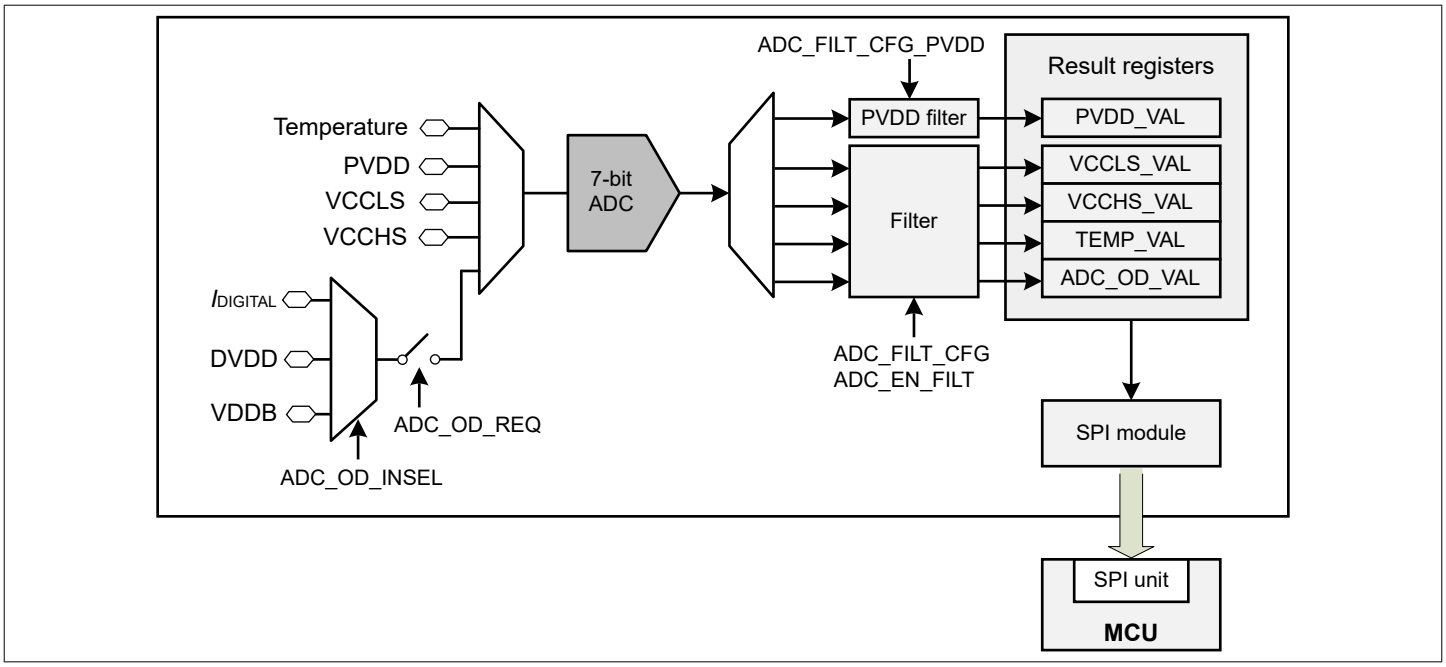

Figure 43 ADC module block diagram

Table 11 summarizes the ADC inputs characteristic including the scaling factors. These scaling factors can be used by an MCU to calculate the real analog values in volts, milliamperes, or degree Celsius.

Table 11 ADC measurements overview

Measurement	On demand conversion	ADC result bitfield	Filter bitfield	Scaling factor
PVDD	N	PVDD_VAL	ADC_FILT_CFG_PVDD	= (0.581 * PVDD_VAL + 5.52)V
Temperature	N	TEMP_VAL	ADC_FILT_CFG	= (2 * TEMP_VAL - 94)°C
VCCLS	N	VCCLS_VAL	ADC_FILT_CFG	= (VCCLS_VAL * 16 / 127)V
VCCHS	N	VCCHS_VAL	ADC_FILT_CFG	= (VCCHS_VAL * 16 / 127)V
Device current (IPVDD)	Y	ADC_OD_VAL	ADC_FILT_CFG	= (0.24 * ADC_OD_VAL)mA
DVDD	Y	ADC_OD_VAL	ADC_FILT_CFG	= (ADC_OD_VAL * $DVDD_{TARGET}$ / 127)V
VDDB	Y	ADC_OD_VAL	ADC_FILT_CFG	= (ADC_OD_VAL * $VDDB_{TARGET}$ / 127)V

For example, DVDD has been set to be 3.3 V ($DVDD_{TARGET}$), the DVDD voltage is the on demand conversion and the MCU reads the bitfield ADC_OD_VAL = 0x78 = 120 decimal value. The DVDD voltage measured by the ADC is calculated as follows:

$$DVDD = ADC\_OD\_VAL * \frac{DVDD_{TARGET}}{127} = 120 * \frac{3.3\ \ V}{127} = 3.118\ \ \ V \quad (2)$$

3.11.1 ADC measurement sequencing and on demand conversion

In active state, the ADC converts repeatedly in loops with the following sequence of six measurements:

1. PVDD
2. Temperature sensor
3. PVDD
4. VCCLS
5. PVDD
6. VCCHS

This is shown in Figure 44. Results of those conversions are placed in the dedicated result registers that can be read via SPI by the MCU. PVDD result is reported in the SUPPLY_ST register, VCCLS and VCCHS are reported in the register CP_ST and the temperature measurement is reported in the register TEMP_ST.

Additional to the standard sequence, the user can select to have other signals converted on demand. Any of this “on demand” conversion inputs, can be injected once in the standard sequence. This is done by selecting the signal to be converted in the bitfield ADC_OD_INSEL and setting b1 to the request bitfield ADC_OD_REQ, both bitfields in the register ADC_CFG.

***Note**: The write of the ADC_CFG bitfields must happen in a single SPI write. A write to a single bitfield overwrites the rest to the default value, so the full desired register value must be given in a single write or via read-modify-write sequence.*

If an on demand conversion is requested, the ADC waits to finish (end of conversion, EOC) the running conversion, if any. Then the requested on demand conversion is started. When the on demand conversion is finished, the bitfield ADC_OD_RDY is set. The MCU can poll this bitfield to make sure the result register contains the newest value of the requested conversion. The result of the on demand conversion is located in the bitfield ADC_OD_VAL and the sequence continues right where it was interrupted after the EOC of the on demand conversion. This is illustrated in Figure 44.

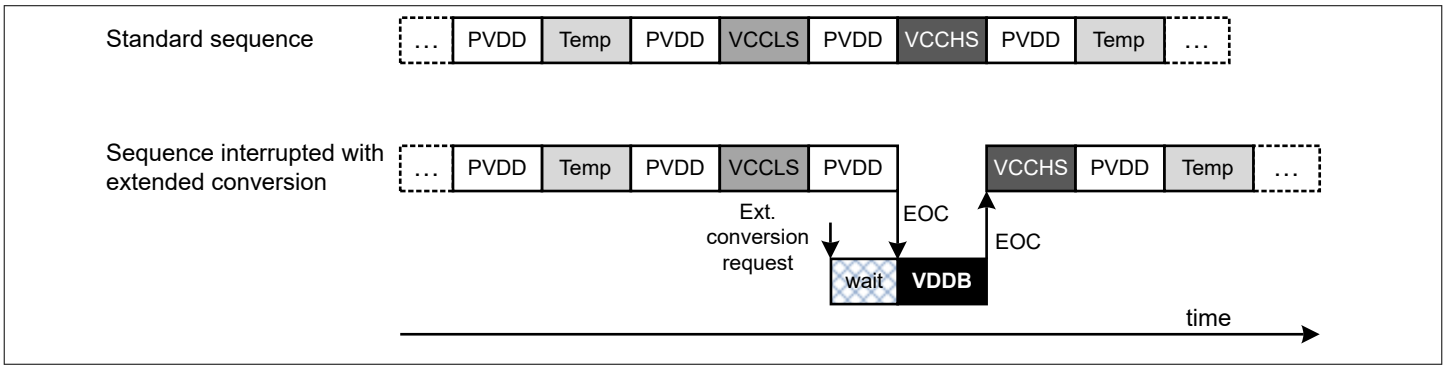

Figure 44 ADC sequencing and interruption by extended conversion request of VDDB signal

3.11.2 Die temperature sensor

A very useful ADC measurement is the device temperature, as 6EDL7151 integrates a die temperature sensor that is sampled by the integrated ADC. The temperature of the device can be read via the bitfield TEMP_VAL of the TEMP_ST register. The value is measured with a resolution of 2 degrees Celsius. For example, TEMP_VAL = 0x4A = 74 decimal value, according to Table 11, the temperature is calculated as:

$$Temperature = (2 * TEMP\_VAL - 94)°C = (2 * 74 - 94)°C = 54°C \quad (3)$$

Additionally, overtemperature warning and shut-down faults are implemented and the threshold values are provided in Table 21. The overtemperature shut-down protection can be disabled via the bitfield OTS_DIS in the register SENSOR_CFG. The occurrence of these faults can be detected by reading the bitfields OTW_FLT and OTS_FLT in the register FAULT_ST.

3.12 Device start-up

The device start-up can be divided in two main periods:

- **Power supply start-up**: Initiated by $V_{CE} > V_{CE\_TH\_R}$, leading to ramp-up of VDDB and DVDD rails.
- **Gate driver and CSAMP start-up**: Begins with EN_DRV rise and results in charge pumps ramp-up and current sense amplifiers activation.

3.12.1 Power supply start-up

Given a steady battery supply voltage (PVDD), the input CE pin controls the start-up of the power supply system. Figure 45 shows graphically the ramp-up of buck converter voltage once the CE voltage goes above the $V_{CE\_TH\_R}$ value. If the external decoupling capacitor is too large, the ramp-up time might be exceeding the value $t_{VDDB\_SFT\_START}$ provided in Table 21. The integrated watchdog can be enabled to monitor and debug the start-up of VDDB, DVDD or charge pumps.

Soft-start for the buck converter is automatically implemented using an integrated DAC for generating the target reference. Once VDDB has reached its UVLO voltage, analog programming starts. This initiates periods of t_{AN_T} when the external resistors at CS_GAIN/AZ and VSENSE/nBRAKE pins are read internally. The analog programming of these two functions can be disabled by the user via OTP programming, therefore reducing the start-up time.

After these analog programming period(s) have elapsed, another OTP programmable delay ($t_{DVDD\_TON\_DELAY}$) is inserted before the DVDD voltage starts ramping up. Longer delays allow the buck converter voltage to stabilize before the DVDD starts charging. If a shorter start-up time is required, the delay can be shortened taking into consideration the buck output voltage and the external components used (L_{BUCK} and C_{VDDB}). DVDD ramps up in a configurable time ($t_{DVDD\_SFTSTRT}$). Tuning this value helps to ensure the proper start-up.

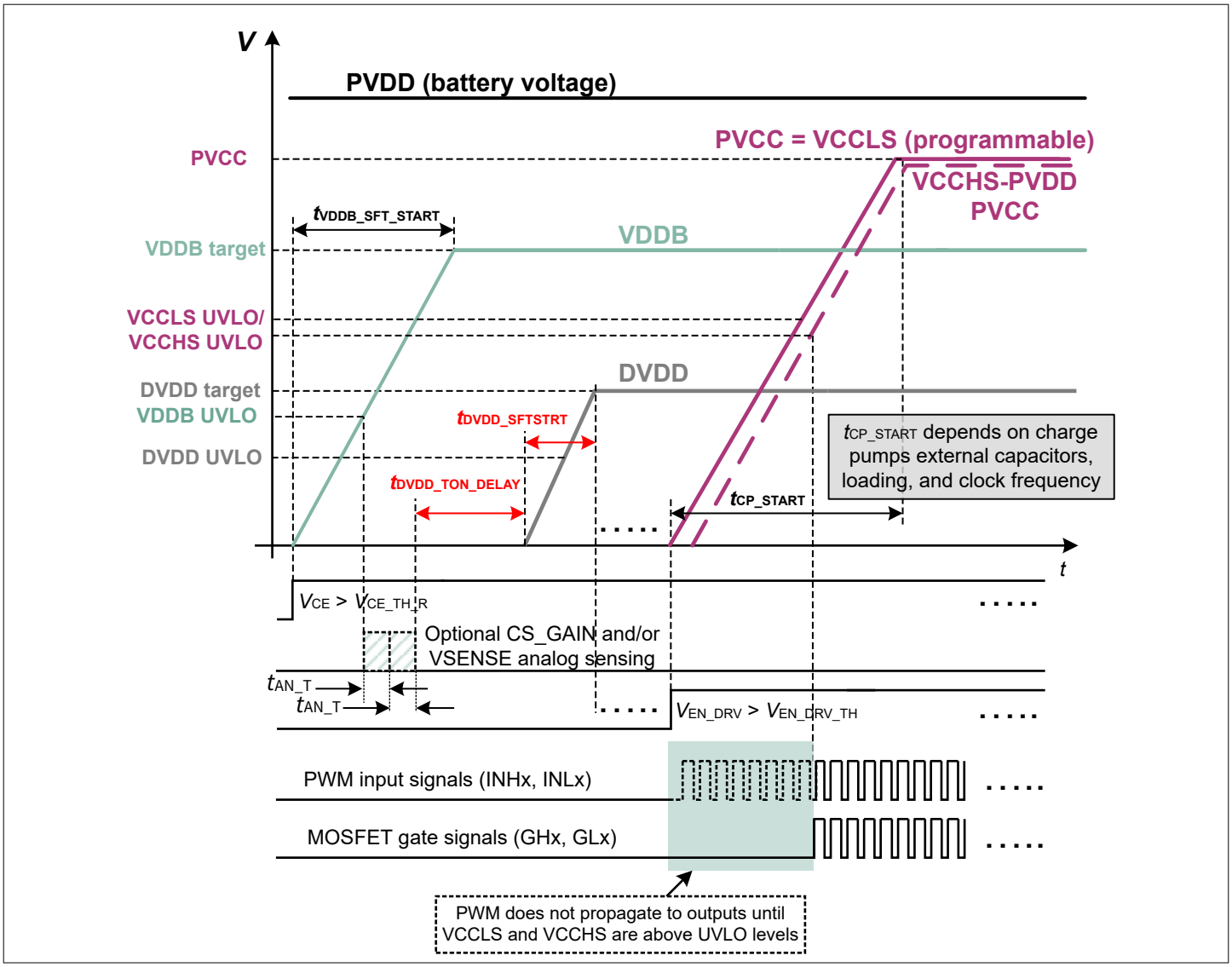

Figure 45 Start-up behavior of supply voltages at steady PVDD supply

If CE is generated from PVDD, for example via a voltage divider as shown in Chapter 5.3, the start-up behavior follows approximately the one in Figure 46 or similar. In such case, it is important to notice that the device does not start, that is, the buck converter does not start switching, until both PVDD UVLO is released and the CE rising voltage thresholds ($V_{CE\_TH\_R}$) are crossed, as can be seen in flowchart in Figure 47. The order of CE and PVDD can swap with similar results.

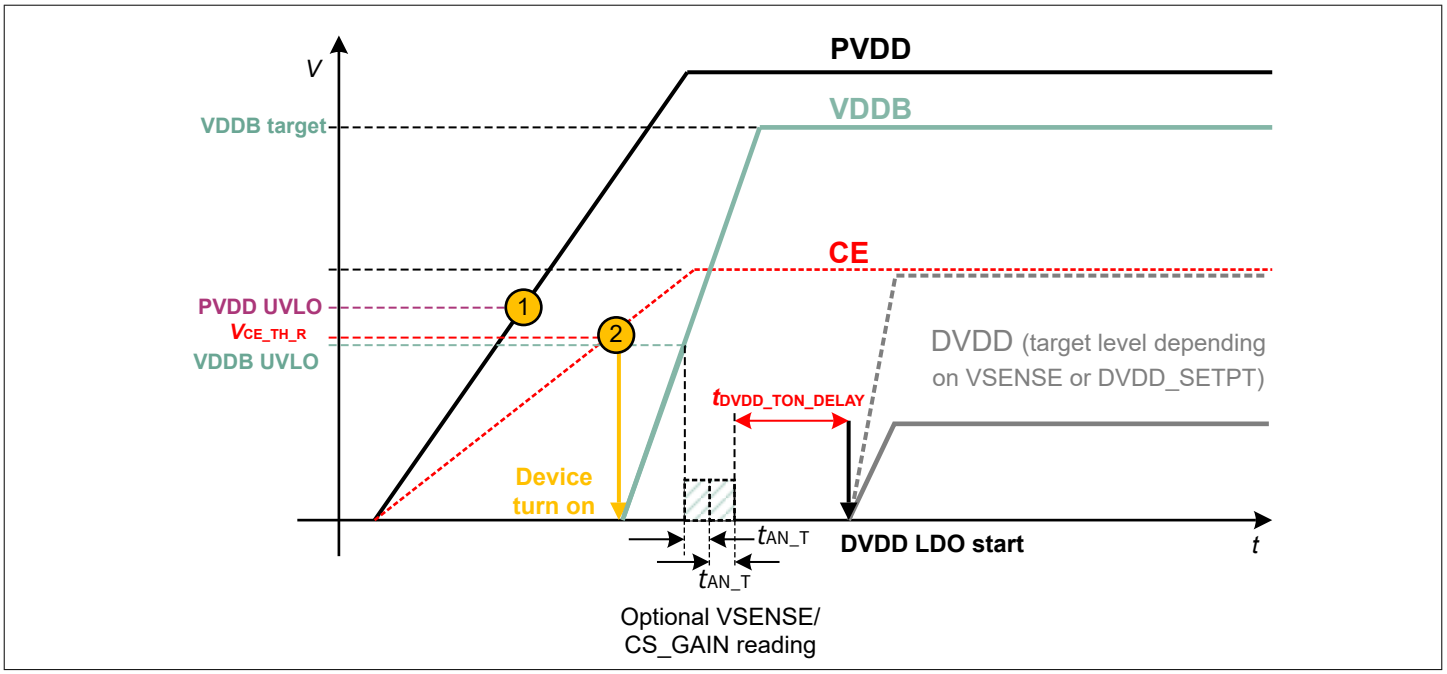

Figure 46 **Start-up behavior when PVDD is ramping up and CE is created with a voltage divider from PVDD. Device will only turn on after events 1 and 2 occurred, and start up the buck converter controller**

3.12.2 Gate driver and CSAMP start-up

Once DVDD is up and stable, the microcontroller can enable the gate driver. The EN_DRV pin needs to be set above the $V_{EN\_DRV\_TH}$ value to enable the driver section. Before this, no PWM signal transfers to the gates of the MOSFETs. Once EN_DRV is above $V_{EN\_DRV\_TH}$, both low-side and high-side charge pumps ramp up to the target value PVCC. The charge pump ramp-up time t_{CP_START} depends on different configurations (capacitors, charge pump frequency, PVCC voltage) as explained in Chapter 3.3.

The high-side charge pump starts after enough voltage is built in the low-side charge pump. After both high-side and low-side charge pumps UVLOs are reached, the PWM path is activated and the gate driver can output signals to the power MOSFETs.

***Note**:* *Depending on timing of PWM send to inputs and charge pump capacitor values, the gate driver could start driving the MOSFETs while the charge pumps are not fully at target voltage if the PWM signal is activated early. The user can delay the start of PWM signals until charge pumps are fully charged if this is required.*

3.13 Device functional states

The functionality of the device is governed by a state machine. A flowchart of this state machine is shown in Figure 47. The VDS sensor activation depends on different factors as explained in Chapter 3.6 and Chapter 3.7.

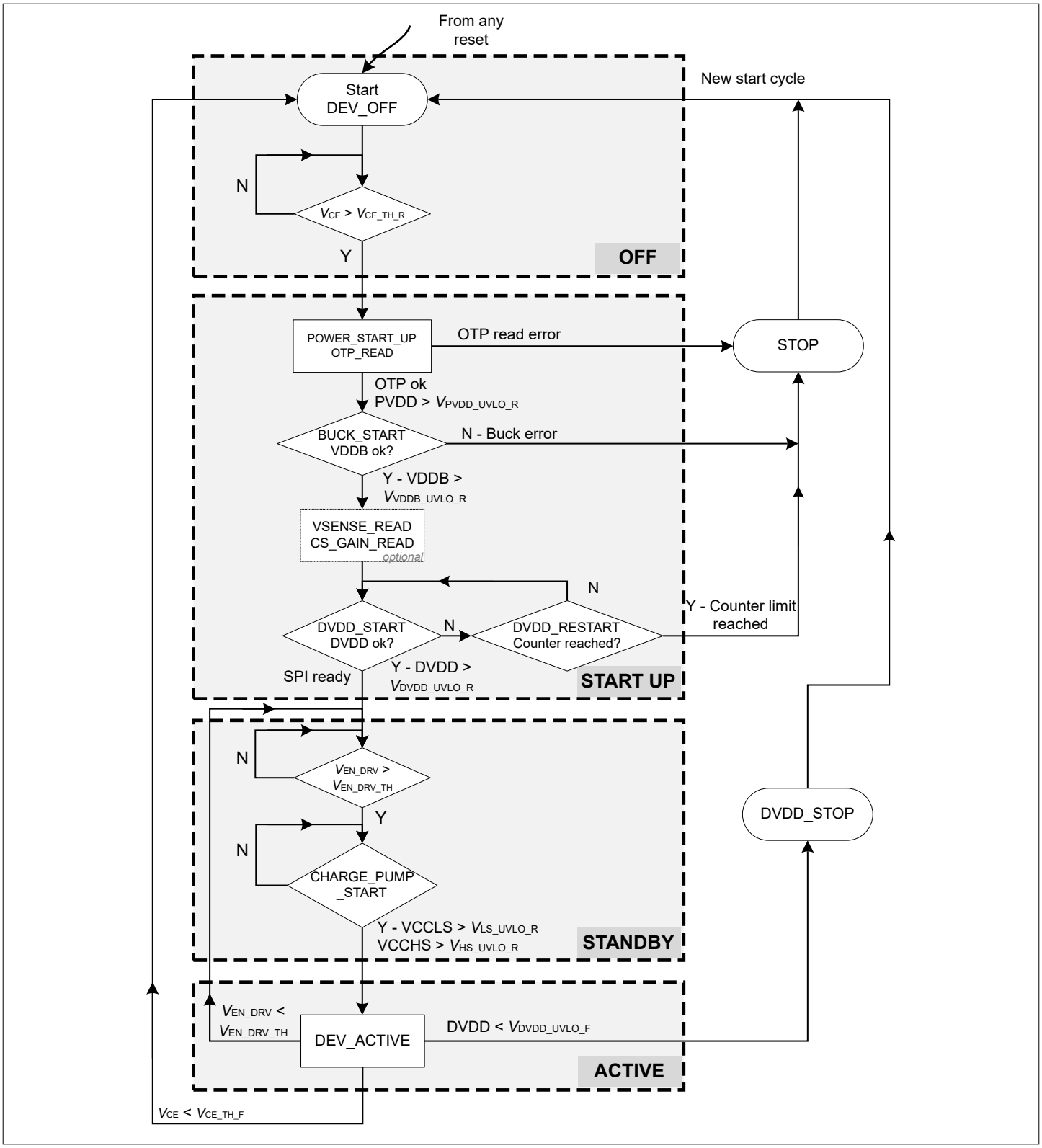

Figure 47 Flowchart diagram for functional states of device

Four main modes can be considered for 6EDL7151: OFF_STATE, START_UP, STANDBY and ACTIVE. States are described as follows:

- **DEV_OFF** - This state is the default state when device in reset.

- **POWER_START_UP**, **OTP_READ** - In this state voltage in PVDD is ramping up and checked by the device. Once ok, the OTP memory is read. This is done before enabling any further blocks to ensure configuration is known. If a fault is signaled by the OTP block, then the STOP state will be entered.
- **BUCK_START** - The buck converter is enabled in this state and the VDDB needs to be correct before leaving this state. If the VDDB has not reached the target voltage in a certain time, then the buck will be shut down and the device set in the STOP state.
- **VSENSE_READ**, **CS_GAIN_READ** - The device will optionally (programmable) sense pins like VSENSE and CS_GAIN for checking parameters to be programmed. If the bitfield CS_GAIN_ANA is set to b0, then the current sense amplifier gain will be set by the register CS_GAIN. Otherwise, if CS_GAIN_ANA is set to b1, the analog programming is enabled.
- **DVDD_START** - At this point, once the buck converter output is stable, the linear voltage regulator for DVDD is ramped up according the start-up delay and soft start programming. At the end of this state, DVDD is at target voltage and stable. With this, the start-up procedure of the device finishes and enters a wait state until EN_DRV signal arrives from a microcontroller for example. This will start the standby section.
- **CHARGE_PUMP_START** - The charge pumps are enabled. If target voltages are reached, the device moves to DEV_ACTIVE.
- **DEV_ACTIVE** (or ACTIVE state) - In this state the driver is ready to be used. The PWM path is enabled. If EN_DRV signal goes low during active the device turns off both charge pumps and disables the PWM path by going into the STANDBY section.
- **DVDD_STOP** - This state is entered from states after DVDD has been powered and DVDD rail fails. Device stops operation and requires a CE toggle or power cycle to restart. Buck converter and ADC remains active.
- **STOP** - If this state is entered it is because a serious fault with either the buck converter DVDD start-up. The device will not operate until a power cycle or EN_DRV toggle takes place. SPI cannot be used during this state.

3.14 Protections and faults handling

The 6EDL7151 contains an extensive number of protections. These are:

- Overcurrent protections (OCP) for:
  - DVDD linear regulator
  - Buck converter
  - Motor leg shunt OCP
- Undervoltage lockout (UVLO) protection for:
  - Gate driver supply voltages for both high-side and low-side drivers
  - Supply voltage PVDD
  - DVDD linear regulator output voltage
  - Buck converter output voltage
- DVDD linear regulator overvoltage lockout (OVLO) protections
- VDS sensors and OFF state diagnostics
- Rotor locked detection based on Hall sensor inputs
- Configurable watchdog
- Overtemperature shutdown (OTS) and overtemperature warning (OTW)
- Overtemperature shutdown for buck converter and LDO
- OTP memory fault

An arbitration state machine takes all the fault inputs from the specific fault blocks and decides which fault needs to be serviced first in case several faults occur at the same time (the same clock cycle). Once a fault is acknowledged, the system takes the specific action as shown in Table 12 and the arbitration round stops until the fault is cleared. The state machine is split in two main independent arbitration sections:

- **Supply faults** (B0 to B4). B0 is the highest priority.
- **Other faults** (F0 to F7). The fault that happens first is dealt first and others are ignored until this fault is removed. If more than one fault happens at the same time, then the one with the highest priority is processed. F0 is the highest priority.

The resultant actions from both sections are OR'ed on the nFAULT pin. If the fault is not latched, the fault status is held but the actions stops when the condition for the fault is released. Additionally to any possible actions like switching off PWM signal, status bits are updated to inform the MCU of any warning or/and fault occurrence. This is done regardless of priority and those status bits can be read via SPI commands by the microcontroller in the system.

***Note**: It is highly recommended to determine the source of the fault by reading the status registers and clear faults as soon as they occur so that new fault events can be captured. A fault is cleared by writing the register FAULTS_CLR via the SPI interface.*

The following registers provide information on the status of the device faults:

- **FAULT_ST**: Holds most of functional related faults. A fault might be triggered only after a number of events of a malfunction. Status immediately records the event information.
- **TEMP_ST**: Provides status on temperature warning and the temperature reading itself.
- **SUPPLY_ST**: Reports on status of all supplies UVLO/OVLO and OCPs.
- **FUNCT_ST**: Status of the gain of current sense amplifiers, Hall sensors, wrong hall pattern, and VDS sensors status.
- **OTP_ST**: Programming and reading of OTP related faults.

To clear faults, the user has to write the bitfield CLR_FLTS in the FAULTS_CLR register via SPI. However, to clear a latched fault, a write to the CLR_LATCH bitfield is required.

If ‘Motor leg shunt OCP’ fault is programmed to be latched, then the fault cannot be cleared until:

- If in OCP counting mode (8, 16 periods) there is one whole PWM period without an OCP event or standby state is entered.
- If in immediate trigger mode then it can be cleared after the fault is gone.

Table 12 Faults and protections table - lower Prio number means higher priority

Name	Description	Program mability	Latched	nFAULT report	Active state	Prio	Action(s)
VCCLS UVLO	Charge pump low-side UVLO fault	–	N	Y	DEV_ACTIVE	F1&2 (shared)	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76
VCCHS UVLO	Charge pump high-side UVLO fault	–	N	Y	DEV_ACTIVE	F1&2 (shared)	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76
DVDD OVLO	DVDD OVLO fault	–	N	Y	STANDBY and DEV_ACTIVE	B1	No action. MCU to perform action
DVDD OCP	DVDD OCP fault	Threshold level	N	Y	STANDBY and DEV_ACTIVE	B3	No action. MCU to perform action

(table continues...)

Table 12 (continued) Faults and protections table - lower Prio number means higher priority

Name	Description	Programmability	Latched	nFAULT report	Active state	Prio	Action(s)
DVDD UVLO	DVDD UVLO fault	–	N(requires power cycle - CE toggle)	Y (however nFAULT is supplied by DVDD)	All states after BUCK_START	B0 and F0	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. Note: the behavior can be interrupted depending on DVDD as logic is supplied by it. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76. These are always active. Waits for power cycle (CE pin low and high). Buck converter continues operation. When DVDD UVLO happens the functional state machine changes from DEV_ACTIVE to DVDD_STOP. Refer to Chapter 3.13 for details. From the application perspective, this fault is the highest priority. Requires a power cycle (CE toggle)
BUCK OCP	Buck converter overcurrent protection	–	N	Y	All states after DVDD ok (after Standby) - fault blanked during charge pump start	B2	No action. MCU to perform action. Protection is blanked during start-up of charge pumps
Motor leg shunt OCP [2:0]	Current sense amplifier overcurrent protection for each phase	Threshold level, count on number of trips, reaction, PWM truncation	Programmable - latched if brake on OCP is active	Y	DEV_ACTIVE	F4	PWM truncation if configured. If fault is configured as “Latched” then: gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76. Brake as defined in PWM_CFG register when CS_OCP_BRAKE register enabled. Fault latched if braking active

(table continues...)

Table 12 (continued) Faults and protections table - lower Prio number means higher priority

Name	Description	Programmability	Latched	nFAULT report	Active state	Prio	Action(s)
VDS Sensor	VDS sensor comparator protection	Threshold, blanking, deglitch filter	Y	Y	DEV_ACTIVE	F5	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76
Locked rotor	Locked rotor watchdog overflow	Timing	Y	Y, Programmable	DEV_ACTIVE	F6	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76. Requires toggle of EN_DRV to re-start normal operation again
Watchdog timers	Watchdog timer overflow. Several inputs programmable	Timing, reaction. Depending on input	Programmable - latched if brake on watchdog fault is enabled	Y (with input EN_DRV only, otherwise not)	Depending on input, either START UP or DEV_ACTIVE	F7	If input: · EN_DRV: gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76. · Buck input: no action required from user or device. · Charge pump input: nFAULT reported. Driver won't start-up. · Others: brake as defined in PWM_CFG register when WD_BRAKE register enabled. Always latched if braked enabled
OTS	Overtemperature shutdown	–	Y	Y	DEV_ACTIVE	F3	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76
OTW	Overtemperature warning	–	N	N (only status register report)	DEV_ACTIVE	F9	No action. MCU to perform action

(table continues...)

Table 12 (continued) Faults and protections table - lower Prio number means higher priority

Name	Description	Program mability	Latched	nFAULT report	Active state	Prio	Action(s)
OTP Fault	OTP read fault or OTP user programming error	–	Y	Y	All states	F8	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 76

3.15 Device programming - OTP and SPI interface

The 6EDL7151 includes some smart features that can be programmed by the user. The configuration of those features, including the gain of amplifiers, driving voltage for gate drivers or fault reactions, is stored in registers while the device is active. The configuration of those functions can be changed during run time operation via SPI commands. These registers are volatile memory cells and therefore, its information is lost every time the power supply is removed from the device.

For this reason, the 6EDL7151 integrates an OTP NVM (One time programmable non-volatile memory) that stores a given default configuration even when power supply is not available. Initially, the device is programmed with the default register settings provided in Chapter 3.16. During start-up phase of the device (see state machine flowchart in Figure 47), the configuration in the OTP is copied or mirrored into the volatile registers. These registers are the ones that govern the actual behavior of the device. This is shown in Figure 48.

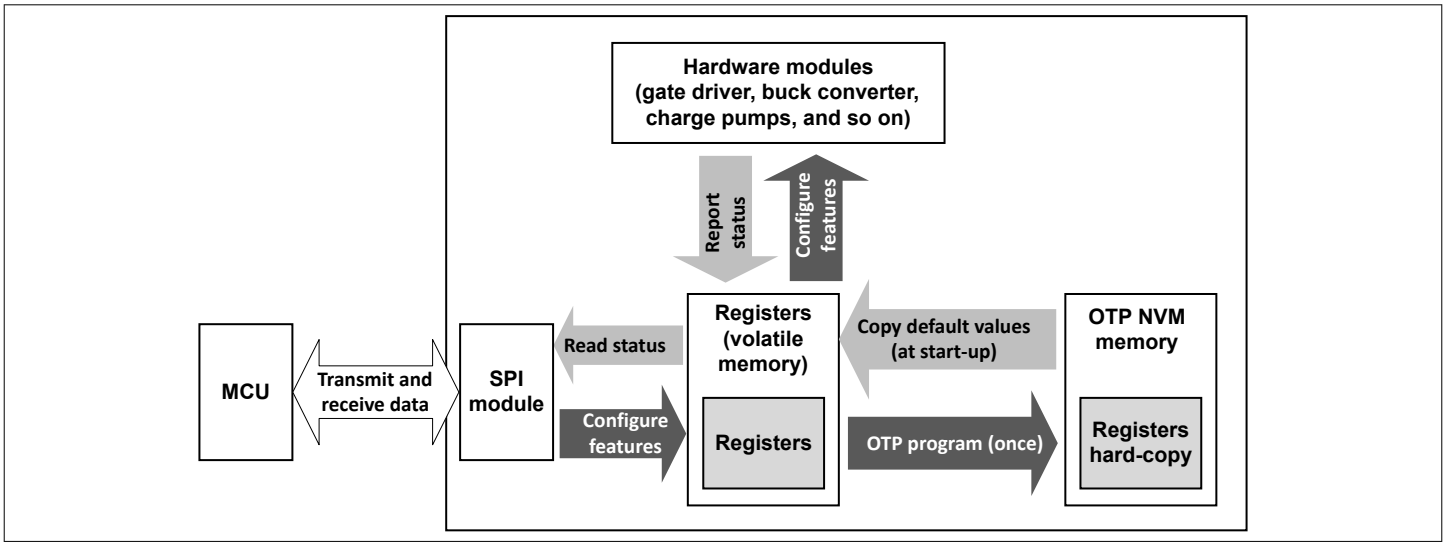

Figure 48 Programming overview

In case the default (“out of the fab”) configuration of the device stored in the OTP not being the desired one, the designer can select a different configuration for his application and store it indefinitely in the OTP memory (hard-copy). See Chapter 3.15.1 for the detailed programming procedure. This action can be done only once. A second write to the OTP is not possible. However, configurations can be overwritten on volatile registers after start-up via SPI commands as mentioned above.

The user configuration can be tracked with a software ID bitfield USER_ID, which is located in the OTP_PROG register.

***Note**: It is recommended that every writing action to the registers in 6EDL7151 is followed by a confirmation read to ensure that written and read data in registers match and thus confirming correct programming.*

3.15.1 OTP user programming procedure: loading custom default values

The 6EDL7151 OTP is used for user configuration storage. The OTP module implements a double error correction, plus one additional error detection when programming it.

OTP programming must only occur in a controlled environment. This requires that the user ensures that programming happens at the correct supply voltage, this is PVDD > $PVDD_{OTP\_PROG}$. Also the temperature must be below T_{OTP_PROG}. Internally both parameters are monitored. This means that if programming is attempted outside of these parameters it will be blocked. If this occurs, then the bitfield OTP_PROG_BLOCK is set to b1 to indicate that one of the parameter is outside of the required range. Default values (as given in bold in Chapter 3.16.2) are used after start-up in such situation. Further programming attempts are possible. OTP_PROG_BLOCK is reset either when the programming finishes successfully or after a power down.

The following programming steps should be performed to write OTP with a specific configuration:

1. Start device into standby mode ($V_{EN\_DRV} < V_{EN\_DRV\_TH}$).
2. Write registers to the desired default values via the SPI write commands.
3. Program these values into OTP using the OTP_PROG bitfield.
   - If the temperature is higher than T_{OTP_PROG} or PVDD < $PVDD_{OTP\_PROG}$, then programming does not start and OTP_PROG_BLOCK is set to b1. Conditions might be modified and the programming can be attempted again. If the programming fails twice, the device is blocked signaled by OTP_USED = b1 and OTP_PASS = b0.
   - If temperature and PVDD values are in range, programming starts, copying register parameters into the OTP memory. This can only be done once.
4. (Recommended) Check if OTP programming succeeded via the bitfields OTP_USED and OTP_PASS or OTP_PROG_FAIL:
   - If the programming of the OTP failed, then the device is locked until a power cycle (CE pin pulled down and up) takes place. Signaled by OTP_USED = b1 and OTP_PASS = b0 or simply OTP_PROG_FAIL = b1. Further programming of OTP is not possible. Memory content is considered corrupted and therefore the part should be discarded.
   - If programming succeeded, then normal function continues. This is signaled by OTP_USED = b1 and OTP_PASS = b1 or simply OTP_PROG_FAIL = b0. It is recommended to perform a power cycle (CE pin pulled down and up) for new values to take effect after a successful programming.

Attempts to write an already programmed OTP are ignored. The OTP status is summarized in Table 13.

Table 13 OTP programming status

Device status	OTP_USED	OTP_PASS	OTP_PROG_BLOCK	OTP_PROG_FAIL	Status description
Non-programmed device	0	0	0	0	Default values used
Successful programming of OTP	1	1	X	X	User programming was successful. Upon start-up, the newly programmed default values are loaded into registers for custom configuration
Programming blocked due to PVDD or temperature conditions	0	0	1	0	Part can be reprogrammed once condition are within limits

(table continues...)

Table 13 (continued) OTP programming status

Device status	OTP_USED	OTP_PASS	OTP_PROG_BLOCK	OTP_PROG_FAIL	Status description
Programming started but failed during operation due to PVDD or temperature conditions	1	0	1	1	Part must be discarded
Programming started but failed due to OTP issue	1	0	0	1	Part must be discarded

An OTP programming failure (wrong copy of registers into OTP memory) forces the device to enter STOP state during read out (see Figure 47). In such case, the fault is reported on the nFAULT pin. The microcontroller, once informed about the fault, can request 6EDL7151 to provide status of memory by reading the bitfields OTP_USED, OTP_PASS, or OTP_PROG_FAIL, and OTP_PROG_BLOCK.

If a user chooses to program OTP during start-up of the microcontroller software, this should check each time that OTP_USED = b1 before programming again. Otherwise incorrect programming could occur.

3.15.2 SPI communication

All communication between 6EDL7151 and an external microcontroller happens through an integrated SPI interface. This module is used to program the configuration registers and therefore to command the device, for example, to change settings or program OTP memory.

The SPI module is based on a 4-pin configuration. Data sampling happens during the falling edge of the SPI clock signal. All communication happens in a 24-bit length shift register.

- 7-bit address
- 16-bit data byte
- 1-bit command

Two commands are defined:

- 1 - Register write
- 0 - Register read

Data is shifted in with MSB first. Figure 49 and Figure 50 show the write and read operations with SPI interface respectively.

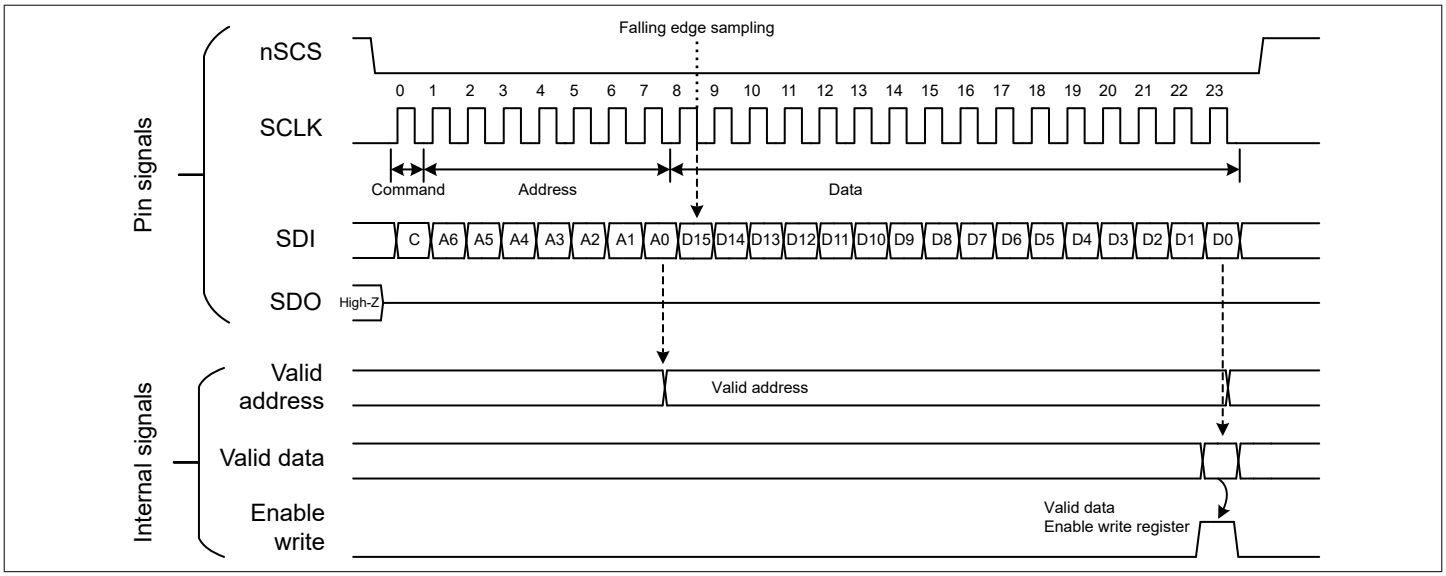

Figure 49 SPI write operation

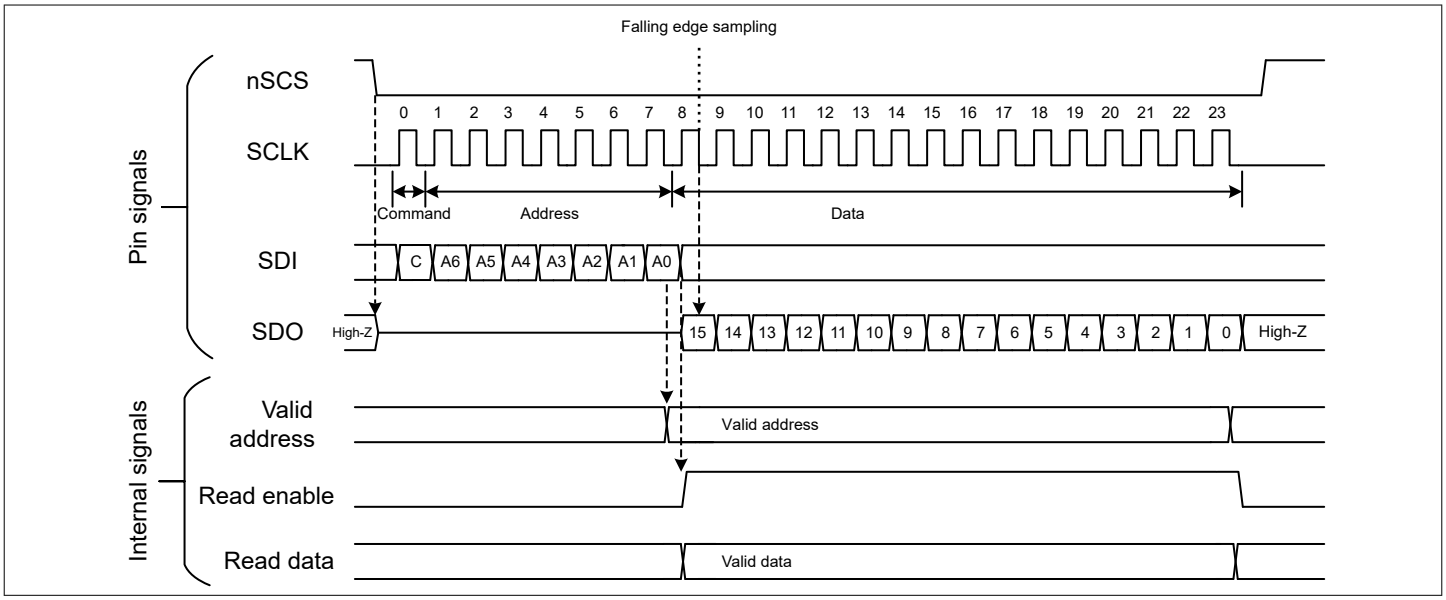

Figure 50 SPI read operation

3.15.2.1 SPI communication example

For example, the user wants to write new values TDRIVE1 = 50 ns (0x01) and TDRIVE2 = 2540 ns (0xFE) to the register TDRIVE_SRC_CFG (address 0x19), then the content of the register needs to be 0xFE01 by collating TDRIVE2 and TDRIVE1 values. So the MCU needs to write the following command in the SPI bus (SDI signal) once nSCS signal is pulled down:

Binary: b 1001 1001 1111 1110 0000 0001

Hexadecimal: 0x99 FE 01

After write, if a read is necessary, then the following sequence must be applied by the MCU. This reads the TDRIVE_SRC_CFG register by writing SDI signal:

Binary: b 0001 1001 ---- ---- ---- ----

Hexadecimal: 0x19 -- --

3.16 Register map

Table 14 shows a complete list of registers in 6EDL7151 accessible via SPI interface.

Table 14 Register map overview

Register name	Short description	Offset address
FAULT_ST	Faults status	00_H
TEMP_ST	Temperature status	01_H
SUPPLY_ST	Power supply status	02_H
FUNCT_ST	Functional status	03_H
OTP_ST	OTP status	04_H
ADC_ST	ADC status	05_H
CP_ST	Charge pump status	06_H
DEVICE_ID	Device ID	07_H
VDS_SENSE_CFG	VDS sensors configuration	$0F_H$
FAULTS_CLR	Faults clear	10_H
SUPPLY_CFG	Power supply configuration	11_H
ADC_CFG	ADC configuration	12_H
PWM_CFG	PWM configuration	13_H
SENSOR_CFG	Sensor configuration	14_H
WD_CFG	Watchdog configuration	15_H
WD_CFG2	Watchdog configuration 2	16_H
IDRIVE_CFG	Gate driver current configuration	17_H
IDRIVE_PRE_CFG	Gate driver precharge current configuration	18_H
TDRIVE_SRC_CFG	TDRIVE source configuration	19_H
TDRIVE_SINK_CFG	TDRIVE sink configuration	$1A_H$
DT_CFG	Dead time configuration	$1B_H$
CP_CFG	Charge pump configuration	$1C_H$
CSAMP_CFG	Current sense amplifier configuration	$1D_H$
CSAMP_CFG2	Current sense amplifier configuration 2	$1E_H$
OTP_PROG	OTP program	$1F_H$

3.16.1 Device programmability

The 6EDL7151 programmable registers can be programmed at any time after the SPI interface is active, however, some of the bitfield changes do not have an effect until certain conditions occur. This is to protect from wrong behaviors or to avoid glitches in the operation. Three categories are defined:

1. **Always** programmable: Programming these bitfields have an effect immediately after programming in any state of the device. The effect can be synchronized with PWM or braking events for some cases.

2. **Standby** programmable: Programming these bitfields have an effect only when the EN_DRV level is low. If programmed when EN_DRV is high, the register shows the new value, but effect does not be applied until EN_DRV is

pulled down. This is to prevent system malfunctions. It is therefore recommended that these registers are programmed before EN_DRV is enabled.

3. **OTP only**: Programming these bitfields have an effect only if programmed in OTP and after device new power up (PVDD). These are settings affecting the start-up of the device, namely bitfields whose effect takes place even before DVDD ramps up, therefore must be burned into OTP to be effective on next power up. As an example, if during ACTIVE state a write happens to a 'Standby' value, the value are written and reads to this register returns the written value, however, the value is not (shadow) transferred to actual effective register until the device state machine goes into the STANDBY state.

Table 15 provides a categorization for every configuration ('rw' or 'w' type bitfield) of the device.

Table 15 Register programmability

Register name	Bitfield name	Programmability
VDS_SENSE_CFG	VDS_HS_TH	Always
	VDS_LS_TH	Always
	VDS_BLANK	Always
	VDS_FILTER	Always
	VDS_FLT_CFG	Always
	VDS_SENSE_EN	Always
SUPPLY_CFG	PVCC_SETPT	Standby
	CS_REF_CFG	Standby
	DVDD_OCP_CFG	Always
	DVDD_SFTSTRT	OTP only
	DVDD_SETPT	OTP only
	BK_FREQ	Standby
	DVDD_TON_DELAY	OTP only
	CP_PRECHARGE_EN	Standby
ADC_CFG	ADC_OD_REQ	Always – no OTP field, just register
	ADC_OD_INSEL	Always – no OTP field, just register
	ADC_EN_FILT	Always – no OTP field, just register
	ADC_FILT_CFG	Always
	ADC_FILT_CFG_PVDD	Always
PWM_CFG	PWM_MODE	Standby
	PWM_FREEW_CFG	Always
	BRAKE_CFG	Always
	PWM_RECIRC	Standby
SENSOR_CFG	HALL_DEGLITCH	Always
	OTS_DIS	Always
	CS_TMODE	Always
	VDS_OFF_DIAG_EN	Standby

(table continues...)

Table 15 (continued) Register programmability

Register name	Bitfield name	Programmability
WD_CFG	WD_EN	Standby
	WD_INSEL	Standby
	WD_FLTCFG	Standby
	WD_TIMER_T	Standby
WD_CFG2	WD_BRAKE	Standby
	WD_EN_LATCH	Standby
	WD_DVDD_RSTRT_ATT	Standby
	WD_DVDD_RSTRT_DLY	Standby
	WD_RLOCK_EN	Always
	WD_RLOCK_T	Always
	WD_BK_DIS	OTP only
IDRIVE_CFG	IHS_SRC	Always
	IHS_SINK	Always
	ILS_SRC	Always
	ILS_SINK	Always
IDRIVE_PRE_CFG	I_PRE_SRC	Always
	I_PRE_SINK	Always
	I_PRE_SRC_DIS	Always
	I_PRE_SNK_DIS	Always
	I_CLAMP_DIS	Always
TDRIVE_SRC_CFG	TDRIVE1	Always
	TDRIVE2	Always
TDRIVE_SINK_CFG	TDRIVE3	Always
	TDRIVE4	Always
DT_CFG	DT_RISE	Always
	DT_FALL	Always
CP_CFG	CP_CLK_ CFG	Always
	CP_CLK_ SS_DIS	Always
CSAMP_CFG	CS_GAIN	Always – recommended to stop PWM first
	CS_GAIN_ANA	Standby (change to digital mode)- change to analog mode only possible if written in OTP followed by power cycle
	CS_EN	Always
	CS_BLANK	Always – recommended to stop PWM first

(table continues...)

Table 15 (continued) Register programmability

Register name	Bitfield name	Programmability
	CS_EN_DCCAL	Standby
	CS_OCP_DEGLITCH	Standby
	CS_OCPFLT_CFG	Standby
CSAMP_CFG2	CS_OCP_PTHR	Always
	CS_OCP_NTHR	Always
	CS_OCP_LATCH	Standby
	CS_MODE	Standby
	CS_OCP_BRAKE	Standby
	CS_TRUNC_DIS	Always
	CS_NEG_OCP_DIS	Always
	CS_AZ_CFG	Always
OTP_PROG	OTP_PROG	Standby (programming of OTP only in Standby)
	USER_ID	Always

Table 16 Register read/write coding description

Code	Access type	Description
RES	No access	Reserved
r	Read	Read only. A write produces no action
rh	Read Hardware	Read only, the bitfield is modified by hardware (typical example: status bitfields)
rw	Read/Write	Read or write by user
w	Write	Write only. A read returns 0

***Note**: Default values of the register bitfields are in bold.*

3.16.2 Register map

3.16.2.1 Faults status register

If the status of one of the bits switches to value b1, the corresponding fault/warning has occurred. To clear the fault use the clear faults bit in FAULTS_CLR register

FAULT_ST Offset address: 00_H

Faults status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			OTP_FLT	WD_FLT	RLOCK_FLT	OTW_FLT	OTS_FLT	BK_OCP_FLT	DVDD_OV_FLT	DVDD_UV_FLT	DVDD_OCP_FLT	CP_FLT	CS_OCP_FLT		
r			rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh		

Field	Bits	Type	Description
CS_OCP_FLT	2:0	rh	**Current sense amplifier OCP fault status** Current sense amplifier OCP fault status bxx0: No fault on phase A bxx1: Fault on phase A bx0x: No fault on phase B bx1x: Fault on phase B b0xx: No fault on phase C b1xx: Fault on phase C
CP_FLT	3	rh	**Charge pumps fault status** Charge pump low-side and high-side combined fault status b0: No fault has occurred b1: A fault has occurred
DVDD_OCP_FLT	4	rh	**DVDD OCP (Over-Current Protection) fault status** DVDD linear voltage regulator Over-Current Protection fault status b0: No fault has occurred b1: A fault has occurred
DVDD_UV_FLT	5	rh	**DVDD UVLO (Under-Voltage Lock-Out) fault status** DVDD UVLO fault status b0: No fault has occurred b1: A fault has occurred
DVDD_OV_FLT	6	rh	**DVDD OVLO (Over-Voltage Lock-Out) fault status** DVDD OVLO fault status b0: No fault has occurred b1: A fault has occurred
BK_OCP_FLT	7	rh	**Buck OCP fault status** Buck Over-Current Protection fault status b0: No fault has occurred b1: A fault has occurred

(table continues...)

(continued)

Field	Bits	Type	Description
OTS_FLT	8	rh	**Overtemperature shutdown fault status** Overtemperature shutdown event status b0: No fault has occurred b1: A fault has occurred
OTW_FLT	9	rh	**Overtemperature warning status** Overtemperature warning signal status b0: No warning signal has occurred b1: A warning signal has occurred
RLOCK_FLT	10	rh	**Locked rotor fault status** Locked rotor fault status using Hall sensors b0: No fault has occurred b1: A fault has occurred
WD_FLT	11	rh	**Watchdog fault status** Watchdog status b0: No fault has occurred b1: A fault has occurred
OTP_FLT	12	rh	**OTP status** OTP (One Time Programmable) memory fault status b0: No fault has occurred b1: A fault has occurred
RES	15:13	r	**Reserved** A read always returns 0

3.16.2.2 Temperature status register

This register contains the temperature value for MCU to read

TEMP_ST Offset address: 01_H

Temperature status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES									**TEMP_VAL**						
r									rh						

Field	Bits	Type	Description
TEMP_VAL	6:0	rh	**Temperature reading** Temperature value in steps of 2 degrees Celsius b000000: -94 degrees Celsius ….. every 2 degrees Celsius b1111111: 160 degrees Celsius
RES	15:7	r	**Reserved** A read always returns 0

3.16.2.3 Power supply status register

This register contains the status of the power supply related blocks

SUPPLY_ST Offset address: 02_H

Power supply status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			**PVDD_VAL**							**VDDB_OVST**	**VDDB_UVST**	**DVDD_OVST**	**DVDD_UVST**	**VCCHS_UVST**	**VCCLS_UVST**
r			rh							rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
VCCLS_UVST	0	rh	**Charge pump low-side UVLO status** b0: Below threshold b1: Above threshold
VCCHS_UVST	1	rh	**Charge pump high-side UVLO status** b0: Below threshold b1: Above threshold
DVDD_UVST	2	rh	**DVDD UVLO status** b0: Below threshold b1: Above threshold
DVDD_OVST	3	rh	**DVDD OVLO (Over-Voltage Lock-Out) status** b0: Below threshold b1: Above threshold
VDDB_UVST	4	rh	**VDDB UVLO status** b0: Below threshold b1: Above threshold
VDDB_OVST	5	rh	**VDDB OVLO status** b0: Below threshold b1: Above threshold
PVDD_VAL	12:6	rh	**PVDD ADC result reading value** Holds the analog to digital conversions value for PVDD input voltage
RES	15:13	r	**Reserved** A read always returns 0

3.16.2.4 Functional status register

Status of various functional signals

FUNCT_ST Offset address: 03_H

Functional status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		VDS_LSC_ST	VDS_HSC_ST	VDS_LSB_ST	VDS_HSB_ST	VDS_LSA_ST	VDS_HSA_ST	CS_GAIN_ST			DVDD_ST	HALLPOL_ST	HALLIN_ST		
r		rh	rh	rh	rh	rh	rh	rh			rh	rh	rh		

Field	Bits	Type	Description
HALLIN_ST	2:0	rh	**Hall sensor inputs status** Hall sensor input status for each phase b0: signal is low b1: signal is high bit 0: Phase A bit 1: Phase B bit 2: Phase C
HALLPOL_ST	3	rh	**Hall sensor polarity equal indicator** Status bit that indicate if all phases of the Hall sensors have the same polarity at the same time b0: Hall sensors have different polarity b1: Hall sensors have the same polarity
DVDD_ST	4	rh	**DVDD set point status** DVDD set point read value. The reading is independent of whether DVDD is analog or digitally programmed b0: 3.3 V b1: 5 V
CS_GAIN_ST	7:5	rh	**Status of the current sense amplifier gain** Shows the value of the current sense amplifier gain independently of whether programmed digitally or via external resistor b000: 4 V/V b001: 8 V/V b010: 12 V/V b011: 16 V/V b100: 20 V/V b101: 24 V/V b110: 32 V/V b111: 64 V/V
VDS_HSA_ST	8	rh	**VDS high-side A sensor status** Indicates the comparator status for high-side phase A b0: No fault has occurred b1: A fault has occurred

(table continues...)

(continued)

Field	Bits	Type	Description
VDS_LSA_ST	9	rh	**VDS low-side A sensor status** Indicates the comparator status for low-side phase A b0: No fault has occurred b1: A fault has occurred
VDS_HSB_ST	10	rh	**VDS high-side B sensor status** Indicates the comparator status for high-side phase B b0: No fault has occurred b1: A fault has occurred
VDS_LSB_ST	11	rh	**VDS low-side B sensor status** Indicates the comparator status for low-side phase B b0: No fault has occurred b1: A fault has occurred
VDS_HSC_ST	12	rh	**VDS high-side C sensor status** Indicates the comparator status for high-side phase C b0: No fault has occurred b1: A fault has occurred
VDS_LSC_ST	13	rh	**VDS low-side C sensor status** Indicates the comparator status for low-side phase C b0: No fault has occurred b1: A fault has occurred
RES	15:14	r	**Reserved** A read always returns 0

3.16.2.5 OTP status register

OTP memory status information is found in this register

OTP_ST Offset address: 04_H

OTP status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES												OTP_PROG_FAIL	OTP_PROG_BLOCK	OTP_PASS	OTP_USED
r												rh	rh	rh	rh

Field	Bits	Type	Description
OTP_USED	0	rh	**OTP used** Shows if OTP memory has been written by user or still holds factory defaults b0: OTP memory is not used: factory defaults b1: OTP memory is used: new custom values loaded
OTP_PASS	1	rh	**User OTP programming passed** Is set if USER OTP programming has passed without error b0: Not programmed or not passed b1: Programming passed without error
OTP_PROG_BLOCK	2	rh	**User OTP programming blocked** Signals if OTP programming has been attempted when voltage or temperature outside range b0: Programming was not blocked b1: Programming blocked
OTP_PROG_FAIL	3	rh	**OTP programming fail** If set, indicates that the programming of the OTP has failed b0: No failure b1: Programming failed
RES	15:4	r	**Reserved** A read always returns 0

3.16.2.6 ADC status register

ADC status register

ADC_ST Offset address: 05_H

ADC status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								**ADC_OD_VAL**							**ADC_OD_RDY**
r								rh							rh

Field	Bits	Type	Description
ADC_OD_RDY	0	rh	**ADC on demand conversion result ready** Indicates if ADC result for one of the extended conversions is ready to be read b0: Not ready b1: Ready
ADC_OD_VAL	7:1	rh	**ADC on demand result value** ADC result value for on demand conversions
RES	15:8	r	**Reserved** A read always returns 0

3.16.2.7 Charge pump status register

Charge pumps status

CP_ST Offset address: 06_H

Charge pump status register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		**VCCLS_VAL**							**VCCHS_VAL**						
r		rh							rh						

Field	Bits	Type	Description
VCCHS_VAL	6:0	rh	**VCCHS ADC result reading value** Holds the analog to digital conversions value for VCCHS voltage
VCCLS_VAL	13:7	rh	**VCCLS ADC result reading value** Holds the analog to digital conversions value for VCCLS voltage
RES	15:14	r	**Reserved** A read always returns 0

3.16.2.8 Device ID register

Device ID

DEVICE_ID Offset address: 07_H

Device ID register AsyncReset value: 0011_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								**DEV_ID**							
r								rh							

Field	Bits	Type	Description
DEV_ID	7:0	rh	**Device ID** Device identifier for user version control
RES	15:8	r	**Reserved** A read always returns 0

3.16.2.9 VDS sensors configuration register

Configures the VDS sensor of the device

VDS_SENSE_CFG Offset address: $0F_H$

VDS sensors configuration register AsyncReset value: $3FFF_H$

15	14	13 12 11	10 9 8	7 6 5 4	3 2 1 0
VDS_SENSE_EN	VDS_FLT_CFG	VDS_FILTER	VDS_BLANK	VDS_LS_TH	VDS_HS_TH
rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
VDS_HS_TH	3:0	rw	**VDS high-side comparator threshold** Configures the threshold of the high-side comparators in the VDS sensor block b0000: 0.1 V b0001: 0.15 V b0010: 0.2 V b0011: 0.25 V b0100: 0.3 V b0101: 0.35 V b0110: 0.4 V b0111: 0.45 V b1000: 0.5 V b1001: 0.55 V b1010: 0.6 V b1011: 0.65 V b1100: 0.8 V b1101: 1.0 V b1110: 1.5 V **b1111: 2.0 V**

(table continues...)

(continued)

Field	Bits	Type	Description
VDS_LS_TH	7:4	rw	**VDS low-side comparator threshold** Configures the threshold of the low-side comparators in the VDS sensor block b0000: 0.1 V b0001: 0.15 V b0010: 0.2 V b0011: 0.25 V b0100: 0.3 V b0101: 0.35 V b0110: 0.4 V b0111: 0.45 V b1000: 0.5 V b1001: 0.55 V b1010: 0.6 V b1011: 0.65 V b1100: 0.8 V b1101: 1.0 V b1110: 1.5 V **b1111: 2.0 V**
VDS_BLANK	10:8	rw	**VDS sensor blanking time** Configures the VDS sensor blanking period during switching transitions b000: 1.0 us b001: 1.5 us b010: 2.0 us b011: 2.5 us b100: 3.0 us b101: 3.5 us b110: 4.0 us **b111: 5.0 us**
VDS_FILTER	13:11	rw	**VDS sensor filter time** Configures the VDS sensor filter time b000: 1.0 us b001: 1.5 us b010: 2.0 us b011: 2.5 us b100: 3.0 us b101: 3.5 us b110: 4.0 us **b111: 5.0 us**
VDS_FLT_CFG	14	rw	**VDS sensor fault configuration** Defines the behavior of the device after a VDS fault has occurred **b0: Register reporting only** b1: Register reporting and nFAULT signal reporting

(table continues...)

(continued)

Field	Bits	Type	Description
VDS_SENSE_EN	15	rw	**VDS sensor enable** Setting this bitfield will enable the VDS sensor module **b0: VDS sensor disabled** b1: VDS sensor enabled

3.16.2.10 Faults clear register

Clear different faults of the device

FAULTS_CLR Offset address: 10_H

Faults clear register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES														CLR_LATCH	CLR_FLTS
r														w	w

Field	Bits	Type	Description
CLR_FLTS	0	w	**Clear all faults** Setting this bitfield will clear all faults of the device excluding latched faults. A reading always returns 0 b0: No action b1: Clear all fault status bits except latched ones
CLR_LATCH	1	w	**Clear all latched faults** Setting this bitfield will clear all (and only) latched faults in the device. A reading always returns 0 b0: No action b1: Clear latched fault status bits
RES	15:2	r	**Reserved** A read always returns 0

3.16.2.11 Power supply configuration register

This register contains bitfields to configure and control power supplies of the device

SUPPLY_CFG Offset address: 11_H

Power supply configuration register AsyncReset value: $F000_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP_PRECHARGE_EN	**DVDD_TON_DELAY**		**BK_FREQ**	**DVDD_SETPT**		**DVDD_SFTSTRT**				**DVDD_OCP_CFG**		**CS_REF_CFG**		**PVCC_SETPT**	
rw	rw		rw	rw		rw				rw		rw		rw	

Field	Bits	Type	Description
PVCC_SETPT	1:0	rw	**PVCC set point** Configures the target PVCC (gate driving voltage) voltage level **b00: 12 V** b01: 15 V b10: 10 V b11: 7 V
CS_REF_CFG	3:2	rw	**Current sense reference configuration** Selects the VREF voltage that is applied as offset in all three current sense amplifiers **b00: 1/2 DVDD** b01: 5/12 DVDD b10: 1/3 DVDD b11: 1/4 DVDD
DVDD_OCP_CFG	5:4	rw	**DVDD OCP threshold configuration** DVDD OCP threshold selection **b00: 450 mA** b01: 300 mA b10: 150 mA b11: 50 mA
DVDD_SFTSTRT	9:6	rw	**DVDD soft start configuration** DVDD linear regulator soft start programming 100 us, stepping 100 us up to 1.6 ms **b0000: 100 us** b0001: 200 us ..... 100 us steps ..... b1111: 1.6 ms

(table continues...)

(continued)

Field	Bits	Type	Description
DVDD_SETPT	11:10	rw	**DVDD set point configuration** Configures DVDD output voltage **b0x: use VSENSE pin for analog programming** b10: DVDD = 3.3 V - digitally programmed b11: DVDD = 5 V - digitally programmed
BK_FREQ	12	rw	**Buck converter switching frequency selection** Configures the switching frequency of the buck converter b0: Low frequency (500 kHz) **b1: High frequency (1 MHz)**
DVDD_TON_DELAY	14:13	rw	**DVDD turn on delay configuration** The device will wait for the configured time before turning on the DVDD starting counting from VDDB UVLO during start-up of the device b00: 200us b01: 400us b10: 600us **b11: 800 us**
CP_PRECHARGE_EN	15	rw	**Charge pump precharge configuration** Enables the precharge of the VCCLS charge pump during start-up b0: Precharge disabled **b1: Precharge enabled**

3.16.2.12 ADC configuration register

Note: The complete content of the register must be written at once (read-modify-write). Writing a single bitfield at a time will set all other bitfields to default.

Configuration of the ADC related functions

ADC_CFG Offset address: 12_H

ADC configuration register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								ADC_FILT_CFG_PVDD		ADC_FILT_CFG		ADC_EN_FILT	ADC_OD_INSEL		ADC_OD_REQ
r								rw		rw		w	rw		w

Field	Bits	Type	Description
ADC_OD_REQ	0	w	**ADC on demand conversion request** Setting this bitfield will inject an additional measurement in the standard sequence. This additional measurement is selected in ADC_IN_SEL bitfield. A read always returns 0 **b0: No action** b1: Request the conversion of the signal selected in ADC_IN_SEL
ADC_OD_INSEL	2:1	rw	**ADC input selection for on demand conversions** Configures the input to the ADC **b00: IDIGITAL: device digital area current consumption** b01: DVDD b10: VDDB b11: Reserved
ADC_EN_FILT	3	w	**Enable filtering for on demand ADC measurement** Enables the moving average filter for on demand ADC measurements. A read always returns 0 **b0: No action** b1: Enable filtering
ADC_FILT_CFG	5:4	rw	**ADC generic filtering configuration** Selects the moving average filter characteristic for ADC measurements except PVDD measurement **b00: 8 samples averaging filter** b01: 16 samples averaging filter b10: 32 samples averaging filter b11: 64 samples averaging filter
ADC_FILT_CFG_PVDD	7:6	rw	**PVDD ADC measurement result filtering configuration** Selects the moving average filter characteristic for PVDD measurement **b00: 32 samples** b01: 16 samples b10: 8 samples b11: 1 sample

(table continues...)

(continued)

Field	Bits	Type	Description
RES	15:8	r	**Reserved** A read always returns 0

3.16.2.13 PWM configuration register

PWM related configurations

PWM_CFG Offset address: 13_H

PWM configuration register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES									PWM_RECIRC	BRAKE_CFG		PWM_FREEW_CFG	PWM_MODE		
r									rw	rw		rw	rw		

Field	Bits	Type	Description
PWM_MODE	2:0	rw	**PWM commutation mode selection** PWM mode selection **b000: 6PWM mode** b001: 3PWM mode b010: 1PWM mode b011: 1PWM with Hall sensors b100: b111: Reserved
PWM_FREEW_CFG	3	rw	**PWM freewheeling configuration** Selects which rectification or freewheeling is desired (only for 1 PWM input modes) **b0: Active freewheeling** b1: Diode freewheeling
BRAKE_CFG	5:4	rw	**Brake configuration** Brake scheme configuration **b00: Low-side** b01: High-side b10: High-Z (non-power) b11: Brake toggle - alternates between low- and high-side braking on every braking event
PWM_RECIRC	6	rw	**PWM recirculation selection (for PWM_MODE = b011 only)** Setting this bitfield will activate the alternating recirculation feature of the 1PWM with Hall sensors and alternating recirculation PWM mode. For PWM_MODE = b011 only **b0: Disable alternating recirculation mode** b1: Enable alternating recirculation mode
RES	15:7	r	**Reserved** A read always returns 0

3.16.2.14 Sensor configuration register

Sensors configuration

SENSOR_CFG Offset address: 14_H

Sensor configuration register AsyncReset value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								VDS_OFF_DIAG_EN	CS_TMODE		OTS_DIS	HALL_DEGLITCH			
r								rw	rw		rw	rw			

Field	Bits	Type	Description
HALL_DEGLITCH	3:0	rw	**Hall sensor deglitch** Deglitch time configuration for Hall sensor inputs in steps of 640 ns b0000: 0 ns **b0001: 640 ns** ... in steps of 640 ns b1111: 9600 ns
OTS_DIS	4	rw	**Overtemperature shutdown disable** This bitfield allows to disable the shutdown feature due to overtemperature in the device **b0: Enable shutdown protection** b1: Disable shutdown protection
CS_TMODE	6:5	rw	**Current sense amplifier timing mode** Configures how the current sense amplifier operates regarding the timing related to the PWM signals **b00: Current sense amplifier outputs are active when GLx signal is high** b01: Current sense amplifier outputs are active when GHx signal is low b1x: Current sense amplifier outputs are always active
VDS_OFF_DIAG_EN	7	rw	**VDS OFF state diagnostics enable** Controls the activation of the OFF state diagnostics mode of the VDS sensor **b0: Disable OFF state diagnostics mode** b1: Enable OFF state diagnostics mode
RES	15:8	r	**Reserved** A read always returns 0

3.16.2.15 Watchdog configuration register

Watchdog configurations

WD_CFG Offset address: 15_H

Watchdog configuration register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	**WD_TIMER_T**										**WD_FLTCFG**	**WD_INSEL**			**WD_EN**
r	rw										rw	rw			rw

Field	Bits	Type	Description
WD_EN	0	rw	**Watchdog enable** Watchdog timer enable **b0: Watchdog timer is disabled** b1: Watchdog timer is enabled
WD_INSEL	3:1	rw	**Watchdog input selection** Selects the input to the watchdog timer **b000: EN_DRV pin (measure input signal frequency)** b001: Reserved b010: DVDD (linear regulator) b011: VCCLS and VCCHS (charge pumps) b100: Status register read b101: Reserved b110: Reserved b111: Reserved
WD_FLTCFG	4	rw	**Watchdog fault configuration** Controls the reaction to a watchdog fault event **b00: Report to status register only** b01: Report to status register and pull down the nFAULT pin
WD_TIMER_T	14:5	rw	**Watchdog timer period value** Configures the period of the watchdog timer. After this time is elapsed with no re-start of the timer by the watchdog input, a watchdog fault is triggered. In 100 us steps. Not applicable for VDDB (buck) and EN_DRV watchdog input **b0000000000: 100 us** b0000000001: 200 us ..... b1111111111: 102.4 ms
RES	15	r	**Reserved** A read always returns 0

3.16.2.16 Watchdog configuration register 2

Watchdog configurations register extension

WD_CFG2 Offset address: 16_H

Watchdog configuration register 2 AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			WD_BK_DIS	WD_RLOCK_T			WD_RLOCK_EN	WD_DVDD_RSTRT_DLY				WD_DVDD_RSTRT_ATT		WD_EN_LATCH	WD_BRAKE
r			rw	rw			rw	rw				rw		rw	rw

Field	Bits	Type	Description
WD_BRAKE	0	rw	**Brake on watchdog timer overflow** Provides the option to configure a braking event when the watchdog overflow occurs **b0: Normal reaction to fault** b1: Brake on watchdog fault (automatically latched). The braking mode is configured in PWM_CFG register. Status register is updated accordingly
WD_EN_LATCH	1	rw	**Enable latching of the watchdog fault** Enable latching of the watchdog fault **b0: Fault not latched** b1: Fault latched
WD_DVDD_RSTRT_ATT	3:2	rw	**Restart delay for DVDD** Number of restart attempts for DVDD WD **b00: 0 attempts** b01: 1 attempt b10: 2 attempts b11: 3 attempts
WD_DVDD_RSTRT_DLY	7:4	rw	**DVDD restart delay** Time after WD trigger signal until restart is attempted again for DVDD. In steps of 0.5 ms **b0000: 0.5 ms** b0001: 1 ms ..... b1110: 7.5 ms b1111: 8 ms
WD_RLOCK_EN	8	rw	**Enable rotor locked detection** Enable rotor lock dedicated watchdog timer input **b0: Disabled** b1: Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
WD_RLOCK_T	11:9	rw	**Rotor locked watchdog timeout** Watchdog timer period value (overflow value). In steps of 1 s **b000: 1 s** b001: 2 s ..... b111: 8 s
WD_BK_DIS	12	rw	**Buck watchdog disable** Buck watchdog (start-up) disable **b0: Buck watchdog enabled** b1: Buck watchdog disabled
RES	15:13	r	**Reserved** A read always returns 0

3.16.2.17 Gate driver current control register

Gate driver current settings for slew rate control

IDRIVE_CFG Offset address: 17_H

Gate driver current control register AsyncReset value: $BBBB_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ILS_SINK				**ILS_SRC**				**IHS_SINK**				**IHS_SRC**			
rw				rw				rw				rw			

Field	Bits	Type	Description
IHS_SRC	3:0	rw	**High-side source current** High-side gate driver rise or pull-up gate current applied during period TDRIVE2 b0000: 10 mA b0001: 20 mA b0010: 30 mA b0011: 40 mA b0100: 50 mA b0101: 60 mA b0110: 80 mA b0111: 100 mA b1000: 125 mA b1001: 150 mA b1010: 175 mA **b1011: 200 mA** b1100: 250 mA b1101: 300 mA b1110: 400 mA b1111: 500 mA
IHS_SINK	7:4	rw	**High-side sink current** High-side gate driver fall or pull-down gate current applied during period TDRIVE4 Same coding as IHS_SRC
ILS_SRC	11:8	rw	**Low-side source current** Low-side gate driver rise or pull-up gate current applied during period TDRIVE2 Same coding as IHS_SRC
ILS_SINK	15:12	rw	**Low-side sink current** Low-side gate driver fall or pull-down gate current applied during period TDRIVE4 ame coding as IHS_SRC

3.16.2.18 Gate driver precharge current control register

Gate driver precharge current settings for slew rate control

IDRIVE_PRE_CFG Offset address: 18_H

Gate driver precharge current control register AsyncReset value: $00BB_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES					I_CLAMP_DIS	I_PRE_SNK_DIS	I_PRE_SRC_DIS	I_PRE_SINK				I_PRE_SRC			
r					rw	rw	rw	rw				rw			

Field	Bits	Type	Description
I_PRE_SRC	3:0	rw	**Precharge source current setting (TDRIVE1)** Rise or pull-up gate current applied during precharge phase (TDRIVE1) b0000: 10 mA b0001: 20 mA b0010: 30 mA b0011: 40 mA b0100: 50 mA b0101: 60 mA b0110: 80 mA b0111: 100 mA b1000: 125 mA b1001: 150 mA b1010: 175 mA **b1011: 200 mA** b1100: 250 mA b1101: 300 mA b1110: 400 mA b1111: 500 mA
I_PRE_SINK	7:4	rw	**Precharge sink current setting (TDRIVE3)** Fall or pull-down current during precharge phase (TDRIVE3) Same coding as I_PRE_SRC
I_PRE_SRC_DIS	8	rw	**Gate driver precharge mode disable for sourcing** Enables extra precharge current configurations for source condition. In case of disabled, 1.5 A are applied during TDRIVE1 period **b0: Precharge sourcing current enabled. Value selected I_PRE_SRC is applied during TDRIVE1 period** b1: Precharge mode disabled. 1.5 A applied during TDRIVE1 period

(table continues...)

(continued)

Field	Bits	Type	Description
I_PRE_SNK_DIS	9	rw	**Gate driver precharge mode disable for sinking** Enables extra precharge current configurations for sinking condition. In case of disabled, 1.5 A are applied during TDRIVE3 period **b0: Precharge current enabled. Value selected in I_PRE_SINK is applied during TDRIVE3 period** b1: Precharge mode disabled. 1.5 A applied during TDRIVE3 period
I_CLAMP_DIS	10	rw	**Gate driver clamp function disable** Disables the gate clamp feature that applies maximum current setting during complementary switch turn on period (TDRIVE1 + TDRIVE2) **b0: Gate clamp feature enabled** b1: Gate clamp feature disabled
RES	15:11	r	**Reserved** A read always returns 0

3.16.2.19 TDRIVE source control register

TDRIVE1 and TDRIVE2 configuration registers for gate driver sourcing mode

TDRIVE_SRC_CFG Offset address: 19_H

TDRIVE source control register AsyncReset value: $FF00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDRIVE2								**TDRIVE1**							
rw								rw							

Field	Bits	Type	Description
TDRIVE1	7:0	rw	**TDRIVE1 timing** TDRIVE1 value for high- and low-side. First turn on or precharge period **b00000000: 0 ns** b00000001: 50 ns (values between 0 ns and 50 ns not allowed) 10 ns steps b11111111: 2590 ns
TDRIVE2	15:8	rw	**TDRIVE2 timing** TDRIVE2 value for high- and low-side b00000000: 0 ns b00000001: 10 ns 10 ns steps **b11111111: 2550 ns**

3.16.2.20 TDRIVE sink control register

TDRIVE3 and TDRIVE4 configuration registers for gate driver sinking mode

TDRIVE_SINK_CFG Offset address: $1A_H$

TDRIVE sink control register AsyncReset value: $FF00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDRIVE4								**TDRIVE3**							
rw								rw							

Field	Bits	Type	Description
TDRIVE3	7:0	rw	**TDRIVE3 timing** TDRIVE3 value for high- and low-side. First turn off or pre-discharge period **b00000000: 0 ns** b00000001: 50 ns (values between 0 ns and 50 ns not allowed) 10 ns steps b11111111: 2590 ns
TDRIVE4	15:8	rw	**TDRIVE4 timing** TDRIVE4 value for high- and low-side b00000000: 0 ns b00000001: 10 ns 10 ns steps **b11111111: 2550 ns**

3.16.2.21 Dead time register

Dead time configurations

DT_CFG Offset address: $1B_H$

Dead time register AsyncReset value: 3131_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DT_FALL								**DT_RISE**							
rw								rw							

Field	Bits	Type	Description
DT_RISE	7:0	rw	**Dead time rise (of phase node voltage)** Dead time rise (of phase node voltage) value b00000000: 120 ns b00000001: 200 ns In steps of 80 ns ... **b00110001: 4040 ns** ... b10010101: 12040 ns b10010110: b11111111: Unused (defaults to 120 ns)
DT_FALL	15:8	rw	**Dead time fall (of phase node voltage)** Dead time fall (of phase node voltage) value b00000000: 120 ns b00000001: 200 ns In steps of 80 ns ... **b00110001: 4040 ns** ... b10010101: 12040 ns b10010110: b11111111: Unused (defaults to 120 ns)

3.16.2.22 Charge pump configuration register

Charge pump related controls

CP_CFG Offset address: $1C_H$

Charge pump configuration register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES													CP_CLK_SS_DIS	CP_CLK_CFG	
r													rw	rw	

Field	Bits	Type	Description
CP_CLK_CFG	1:0	rw	**Charge pump clock frequency configuration** Charge pump clock frequency configuration **b00: 781.25 kHz** b01: 390.625 kHz b10: 195.3125 kHz b11: 1.5625 MHz
CP_CLK_SS_DIS	2	rw	**Charge pump clock spread spectrum disable** Charge pump clock spread spectrum disable **b0: Spread spectrum is enabled** b1: Spread spectrum disabled
RES	15:3	r	**Reserved** A read always returns 0

3.16.2.23 Current sense amplifier configuration register

Current sense amplifier configurations

CSAMP_CFG Offset address: $1D_H$

Current sense amplifier configuration register AsyncReset value: 2028_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS_OCPFLT_CFG		**CS_OCP_DEGLITCH**		**CS_EN_DCCAL**	**CS_BLANK**				**CS_EN**			**CS_GAIN_ANA**	**CS_GAIN**		
rw		rw		rw	rw				rw			rw	rw		

Field	Bits	Type	Description
CS_GAIN	2:0	rw	**Gain of current sense amplifiers** Selects the gain of the current sense amplifier when digitally programmed **b000: 4 V/V** b001: 8 V/V b010: 12 V/V b011: 16 V/V b100: 20 V/V b101: 24 V/V b110: 32 V/V b111: 64 V/V
CS_GAIN_ANA	3	rw	**Current sense amplifier gain analog programming enable** Current sense amplifier gain analog programming enable b0: Gain is selected via register configuration (CS_GAIN bitfield) **b1: Gain is defined by CS_GAIN pin resistor**
CS_EN	6:4	rw	**Enable of each current sense amplifier** Enable of each current sense amplifier bit 0: phase A **bit 1: phase B** bit 2: phase C b0: Amplifier disabled **b1: Amplifier enabled**

(table continues...)

(continued)

Field	Bits	Type	Description
CS_BLANK	10:7	rw	**Current sense amplifier blanking time** Current sense amplifier blanking time **b0000: 0 ns** b0001: 50 ns b0010: 100 ns b0011: 200 ns b0100: 300 ns b0101: 400 ns b0110: 500 ns b0111: 600 ns b1000: 700 ns b1001: 800 ns b1010: 900 ns b1011: 1 us b1100: 2 us b1101: 4 us b1110: 6 us b1111: 8 us
CS_EN_DCCAL	11	rw	**DC calibration of current sense amplifier** DC calibration of current sense amplifier **b0: No calibration is executed** b1: DC calibration mode executed, all power stages in high-Z (powered but not driving)
CS_OCP_DEGLITCH	13:12	rw	**Current sense amplifier OCP deglitch** OCP deglitch timing configuration of the OCP on current sense amplifiers - deglitch disabled if CS_TRUNC_DIS = b0 (PWM truncation disabled in register CSAMP_CFG2) b00: 0 us b01: 2 us **b10: 4 us** b11: 8 us
CS_OCPFLT_CFG	15:14	rw	**Current sense amplifier OCP fault trigger configuration** OCP fault trigger configuration **b00: Count 8 OCP events** b01: Count 16 OCP events b10: Trigger on all OCP events b11: No fault trigger (PWM truncation continues as defined in bitfield CS_TRUNC_DIS in register CSAMP_CFG2)

3.16.2.24 Current sense amplifier configuration register 2

Current sense amplifier configurations extension register

CSAMP_CFG2 Offset address: $1E_H$

Current sense amplifier configuration register 2 AsyncReset value: 0833_H

15 14	13	12	11	10	9	8	7 6 5 4	3 2 1 0
CS_AZ_CFG	**CS_NEG_OCP_DIS**	**RES**	**CS_TRUNC_DIS**	**CS_OCP_BRAKE**	**CS_MODE**	**CS_OCP_LATCH**	**CS_OCP_NTHR**	**CS_OCP_PTHR**
rw	rw	r	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CS_OCP_PTHR	3:0	rw	**Current sense amplifier OCP positive thresholds** Configures the threshold level for the positive OCP b0000: 300 mV b0001: 250 mV b0010: 225 mV **b0011: 200 mV** b0100: 175 mV b0101: 150 mV b0110: 125 mV b0111: 100 mV b1000: 90 mV b1001: 80 mV b1010: 70 mV b1011: 60 mV b1100: 50 mV b1101: 40 mV b1110: 30 mV b1111: 20 mV

(table continues...)

(continued)

Field	Bits	Type	Description
CS_OCP_NTHR	7:4	rw	**Current sense amplifier OCP negative thresholds** Configures the threshold level for the negative OCP b0000: -300 mA b0001: -250 mA b0010: -225 mA **b0011: -200 mV** b0100: -175 mA b0101: -150 mA b0110: -125 mA b0111: -100 mA b1000: -90 mA b1001: -80 mA b1010: -70 mA b1011: -60 mA b1100: -50 mA b1101: -40 mA b1110: -30 mA b1111: -20 mA
CS_OCP_LATCH	8	rw	**OCP latch choice** OCP fault can be selected with this bitfield to be a latched **b0: Unlatched** b1: Latched
CS_MODE	9	rw	**Current sense amplifier sensing mode** Select between shunt resistor and RDSON sensing modes **b0: Shunt resistor sensing** b1: RDSON sensing - CS_TMODE forced to be GL ON only
CS_OCP_BRAKE	10	rw	**Current sense amplifier brake on OCP configuration** Brake on OCP **b0: No braking upon OCP fault** b1: Brake on OCP fault (fault set to latched). The braking mode is configured in PWM_CFG register
CS_TRUNC_DIS	11	rw	**PWM truncation disable** Disables the PWM truncation when an OCP occurs. This does not affect fault triggering b0: PWM truncation enabled **b1: PWM truncation disabled**
RES	12	r	**Reserved** A read always returns 0

(table continues...)

(continued)

Field	Bits	Type	Description
CS_NEG_OCP_DIS	13	rw	**Current sense negative OCP disable** Disables the negative Over Current Protection in the current sense amplifiers including both the PWM truncation and fault reporting **b0: Negative OCP fault is enabled** b1: Negative OCP fault is disabled
CS_AZ_CFG	15:14	rw	**Current sense auto-zero configuration** Configures the auto-zero feature **b00: Auto-zero enabled with internal synchronization** b01: Auto-zero disabled b10: Auto-zero enabled with external synchronization b11: Auto-zero enabled with external synchronization and charge pump clock gating

3.16.2.25 OTP program register

OTP program command and user ID

OTP_PROG Offset address: $1F_H$

OTP program register AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES											USER_ID				OTP_PROG
r											rw				w

Field	Bits	Type	Description
OTP_PROG	0	w	**Program OTP** Setting this bitfield starts programming the OTP
USER_ID	4:1	rw	**User ID** Space for user to enter an ID into OTP for version control
RES	15:5	r	**Reserved** A read always returns 0

4 Electrical characteristics

All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters, and DGND for the rest) unless otherwise specified. The voltage levels are valid if other ratings are not violated. Figure 51 illustrates the definition for the voltage and current parameters used in this datasheet.

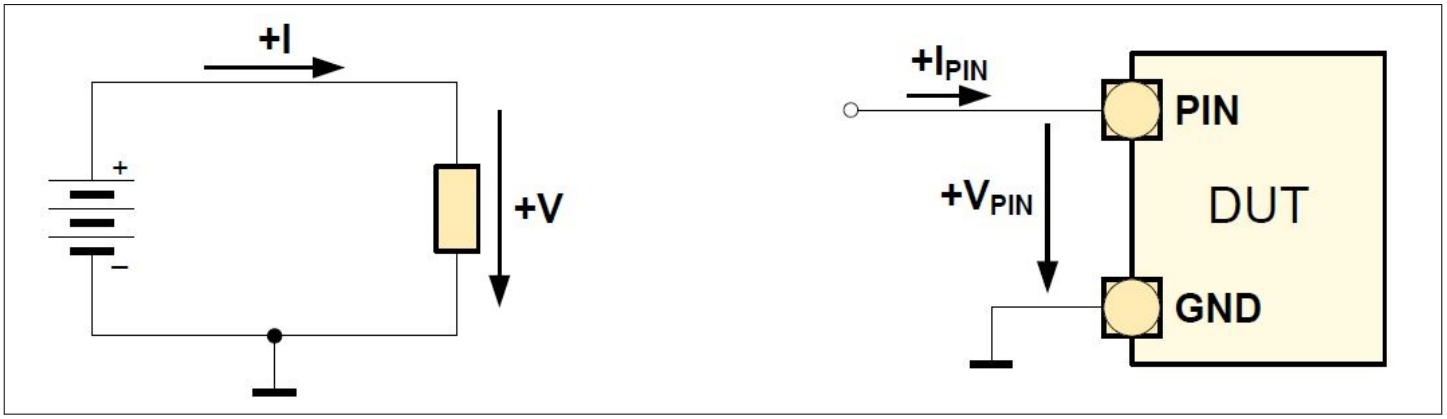

Figure 51 Voltage and current definitions

4.1 Absolute maximum ratings

***Note**: Absolute maximum ratings are intended in the temperature range T_J = -40°C to T_J = 150°C, unless otherwise specified.*

***Note**: Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.*

***Note**: Absolute maximum ratings are not subject to production test, specified by design.*

Table 17 Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	PVDD	-0.3	–	80	V	–
Supply voltage slew rate, start-up	$SR_{PVDD\_START\_UP}$	–	–	2	V/µs	During start-up
Supply voltage slew rate, active	SR_{PVDD_ACTIVE}	–	–	0.25	V/µs	During active mode
CE pin voltage	V_{CE}	-0.3	–	7	V	–
Power ground to digital ground voltage	PGND - DGND	-0.3	–	0.3	V	–
Low-side gate driver supply voltage	VCCLS	-0.3	–	16.5	V	This is the same as PVCC

(table continues...)

Table 17 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCCHS voltage	VCCHS	PVDD - 0.3	–	86.5	V	VCCHS = PVDD + PVCC
VCCHS - VSHx voltage	VCCHS - V_{SHx}	–	–	86.5	V	–
VCCHS - VGHx voltage	VCCHS - V_{GHx}	–	–	86.5	V	–
Source high-side voltage, DC voltage	V_{SHx_DC}	-8	–	80	V	DC voltage
Source high-side voltage, 500 ns pulse	V_{SHx_500ns}	-10	–	80	V	500 ns pulse max
Source low-side voltage / amplifier positive input voltage, DC voltage	V_{SLx_DC}	-8	–	8	V	DC voltage
Source low-side voltage / amplifier positive input voltage, 500 ns pulse	V_{SLx_500ns}	-10	–	10	V	500 ns pulse max
Gate high-side voltage, DC voltage	V_{GHx_DC}	-8	–	VCCHS + 0.3	V	DC voltage
Gate high-side voltage, 500 ns pulse	V_{GHx_500ns}	-10	–	VCCHS + 0.3	V	500 ns pulse max
Gate low-side voltage, DC voltage	V_{GLx_DC}	-8	–	VCCLS + 0.3	V	DC voltage
Gate low-side voltage, 500 ns pulse	V_{GLx_500ns}	-10	–	VCCLS + 0.3	V	500 ns pulse max
Gate to source high-side voltage, DC voltage	$(V_{GHx} - V_{SHx})_{DC}$	-0.3	–	16	V	DC voltage, T_J = 25°C

(table continues...)

Table 17 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Gate to source high-side voltage, 500 ns pulse	$(V_{GHx} - V_{SHx})_{500ns}$	-2	–	16	V	500 ns pulse max, T_J = 25°C
Gate to source low-side voltage, DC voltage	$(V_{GLx} - V_{SLx})_{DC}$	-0.3	–	16	V	DC voltage, T_J = 25°C
Gate to source low-side voltage, 500 ns pulse	$(V_{GLx} - V_{SLx})_{500ns}$	-2	–	16	V	500 ns pulse max, T_J = 25°C
VDRAIN voltage	VDRAIN	-0.3	–	80	V	–
Amplifier negative input voltage	V_{CSN}	-0.3	–	DVDD + 0.3	V	–
Flying capacitor 1 voltage	$V_{CP1H} - V_{CP1L}$	-0.3	–	9	V	–
CP1L pin voltage	V_{CP1L}	-0.3	–	9	V	–
CP1H pin voltage	V_{CP1H}	-0.3	–	16.5	V	–
Flying capacitor 2 voltage	$V_{CP2H} - V_{CP2L}$	-0.3	–	80	V	–
CP2L pin voltage	V_{CP2L}	-0.3	–	16.5	V	–
CP2H pin voltage	V_{CP2H}	-0.3	–	86.5	V	–
Buck converter output voltage	VDDB	-0.3	–	9	V	–
Buck converter phase voltage, DC condition	V_{PH_DC}	-0.3	–	80	V	DC condition
Buck converter phase voltage, less than 20 ns pulse	V_{PH_20ns}	-5	–	80	V	Less than 20 ns pulse
DVDD regulator output voltage	DVDD	-0.3	–	6	V	–

(table continues...)

Table 17 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input/output pin voltage	V_{INHx}, V_{INLx}, V_{nFAULT}, V_{SCLK}, V_{nSCS}, V_{SDI}, V_{SDO}, V_{CSOx}	-0.3	–	DVDD + 0.3	V	–
Maximum current for digital pins	$I_{DIG\_IN\_MAX}$	-1	–	1	mA	–
Analog input pin voltage	V_{EN_DRV}, $V_{VSENSE/nBRAKE}$, $V_{CS\_GAIN/AZ}$	-0.3	–	7	V	Analog, or analog and digital pins
Maximum current for analog inputs	$I_{AN\_IN\_MAX}$	-1	–	10	mA	–
Maximum sink current for open-drain pin	$I_{OD\_SINK\_MAX}$	–	–	7	mA	–
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_S	-55	–	150	°C	–
Case temperature	T_{CASE}	–	–	145	°C	–

4.2 ESD robustness

***Note**: ESD robustness data is not subject to production test, specified by design.*

Table 18 ESD robustness

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness all pins, HBM	$\lvert V_{ESD\_HBM}\rvert$	–	–	2000	V	HBM [1)]
ESD robustness all pins, CDM	$\lvert V_{ESD\_CDM\_1}\rvert$	–	–	500	V	CDM [2)]
ESD robustness corner pins, CDM	$\lvert V_{ESD\_CDM\_2}\rvert$	–	–	750	V	CDM [2)] for corner pins only

1) ESD robustness, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

2) ESD robustness, Charged Device Model (CDM) according to ANSI/ESDA/JEDEC JS-002.

4.3 Package characteristics

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.*

***Note**: Thermal data is not subject to production test, specified by design.*

Table 19 Package characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-ambient thermal resistance	R_{thJA}	–	33.72	–	°C/W	T_A = 25°C, FR4 PCB, size: 60.0 mm x 40.0 mm x 1.5 mm, stack 2S2P
Junction-to-case (top) thermal resistance	$R_{thJC(top)}$	–	23.66	–	°C/W	T_A = 25°C
Junction-to-case (bottom) thermal resistance	$R_{thJC(bot)}$	–	4.72	–	°C/W	T_A = 25°C

4.4 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

***Note**: Within the functional or operating range, the IC operates as described in the functional description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

Table 20 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	PVDD	5.5	–	70	V	–
Supply voltage slew rate, start-up	$SR_{PVDD\_START\_UP}$	–	–	2	V/µs	During start-up
Supply voltage slew rate, active	SR_{PVDD_ACTIVE}	–	–	0.25	V/µs	During active mode
CE pin voltage	V_{CE}	0	–	6	V	–

(table continues...)

Table 20 (continued) Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Buck converter phase voltage, DC condition	V_{PH_DC}	0	–	70	V	DC condition
Buck converter phase voltage, less than 20 ns pulse	V_{PH_20ns}	0	–	70	V	Less than 20 ns pulse
Inverter phase voltage	V_{SHx}	-8	–	70	V	–
VDRAIN voltage	VDRAIN	5.5	–	70	V	–
Gate driver maximum operating frequency	f_{PWM_GD}	0	–	200	kHz	–
Digital pin I/O voltage range	V_{INHx}, V_{INLx}, V_{nFAULT}, $V_{CS\_GAIN/AZ}$, V_{EN_DRV}, V_{SCLK}, V_{nSCS}, V_{SDI}, V_{SDO}	0	–	DVDD	V	When CS_GAIN/AZ pin works as digital input
Analog pins voltage range	V_{CSOx}, $V_{VSENSE/nBRAKE}$, $V_{CS\_GAIN/AZ}$	0	–	DVDD	V	When CS_GAIN/AZ and VSENSE/nBRAKE pins work as analog pins
Amplifier input voltage range	V_{SLx}, V_{CSNx}	-0.3	–	0.3	V	Current sense amplifier configured for shunt resistor sensing
Junction temperature	T_J	-40	–	125	°C	–

4.5 Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature. Typical values represent the median values related to T_A = 25°C unless otherwise specified.

Table 21 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption						
PVDD current, active mode	I_{PVDD_ACTIVE}	20	–	50	mA	$V_{EN\_DRV} > V_{EN\_DRV\_TH}$, $V_{CE} > V_{CE\_TH\_R}$, PVDD = 40 V, typical application run

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PVDD current, standby mode	$I_{PVDD\_STANDBY}$	3	–	8	mA	$V_{EN\_DRV} < V_{EN\_DRV\_TH}$, $V_{CE} > V_{CE\_TH\_R}$, PVDD = 40 V
PVDD current, OFF mode	I_{PVDD_OFF}	25	–	40	µA	$V_{EN\_DRV} < V_{EN\_DRV\_TH}$, $V_{CE} < V_{CE\_TH\_F}$, PVDD = 40 V
VDRAIN current, active mode	I_{VDRAIN_ACTIVE}	–	–	200	nA	$V_{EN\_DRV} > V_{EN\_DRV\_TH}$, $V_{CE} > V_{CE\_TH\_R}$, VDRAIN = PVDD = 40 V, typical application run
VDRAIN current, standby mode	$I_{VDRAIN\_STANDBY}$	–	–	200	nA	$V_{EN\_DRV} < V_{EN\_DRV\_TH}$, $V_{CE} > V_{CE\_TH\_R}$, VDRAIN = PVDD = 40 V
VDRAIN current, OFF mode	I_{VDRAIN_OFF}	–	–	200	nA	$V_{EN\_DRV} < V_{EN\_DRV\_TH}$, $V_{CE} < V_{CE\_TH\_F}$, VDRAIN = PVDD = 40 V
Gate driver						
Low-side gate driver supply voltage target	VCCLS	7	–	15	V	Generated from charge pump. Gate driver supply voltage programmable via SPI
High-side gate driver supply voltage target	VCCHS	10.8	–	84.3	V	Generated from charge pump. Gate driver supply voltage programmable via SPI according to VCCLS
High-side gate driver output	V_{GHx} - V_{SHx}	–	–	VCCLS - 0.7	V	More details in Chapter 4.6
Low-side gate driver output	V_{GLx} - V_{SLx}	–	–	VCCLS	V	More details in Chapter 4.6
Peak source current (high-side and low-side drivers)	$I_{GD\_SRC\_PEAK}$	–	1.5	–	A	Current flowing from pin. Gate driver current programmable via SPI
Peak sink current (high-side and low-side drivers)	$I_{GD\_SNK\_PEAK}$	–	1.5	–	A	Current into the pin. Gate driver current programmable via SPI
Hold gate current, low-side	I_{HOLD_LS}	–	250	–	mA	[1] Low-side gate driver
Hold gate current, high-side	I_{HOLD_HS}	–	50	–	mA	[1] High-side gate driver
Source and sink current accuracy	A_{IGD}	-20		20	%	With respect to gate driver current mean value. Mean value for the different programmed settings can deviate from target value

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Charge pump clock frequency	f_{CP_CLK}	190	–	1600	kHz	Programmable via SPI
Charge pump clock accuracy	A_{CP_CLK}	-5	–	5	%	–
Charge pump clock frequency spread spectrum	$f_{CP\_CLK\_SS}$	0	–	30	%	1)
High-side gate driver average current, PVDD ≥ 9.5 V	$I_{GD\_VCCHS\_PVD\_D\geq 9.5V}$	–	–	60	mA	PVDD ≥ 9.5 V operation
High-side gate driver average current, PVDD < 9.5 V	$I_{GD\_VCCHS\_PVD\_D<9.5V}$	–	–	30	mA	PVDD < 9.5 V operation
Low-side gate driver average current, PVDD ≥ 9.5 V	$I_{GD\_VCCLS\_PVD\_D\geq 9.5V}$	–	–	60	mA	PVDD ≥ 9.5 V operation
Low-side gate driver average current, PVDD < 9.5 V	$I_{GD\_VCCLS\_PVD\_D<9.5V}$	–	–	30	mA	PVDD < 9.5 V operation
Charge pump ramp up time, PVDD ≥ 10 V	$t_{CP\_START\_PVD\_D\geq 10V}$	–	–	250	µs	1) PVDD ≥ 10 V. C_{CPx} = 220 nF, C_{VCCLS} = 1 µF, I_{LOAD} < 50 µA, PVCC = 12 V. Depends on capacitance values and features like charge pump precharge for VCCLS
Charge pump ramp up time, PVDD < 10 V	$t_{CP\_START\_PVD\_D<10V}$	–	–	1	ms	1) PVDD < 10 V. C_{CPx} = 220 nF, C_{VCCLS} = 1 µF, I_{LOAD} < 50 µA, PVCC = 12 V. Depends on capacitance values and features like charge pump precharge for VCCLS
Gate driver PWM frequency	f_{PWM_GD}	–	–	200	kHz	1)
Input pin pulse width	t_{INx_PW}	80	–	–	ns	Applies to INHx and INLx pins. Precharge current disabled, current setting to 1.5 A
Dead time	t_{DT_RISE}, t_{DT_FALL}	120	–	12040	ns	1) Programmable via SPI. This is the minimum dead time value possible. If input PWM signals have dead time lower than this, this value applies otherwise PWM signal dead time is used.

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Dead time matching, channel-to-channel	$\Delta t_{DT\_CH\_CH}$	0	–	10	ns	1)
Gate to source passive weak pull-down resistor	$R_{GS\_PD\_WEAK}$	70	100	130	kΩ	Always active
Gate to source active strong pull-down resistor	$R_{GS\_PD\_STRONG}$	0.25	1	2	kΩ	Pull-down resistor enabled when EN_DRV or PVDD are off and V_{Gxy} - V_{Sxy} ≥ 2 V. Both high-side and low-side drivers
Propagation delay INHx to GHx	t_{PROP_HS}	80	–	250	ns	Dead time not considered. From 50% input to 50% output
Propagation delay INLx to GLx	t_{PROP_LS}	80	–	250	ns	Dead time not considered. From 50% input to 50% output
Propagation delay matching, high-low side	$\Delta t_{PROP\_HS\_LS}$	0	25	–	ns	1)
Propagation delay matching, channel-to-channel	$\Delta t_{PROP\_CH\_CH}$	0	–	10	ns	1)
Gate to source comparator threshold	$V_{GS\_CMP\_TH}$	–	250	–	mV	Threshold voltage referred to: For pull down GHx - SHx (resp. GLx - SLx for low-side driver). For pull up VCCHS - GHx (resp. VCCLS - GLx for low-side driver)
Gate to source comparator deglitch time	$t_{VGS\_CMP\_DEGLITCH}$	–	500	–	ns	1)
Synchronous buck converter						
Buck converter output target voltage, PVCC_SETPT = b11	$VDDB_{NOM\_b11}$	–	6.5	–	V	PVCC_SETPT = b11, PVDD ≥ 8 V, I_{VDDB} = 0 A

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Buck converter output target voltage, PVCC_SETPT = b10	$VDDB_{NOM\_b10}$	–	7.0	–	V	PVCC_SETPT = b10, PVDD ≥ 8.5 V, I_{VDDB} = 0 A
Buck converter output target voltage, PVCC_SETPT = b0x	$VDDB_{NOM\_b0x}$	–	8.0	–	V	PVCC_SETPT = b0x, PVDD ≥ 9.5 V, I_{VDDB} = 0 A
Buck regulator output voltage at low input voltage (PVDD), PVCC_SETPT = b11	$VDDB_{NOM\_LV\_b11}$	4.6	6.5	6.65	V	PVCC_SETPT = b11, 5.5 V ≤ PVDD < 8 V. Buck with fixed duty cycle. VDDB dependent on I_{VDDB}. Min value defined at I_{VDDB} = 200 mA condition
Buck regulator output voltage at low input voltage (PVDD), PVCC_SETPT = b10	$VDDB_{NOM\_LV\_b10}$	4.6	7.0	7.15	V	PVCC_SETPT = b10, 5.5 V ≤ PVDD < 8.5 V. Buck with fixed duty cycle. VDDB dependent on I_{VDDB}. Min value defined at I_{VDDB} = 200 mA condition
Buck regulator output voltage at low input voltage (PVDD), PVCC_SETPT = b0x	$VDDB_{NOM\_LV\_b0x}$	4.6	8.0	8.21	V	PVCC_SETPT = b0x, 5.5 V ≤ PVDD < 9.5 V. Buck with fixed duty cycle. VDDB dependent on I_{VDDB}. Min value defined at I_{VDDB} = 200 mA condition
Buck converter output voltage load regulation, 500 kHz	$\Delta VDDB_{LOAD\_500kHz}$	-10	–	9	%	[1] PVDD > $VDDB_{NOM\_bxx}$ + 2.5 V, I_{VDDB} transient from 60 mA to 540 mA (10% to 90% load transient), C_{VDDB} = 47 µF, L_{BUCK} = 22 µH, f_{BUCK_SW} = 500 kHz
Buck converter output voltage load regulation, 1000 kHz	$\Delta VDDB_{LOAD\_1000kHz}$	-9.5	–	5	%	[1] PVDD > $VDDB_{NOM\_bxx}$ + 2.5 V, I_{VDDB} transient from 60 mA to 540 mA (10% to 90% load transient), C_{VDDB} = 47 µF, L_{BUCK} = 10 µH, f_{BUCK_SW} = 1000 kHz
Buck converter maximum average current, PVDD ≥ 9.5 V	$I_{VDDB\_MAX\_PVDD\geq9.5V}$	–	–	600	mA	PVDD ≥ 9.5 V. VDDB supplies charge pumps, DVDD linear regulator and VDDB pin

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Buck converter maximum average current, PVDD at low voltage	$I_{VDDB\_MAX\_PVDD\_LOW}$	–	–	200	mA	PVDD at low input voltage range so VDDB = $VDDB_{NOM\_LV\_bxx}$. VDDB supplies charge pumps, DVDD linear regulator and VDDB pin
Buck converter maximum duty cycle	D_{BUCK_MAX}	–	95	–	%	–
Buck converter high-side switch RDSON	$R_{DSON\_BUCK\_HS}$	0.7	1.4	2.2	Ω	–
Buck converter low-side switch RDSON	$R_{DSON\_BUCK\_LS}$	0.3	0.45	1.0	Ω	–
Buck switching frequency, 500 kHz	$f_{BUCK\_SW\_500kHz}$	450	500	590	kHz	[1] Configurable via OTP write. May vary during load steps. Valid for the recommended component values L_{BUCK} = 22 µH and C_{VDDB} = 47 µF. See Table 22
Buck switching frequency, 1000 kHz	$f_{BUCK\_SW\_1000kHz}$	850	1000	1150	kHz	[1] Configurable via OTP write. May vary during load steps. Valid for the recommended component values L_{BUCK} = 10 µH and C_{VDDB} = 47 µF. See Table 22
Buck converter soft start timing	$t_{VDDB\_SFT\_START}$	–	–	1500	µs	[1] Actual value depends on buck output filter
Linear regulator DVDD						
Regulator target output voltage, 3.3 V	$DVDD_{3.3V}$	–	3.3	–	V	Programmable via SPI or external pull down resistor on VSENSE pin: R_{SENSE} ≤ 3.3 kΩ => DVDD = 3.3 V
Regulator target output voltage, 5 V	$DVDD_{5V}$	–	5	–	V	Programmable via SPI or external pull down resistor on VSENSE pin: R_{SENSE} ≥ 10 kΩ => DVDD = 5 V
Output voltage accuracy	A_{DVDD}	-2.5	–	2.5	%	–
Load current of DVDD	I_{DVDD}	–	–	300	mA	–
Static line regulation	$\Delta DVDD_{LINE}$	–	–	10	mV	VDDB = 6.5 V to 8 V, I_{DVDD} = 300 mA
Static load regulation	$\Delta DVDD_{LOAD}$	–	–	40	mV	VDDB = DVDD + 1.5 V, I_{DVDD} = 1 mA to 300 mA step

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Analog programming pins period	t_{AN_T}	–	25	–	µs	1) Each VSENSE and/or CS_GAIN
DVDD turn on delay	$t_{DVDD\_TON\_DELAY}$	200	–	800	µs	1) Programmable via SPI. Delay between VDDB UVLO until DVDD ramp up start
DVDD soft start timing	$t_{DVDD\_SFTSTRT}$	100	–	1600	µs	1) Configurable via SPI. Current limited by $I_{DVDD\_I\_LIM}$. If programmed timing is not achievable due to large C_{DVDD} value, start-up time is defined by $t_{DVDD\_SFT\_START} = (C_{DVDD} * DVDD) / I_{DVDD\_I\_LIM}$
Current sense amplifier						
Closed loop gain	G_{CS}	4	–	64	V/V	Configured via either external resistor or SPI
Gain error	ΔG_{CS_ERR}	-1	–	1	%	1) Measured at V_{SLx} - V_{CSNx} = 0.025 V
Offset input referred	V_{CS_OS}	-600	200	600	µV	1) Gain = 32, inputs shorted
Offset temperature drift	$\Delta V_{CS\_OS} / \Delta T$	–	5	–	µV/°C	1)
Current sense blanking time	t_{CS_BLANK}	0	–	8	µs	1) Programmable via SPI
Amplifier output settling time, low gain	$t_{CSO\_SETTLING\_LOW}$	–	600	–	ns	1) Time from input signal step to output within 1% of final output voltage. Input voltage step of 0.2 V. Gain = 4 to 24
Amplifier output settling time, high gain	$t_{CSO\_SETTLING\_HIGH}$	–	1000	–	ns	1) Time from input signal step to output within 1% of final output voltage. Input voltage step of 0.2 V. Gain = 32 to 64
Unity gain bandwidth	GBW	5	8	–	MHz	1)
Common mode rejection ratio	CMRR	60	80	–	dB	1) Gain = 8, f_{SW} from 0 Hz to 80 kHz
Power supply rejection ratio, 1 MHz	$PSRR_{1MHz}$	60	–	–	dB	1) Gain = 8, f < 1 MHz
Power supply rejection ratio, 10 MHz	$PSRR_{10MHz}$	40	–	–	dB	1) Gain = 8, f < 10 MHz
Input bias current	I_{BIAS}	–	–	50	µA	Current drawn into pin

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Common mode input range	V_{CS_COM}	-0.3	–	0.3	V	[1]
Differential mode input range	V_{CS_DIFF}	-0.3	–	0.3	V	–
Current sense output voltage range	V_{CSO}	0.3	–	DVDD - 0.3	V	–
Output voltage slew rate	SR_{CSO}	-10	–	10	V/µs	[1] Gain = 8, R_L = 470 Ω, C_L = 330 pF. V_{SLx} = +/- 250 mV
Propagation delay from gate driver (Gxy) transition to CSOx activation, shunt resistor sensing	$t_{CSAMP\_PROP\_SHUNT}$	–	130	–	ns	[1] Shunt resistor sensing
Propagation delay from gate driver (Gxy) transition to CSOx activation, RDSON sensing	$t_{CSAMP\_PROP\_RDSON}$	–	400	–	ns	[1] R_{DSON} sensing
Output target voltage reference (offset) – VREF	V_{CS_REF}	1/4 x DVDD	–	1/2 x DVDD	V	Depending on DVDD selected value: DVDD = 3.3 V or DVDD = 5 V
Accuracy of output voltage reference (offset) – VREF	A_{CS_REF}	-2	–	2	%	[1] Current sense amplifier internal offset voltage error. DVDD error excluded
Output short circuit limit	I_{CS_SC}	–	20	–	mA	Pin CSOx shorted to ground
Auto-zero active time, shunt resistor sensing	$t_{AUTO\_ZERO\_SHUNT}$	–	1.7	–	µs	[1] Shunt resistor sensing
Auto-zero active time, RDSON sensing	$t_{AUTO\_ZERO\_RDSON}$	–	2	–	µs	[1] R_{DSON} sensing

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Auto-zero cycle time, GHx switching	$t_{AUTO\_ZERO\_CYCLE\_SWITCHING}$	–	–	100	µs	1) GHx is switching
Auto-zero cycle time, GHx not switching	$t_{AUTO\_ZERO\_CYCLE\_NO\_SWITCHING}$	–	–	200	µs	1) GHx is not switching
CS_GAIN/AZ external auto-zero signal frequency	$f_{AZ\_CPCLK\_OFF}$	5	–	100	kHz	1)
CS_GAIN/AZ external auto-zero signal pulse width	$t_{AZ\_EXT\_PW}$	0.1	–	3.5	µs	1)
Current sense amplifier over-current protection comparator and DAC						
Current sense over-current comparator hysteresis	$V_{CS\_OC\_HYS}$	–	–	5	mV	–
Overcurrent comparator input offset	$V_{CS\_OCP\_OFFS}$	-12	–	12	mV	$V_{CS\_OCP\_PTHR}$ = 200 mV, $V_{CS\_OCP\_NTHR}$ = -200 mV
Overcurrent deglitch time	$t_{CS\_OCP\_DEGLITCH}$	0	–	8	µs	1) Programmable via SPI
Current sense input referred OCP threshold positive target level	$V_{CS\_OCP\_PTHR}$	20	–	300	mV	Programmable via SPI
Current sense input referred OCP threshold negative target level	$V_{CS\_OCP\_NTHR}$	-300	–	-20	mV	Programmable via SPI
VDS sensor						
VDS comparator threshold target voltage, VDS_xS_TH = b0000	$V_{VDS\_HS\_TH\_b0000}$, $V_{VDS\_LS\_TH\_b0000}$	0.071	0.10	0.129	V	VDS_HS_TH = b0000, VDS_LS_TH = b0000

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDS comparator threshold target voltage, VDS_xS_TH = b0001	$V_{VDS\_HS\_TH\_b0001}$, $V_{VDS\_LS\_TH\_b0001}$	0.122	0.15	0.178	V	[1] VDS_HS_TH = b0001, VDS_LS_TH = b0001
VDS comparator threshold target voltage, VDS_xS_TH = b0010	$V_{VDS\_HS\_TH\_b0010}$, $V_{VDS\_LS\_TH\_b0010}$	0.171	0.20	0.229	V	[1] VDS_HS_TH = b0010, VDS_LS_TH = b0010
VDS comparator threshold target voltage, VDS_xS_TH = b0011	$V_{VDS\_HS\_TH\_b0011}$, $V_{VDS\_LS\_TH\_b0011}$	0.219	0.25	0.281	V	[1] VDS_HS_TH = b0011, VDS_LS_TH = b0011
VDS comparator threshold target voltage, VDS_xS_TH = b0100	$V_{VDS\_HS\_TH\_b0100}$, $V_{VDS\_LS\_TH\_b0100}$	0.268	0.30	0.332	V	[1] VDS_HS_TH = b0100, VDS_LS_TH = b0100
VDS comparator threshold target voltage, VDS_xS_TH = b0101	$V_{VDS\_HS\_TH\_b0101}$, $V_{VDS\_LS\_TH\_b0101}$	0.310	0.35	0.390	V	VDS_HS_TH = b0101, VDS_LS_TH = b0101
VDS comparator threshold target voltage, VDS_xS_TH = b0110	$V_{VDS\_HS\_TH\_b0110}$, $V_{VDS\_LS\_TH\_b0110}$	0.364	0.40	0.436	V	[1] VDS_HS_TH = b0110, VDS_LS_TH = b0110
VDS comparator threshold target voltage, VDS_xS_TH = b0111	$V_{VDS\_HS\_TH\_b0111}$, $V_{VDS\_LS\_TH\_b0111}$	0.412	0.45	0.488	V	[1] VDS_HS_TH = b0111, VDS_LS_TH = b0111
VDS comparator threshold target voltage, VDS_xS_TH = b1000	$V_{VDS\_HS\_TH\_b1000}$, $V_{VDS\_LS\_TH\_b1000}$	0.460	0.50	0.540	V	[1] VDS_HS_TH = b1000, VDS_LS_TH = b1000

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDS comparator threshold target voltage, VDS_xS_TH = b1001	$V_{VDS\_HS\_TH\_b1001}$, $V_{VDS\_LS\_TH\_b1001}$	0.508	0.55	0.592	V	1) VDS_HS_TH = b1001, VDS_LS_TH = b1001
VDS comparator threshold target voltage, VDS_xS_TH = b1010	$V_{VDS\_HS\_TH\_b1010}$, $V_{VDS\_LS\_TH\_b1010}$	0.556	0.60	0.644	V	1) VDS_HS_TH = b1010, VDS_LS_TH = b1010
VDS comparator threshold target voltage, VDS_xS_TH = b1011	$V_{VDS\_HS\_TH\_b1011}$, $V_{VDS\_LS\_TH\_b1011}$	0.605	0.65	0.695	V	1) VDS_HS_TH = b1011, VDS_LS_TH = b1011
VDS comparator threshold target voltage, VDS_xS_TH = b1100	$V_{VDS\_HS\_TH\_b1100}$, $V_{VDS\_LS\_TH\_b1100}$	0.744	0.80	0.856	V	VDS_HS_TH = b1100, VDS_LS_TH = b1100
VDS comparator threshold target voltage, VDS_xS_TH = b1101	$V_{VDS\_HS\_TH\_b1101}$, $V_{VDS\_LS\_TH\_b1101}$	0.937	1.00	1.063	V	1) VDS_HS_TH = b1101, VDS_LS_TH = b1101
VDS comparator threshold target voltage, VDS_xS_TH = b1110	$V_{VDS\_HS\_TH\_b1110}$, $V_{VDS\_LS\_TH\_b1110}$	1.415	1.50	1.585	V	1) VDS_HS_TH = b1110, VDS_LS_TH = b1110
VDS comparator threshold target voltage, VDS_xS_TH = b1111	$V_{VDS\_HS\_TH\_b1111}$, $V_{VDS\_LS\_TH\_b1111}$	1.890	2.00	2.110	V	VDS_HS_TH = b1111, VDS_LS_TH = b1111
VDS comparator propagation delay	$t_{VDS\_CMP\_PROP}$	–	–	250	ns	1) $V_{VDS\_xS\_TH}$ = 200 mV and overdrive 100 mV at comparator input
Digital blanking time target	t_{VDS_BLANK}	1.0	–	5.0	µs	1) Programmable via SPI
Digital blanking time accuracy	Δt_{VDS_BLANK}	–	10	–	ns	1)

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital filter time target	t_{VDS_FILTER}	1.0	–	5.0	µs	1) Programmable via SPI
Digital filter time accuracy	Δt_{VDS_FILTER}	–	10	–	ns	1)
Filter timer reset off time	$t_{FLT\_RESET\_OFF}$	–	100	–	ns	1) Comparator must be low for this time for filter to reset and therefore fault not to trigger. 1 V threshold, 1 V overdrive (highly dependent on overdrive)
SHx maximum slew rate	SR_{SHx}	–	–	5	V/ns	1)
SHx pin current	I_{SHx}	-600	–	500	µA	1) See Chapter 4.6
Analog to Digital Converter (ADC)						
ADC resolution	ADC_{RES}	–	7	–	bits	–
ADC gain error	$\varepsilon_{ADC\_GAIN\_ERR}$	-1.05	–	1.05	%	–
ADC offset error	$\varepsilon_{ADC\_OFFS\_ERR}$	-2	–	2	LSB	–
ADC conversion time	t_{CONV}	–	1.28	–	µs	–
Digital inputs (INHx, INLx, SCLK, nSCS)						
Input logic low voltage, DVDD = 3.3 V	$V_{INPUT\_IL\_3.3V}$	–	–	0.8	V	DVDD = 3.3 V. Applies also to nBRAKE function in VSENSE/nBRAKE pin
Input logic low voltage, DVDD = 5 V	$V_{INPUT\_IL\_5V}$	–	–	1.8	V	DVDD = 5 V. Applies also to nBRAKE function in VSENSE/nBRAKE pin
Input logic high voltage, DVDD = 3.3 V	$V_{INPUT\_IH\_3.3V}$	1.8	–	–	–	DVDD = 3.3 V. Applies also to nBRAKE function in VSENSE/nBRAKE pin
Input logic high voltage, DVDD = 5 V	$V_{INPUT\_IH\_5V}$	3.0	–	–	V	DVDD = 5 V. Applies also to nBRAKE function in VSENSE/nBRAKE pin
Internal pull-down resistor to GND	R_{PD_DIG}	–	200	–	kΩ	Applies to INHx, INLx and SCLK pins
Internal pull-up resistor to DVDD, nSCS	R_{PU_nSCS}	–	200	–	kΩ	–

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital inputs (CE, EN_DRV)						
Internal pull-down resistor to GND, CE	R_{PD_CE}	350	625	850	kΩ	–
Internal pull-down resistor to GND, EN_DRV	$R_{PD\_EN\_DRV}$	–	500	–	kΩ	–
CE threshold voltage rising	$V_{CE\_TH\_R}$	2.7	–	–	V	T_A = -40°C to 125°C. This is the minimum CE pin voltage above which, any device (operated within operating conditions) will activate the device operation.
CE threshold voltage falling	$V_{CE\_TH\_F}$	–	–	0.6	V	T_A = -40°C to 125°C. This is the maximum CE pin voltage below which, any device (operated within operating conditions) will stop the device operation.
CE pin sink current	I_{CE_SNK}	–	–	10	µA	Current flowing into CE pin
EN_DRV threshold voltage	$V_{EN\_DRV\_TH}$	–	0.5 x DVDD	–	V	–
EN_DRV watchdog function threshold voltage high	$V_{EN\_DRV\_WD\_THH}$	–	0.8 x DVDD	–	V	–
EN_DRV watchdog signal threshold voltage low	$V_{EN\_DRV\_WD\_THL}$	–	0.2 x DVDD	–	V	–
EN_DRV threshold voltage hysteresis	$V_{EN\_DRV\_TH\_HYS}$	–	4	–	%	Applies to $V_{EN\_DRV\_TH}$, $V_{EN\_DRV\_WD\_THH}$ and $V_{EN\_DRV\_WD\_THL}$ thresholds
Digital output (nFAULT)						
Output logic low voltage	V_{OL}	–	–	0.6	V	I_o = 5 mA
Internal pull-up resistor to DVDD, nFAULT	R_{PU_nFAULT}	–	200	–	kΩ	Pull up resistor for nFAULT

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Digital output (SDO)						
Output logic low voltage, DVDD = 3.3 V	$V_{OL\_3.3V}$	–	–	0.7	V	DVDD = 3.3 V, I_o = 5 mA
Output logic low voltage, DVDD = 5 V	V_{OL_5V}	–	–	0.9	V	DVDD = 5 V, I_o = 5 mA
Output logic high voltage, DVDD = 3.3 V	$V_{OH\_3.3V}$	2.4	–	–	V	DVDD = 3.3 V, I_o = 5 mA
Output logic high voltage, DVDD = 5 V	V_{OH_5V}	4.1	–	–	V	DVDD = 5 V, I_o = 5 mA
Internal pull-down resistor to GND, SDO	R_{PD_SDO}	–	200	–	kΩ	When nSCS is high
OTP programming						
OTP programming supply voltage	$PVDD_{OTP\_PROG}$	13	–	–	V	[1] Below this value an OTP blocking will occur
OTP programming temperature	T_{OTP_PROG}	–	–	150	°C	[1] Above this value an OTP blocking will occur
Watchdog						
Watchdog period for buck converter watchdog timer	$t_{WD\_BUCK\_T}$	–	1.5	–	ms	Not configurable
Watchdog EN_DRV frequency	$f_{WD\_EN\_DRV}$	450	500	550	Hz	[1]
Overload protections - gate driver						
PVDD UVLO threshold rising	$V_{PVDD\_UVLO\_R}$	4.95	5.1	5.25	V	–
PVDD UVLO threshold falling	$V_{PVDD\_UVLO\_F}$	4.85	5.0	5.15	V	–
VCCHS UVLO threshold rising, PVCC = 7 V	$V_{HS\_UVLO\_R\_7V}$	5.6	5.85	6.1	V	PVCC = 7 V

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCCHS UVLO threshold falling, PVCC = 7 V	$V_{HS\_UVLO\_F\_7V}$	4.60	4.85	5.10	V	PVCC = 7 V
VCCLS UVLO threshold rising, PVCC = 7 V	$V_{LS\_UVLO\_R\_7V}$	6.1	6.45	6.7	V	PVCC = 7 V
VCCLS UVLO threshold falling, PVCC = 7 V	$V_{LS\_UVLO\_F\_7V}$	4.60	4.85	5.1	V	PVCC = 7 V
VCCHS UVLO threshold rising, PVCC = 10 V, 12 V or 15 V	$V_{HS\_UVLO\_R\_10TO15V}$	7.0	7.25	7.5	V	PVCC = 10 V, 12 V or 15 V
VCCHS UVLO threshold falling, PVCC = 10 V, 12 V or 15 V	$V_{HS\_UVLO\_F\_10TO15V}$	6.0	6.25	6.5	V	PVCC = 10 V, 12 V or 15 V
VCCLS UVLO threshold rising, PVCC = 10 V, 12 V or 15 V	$V_{LS\_UVLO\_R\_10TO15V}$	7.70	7.95	8.2	V	PVCC = 10 V, 12 V or 15 V
VCCLS UVLO threshold falling, PVCC = 10 V, 12 V or 15 V	$V_{LS\_UVLO\_F\_10TO15V}$	6.60	6.85	7.10	V	PVCC = 10 V, 12 V or 15 V
Overload protections - power supply system						
VDDB UVLO rising threshold	$V_{VDDB\_UVLO\_R}$	4.2	4.3	4.4	V	–
VDDB UVLO falling threshold	$V_{VDDB\_UVLO\_F}$	4.1	4.2	4.3	V	–
VDDB OVLO rising threshold	$V_{VDDB\_OVLO\_R}$	105	108	111	%	Percentage of target output value
VDDB OVLO falling threshold	$V_{VDDB\_OVLO\_F}$	101	105	107	%	Percentage of target output value
Buck OCP (inductor current) threshold, 500 kHz	$I_{BUCK\_OCP\_TH\_500kHz}$	–	1.0	–	A	f_{BUCK_SW} = 500 kHz

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Buck OCP (inductor current) threshold, 1000 kHz	$I_{BUCK\_OCP\_TH\_1000kHz}$	–	1.3	–	A	f_{BUCK_SW} = 1000 kHz
Buck OCP hysteresis	$I_{BUCK\_OCP\_HYS}$	–	50	–	mA	–
DVDD UVLO rising threshold	$V_{DVDD\_UVLO\_R}$	–	85	–	%	Percentage of target output value
DVDD UVLO falling threshold	$V_{DVDD\_UVLO\_F}$	–	75	–	%	Percentage of target output value
DVDD OVLO rising threshold	$V_{DVDD\_OVLO\_R}$	–	110	–	%	Percentage of target output value
DVDD OVLO falling threshold	$V_{DVDD\_OVLO\_F}$	–	105	–	%	Percentage of target output value
DVDD target output current limit	$I_{DVDD\_I\_LIM}$	50	–	450	mA	Programmable via SPI
DVDD target output current limit accuracy, 50 mA	$A_{DVDD\_I\_LIM\_50mA}$	-30	–	10	%	T_J = -40°C to 125°C, limit setting to 50 mA
DVDD target output current limit accuracy, 150 mA, 300 mA or 450 mA	$A_{DVDD\_I\_LIM\_150TO450mA}$	-18	–	10	%	T_J = -40°C to 125°C, limit setting to 150 mA, 300 mA or 450 mA
Overtemperature protection						
Overtemperature warning threshold	T_{OTW_TH}	–	125	–	°C	Measured via internal ADC
Overtemperature warning hysteresis	$T_{OTW\_TH\_HYS}$	–	10	–	°C	–
Overtemperature shut-down threshold	T_{OTS_TH}	–	150	–	°C	–
Overtemperature shut-down hysteresis	$T_{OTS\_TH\_HYS}$	–	10	–	°C	–

(table continues...)

Table 21 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Locked rotor protection						
Locked rotor detect time	t_{LOCK}	1	–	8	s	[1] Programmable via SPI
SPI timing requirements [1]						
Clock period	t_{CLK}	77	–	–	ns	–
Clock high time	t_{CLKH}	20	–	–	ns	–
Clock low time	t_{CLKL}	20	–	–	ns	–
SDI input data setup time	t_{SET_SDI}	10	–	–	ns	–
SDI input data hold time	t_{HD_SDI}	10	–	–	ns	–
SDO output data delay time	t_{DLY_SDO}	0	–	20	ns	SCLK high to SDO valid
SDO rise and fall time	t_{RF_SDO}	–	–	10	ns	–
nSCS enable time	t_{EN_nSCS}	–	–	50	ns	nSCS low to SDO transition
nSCS disable time	t_{DIS_nSCS}	–	–	50	ns	nSCS high to SDO high impedance
nSCS hold time	t_{HD_nSCS}	50	–	–	ns	Falling SCLK to rising nSCS
nSCS setup time	t_{SET_nSCS}	50	–	–	ns	Falling nSCS to rising SCLK
nSCS sequential delay time	t_{SEQ_nSCS}	450	–	–	ns	Rising nSCS to falling nSCS

1) Not subject to production test.

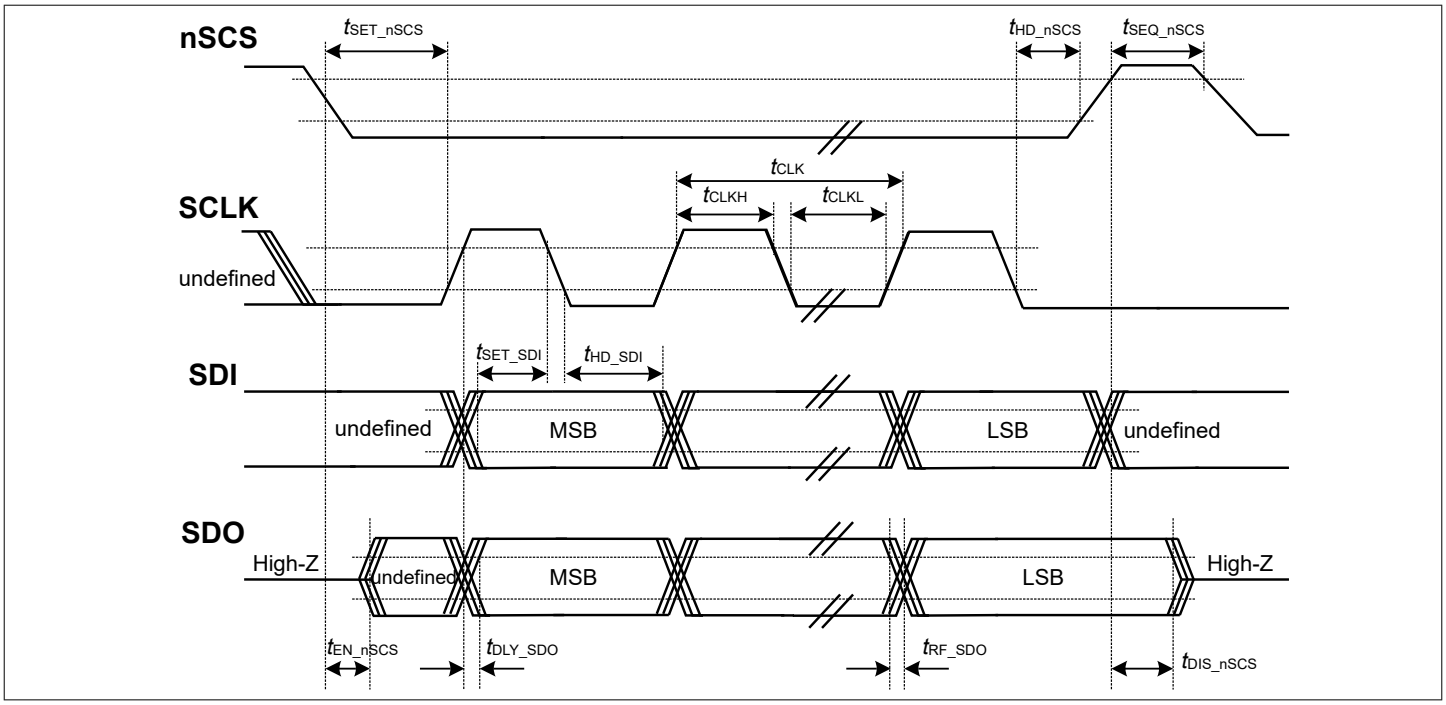

Figure 52 SPI timing diagram during active mode

4.6 Characteristic graphs

The following graphs provide information on the behavior of the device at different conditions. This data is not subject to production test. T_A = 25°C, unless otherwise specified. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), unless otherwise specified.

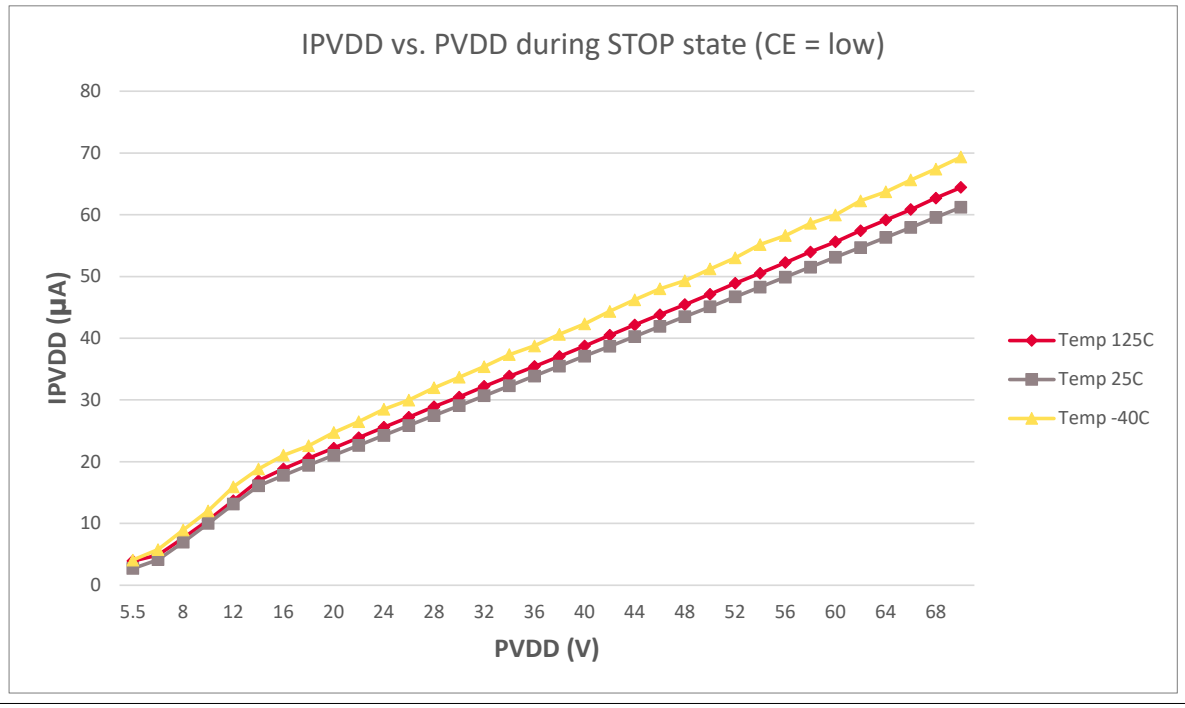

Figure 53 Power consumption on PVDD pin versus PVDD voltage during STOP state - both CE and EN_DRV are below active thresholds

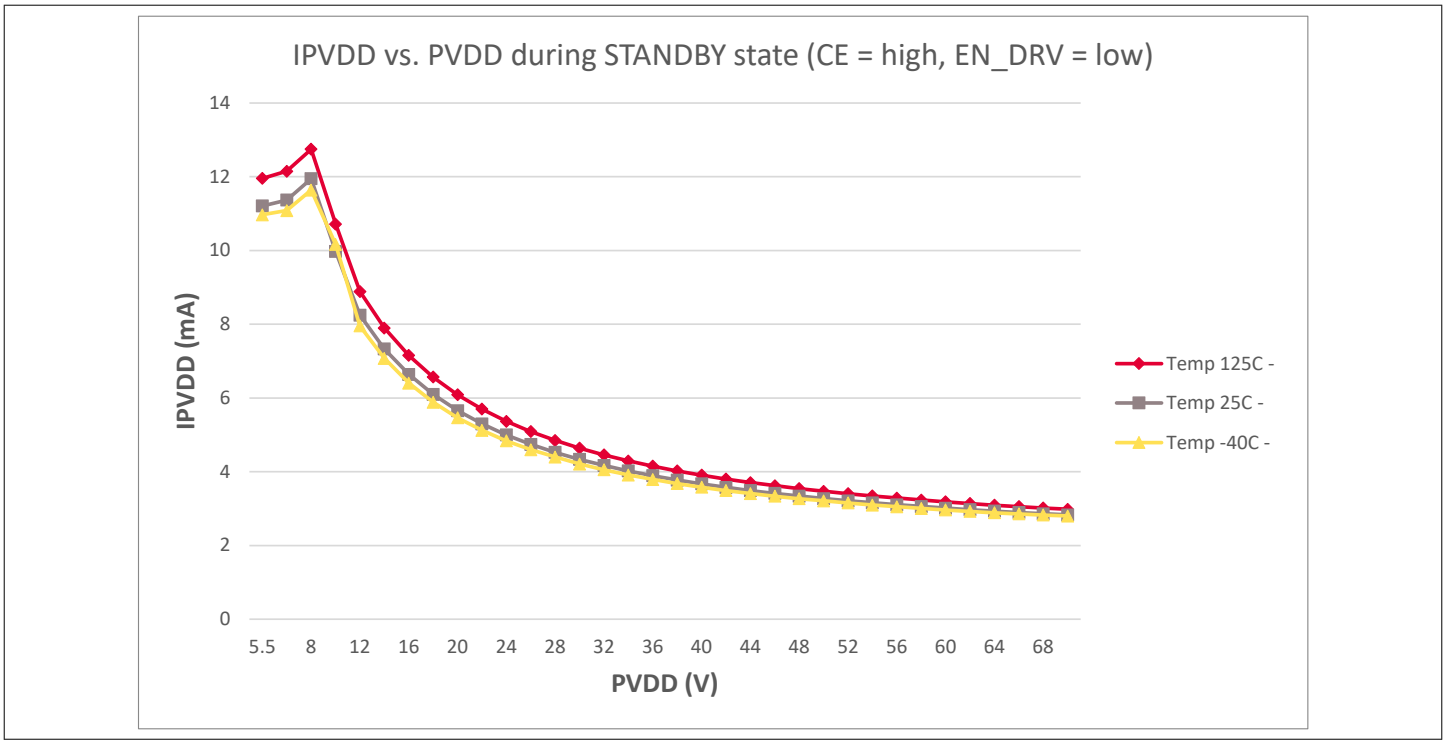

Figure 54 **Figure: Power consumption on PVDD versus PVDD voltage during STANDBY state - CE is above active threshold and EN_DRV is below**

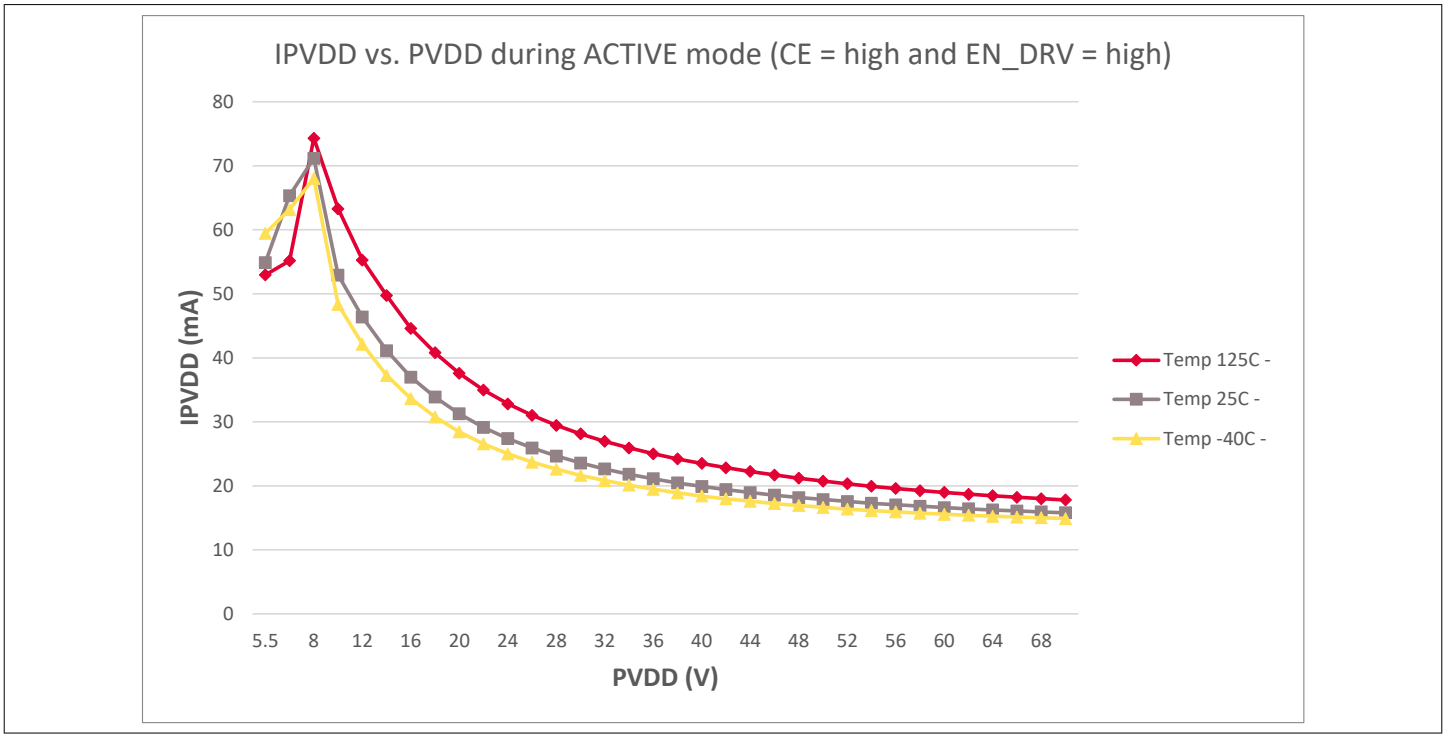

Figure 55 **Power consumption on PVDD versus PVDD voltage during ACTIVE state in a typical application - both CE and EN_DRV are above active thresholds**

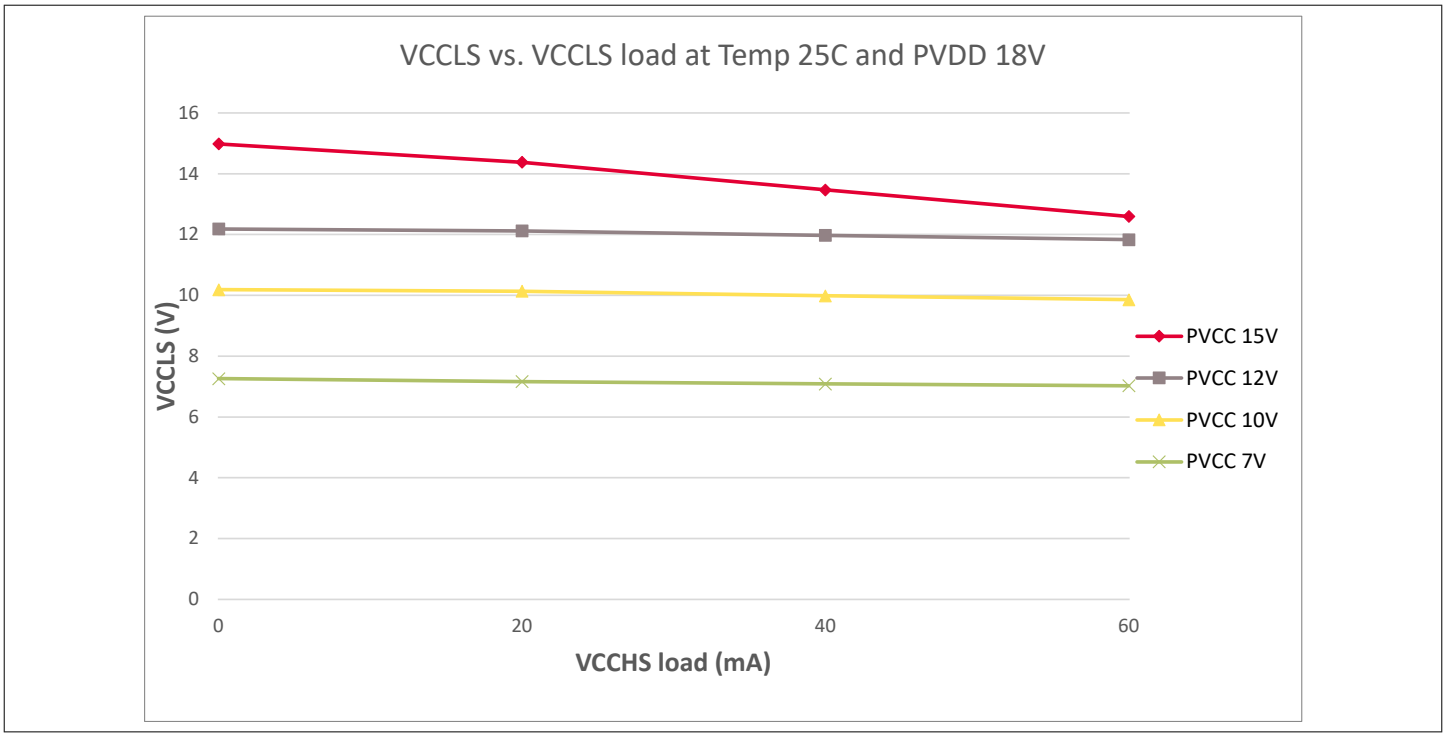

Figure 56 **VCCLS average voltage versus VCCLS load for different PVCC configurations at PVDD 18 V, typical application with $C_{CP1(2)}$ = 220 nF and C_{VCCLS} = 1 µF, VCCHS load 20 mA**

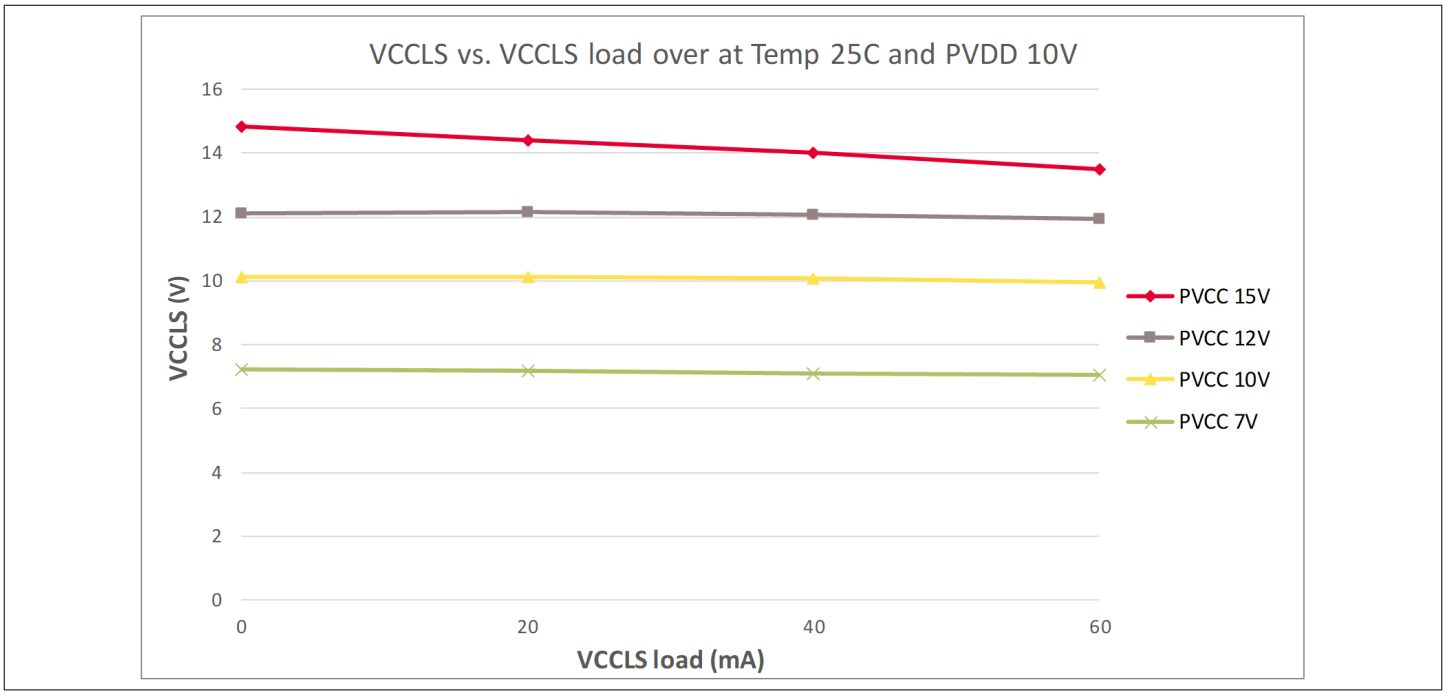

Figure 57 **VCCLS average voltage versus VCCLS load for different PVCC configurations at PVDD 10 V, typical application with $C_{CP1(2)}$ = 220 nF and C_{VCCLS} = 1 µF, VCCHS load 20 mA**

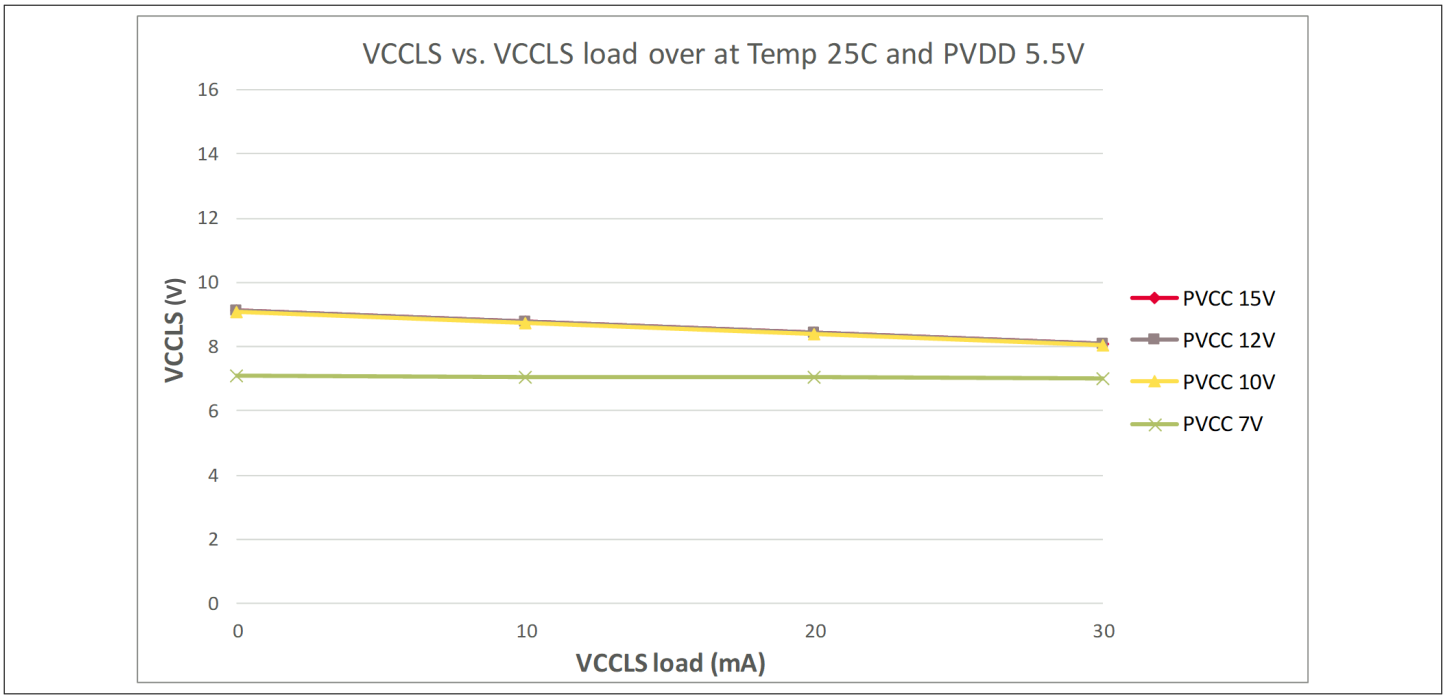

Figure 58 **VCCLS average voltage versus VCCLS load for different PVCC configurations at PVDD 5.5 V, typical application with $C_{CP1(2)}$ = 220 nF and C_{VCCLS} = 1 µF, VCCHS load 20 mA**

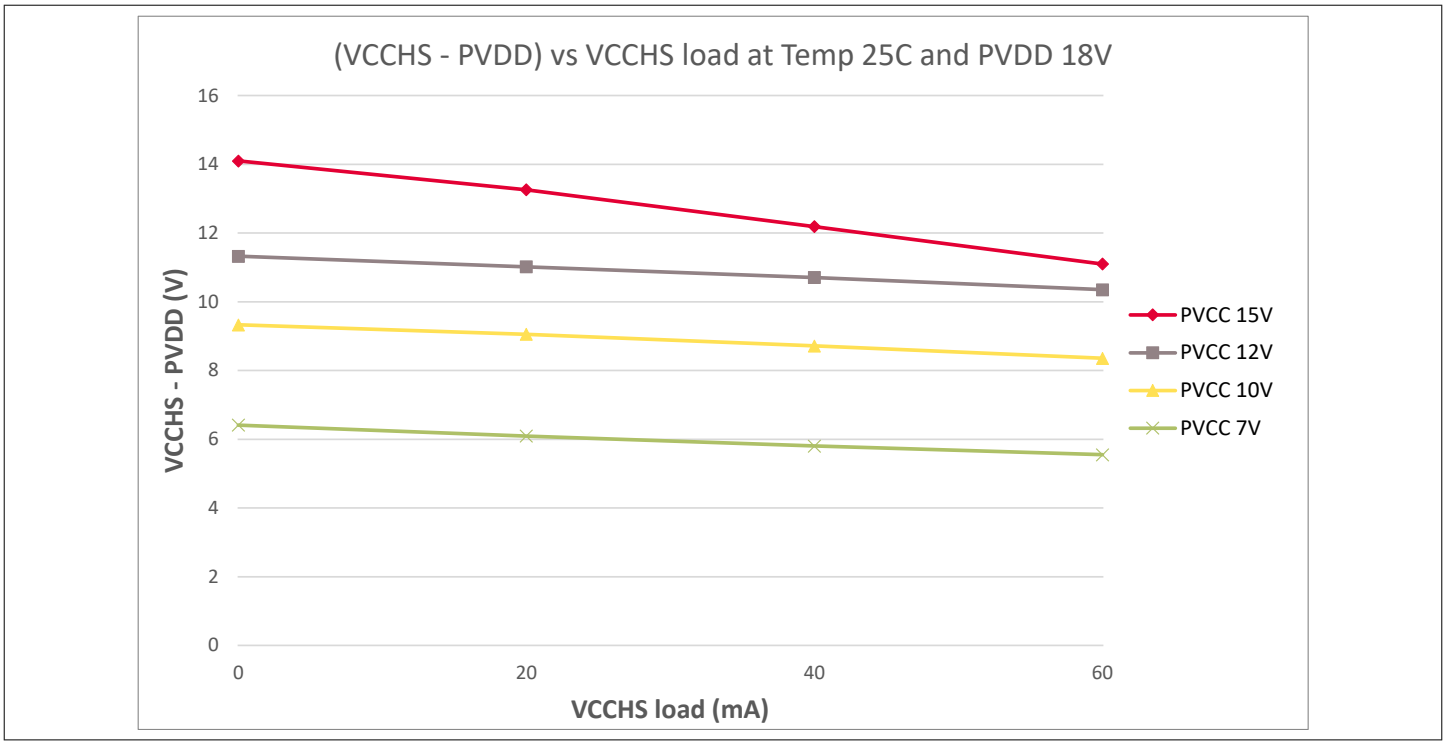

Figure 59 **High-side gate driver supply (VCCHS - PVDD) average voltage versus VCCHS load for different PVCC configurations at PVDD 18 V, typical application with $C_{CP1(2)}$ = 220 nF and C_{VCCHS} = 1 µF, VCCLS load 20 mA**

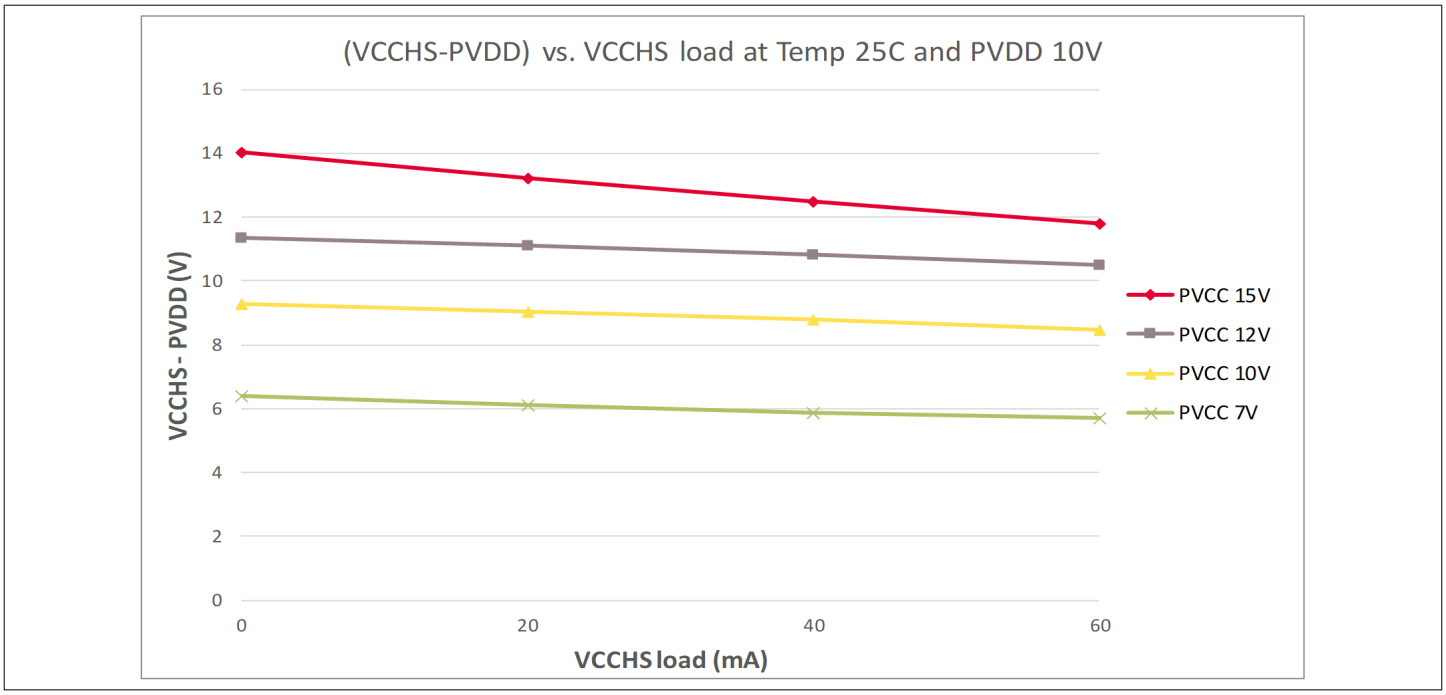

Figure 60 **High-side gate driver supply (VCCHS - PVDD) average voltage versus VCCHS load for different PVCC configurations at PVDD 10 V, typical application with $C_{CP1(2)}$ = 220 nF and C_{VCCHS} = 1 µF, VCCLS load 20 mA**

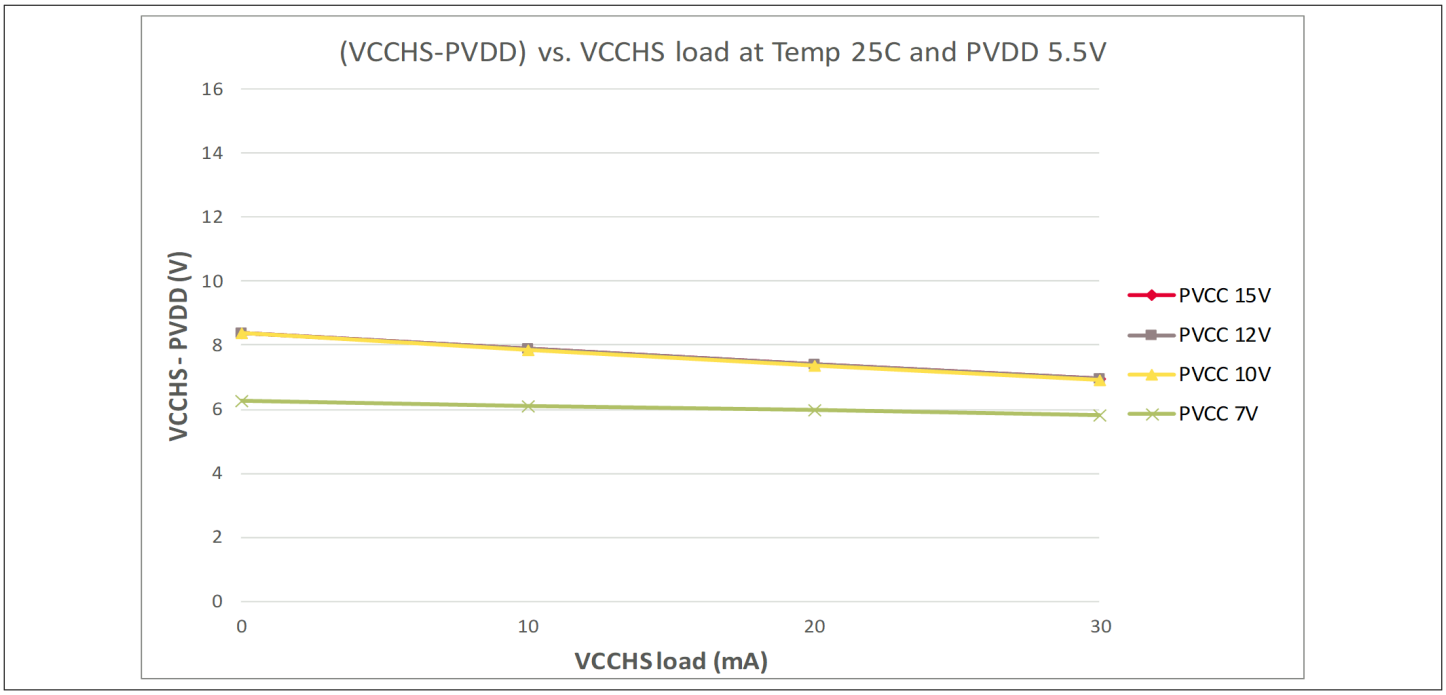

Figure 61 **High-side gate driver supply (VCCHS - PVDD) average voltage versus VCCHS load for different PVCC configurations at PVDD 5.5 V, typical application with $C_{CP1(2)}$ = 220 nF and C_{VCCHS} = 1 µF, VCCLS load 20 mA**

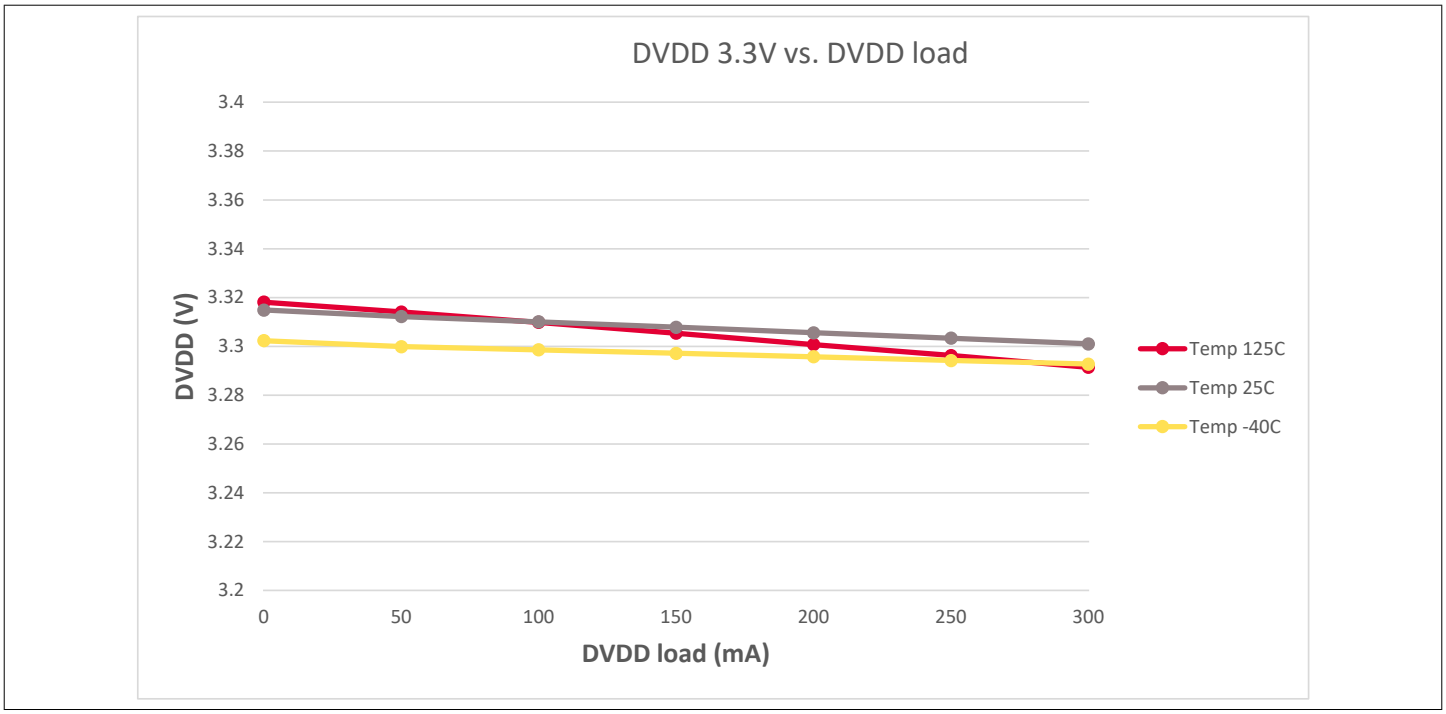

Figure 62 DVDD 3.3 V output voltage versus DVDD load at different temperatures

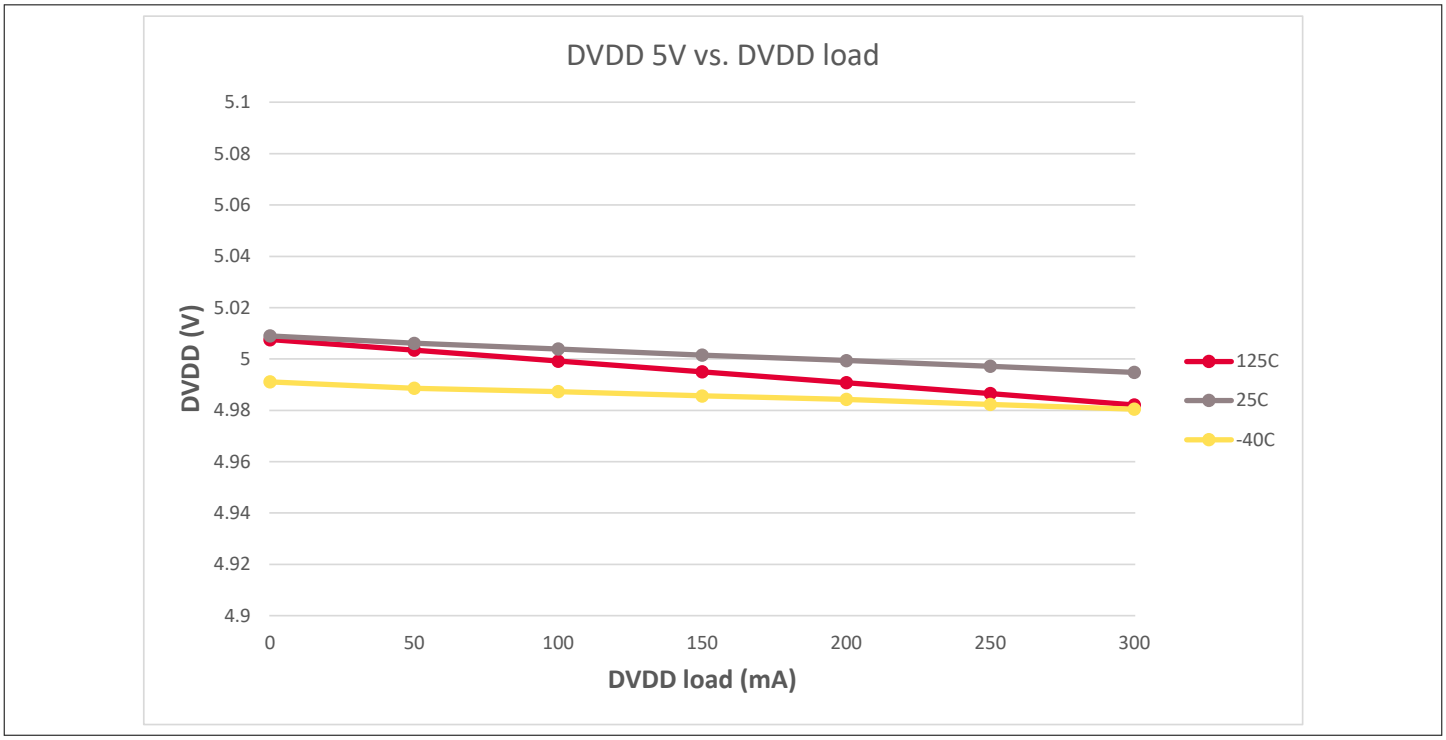

Figure 63 DVDD 5 V output voltage versus DVDD load at different temperatures

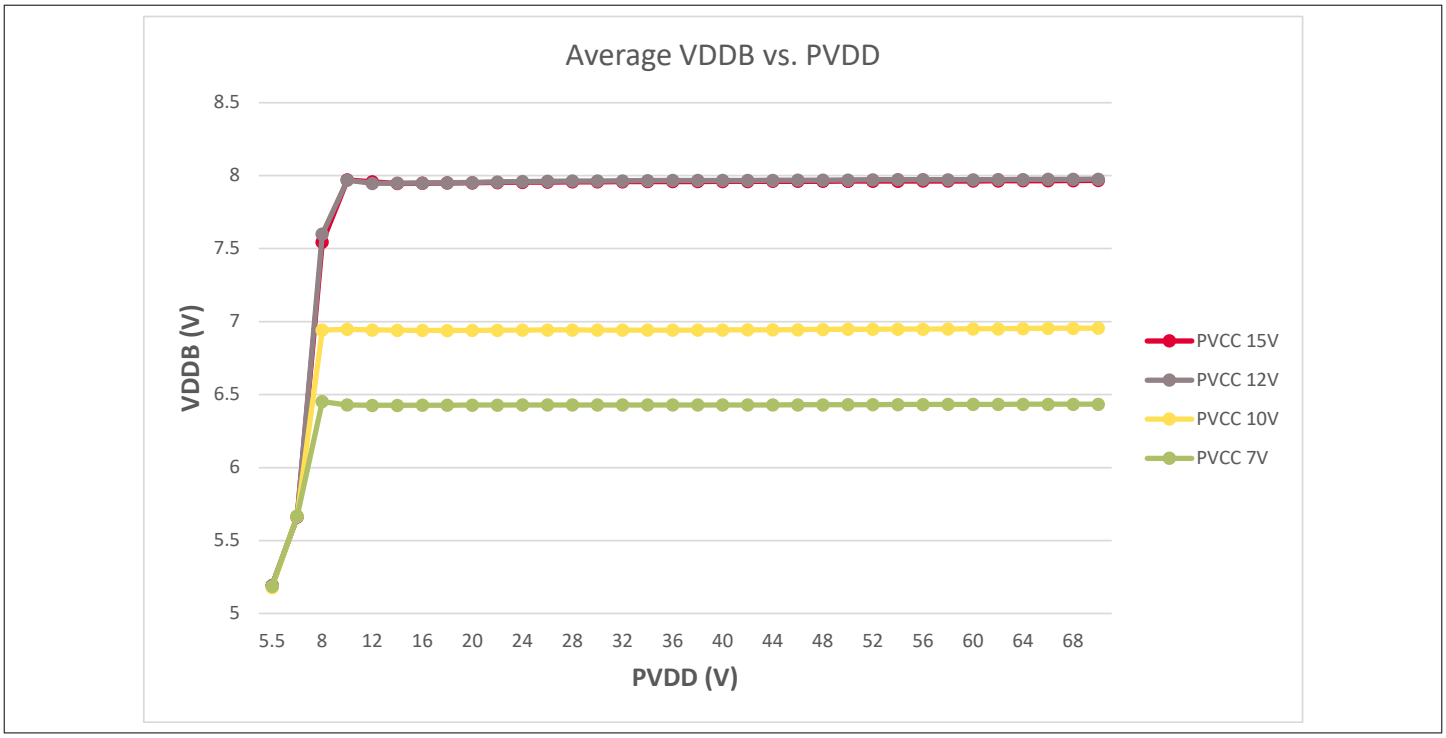

Figure 64 **Buck converter average output voltage (VDDB) versus PVDD voltage. Typical configuration, VDDB load 200 mA, buck converter switching frequency 500 kHz**

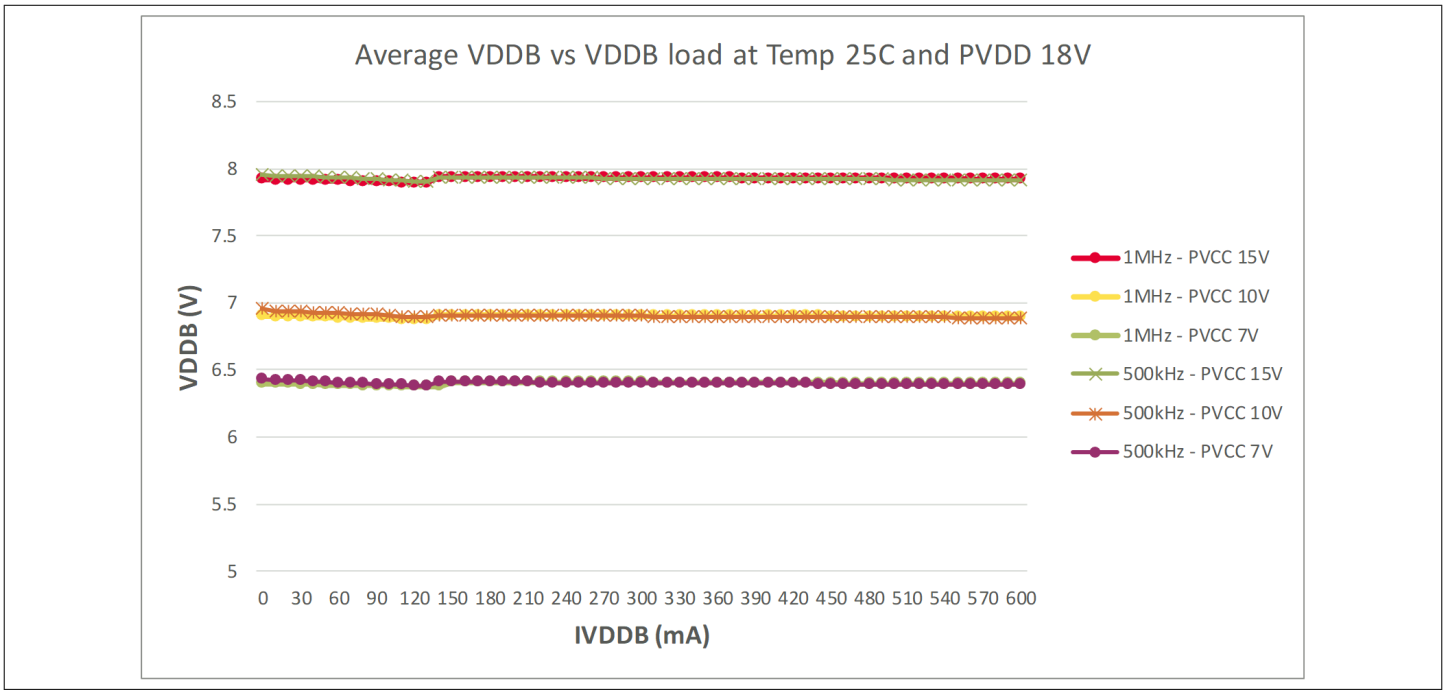

Figure 65 **Buck converter average output voltage (VDDB) versus VDDB load (I_{VDDB}) for different PVCC and buck switching frequency operations. Typical configuration**

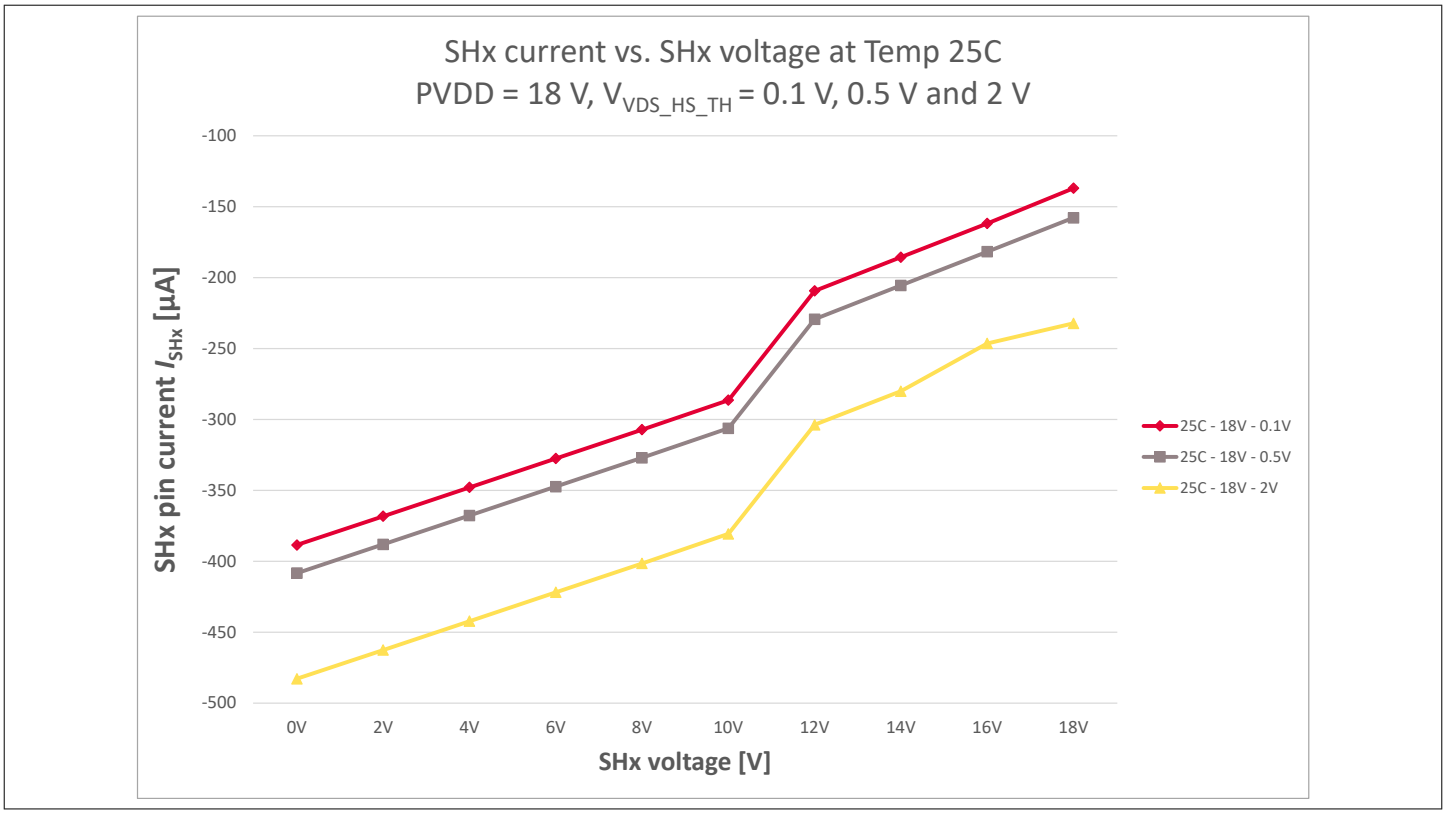

Figure 66 **SHx pin current versus SHx voltage, with 18 V PVDD and VDS comparator threshold voltages of 0.1 V, 0.5 V and 2 V, OFF state diagnostics and VDS sensors enabled**

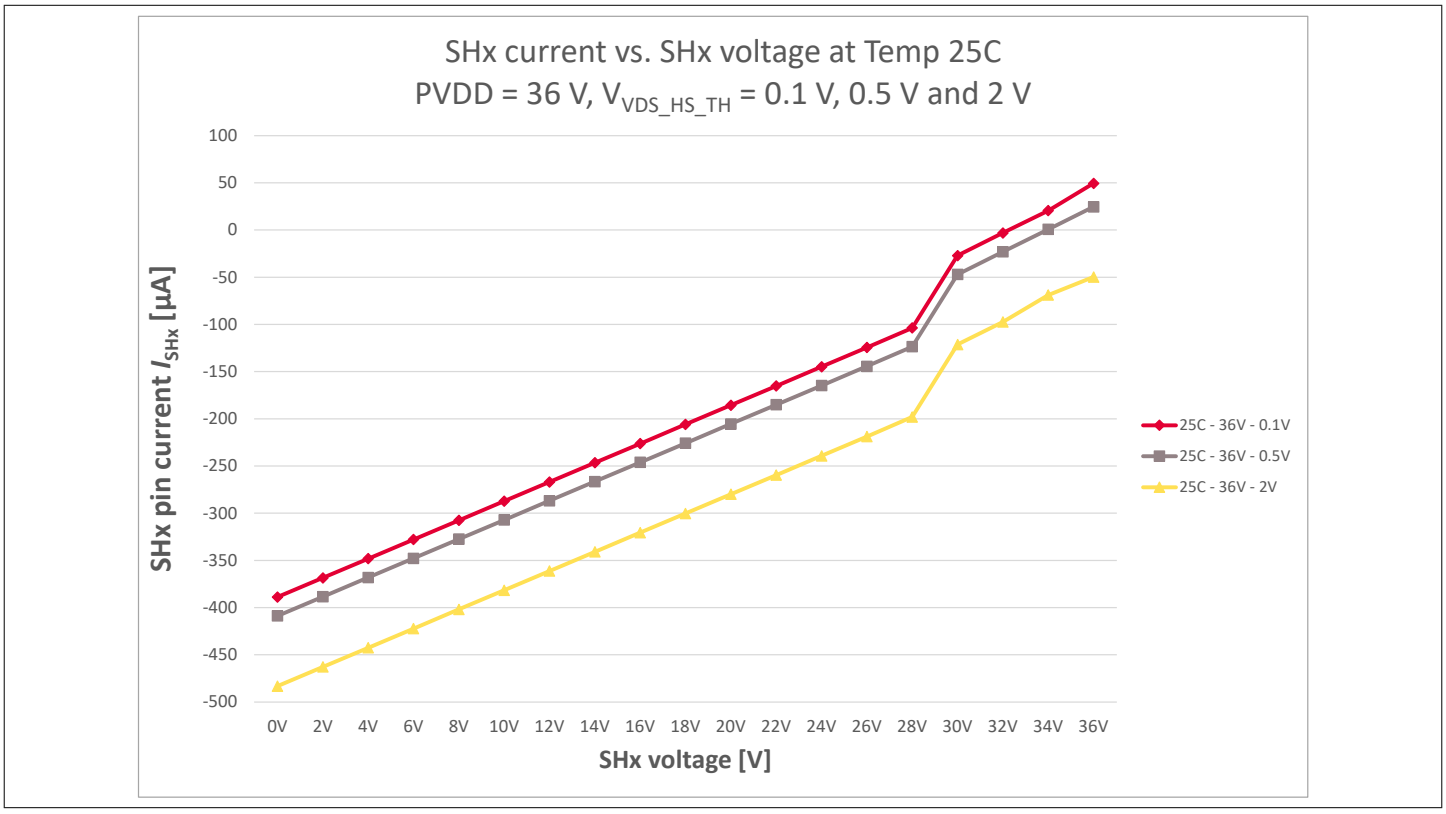

Figure 67 **SHx pin current versus SHx voltage, with 36 V PVDD and VDS comparator threshold voltages of 0.1 V, 0.5 V and 2 V, OFF state diagnostics and VDS sensors enabled**

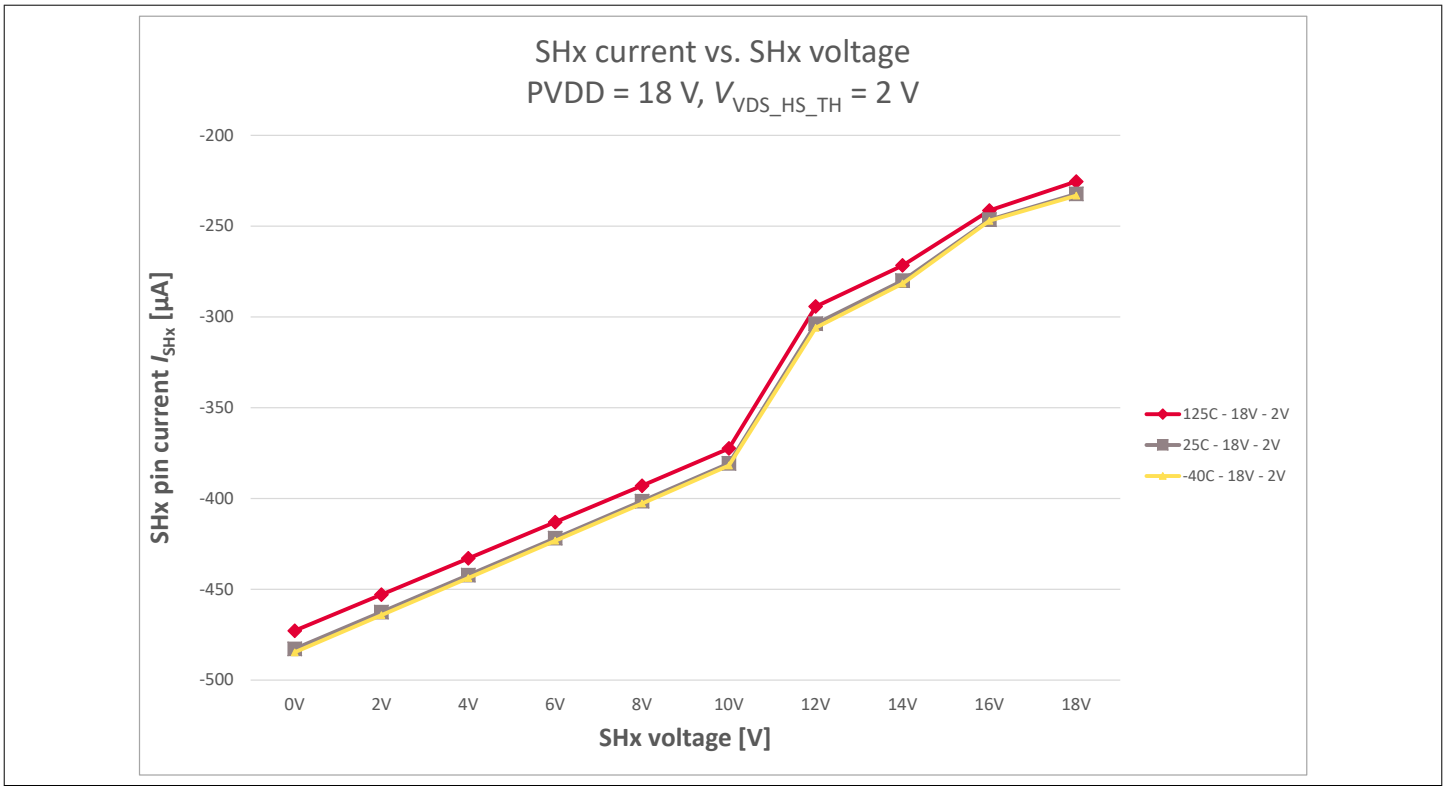

Figure 68 **SHx pin current versus SHx voltage, with 18 V PVDD and VDS comparator threshold voltage 2 V, OFF state diagnostics and VDS sensors enabled**

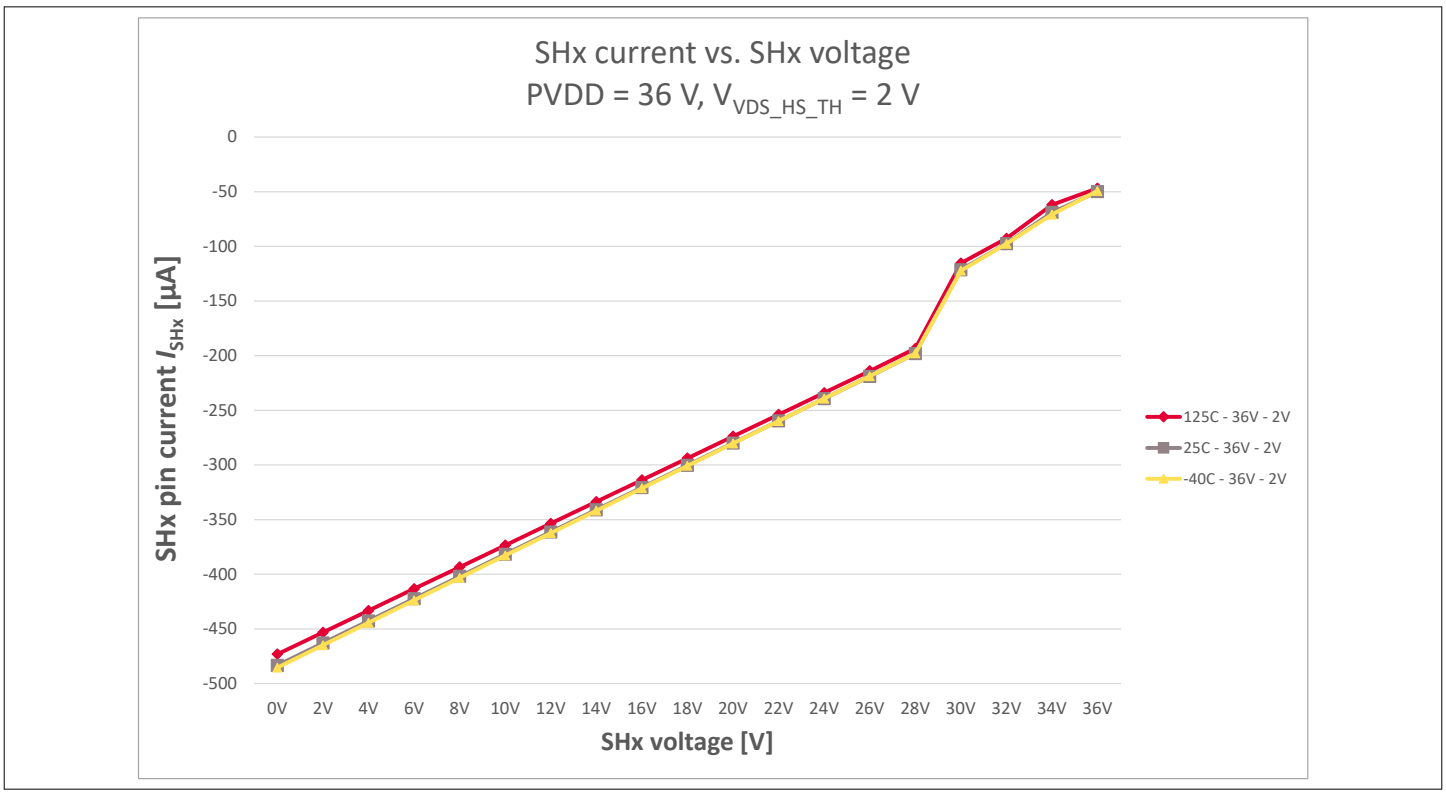

Figure 69 **SHx pin current versus SHx voltage, with 36 V PVDD and VDS comparator threshold voltage 2 V, OFF state diagnostics and VDS sensors enabled**

5 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

5.1 Recommended external components

6EDL7151 requires some external components for proper operation. Recommended components and values are listed in Table 22.

Table 22 Recommended external components

Element	Pin1	Pin2	Recommended value	Rating	Note
C_{PVDD}	PVDD	PGND	4.7 µF	According to PVDD	–
C_{DVDD}	DVDD	DGND	10 µF and 0.1 µF	16 V	According to MCU or other ICs' specifications
C_{VCCHS}	VCCHS	PVDD	1 µF < C_{VCCHS} < 2.2 µF	25 V if connected to PVDD or according to (PVDD + PVCC) if connected to PGND	Depending on VCCHS ripple and start-up requirements
C_{VCCLS}	VCCLS	PGND	1 µF < C_{VCCLS} < 4.7 µF	25 V	Depending on VCCLS ripple and start-up requirements
C_{CP1}	CP1H	CP1L	220 nF < C_{CP1} < 1 µF	25 V	0.47 µF recommended
C_{CP2}	CP2H	CP2L	220 nF < C_{CP2} < 1 µF	According to PVDD	0.47 µF recommended
L_{BUCK}	PH	VDDB	22 µH	According to max expected peak current - (device limit $I_{BUCK\_OCP\_TH}$)	500 kHz configuration
			10 µH		1 MHz configuration
C_{VDDB}	VDDB	PGND	47 µF	16 V	500 kHz configuration
			47 µF		1 MHz configuration
R_{SENSE}	VSENSE/nBRAKE	DGND	R_{SENSE} = *3.3 kΩ* => *DVDD = 3.3 V*	–	Selects DVDD 3.3 V or 5 V respectively. Tolerance 5% or better
			R_{SENSE} = *10 kΩ* => *DVDD = 5 V*		
			Diode for nBRAKE (see Chapter 5.3)		
R_{CS_GAIN}	CS_GAIN/AZ	DGND	See Table 9 for gain programming	–	1% tolerance is recommended
R_{AZ}	CS_GAIN/AZ	DVDD	1 kΩ - 10 kΩ	–	Pull up to DVDD. Diode may be required (see Chapter 3.10.3)
R_{nFAULT}	nFAULT	DVDD	1 kΩ - 10 kΩ	–	–
R_{DRAIN}	PVDD	VDRAIN	2 kΩ	–	–

5.2 PCB layout recommendations

Layout is critical to ensure high quality signals and sensing. Different recommendations are provided in this section for the best electrical, thermal and EMI results.

5.2.1 Grounding and supply

PGND is the ground used for the following sections in 6EDL7151:

- Buck converter
- Charge pumps
- Gate drivers for low-side and high-side

DGND is used for:

- DVDD linear regulator
- Digital logic
- Current sense amplifiers

It is recommended to cover the PGND-referred components with PGND solid planes and DGND-referred components with DGND solid plane, also ensure that there is no overlap between PGND and DGND planes to prevent cross-coupling.

However, PGND and DGND have be connected to the same electrical potential and must be connected to each other in one place in the PCB, and the location depends on many factors. Sometimes close to the negative (return) of the supply or battery can lead to the best results.

Decoupling capacitors for supply pin (PVDD) should be as close as possible to the PVDD pin and PGND pin. It can as well be helpful to add a small 0.1 µF capacitor for high frequency glitches suppression.

Generally speaking, shielding of critical signals like gate and sensing signals is important to prevent noise coupling and injection from other noisy areas. If the battery voltage is expected to drop transiently close to the UVLO level of PVDD, it is recommended to have large capacitors that can maintain the supply voltage during those transients. Alternatively, a diode (for example, a Schottky diode) can be used in series with PVDD and before the PVDD decoupling capacitors. This can prevent the PVDD decoupling capacitors from discharging to the battery (or other power supply) if the battery voltage briefly drops below the PVDD UVLO level of the 6EDL7151.

Similarly, CE signal might be affected by these transients if it is derived from the battery voltage with a resistor divider. It is a good practice to add a small capacitor close to CE pin to ensure these noises do not switch off the device. However, the current consumption of CE pin is extremely low. So the device might stay on for a long period if the CE pin is the only way to discharge the CE capacitor after the battery is switched off. Then it will be useful to design a discharge path in case this causes a problem.

5.2.2 Thermal design

Depending on the configurations of the device and the usage of the different integrated power converters like synchronous buck, DVDD LDO and charge pumps, the device presents different power losses that translate into self-heating. For example, the user can choose the DVDD LDO output voltage to 5 V instead of 3.3 V to reduce the losses of the LDO module. Another example, the buck converter output voltage (which is the input for the DVDD LDO), can be configured according to the gate driving voltage needs. If gate driving voltage 12 V and 15 V are not required, the user can configure the buck converter to produce 7 V output voltage, reducing the losses as well in the LDO when compared with the standard case 8 V.

To dissipate the generated heat to the PCB, it is critical to have a solid connection of the device exposed pad to the PCB thermal pad (DGND pad). It is also highly recommended to have a good amount of thermal vias that can transfer the heat from the thermal pad to the PCB efficiently. An example is presented in Figure 70.

As a general rule, thicker PCB layers (copper thickness 2 oz/ft^2 that is 70 µm, or above) can help to dissipate the heat generated by the device faster.

5.2.3 Buck converter and DVDD linear regulator

The relatively high switching frequency and high voltage switching (PVDD to PGND) of the buck converter makes it a sensitive block in the device and need extra attention during the design phase.

The main goal is to reduce the buck switching loop (PH-Inductor-Capacitor-VDDB) as much as possible. In 6EDL7151, most elements in the synchronous buck, like the external diode, the low-side MOSFET as well as the feedback or reference resistors, are integrated to mitigate the EMI emissions.

Apart from the loop itself, it is very important to reduce the PH traces to the shortest and avoid any large copper amount in the inductor connection. This PH node is switching with an amplitude of PVDD voltage at high frequency and therefore can be a source of noise to other elements, so this trace must be as far as possible from sensitive analog sensing like current sensing.

Figure 70 shows a possible buck converter layout with minimized PH trace and buck loop area.

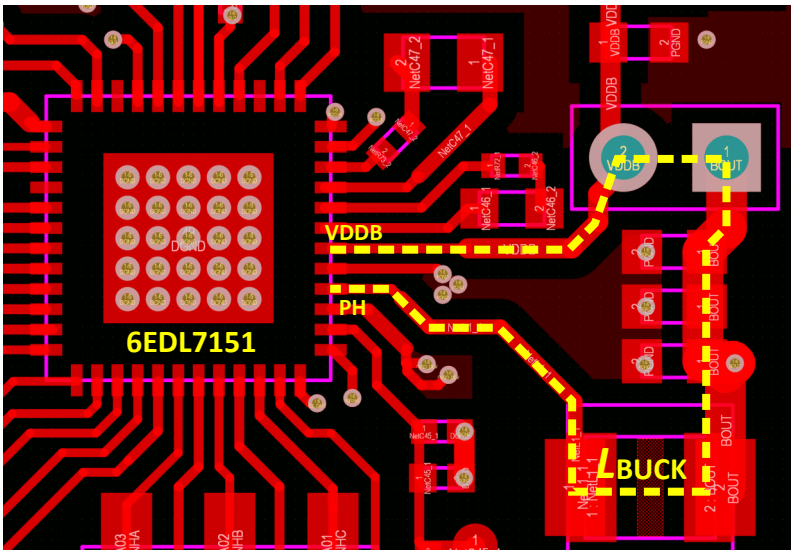

Figure 70 Buck converter layout recommendation, PH trace and buck loop area (highlighted in yellow) must be minimized

DVDD linear regulator must be decoupled with capacitors placed as close as possible to the DVDD pin and connect as short as possible to DGND on the other terminal. MCU and other components supplied by DVDD voltage are recommended to use additional local decoupling capacitors at those components. This is helpful to suppress the noise captured by the routing of those traces.

5.2.4 Gate driver and charge pumps

Maintain gate signals as symmetric as possible including symmetry between phases (similar length for phase A, B and C) to minimize the propagation delay mismatches. Keep gate current loops as short as possible and try to have as close as possible send and return signals.

The source signals of low-side SLx, are shared between source of low-side MOSFETs and top side sensing for shunt elements. It is recommended to optimize for the current sensing (symmetric tap of shunt terminal and parallel routing till current sense inputs), however, if current sense is not used, optimizing for gate driver performance is a good option.

Charge pump loops should be as small as possible, the charge pump flying capacitors must be placed close to the pins 19, 20, 21 and 22. Similar for the tank capacitors in VCCHS (pin 24) and VCCLS (pin 23). It is possible to place some of these capacitors in different layers as long as the distance to the device is the shortest possible.

The VDRAIN signal can be connected to the high-side drain where the signal is quiet and easy to access, ideally routing in a low noise PCB section or shielding the signal properly.

Figure 71 shows an example of the 6EDL7151 layout highlighting the gate driver signals and the current sensing in a three-phase inverter with dual MOSFETs.

Gate resistor R_g may be used. However, the user must know that the slew rate control of 6EDL7151 provides a new approach to fine tune the MOSFET switching speed in a programmable manner. Having R_g resistors adds additional voltage drops between the 6EDL7151 and the gate of the MOSFET. Similarly, snubber elements (in parallel with MOSFETs) and bypass capacitors (high-side drain to low-side source) in the inverter may be used. Nevertheless, the flexibility of the slew rate control of the 6EDL7151 allows the user to remove those external components specially in a

high-density PCB layout, so that more space can be used for the power section, for example, for better heat distribution in the PCB. It also minimizes the BOM.

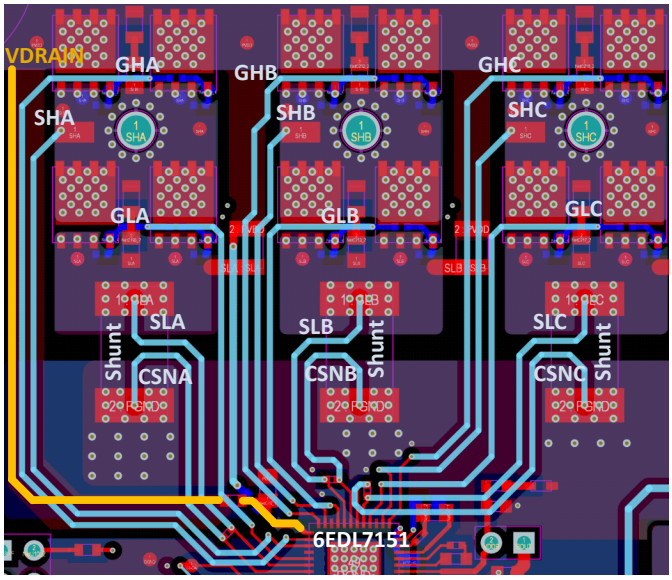

Figure 71 Gate driver and current sensing layout example. Signals are routed in a middle layer

5.2.5 Current sensing

RC filter at SLx and CSNx is not preferred and hence must be done with care. Resistors *R*1 and *R*2 as shown in Figure 72 introduce unexpected voltage drops due to amplifier bias current and/or gate driver current, which affect the R_{SHUNT} current sensing accuracy. *R*1 also limits the current of low-side (LS) gate driver and acts in fact as a R_g resistor. A parallel capacitor (*C*1 as shown below) between SLx and CSNx can be used. This can increase switching noise during MOSFET switching, at the same time improve steady state value. Larger capacitor values will accentuate this effect. Depending on application this value can be adjusted. The parallel capacitor should be close to the SLx and CSNx inputs pins on PCB and values between 100 pF to 1 nF can be a good starting point.

It is strongly recommended to use RC filter between current sense amplifier outputs (CSOx) and the ADC inputs in the MCU. Typical cut off frequency of 1 MHz can be a good compromise between filtering capability and dynamic behavior, but the user must decide depending on overall performance target.

Kelvin connection of shunt resistor is highly recommended as shown in Figure 71. Traces of SLx and CSNx are routed in a middle layer in this case and covered with solid ground planes.

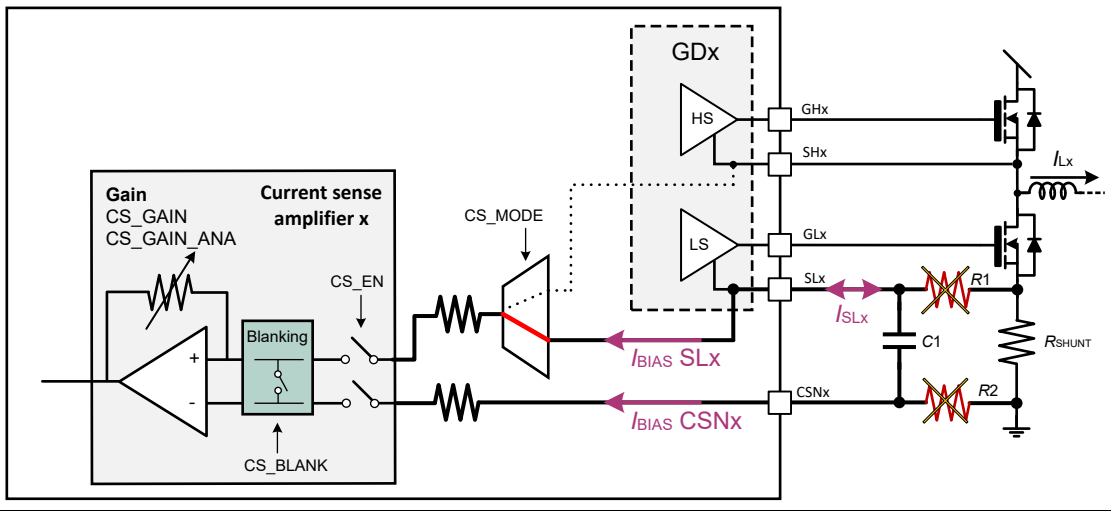

Figure 72 Current sense amplifier input filtering

5.3 Typical applications

Hall sensors can be directly connected to 6EDL7151 inputs INLA, INLB and INLC. An example configuration of this solution is presented in Figure 73. In this case, 6EDL7151 is configured to 1PWM mode with Hall sensors for trapezoidal control. A signal “Direction” is generated by MCU GPIO to change the motor turning direction. SPI interface allows the programming of 6EDL7151. MCU supply voltage DVDD is set to 5 V by using the R_{SENSE} resistor.

Figure 74 shows an alternative application with 6PWM mode. It illustrates a typical sensorless control for BLDC motors. DVDD is programmed via OTP configuration (SPI register) and can be configured to either 3.3 V or 5 V. All three integrated current sense amplifiers are used and their outputs are connected to MCU to measure the current flowing through the shunt resistors for proper motor control. The nFAULT signal reports any malfunction occurring in 6EDL7151 and MCU can brake the motor by pulling down the nBRAKE pin when necessary.

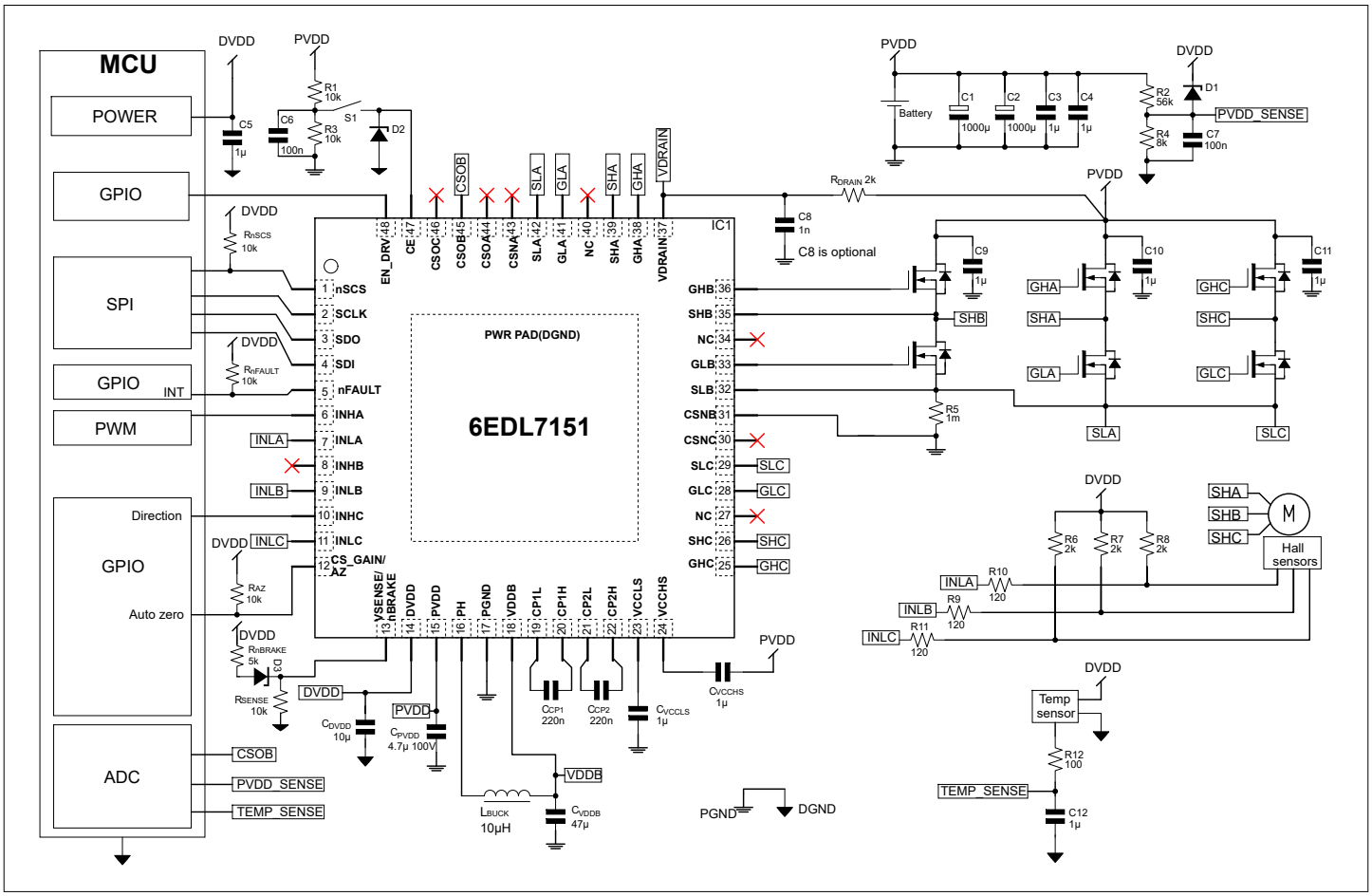

Figure 73 Example schematic for trapezoidal control of BLDC motors using 1PWM mode with Hall sensors and single shunt current measurement

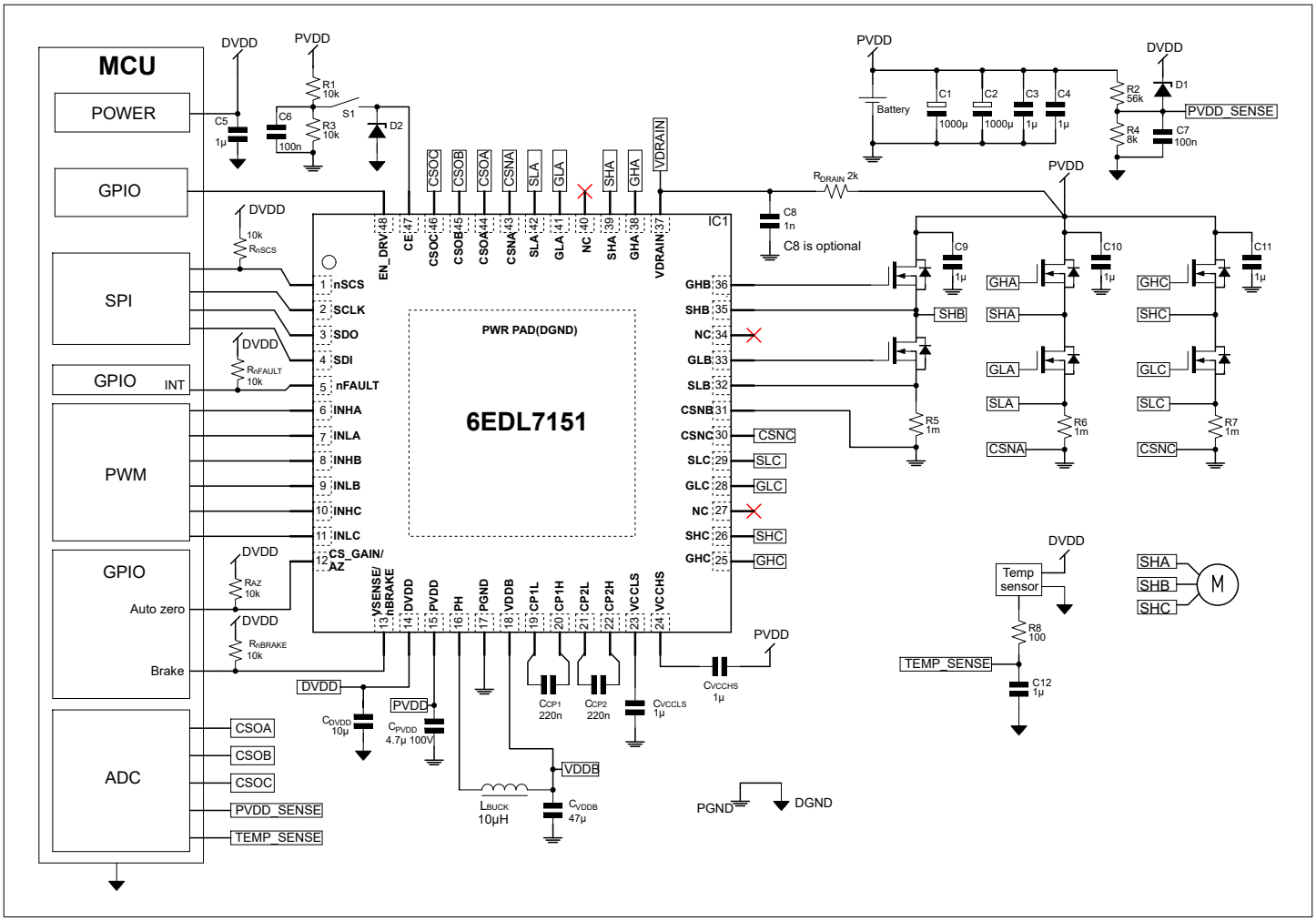

Figure 74 Example schematic for sensorless control of BLDC motors using 6PWM mode and three-shunt current measurement

6 ESD protection and pin diagram

The following diagrams show the ESD protections and internal diagrams of different pins.

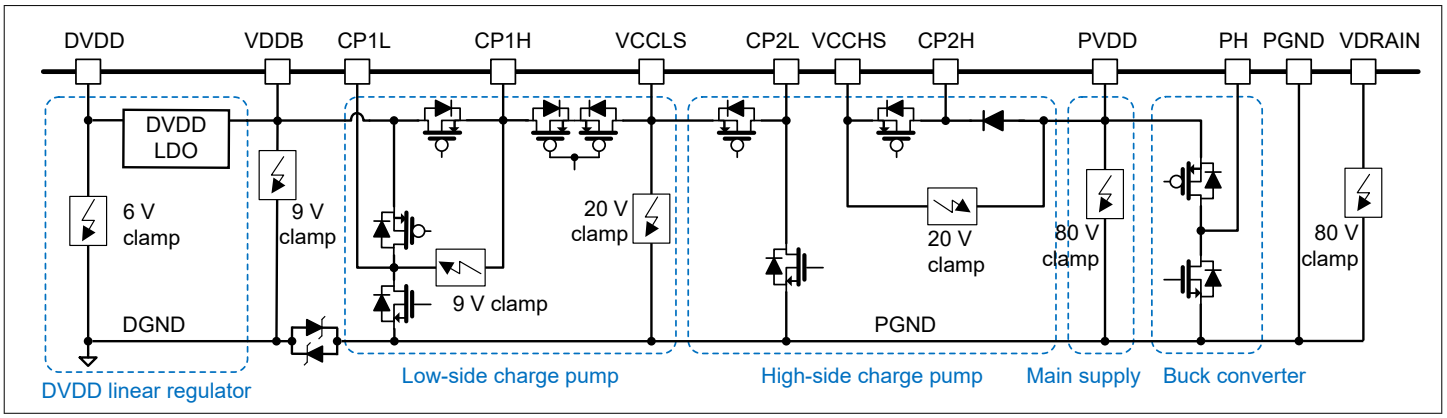

Figure 75 ESD protection diagram for power supply related pins

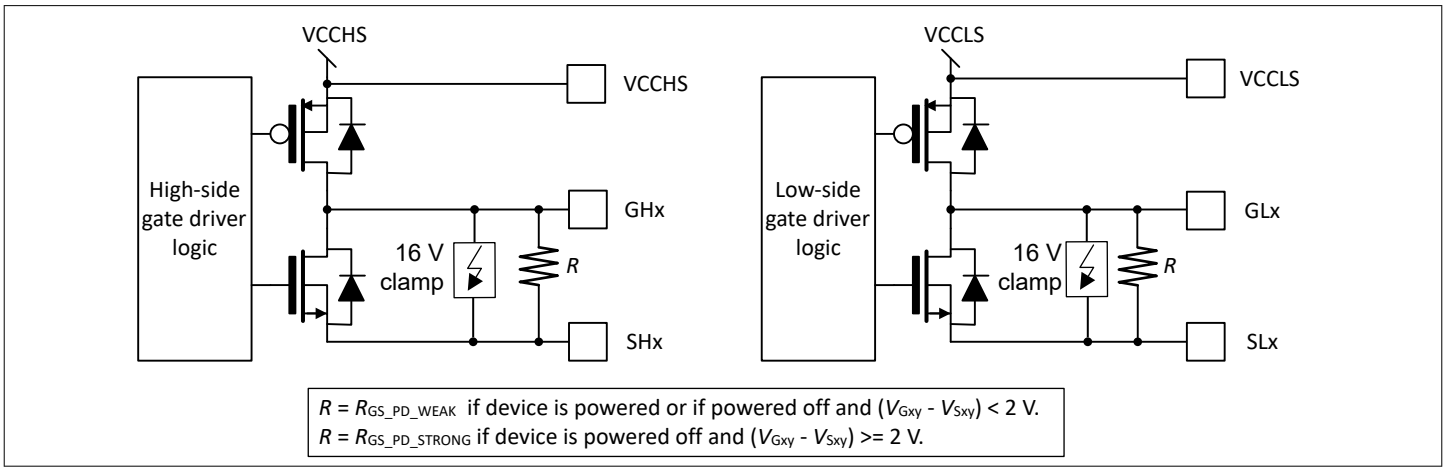

Figure 76 Pin diagram for gate driver output pins

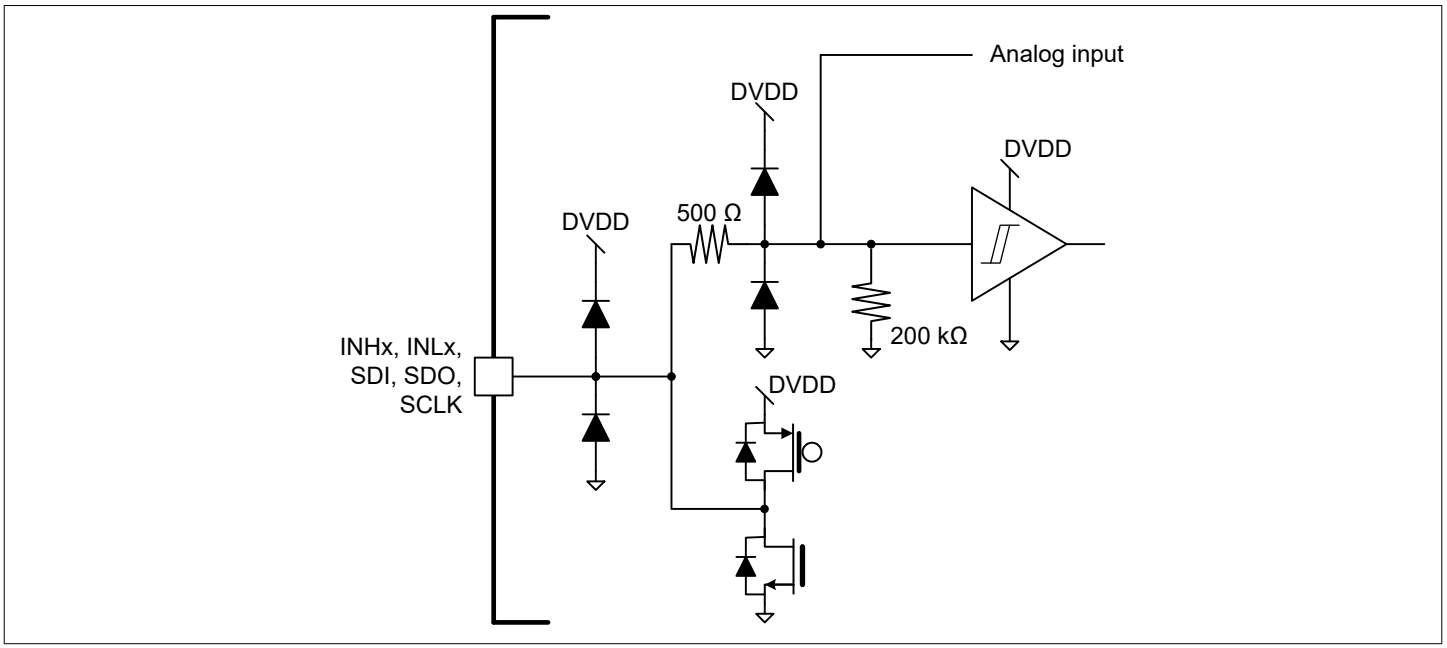

Figure 77 ESD protection and pin diagram for digital pins active high

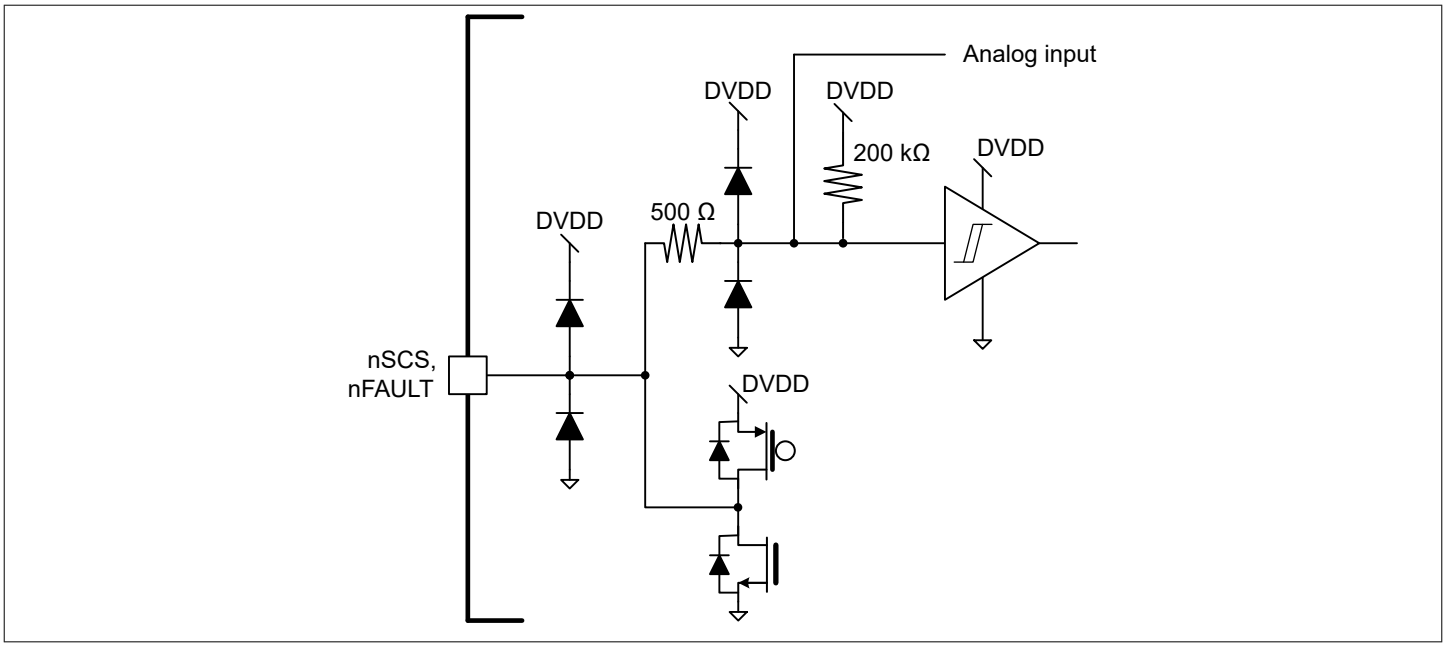

Figure 78 ESD protection and pin diagram for digital pins active low

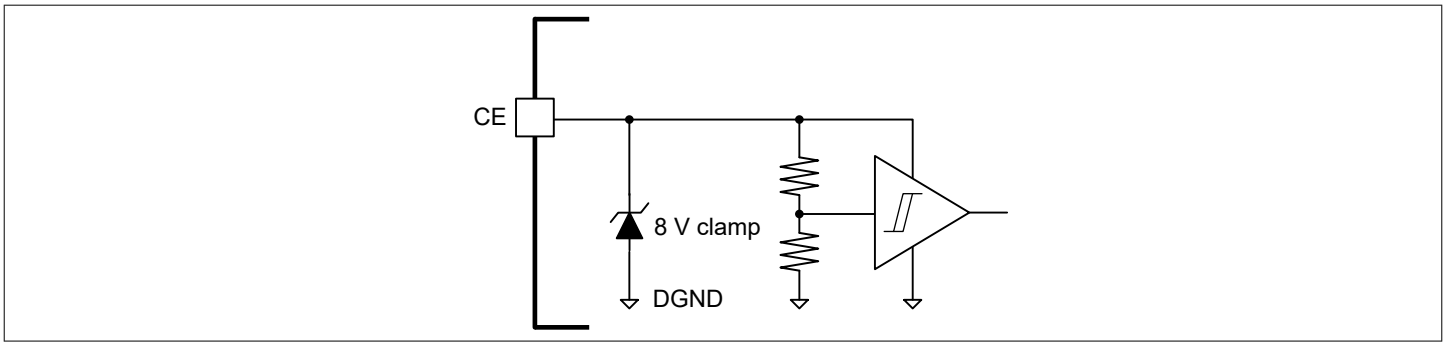

Figure 79 ESD protection and pin diagram for CE pin

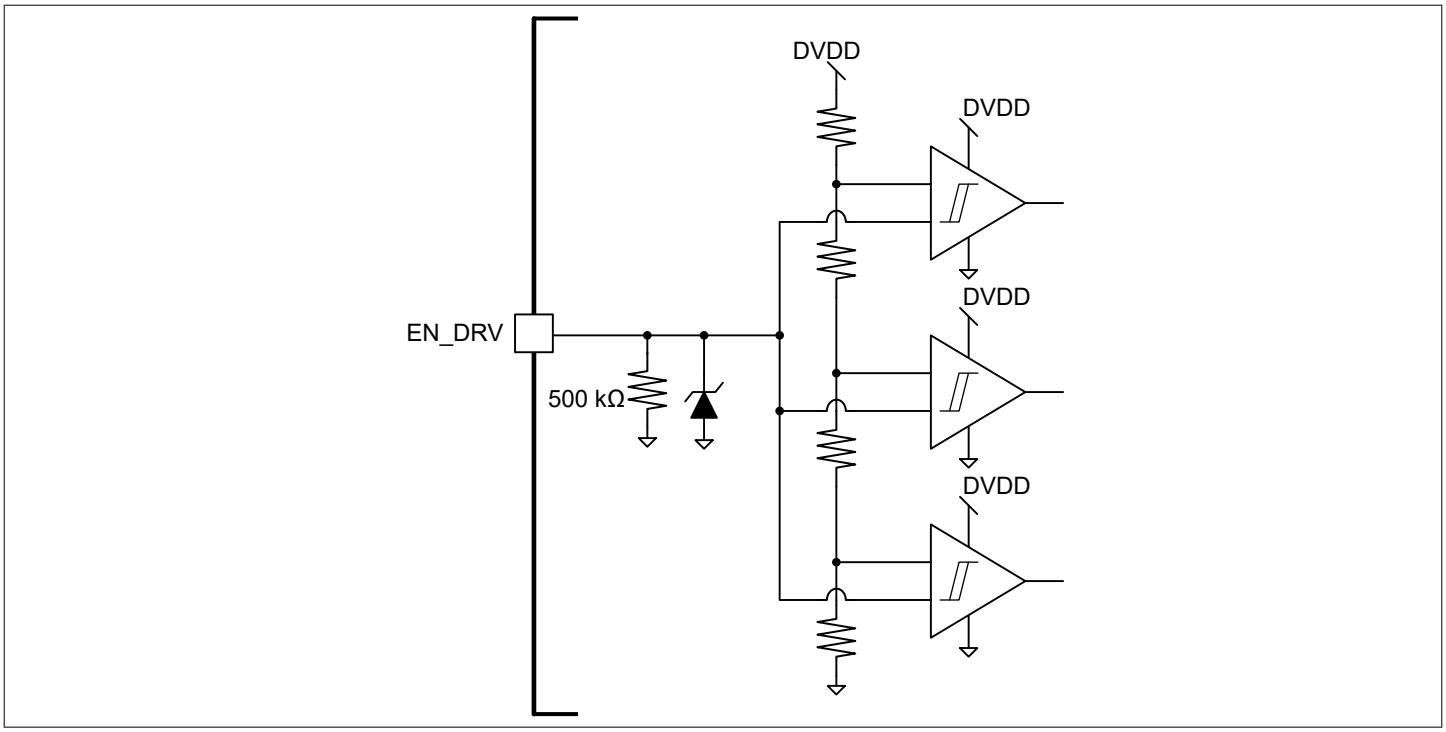

Figure 80 ESD protection and pin diagram for EN_DRV pin

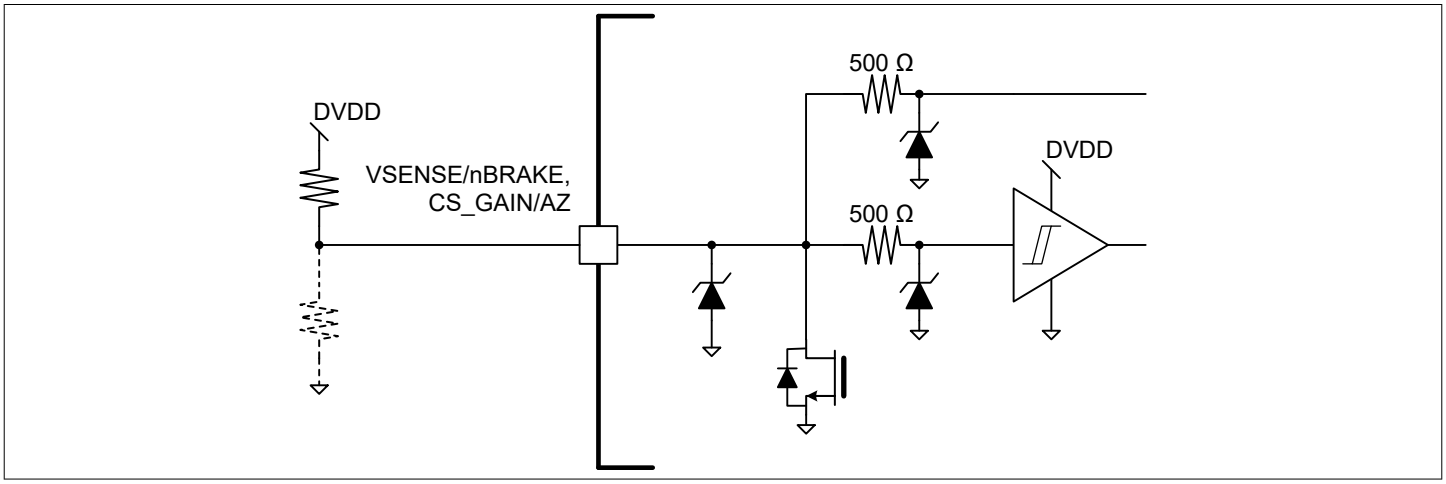

Figure 81 ESD protection and pin diagram for VSENSE/nBRAKE and CS_GAIN/AZ pins

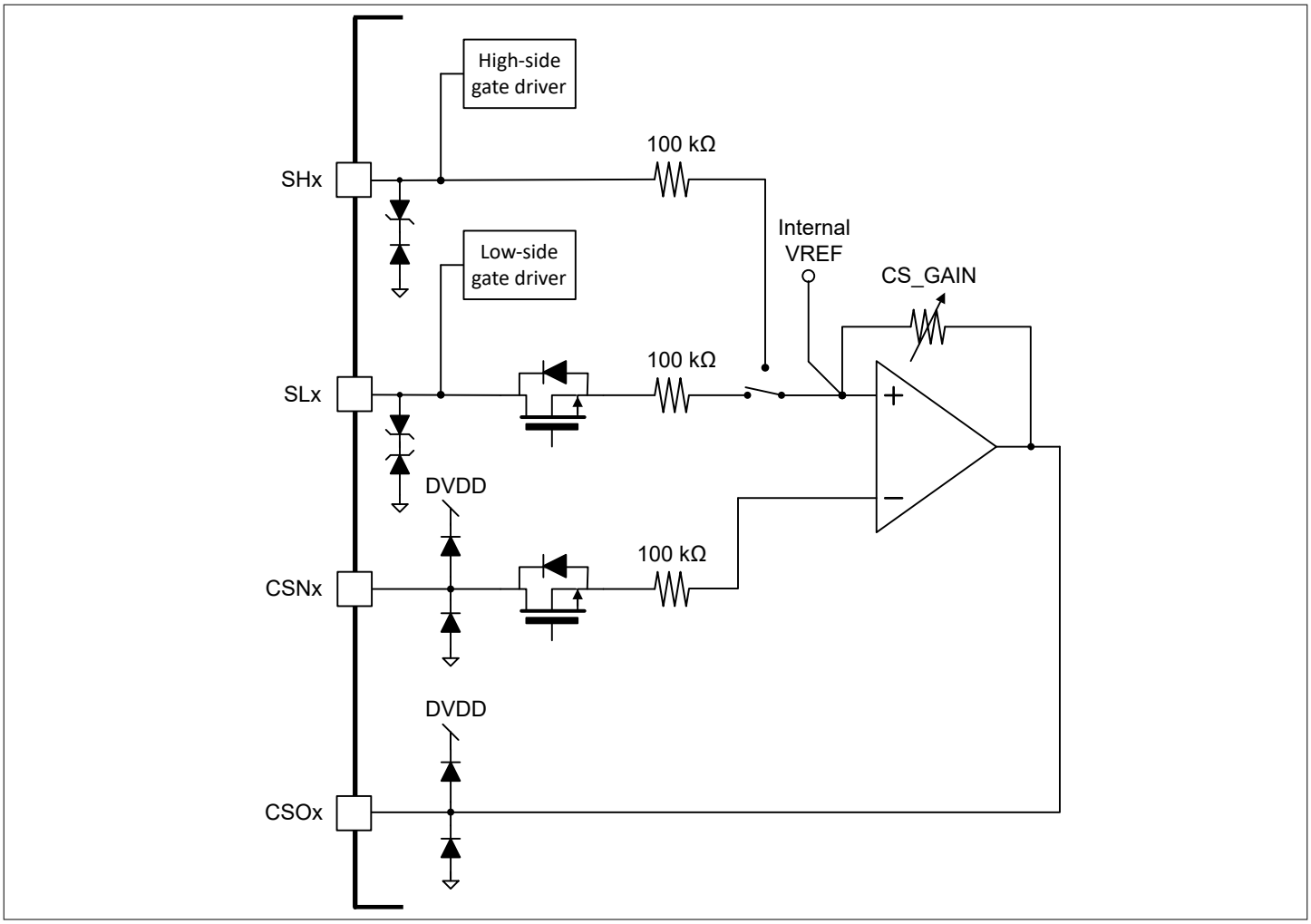

Figure 82 ESD protection and pin diagram for current sense amplifier related pins

7 Package information

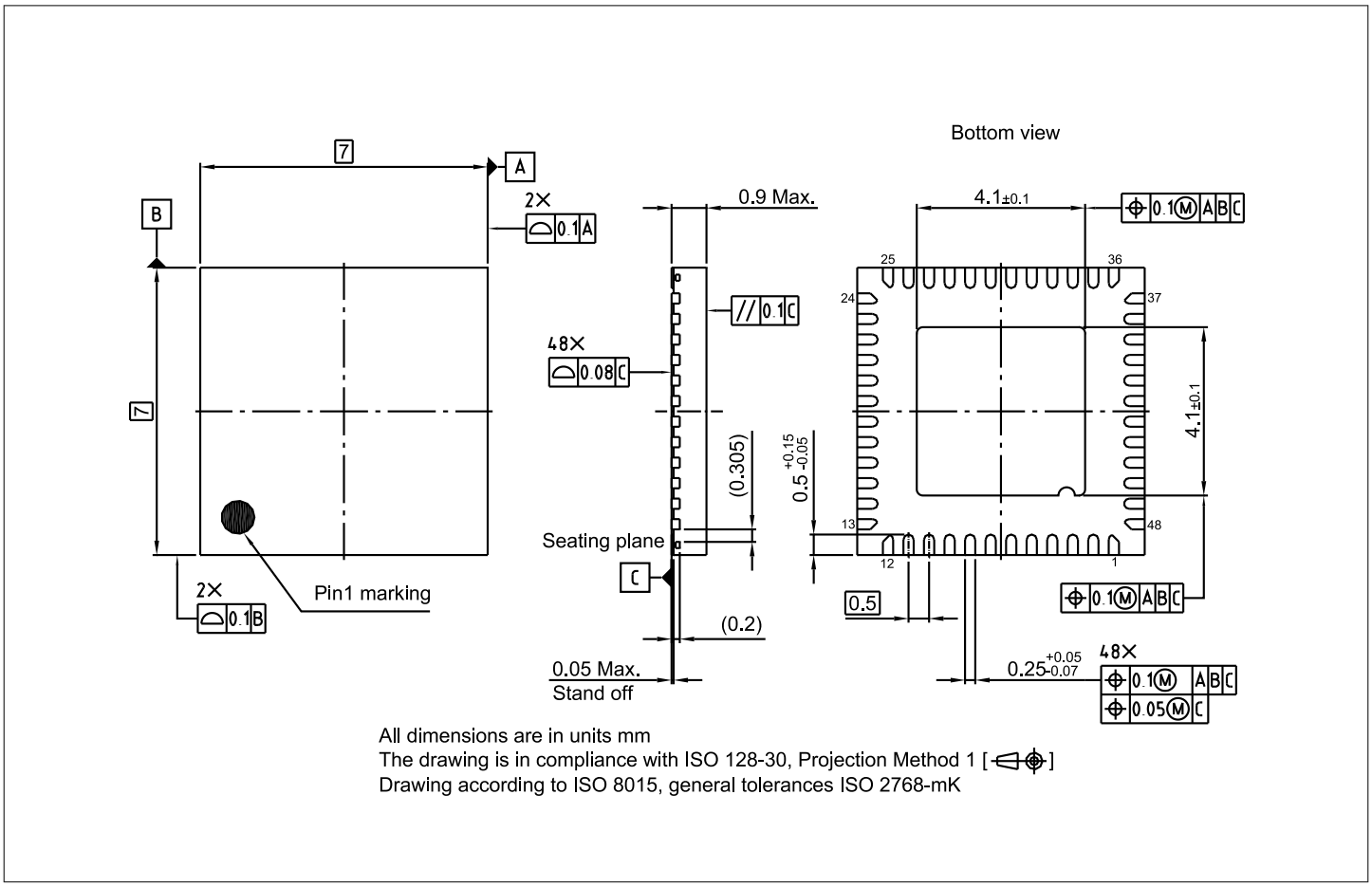

Figure 83 PG-VQFN-48-78 package outline

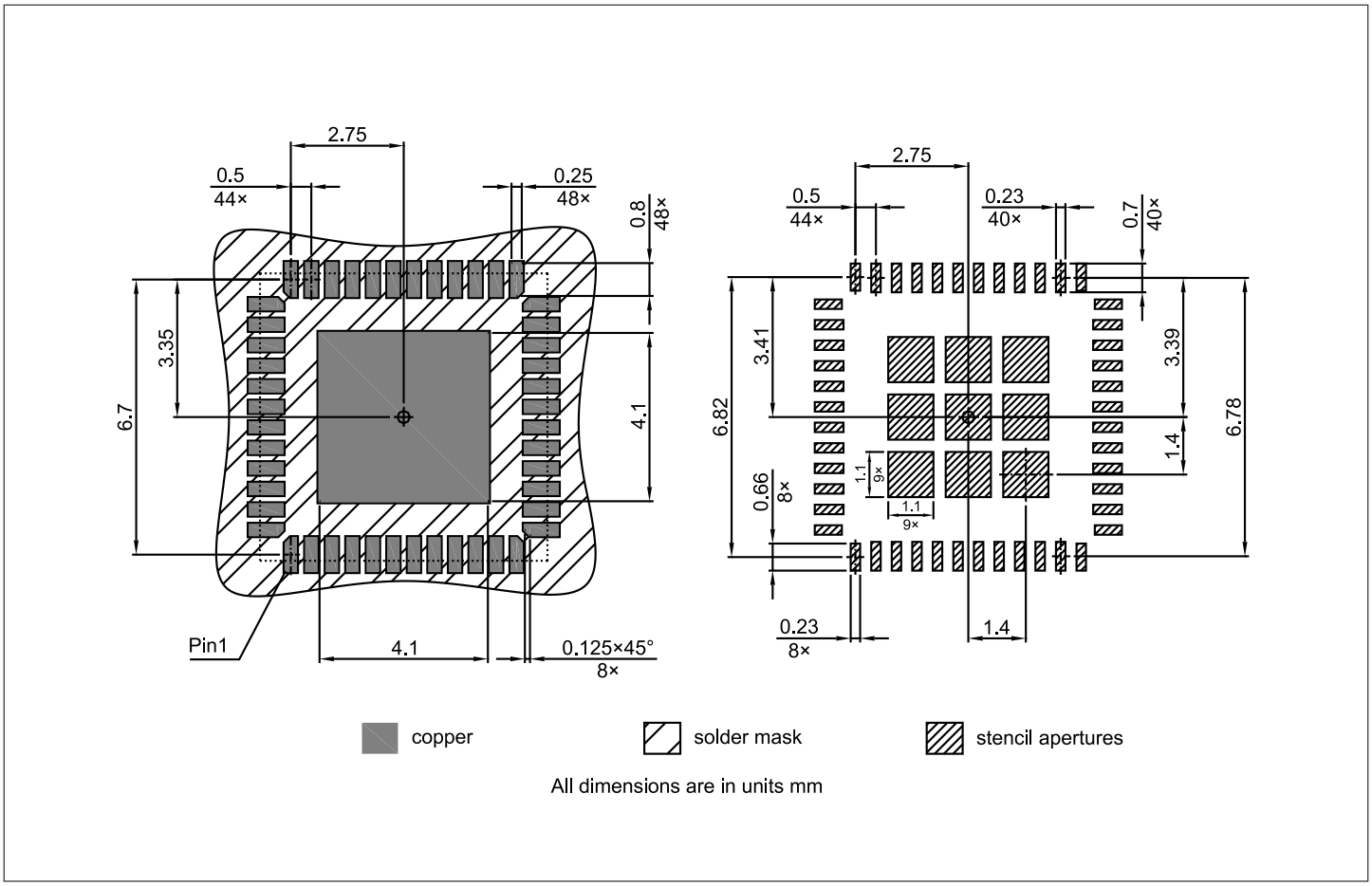

Figure 84 PG-VQFN-48-78 PCB footprint dimensions

Green product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

8 Revision history

Revision	Date	Changes
1.0	2024-05-28	Initial release

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Edition 2024-05-28

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

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Document reference
IFX-bux1710506559272

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