A large, light blue decorative graphic consisting of a thick, curved line that forms a partial circle, with a small circle at its top end, is centered on the page.

Thermal Resistance Calculation

Application Note AN077

Revision: Rev. 2.0
2013-10-01

Edition 2013-10-01

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2014 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Application Note AN077
Revision History: 2013-10-01
Previous Revision: Rev. 1.0

Page	Subjects (major changes since last revision)
All	This Application Note replaces the revision from 2007-01-08.
All	The AN has been revised completely.

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2011-11-11

Thermal Resistance Definition

Table of Content

1 Thermal Resistance Definition.....5
 2 Thermal Resistance of Transistors and Diodes in SMD Packages.....6
 2.1 Permissible Total Power Dissipation in Continuous Operation.....9
 2.2 Permissible Total Power Dissipation in Pulse Operation 11

List of Figures

Figure 1 Static Thermal Equivalent Circuit5
 Figure 2 Gull-wing (or J-lead) Package on Substrate (pc board) 6
 Figure 3 Static Equivalent Circuit of Thermal Resistance 6
 Figure 4 Estimated thermal resistance between soldering point and ambient for a typical PCB..... 8
 Figure 5 Example for Total Power Dissipation $P_{tot} = f(T_S; T_A^{(1)})$ 10
 Figure 6 Example for Forward Current $I_F = f(T_S; T_A^{(1)})$ 10
 Figure 7 Pulse Load Thermal Resistance $R_{thJS} = f(t_p)$ 12
 Figure 8 Pulse Load Permissible Total Power Dissipation $P_{totmax} / P_{totDC} = f(t_p)$ 12

List of Tables

Table 1 Abbreviations of Thermal Resistances 7

1 Thermal Resistance Definition

A thermal equivalent circuit is a behavior model to describe the heat transportation between various locations. A static thermal equivalent circuit is analog to an electrical circuit. A static thermal equivalent circuit usually consists of the following elements:

- heat source P_V (analog to current source in a electrical circuit), where the heat is generated with the unit watt (W),
- temperature T (analog to the potential in a electrical circuit) with the unit Kelvin (K),
- thermal resistance R_{th} (analog to ohmic resistance in a electrical circuit) with the unit (K/W).

The thermal resistance describes the thermal conductivity of a thermal media between two locations.

Figure 1 shows a static thermal equivalent circuit that heat P_V is generated in a thermal conductive material (represented by its temperature of T_J and thermal resistance R_{th}) and dissipated to the environment with ambient temperature of T_a . The relationship between the elements can be written as following:

$$T_J - T_A = P_V \cdot R_{th}$$

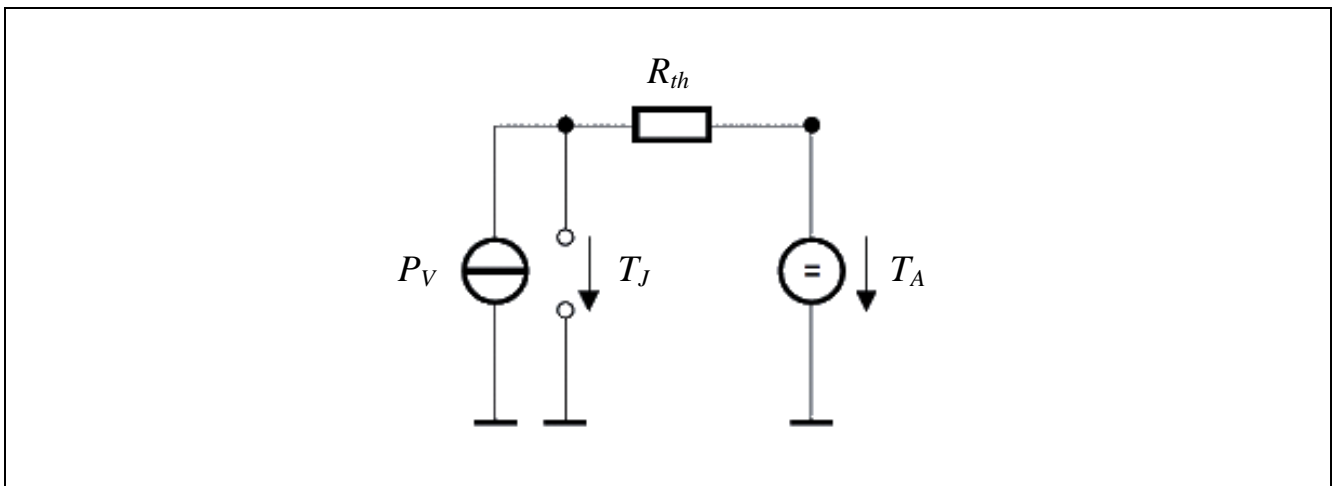


Figure 1 Static Thermal Equivalent Circuit

2 Thermal Resistance of Transistors and Diodes in SMD Packages

Figure 2 shows a general thermal case for packaged devices such as transistors and diodes soldered on PCB. The heat caused by the power dissipation P_{tot} in the active region of a semiconductor device during operation results in an increased temperature of the component. A general equivalent circuit is presented by **Figure 3**.

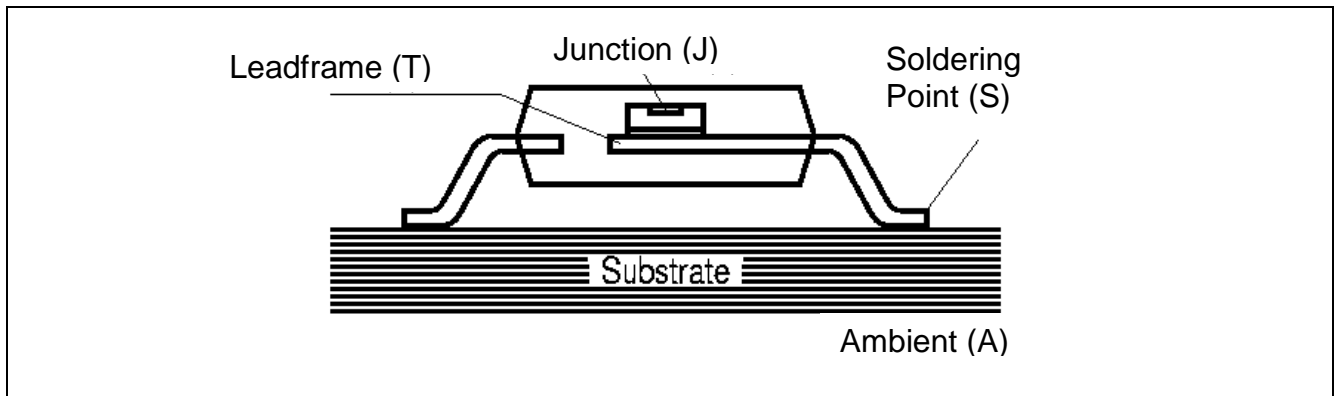


Figure 2 Gull-wing (or J-lead) Package on Substrate (e.g. PCB)

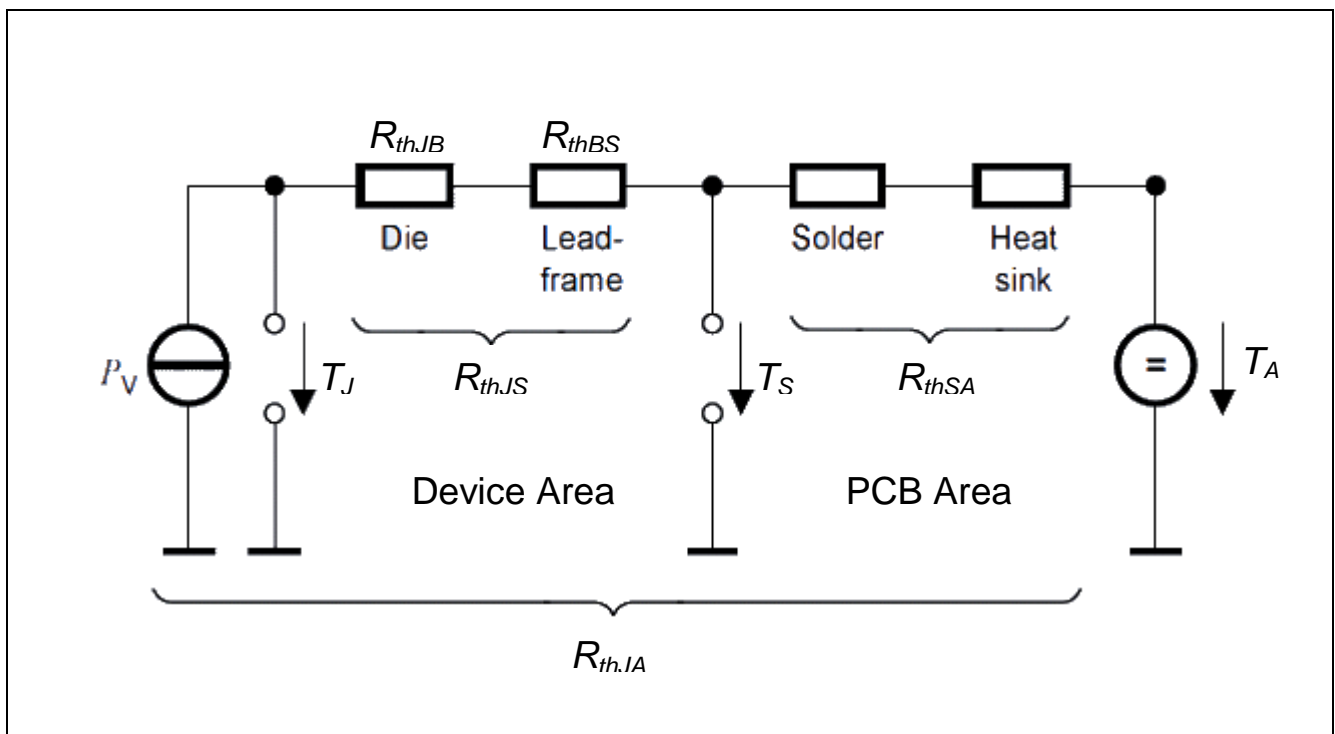


Figure 3 Static Equivalent Circuit of Thermal Resistance

The heat is conducted from its source (junction J or channel Ch) through the chip, along the package leadframes, the soldering Point S and through the substrate (PCB) to the heat sink (ambient A). The junction temperature T_J for a given ambient temperature T_A is determined by the thermal resistance R_{thJA} and the power dissipation P_{tot}

$$T_J = T_A + P_{tot} * R_{thJA}$$

(with R_{thJA} in K/W or °C/W)

In SMD packages the heat is primarily conducted via the leads to the external pins respectively soldering points. The total thermal resistance consists of the following components:

$$R_{thJA} = R_{thJS} + R_{thSA}$$

with

$$R_{thJS} = R_{thJB} + R_{thBS}$$

Table 1 Abbreviations of Thermal Resistances

R_{thJA}	Thermal resistance between junction and ambient (total thermal resistance)
R_{thJS}	Thermal resistance between junction and soldering point (e.g. footprint on PCB)
R_{thJB}	Thermal resistance between junction and chip backside (chip thermal resistance)
R_{thBS}	Thermal resistance between chip backside and soldering point (package thermal resistance)
R_{thSA}	Thermal resistance between soldering point and ambient (substrate thermal resistance)

R_{thJS} contains all device internal thermal resistances. Knowing R_{thJS} it is possible to calculate the junction respectively channel temperature T_J for a given power dissipation P_{tot} and soldering point temperature T_S . T_S is the temperature of the hottest soldering point that is measured at the lead on which the chip is assembled.

$$T_J = T_S + P_{tot} * R_{thJS}$$

The temperature of the soldering point T_S in turn depends on the dissipated power P_{tot} , the ambient temperature T_A and the thermal resistance R_{thSA} of the pc board (substrate).

$$T_S = T_A + P_{tot} * R_{thSA}$$

hence

$$T_J = T_A + P_{tot} * (R_{thJS} + R_{thSA})$$

In product datasheets only the R_{thJS} value can be stated, since only this part of the total thermal resistance R_{thJA} is controlled by the device manufacturer.

Estimated R_{thSA} values for different substrate materials as a function of the area of the mounting pad respectively substrate can be found in the both diagrams below, the parameter is $(T_S - T_A)$. Depending on the application, various substrates such as FR4, Rogers, LTCC and Alumina are used. In consumer and wireless applications, FR4 is the major material used as PCB material. It composites several layers of copper and glass-reinforced polymer stacked. FR4 material usually has thermal resistance in the range of 250 to 300 K/W, depending on the total thickness of copper and the via hole placement between the layers (**Figure 4**).

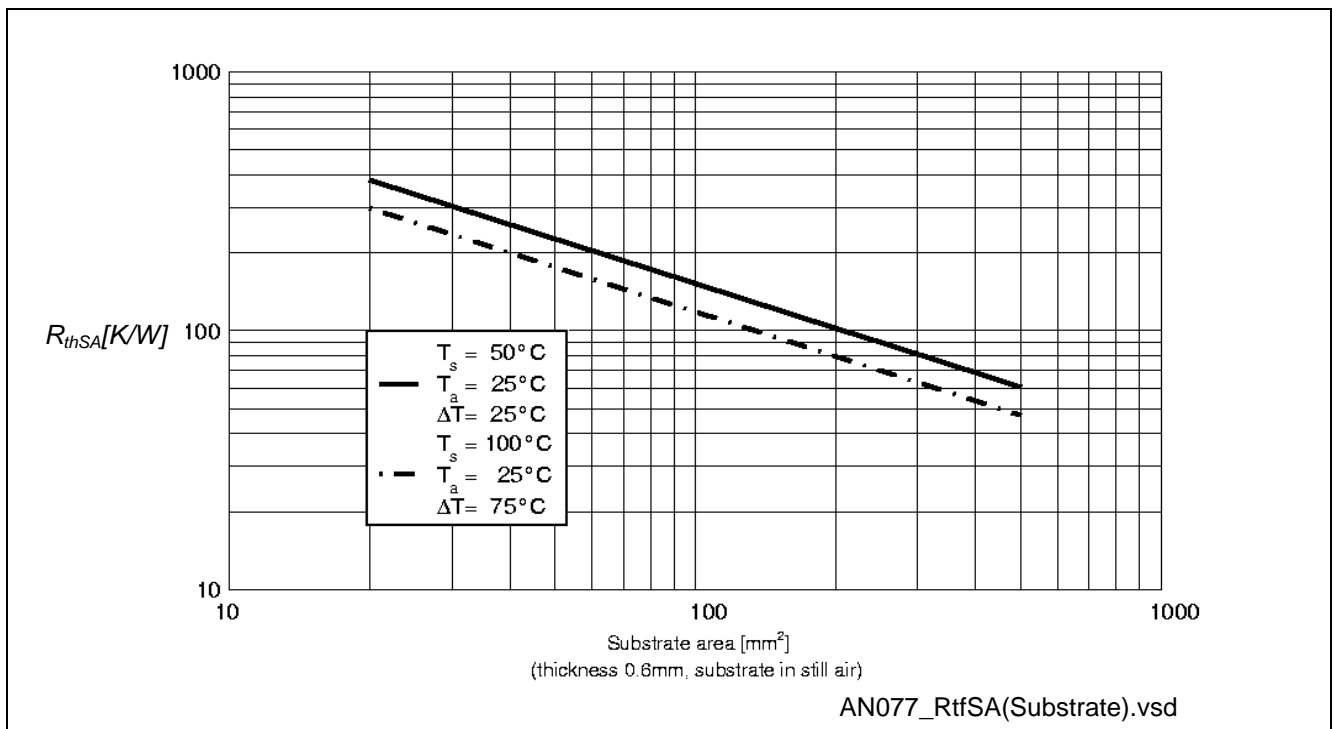


Figure 4 Estimated thermal resistance between soldering point and ambient for a typical PCB

2.1 Permissible Total Power Dissipation in Continuous Operation

In the maximum ratings section of product datasheets the maximum permissible total power dissipation P_{totmax} is specified. P_{totmax} may only be applied if the maximum junction or channel temperature T_{Jmax} is not exceeded. Otherwise the allowable power dissipation P_{tot} has to be reduced, as shown in a so called derating curve. In the example of **Figure 5** up to a soldering point temperature T_{Smax} of 94 °C the maximum permissible total power dissipation P_{totmax} may be applied, in this case 600 mW. The junction temperature T_{J} is then lower than T_{Jmax} , which is often 150 °C for silicon devices. For higher soldering point temperatures T_{S} the power dissipation P_{tot} has to be reduced according to the derating curve, on each point of the declining curve the junction temperature attains its maximum permissible value T_{Jmax} . The soldering point temperature T_{S} where P_{tot} has to be reduced can be calculated according to

$$T_{\text{Smax}} = T_{\text{Jmax}} - P_{\text{totmax}} \times R_{\text{thJS}}$$

Accordingly the ambient temperature from which the power dissipation P_{tot} has to be reduced calculates according to

$$T_{\text{Amax}} = T_{\text{Jmax}} - P_{\text{totmax}} \times R_{\text{thJA}}$$

In diodes the power dissipation is mainly caused by internal resistances. So the diagram has to be translated into the form $I_{\text{F}} = f(T_{\text{S}}; T_{\text{A}})$, what results in derating curves with a bent shape, see **Figure 6**. Please regard that the derating curves shown in **Figure 5** and **Figure 6** are examples.

Thermal Resistance of Transistors and Diodes in SMD Packages

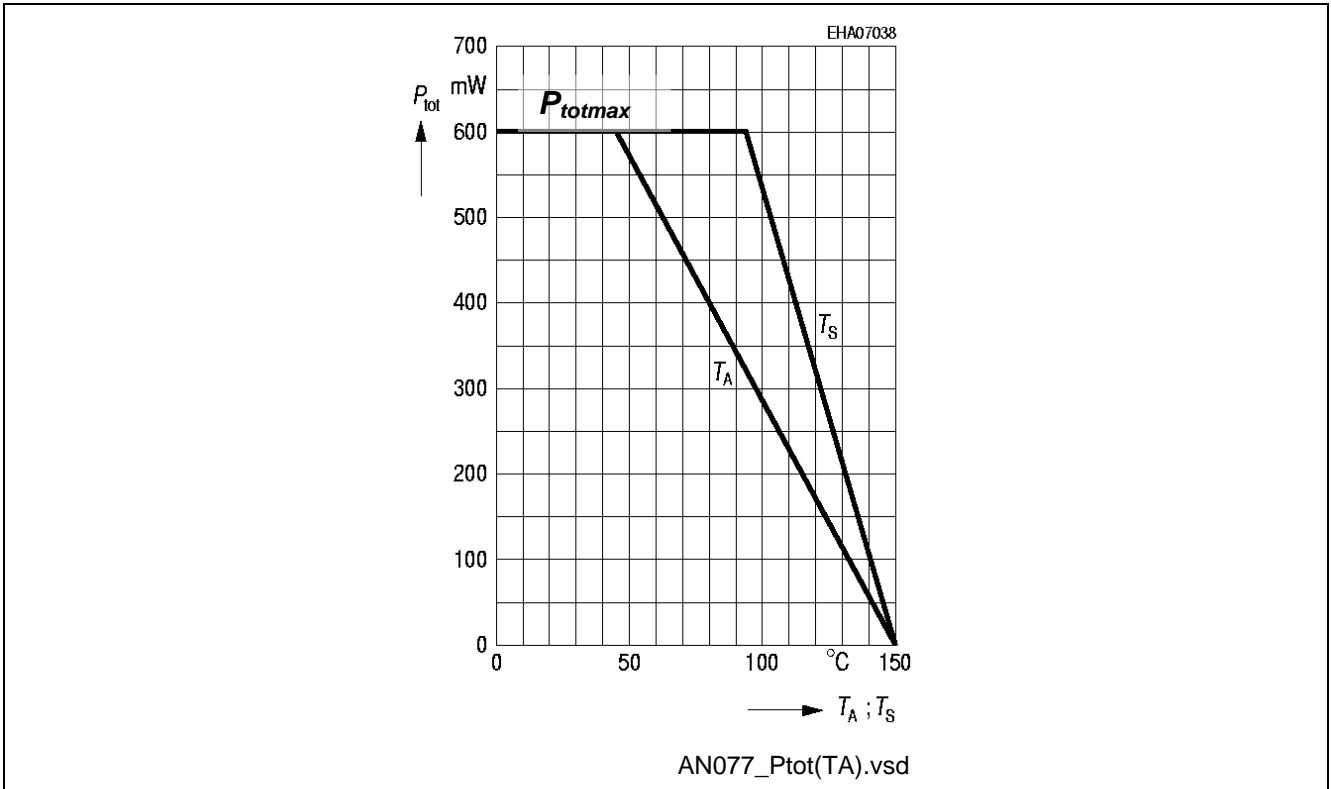


Figure 5 Example for Total Power Dissipation $P_{tot} = f(T_S; T_A^{1})$

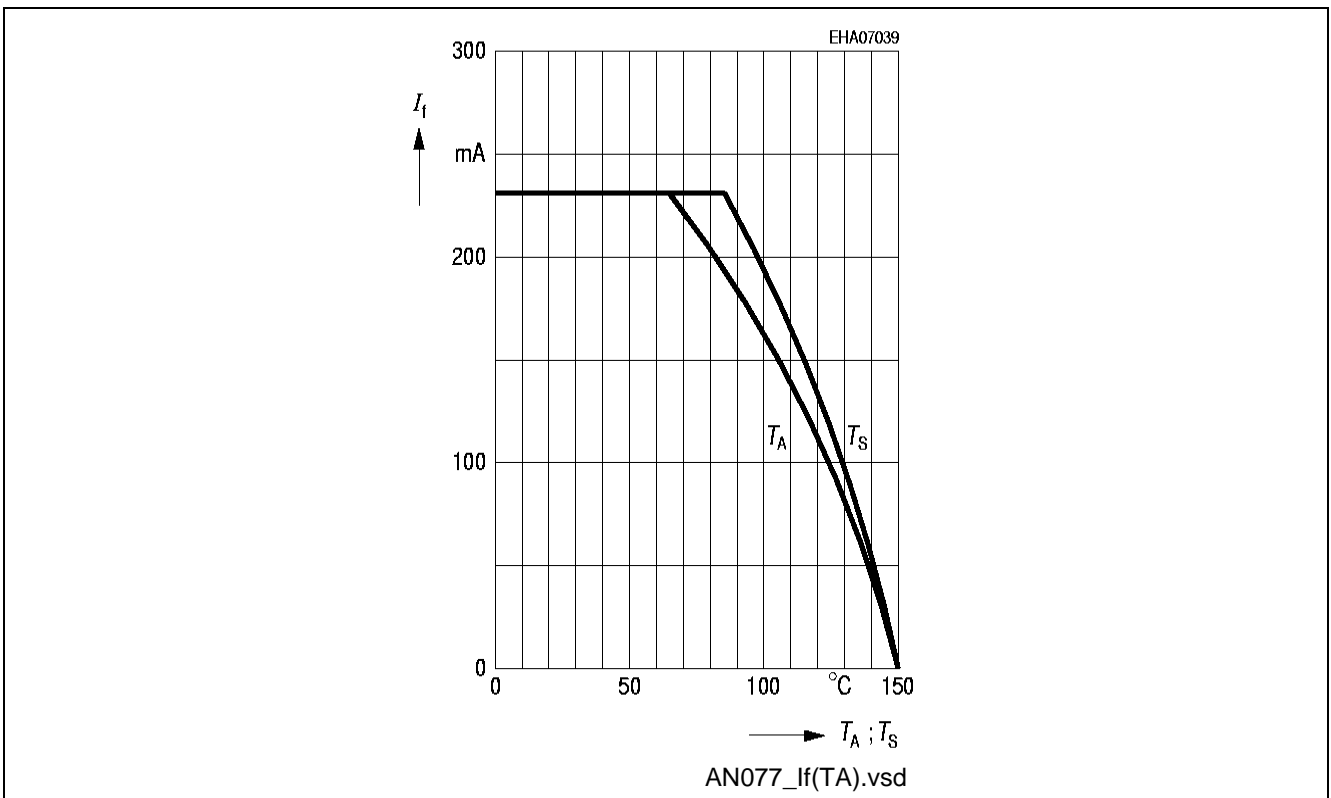


Figure 6 Example for Forward Current $I_F = f(T_S; T_A^{1})$

1) Al_2O_3 -substrate 15 mm x 16.7 mm x 0.7 mm. Package mounted on aluminum 15 mm x 16.7 mm x 0.7 mm

2.2 Permissible Total Power Dissipation in Pulse Operation

In pulse operation under certain circumstances higher total power dissipation can be permitted as in continuous operation. This is the case if the pulse duration t_p , i.e. the length of time interval where the power is applied, is short compared to the thermal time constant of the system. The thermal time constant, i.e. the time until the static temperature respectively thermal equilibrium is approximately reached, depends on the thermal capacitances and resistances of the component and the substrate. The higher permissible total power dissipation in pulse load operation can also be understood as a smaller thermal resistance. **Figure 7** shows an example of a pulse load thermal resistance versus pulse duration t_p , **Figure 8** an example for a pulse load permissible total power dissipation (normalized to its continuous value) versus pulse duration t_p . In these charts T is the duration of a full signal cycle, that is ON + OFF time.

For more detailed information about thermal resistance of semiconductor devices please refer Infineon's online white paper for thermal resistance: [Thermal Resistance Theory and Practice](#).

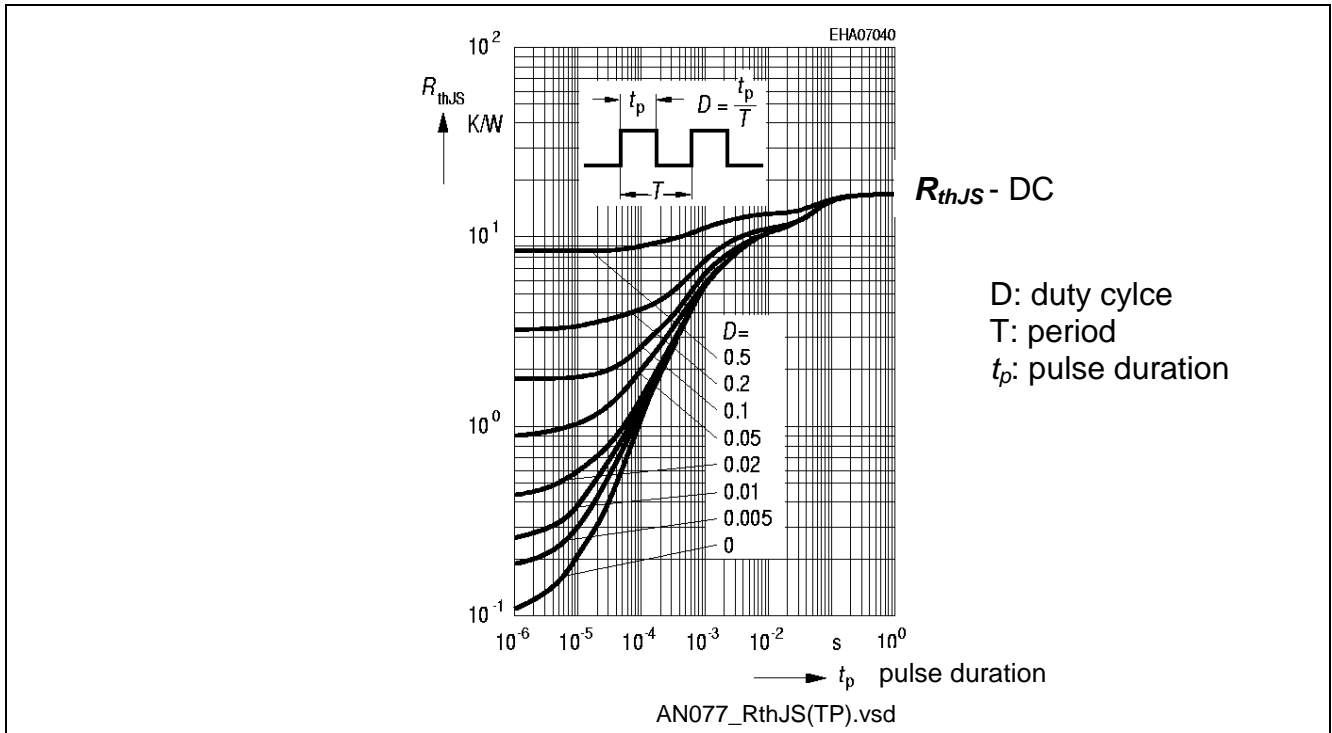


Figure 7 Pulse Load Thermal Resistance $R_{thJS} = f(t_p)$

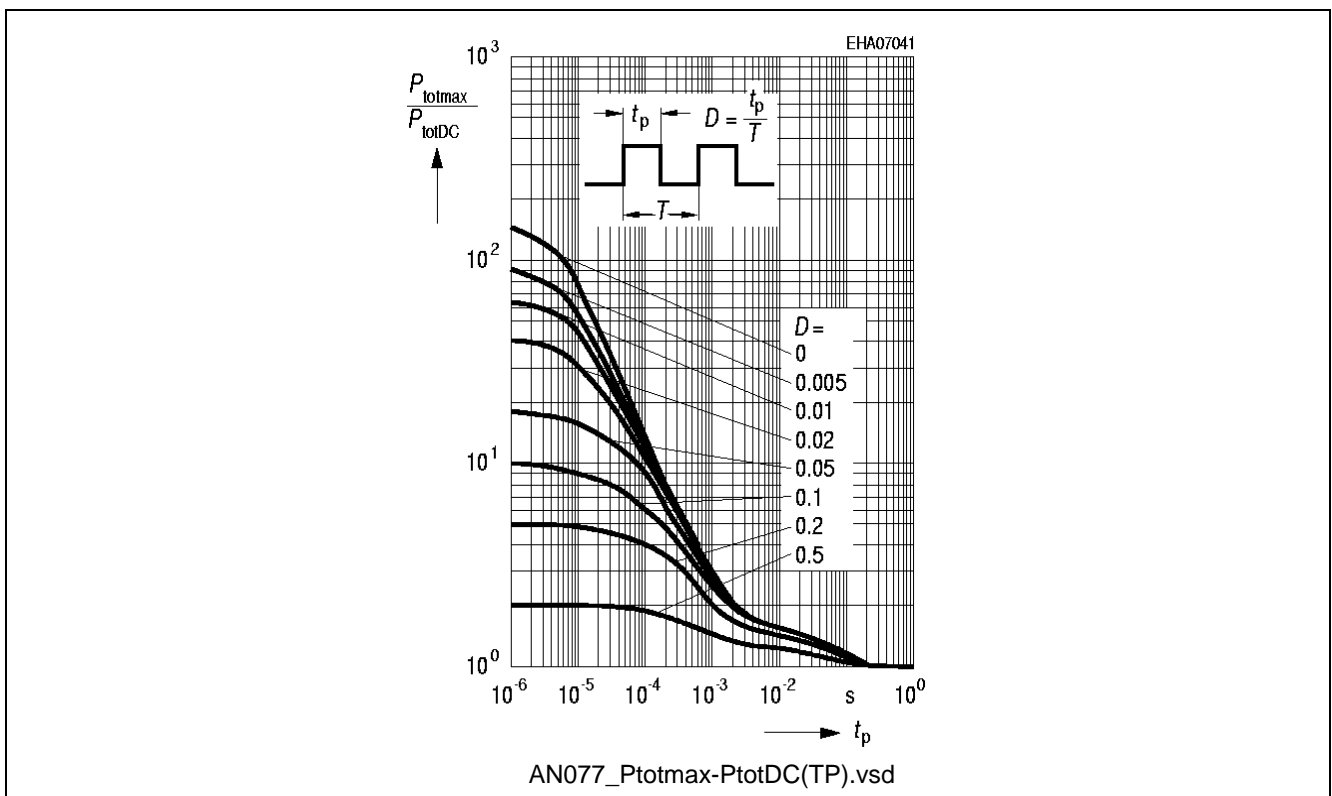


Figure 8 Pulse Load Permissible Total Power Dissipation $P_{totmax} / P_{totDC} = f(t_p)$

www.infineon.com