Replacing SRAM with FM1608B, FM16W08, FM1808B, or FM18W08

About this document

Scope and purpose

AN100 provides the design considerations for replacing battery-backed SRAMs with FM1608B/FM16W08/FM1808B/FM18W08 F-RAM devices.

Intended audience

It is intended for users who plan to use FM1608B, FM16W08, FM1808B, or FM18W08 as a replacement for SRAM.

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1 Introduction

Designs that require both nonvolatility through power-down events and the fast random access of SRAMs will often include batteries to hold the SRAM V_{DD} level up when system power is lost. Infineon offers a range of F-RAM and nvSRAM devices in different densities that are pin-compatible with industry-standard SRAMs and which solve this problem without requiring batteries. These two technologies, F-RAM and nvSRAM, have different values and characteristics.

This application note highlights the design considerations that you need to review when replacing an SRAM plus battery design with the F-RAM products FM1608B/FM16W08 (64-Kbit (8K x 8)) and FM1808B/FM18W08 (256-Kbit (32K x 8)).

2 Parallel F-RAM Design Considerations

2.1 Memory Access

SRAMs and these F-RAM devices begin each read/write cycle with a new address being driven before the chip-enable transitions LOW. For subsequent memory accesses, SRAMs allow the $\overline{CE}$ to remain LOW while the address bus changes. These four F-RAM devices, FM1608B, FM16W08, FM1808B, and FM18W08, do not allow this signaling. Every F-RAM memory access requires a falling edge of $\overline{CE}$, and therefore the $\overline{CE}$ pin cannot be held LOW as in an SRAM device. The $\overline{CE}$ must be toggled HIGH to LOW to latch each new address and it must be HIGH for the specified pre-charge period after the access.

Note: *This is applicable only to FM1608B, FM16W08, FM1808B, and FM18W08 devices. Other parallel F-RAM devices do not have this design constraint.*

If you are modifying the existing design to use one of these F-RAM devices, you must check the memory controller's timing compatibility to generate the needed $\overline{CE}$ and the address timing. Each memory access requires a LOW transition of $\overline{CE}$. In many cases, this is the only change required. **Figure 1** shows an example of F-RAM signal relationships. **Figure 2** shows a common SRAM signal relationship that will not work for these F-RAM devices.

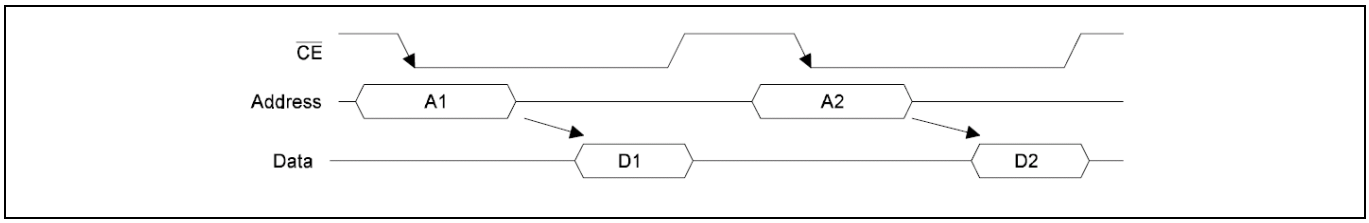

Figure 1 Valid Memory Read Relationship (F-RAM Signaling)

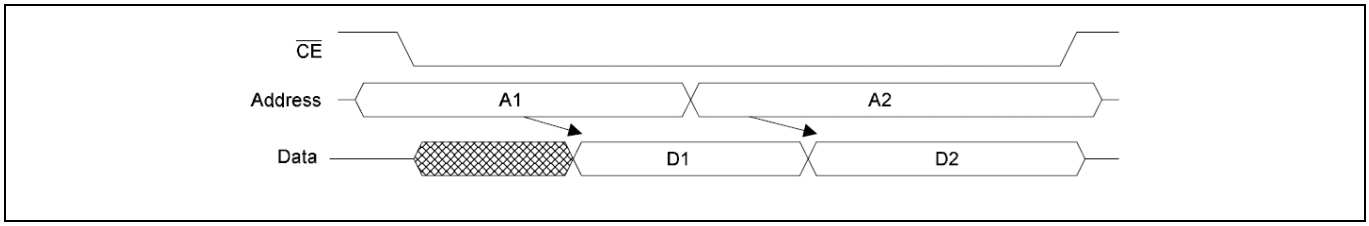

Figure 2 Invalid Memory Read Relationship (SRAM Signaling)

2.2 Confirm Power Supply Level

A second design consideration relates to the level of V_{DD} during device operation. Battery-backed SRAMs typically include a controller that monitors V_{DD} so the switch between V_{DD} and the battery happens as needed. Battery-backed SRAM devices typically block user access below a certain V_{DD} level to minimize the battery drain from an otherwise active SRAM. Therefore, in a power-down situation, you may be abruptly cut off from access to the memory without any warning. F-RAM memories do not need this system overhead. The memory will not block access at any V_{DD} level. However, you must prevent the processor from accessing the memory when V_{DD} is out of tolerance. Refer to the minimum and maximum V_{DD} specifications provided in the F-RAM datasheet. The common design practice of holding a processor in reset when V_{DD} drops is sufficient. You do not have to make any special provision for F-RAM designs.

3 Summary

This application note provides design consideration for memory access when you replace battery-backed SRAMs with FM1608B/FM16W08/FM1808B/FM18W08 F-RAM devices. It also explains the benefit of F-RAM which removes the V_{DD} monitoring overhead in battery-backed SRAM systems.

Revision history

Document version	Date of release	Description of changes
**	2013-06-07	New Spec.
*A	2014-03-18	Updated the application note w.r.t battery-backed SRAM applications
*B	2016-06-02	Updated to new template.
*C	2017-08-17	Updated logo and copyright.
*D	2021-05-26	Migrated to IFX template.

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