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AN201241

S25FL-A to S25FL-P Migration Guide

Author: Doug Kearns

This application note discusses the specification differences that must be considered when migrating from the obsolete S25FL-A devices to a S25FL-P Serial Peripheral Interface (SPI) NOR Flash family made on the Cypress 90-nm MirrorBit process in existing designs.

1 Introduction

The S25FL-A Serial Peripheral Interface (SPI) NOR Flash family made on the Cypress 200 nm MirrorBit® process is obsolete. The S25FL-P Serial Peripheral Interface (SPI) NOR Flash family made on the Cypress 90 nm MirrorBit process is a suitable replacement. This application note discusses the specification differences that must be considered when migrating from a S25FL-A to a S25FL-P flash device on an existing design.

2 Feature Comparison

The S25FL-P is a feature enhanced SPI family that supports all legacy features of the S25FL-A SPI family. Table 1 details the feature similarities and differences between the S25FL-A and S25FL-P families. The most significant new feature in the S25FL-P family is the ability to support single, dual, or quad mode reads within the same device. Note that use and enabling of this and of all the additional features supported by the S25FL-P are strictly optional. A S25FL-P device will behave as a single I/O, uniform sector SPI flash device, equivalent to the S25FL-A, unless the additional features are enabled by system software or hardware.

Table 1. Feature Comparison (Sheet 1 of 2)

Feature	S25FL-A	S25FL-P
MirrorBit NOR process technology	200 nm	90 nm
Supply Voltage V_{CC} Range	2.7 – 3.6 V	2.7 – 3.6 V
Operating Temperature Range	–40 to +85·C	–40 to +85·C
Density Options	4, 8, 16, 32, 64 Mbit	32, 64, 128 Mbit
IO Quantity	x1	x1, x2, x4
Clock Speed (Standard Read, Single IO)	33 MHz	40 MHz
Clock Speed (Fast Read, Single IO)	50 Mhz	104 MHz
Boot Parameter Sector Size	4, 12, 16 KB (1)	4 KB (2)(3)
Uniform Sector Size	64 KB	64, 256 KB (4)
Program Page (max)	256 B	256 B
Accelerated Programming	No	Yes (5)
Quad-Page Programming	No	Yes
Erase and Program Status SR Bits	No	Yes
Configuration Register	No	Yes
JEDEC standard two-byte Signature	Yes	Yes
RES single byte legacy Signature	Yes	Yes
Extended RDID Cycles	No	Yes
Common Flash Interface (CFI)	No	Yes
Top-down Fractional Array Protection	Yes	Yes
Bottom-up Fractional Array Protection	No	Yes

Table 1. Feature Comparison (Sheet 2 of 2)

Feature	S25FL-A	S25FL-P
Full Array Program/Erase Lock Capability	No	Yes (6)
One Time Programmable (OTP Region)	No	506 B

Notes

1. *Boot Sectors only available on S25FL040A models "01" & "02".*
2. *Boot Parameter Sectors currently only available on S25FL032P and S25FL064P.*
3. *Up to thirty two (32) 4 KB parameter sectors.*
4. *256 KB Uniform sectors only available on S25FL128P model "01".*
5. *Accelerated Programming via application of 9 V to W#/ACC pin on S25FL-P only.*
6. *Full Array Lock currently only available on S25FL032P and S25FL064P "S" models.*

3 Sector Architecture Comparison

The S25FL-A SPI flash was available with several sector (erase block) architectures. The S25FL040A was available with either a uniform 64 KB sector architecture or boot sector architecture where either the top or bottom 64 KB of the array is made up of six smaller sectors (two 16 KB, two 4 KB, and two 12 KB boot sectors). The S25FL008A, S25FL016A, S25FL032A and S25FL064A were only available with uniform 64 KB sectors.

In comparison, the S25FL032P and S25FL064P devices suitable for S25FL-A replacement support uniform sector architecture emulation as well as a user configurable top or bottom small boot parameter sector partition architecture where the user determines, via a configuration bit (TBPARM), whether the top or bottom 128 KB of the array is subdivided into thirty-two 4 KB parameter sectors. Table 2 details the sector architectural differences.

Table 2. Comparative Bank and Sector Orientation

Model	Erase Block Quantity	Uniform or Boot Parameter Architecture	Erase Block Architecture
S25FL040A-00	8	Uniform	16x64 KB
S25FL040A-01	13	Top Boot	7x64 KB + 2x12 KB + 4x4 KB + 2x16 KB
S25FL040A-02	13	Bottom Boot	2x16 KB + 4x4 KB + 2x12 KB + 7x64 KB
S25FL008A	16	Uniform	16 x 64 KB
S25FL016A	32	Uniform	32 x 64 KB
S25FL032A	64	Uniform	64 x 64 KB
S25FL064A	128	Uniform	128 x 64 KB
S25FL032P	64 or 94 or 94	Uniform or Bottom Boot or Top Boot	64x64 KB or 32x4 KB + 62x64 KB or 62x64 KB + 32x4 KB
S25FL064P	128 or 158 or 158	Uniform or Bottom Boot or Top Boot	128x64 KB or 32x4 KB + 126x64 KB or 126x64 KB + 32x4 KB

In order to facilitate migration from the uniform sector S25FL-A devices to the S25FL-P device family without system software modification, Cypress has restricted the legacy sector erase command, SE (D8h), to erasing only 64 KB aligned erase blocks on the S25FL-P. Cypress has added support for two additional boot parameter sector erase commands, P4E (20h) for erasing individual 4 KB boot parameter sectors, and P8E (40h) for erasing two adjacent 4 KB boot parameter sectors (8 KB address aligned boot partition group). In this way, the S25FL-P flash family when operated with legacy software will operate as a uniform 64 KB sector architecture device family.

In applications where the S25FL-P is to be used as a uniform 64 KB sector device, for example, as a replacement for a uniform sector S25FL-A device, the TBPARM configuration bit would not be programmed to set boot parameter sector location and the new P4E and P8E commands would not be used.

4 Command and Register Comparison

The S25FL-P family was designed to support migration from S25FL-A with minimal software changes. All commands supported by the S25FL-A are supported by the S25FL-P. Several additional commands are supported by the S25FL-P to enable new features. Table 3 provides a support matrix of SPI commands.

Table 3. Software Commands

Command	Description	Code	S25FL-A	S25FL-P
READ	Read Data Bytes	03h		
FAST_READ	High Speed Read Data Bytes	0Bh		
RDID	Read Identification	9Fh		
WREN	Write Enable	06h		
WRDI	Write Disable	04h		
SE	Sector Erase	D8h		(1)
BE	Bulk Erase	C7h		
	Bulk Erase	60h		
PP	Page Program	02h		
RDSR	Read from Status Register	05h		
WRSR	Write to Status Register	01h		
DP	Deep Power-Down (DPD)	B9h		
RES	Release from DPD	ABh		
DOR	Dual Output Read	3Bh		
DIOR	Dual I/O High Performance Fast_Read	BBh		
QOR	Quad Output Read	6Bh		
QIOR	Quad I/O High Performance Fast_Read	EBh		
READ_ID	Read Mfg and Device ID	90h	(2)	
P4E	4 KB Parameter Sector Erase	20h		(1)
P8E	8 KB (2x4 KB) Parameter Sector Erase	40h		(1)
QPP	Quad Page Programming	32h		
RCR	Read Configuration Register	35h		
CLSR	Reset Erase and Program Flag	30h		
OTPP	Program one byte in OTP area	42h		
OTPR	Read data in OTP area	4Bh		

Notes

1. *In S25FL-P, the SE command only erases 64 KB or 256 KB sectors and the P4E and P8E commands enable erasure of 4 KB boot parameter sectors.*
2. *READ_ID command only supported for Top and Bottom boot sector S25FL040A models. Use of JEDEC standard RDID (9Fh) command is recommended.*

When migrating from a uniform sector S25FL-A to a S25FL-P, the only software modifications that may be required relate to device identification. Table 4 provides a RDID (9Fh) returned value matrix for all S25FL-A and S25FL-P devices, which also includes the Electronic Signature Byte returned with the RES (ABh command). If migrating between S25FL-A and S25FL-P devices of the same density, no software modifications to the system software device identification routines are required. When migrating from a smaller density S25FL-A to a S25FL032P, if the application uses the Device ID or Electronic Signature values, system software will require modification if the S25FL032A identification values are not supported in the existing system software.

Table 4. RDID Command (JEDEC 9Fh) Device Identification

Device	Manufacturer ID Byte 0	Device ID Byte 1	Device ID Byte 2	Extended ID Byte 3	Extended ID Byte 4
S25FL040A-00 (Uniform)	01h	02h	12h	N/A	N/A
S25FL040A-01 (Top)	01h	02h	25h	N/A	N/A
S25FL040A (Bottom)	01h	02h	26h	N/A	N/A
S25FL008A	01h	02h	13h	N/A	N/A
S25FL016A	01h	02h	14h	N/A	N/A
S25FL032A	01h	02h	15h	N/A	N/A
S25FL064A	01h	02h	16h	N/A	N/A
S25FL032P	01h	02h	15h	4Dh	Reserved
S25FL064P	01h	02h	16h	4Dh	Reserved
S25FL128P (64 KB sectors)	01h	20h	18h	03h	01h
S25FL128P (256 KB sectors)	01h	20h	18h	03h	00h

Note:
Electronic Signature (RES command ABh) outputs Device ID Byte 2. For S25FL040A, 12h is output for all models.

5 DC and AC Specification Comparison

The S25FL-P family was designed to have DC and AC specifications very similar to the S25FL-A to facilitate migration without modification to system hardware, software, or firmware, e.g. host SPI interface controller timing. Table 5 and Table 6 provide side-by-side comparisons of DC and AC parameter differences, respectively, for single IO applications of the S25FL-A and S25FL-P. Included are comments that indicate the potential for a given S25FL-P specification difference to impact a migration from a S25FL-A device in an existing application. It is advised that customers evaluate the potential impact of any parameter specification difference that has a migration issue severity not equal to "None".

Table 5. DC Parameter Specification Differences

Feature	S25FL-A	S25FL-P	Migration Issue Severity
Output High Voltage V_{OH} (min)	V_{CC} – 0.2 V	V_{CC} – 0.6 V	None
Page Program Current I_{CC2} (max)	28 mA	26 mA	None
Erase Current $I_{CC4,5}$ (max)	24 mA	26 mA	None
I/O Leakage Current (max)	± 1 µA	± 2 µA	None
Standby Current I_{SB} (typ / max)	20 / 50 µA	80 / 200 µA	Low
Deep Power-Down Current I_{PD} (typ / max)	1.5 / 5 µA	3 / 10 µA	Low

The higher Standby Current consumption (I_{SB}) and Deep Power-Down Current consumption (I_{PD}) of the S25FL-P could cause issues when migrating to the S25FL-P from the S25FL-A. If an application requires minimal idle power consumption, the application software should place the SPI flash in Deep Power-Down mode using the Deep Power-Down (DP) command to minimize idle power consumption.

Table 6. AC Parameter Specification Differences

Feature	S25FL-A	S25FL-P	Migration Issue Severity
READ Command Clock (max)	33 MHz (1)	40 MHz	None
Fast Read / other command Clock Frequency (max)	50 Mhz	104 MHz	None
Clock Low Period t_{WH} (min)	9 ns	4.5 ns	None
Clock Low Period t_{WL} (min)	9 ns	4.5 ns	None
CS# Setup to SCK t_{CSS} (min)	5 ns	3 ns	None
CS# Hold from to SCK t_{CSH} (min)	5 ns	3 ns	None
CS# High Time t_{CS} (Read Instruction) (min)	100 ns	10 ns	None
CS# High Time t_{CS} (Program/Erase) (min)	100 ns	50 ns	None
DATA Setup to SCK $t_{SU:DAT}$ (min)	5 ns	3 ns	None
DATA Hold from to SCK $t_{HD:DAT}$ (min)	5 ns	2 ns	None
SCK Low to Output Valid t_V (single output) (max)	10 ns	8 ns	None
HOLD# Setup to SCK t_{HLCH} (min)	5 ns	3 ns	None
HOLD# Hold from to SCK t_{HLHH} (min)	5 ns	3 ns	None
HOLD# enable to Output Invalid t_{HZ} (max)	10 ns	8 ns	None
HOLD# disable to Output Valid t_{LZ} (max)	10 ns	8 ns	None
CS# disable to Deep Power Down t_{DP} (max)	3 µs	10 µs	Low
Write Protect Set Up Time t_{WPS} (min)	15 ns	20 ns	Low
Write Protect Hold Time t_{WPH} (min)	15 ns	100 ns	Medium
Write Status Register Time t_W (max)	150 ns	50 ns	None
Page Program Time t_{PP} (typ / max)	1.5 / 3 ms	1.5 / 3 ms	None
Accelerated Page Program Time t_{EP} (typ / max)	n/a	1.2 / 2.4 ms	None
Sector Erase Time t_{SE} (64 KB sector) (typ / max)	0.5 / 3 s	0.5 / 2 s	None
Bulk Erase Time t_{SE} (32 Mbit (2)) (typ / max)	25 / 192 s	32 / 64 s	None
V_{CC} Power Up to Device Ready t_{PU} (min)	10 ms	300 µs	None

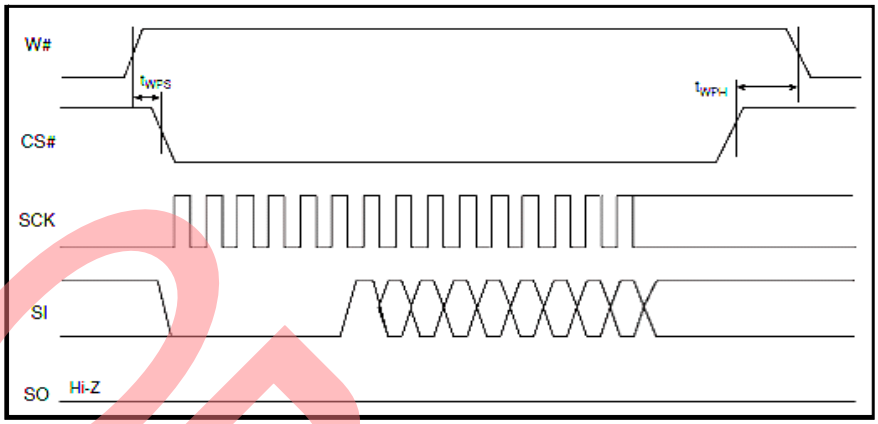
Notes

1. *25 MHz max for S25FL064A.*
2. *Comparison between identical density S25FL032A and S25FL032P.*

The longer transition to Deep Power-Down mode (t_{DP}) from CS# negation of the S25FL-P will not cause migration issues from the S25FL-A. This specification difference will only have a system level impact on those battery powered applications with extreme energy storage constraints that frequently re-enter Deep Power-Down mode. The specification difference ramification is a slightly higher overall power consumption (0.68 mW maximum) for the 7 µs maximum longer transition into Deep Power-Down mode of the S25FL-P versus the S25FL-A.

The longer Write Protect Set Up time (t_{WPS}) of the S25FL-P is unlikely to cause migration issues from the S25FL-A. The longer Write Protect Hold time (t_{WPH}) of the S25FL-P may cause migration issues from the S25FL-A, depending on host SPI and/or GPIO controller timing. Figure 1 depicts the relative W# and CS# inputs edge timing requirements when performing a Write Registers command in the specific case where the device was in and is returning to the Hardware Protected mode (HPM). HPM is entered by setting the Status Register Write Disable bit (SRWD = 1) and asserting W# < Vil. The implication of these specification differences are the W# input must be disabled at least 20 ns prior to CS# assertion initiating a WRR command entry (a 5 ns increase over the S25FL-A) and the W# input must not be asserted for 100 ns following CS# negation concluding a WRR command entry (a 85 ns increase over the S25FL-A). If an application uses the W# and SRWD write protection mode feature, these timing requirements must be verified to avoid issues when migrating to the S25FL-P from the S25FL-A.

Figure 1. Write Protect Setup and Hold Timing During WRR When SRWD = 1



6 Package Options and Recommended Migration Part Numbers

The S25FL-A and S25FL-P devices are made available in a variety of package options. Table 7 provides details of the different package options by SPI flash family and density. Footprint compatible S25FL-P migrations options exist for the majority of S25FL-A devices. Table 8 details the recommended S25FL-P ordering part number (OPN) migration path from all S25FL-A OPNs. All packages are supported in Pb-free plating only.

Table 7. SPI Package Options

Device	SO-8 (150 mil)	SO-8 (208 mil)	USON-8	WSON-8	SO-16
S25FL040A					
S25FL008A					
S25FL016A					
S25FL032A					
S25FL064A					
S25FL032P					
S25FL064P					
S25FL128P					

Table 8. Recommended Model to Model Migrations (Sheet 1 of 2)

S25FL-A Ordering Part Number	Package	Recommended S25FL-P Ordering Part Number	Footprint Compatible
S25FL040A0LM(A,F)I00(0,1,3)	SO-8 (208 mil)	S25FL032P0XMFI01(0,1,3)	Yes
S25FL040A0LM(A,F)I01(0,1,3)	SO-8 (208 mil)	S25FL032P0XMFI01(0,1,3)	Yes
S25FL040A0LM(A,F)I02(0,1,3)	SO-8 (208 mil)	S25FL032P0XMFI01(0,1,3)	Yes
S25FL040A0LN(A,F)I00(0,1,3)	USON-8	S25FL032P0XNFI01(0,1,3)	Yes
S25FL040A0LN(A,F)I01(0,1,3)	USON-8	S25FL032P0XNFI01(0,1,3)	Yes
S25FL040A0LN(A,F)I02(0,1,3)	USON-8	S25FL032P0XNFI01(0,1,3)	Yes
S25FL040A0LV(A,F)I00(0,1,3)	SO-8 (150 mil)	S25FL032P0XMFI01(0,1,3)	No

Table 8. Recommended Model to Model Migrations (Sheet 2 of 2)

S25FL-A Ordering Part Number	Package	Recommended S25FL-P Ordering Part Number	Footprint Compatible
S25FL040A0LV(A,F)I01(0,1,3)	SO-8 (150 mil)	S25FL032P0XMFI01(0,1,3)	No
S25FL040A0LV(A,F)I02(0,1,3)	SO-8 (150 mil)	S25FL032P0XMFI01(0,1,3)	No
S25FL008A0LM(A,F)I00(0,1,3)	SO-8 (208 mil)	S25FL032P0XMFI01(0,1,3)	Yes
S25FL008A0LN(A,F)I00(0,1,3)	USON-8	S25FL032P0XNFI01(0,1,3)	Yes
S25FL016A0LM(A,F)I00(0,1,3)	SO-16	S25FL032P0XMFI00(0,1,3)	Yes
S25FL016A0LM(A,F)I01(0,1,3)	SO-8 (208 mil)	S25FL032P0XMFI01(0,1,3)	Yes
S25FL016A0LN(A,F)I00(0,1,3)	WSON-8	S25FL032P0XNFI00(0,1,3)	Yes
S25FL032A0LM(A,F)I00(0,1,3)	SO-16	S25FL032P0XMFI00(0,1,3)	Yes
S25FL064A0LM(A,F)I00(0,1,3)	SO-16	S25FL064P0XMFI00(0,1,3)	Yes

7 Conclusion

The S25FL-A can be replaced with the S25FL-P in most applications without any hardware or software modifications. A small number of parameter specification differences exist between these two SPI flash families and it is important that careful examination of the impact of these specification differences be reviewed for each design.

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