AN201383

S25FL-P SPI Flash Family PCB Layout Guide

Author: Feng Liu

Associated Part Family:S25FL-P

AN201383 document discusses the PCB layout and provides the recommendations for using Cypress Serial Flash S25FL-P family high-speed synchronous access memory devices.

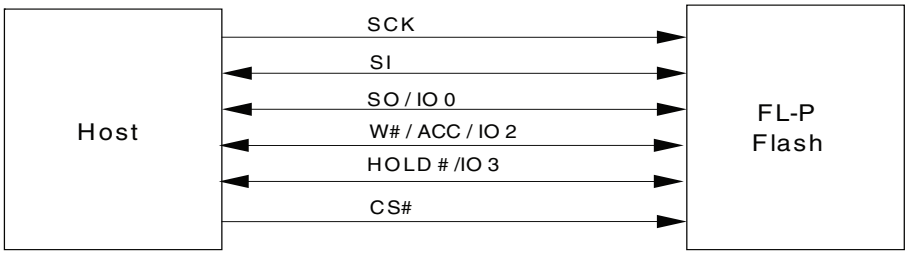
1 Introduction

The Cypress Serial Flash S25FL-P family is a high speed (up to 104 MHz) synchronous access memory device. For the PCB design, standard high speed layout practices should be followed when using FL-P Flash family. This document discusses, in general, the PCB layout and provides the recommendations for using the FL-P product family.

2 FL-P Flash Family

The FL-P Flash family provides high speed Single or /Multi I/O (MIO) Serial Peripheral Interface (SPI) to the host controller. It can run single I/O, Dual I/O, or Quad I/O bus for device access. There are three package options available, 16-pin SO, 8-contact WSON, and 24-ball BGA. In addition, the 32 Mb Multi I/O SPI device also offers 8-pin SO and USON 5x6 packages. Figure 1 shows the simplified signal connections between a host controller and the FL-P Flash memory.

Figure 1. Simplified MIO SPI Interface Connection

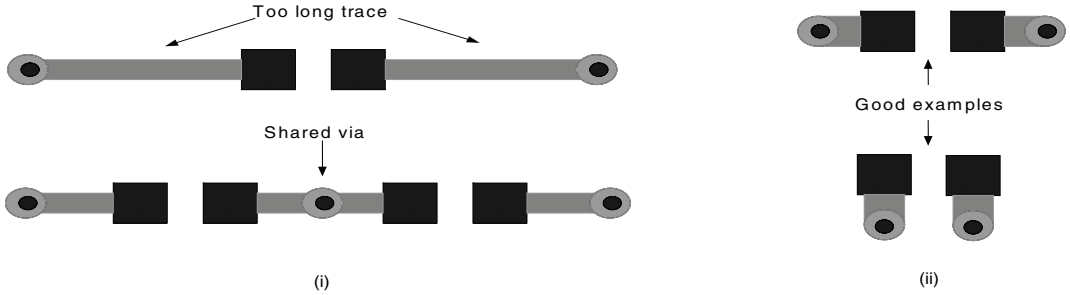


3 Power Supply Decoupling

The FL-P Flash (in all three packages) has one power supply pin (VCC) and one ground pin (GND). A 0.1 µF ceramic capacitor is recommended for power supply decoupling. This capacitor should be placed as close as possible to the power supply pin of the package.

The routing of the capacitor (normally 0603 or 0402 package) should be optimized to achieve lower inductance. It is recommended to keep the power trace length (from the package pads to the vias) shorter with the trace width around 24 mils. Also, it is good design practice to avoid sharing the same via with two or more decoupling capacitors. Figure 2 shows examples of routing the decoupling capacitor.

Figure 2. Routing with Decoupling Capacitor



4 Clock Signal Routing

In high speed synchronous data transfer, good signal integrity in a PCB design is of importance, especially for the clock signal. When routing the clock signal, special cares should be taken. The following practices are recommended.

- Run the clock signal at least 3x of the trace width away from all other signal traces. This helps to keep clock signal clean from noise. See Figure 3.
- Use as less via(s) as possible for the whole path of clock signal. Via will cause impedance change and signal reflection.
- Run the clock trace as straight as possible and avoid using serpentine routing. See Figure 4.
- Keep a continuous ground in the next layer as reference plane.
- Route the clock trace with controlled impedance.

Figure 3. Separate Clock From Other Signals

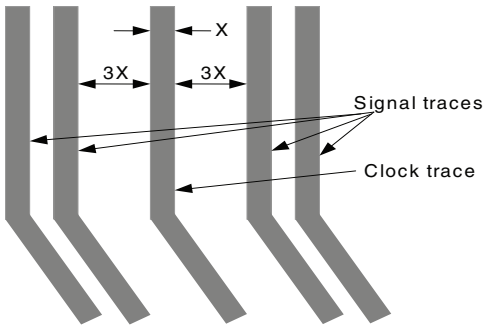
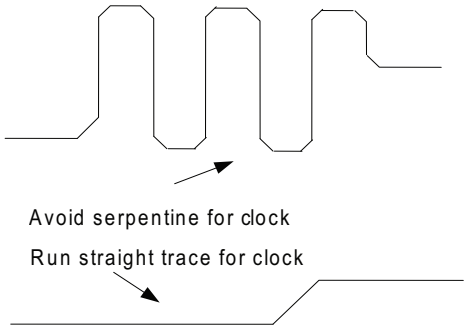


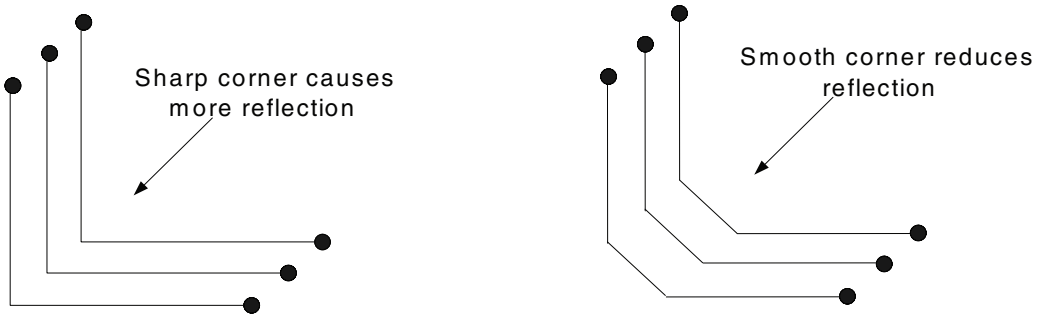
Figure 4. Run Straight Trace for Clock



5 Data Signal Routing

The FL-P Flash has a 4-bit data bus, IO0 - IO3. In order to keep the correct timing for the data transfer, in the PCB routing, the data traces should match the time delay with the clock trace from the host controller to the Flash. The data signals should be routed with the traces of controlled impedance to reduce the signal reflection. It should be avoided to route the traces with 90· angle corner. The recommendation is to cut the corner and smooth the trace when trace route needs to change direction. Figure Figure 5 shows the example of trace routing at the corner. To further improve the signal integrity, it should be considered to avoid using multiple signal layers for data signal routing. All signal traces should have a continuous reference plane.

Figure 5. Signal Routing at the Corner



6 A Check List of Recommendations

The following is a check list of PCB design recommendations.

- Put the decoupling capacitor as close as possible to the power pin. A value of around 0.1 µF ceramic capacitor with 0603/0402 package is a good choice.
- Clock should be routed straight and with less vias if possible. Separation of clock and other signals is important to make the clock clean.
- All signal traces should go with a solid reference plane (either GND or VCC).
- All signals should be routed with controlled impedance. Typically, the PCB is recommended to be built using 50-75 Ohm trace impedance with +/- 5% tolerance. If the PCB has to be designed with a trace impedance beyond this range, a simulation is strongly recommended with Cypress's IBIS model to determine if a serial termination resister is needed for the data lines.
- Data bus should be routed with matching length to the reference of the clock. The matching length, typically, is recommended within +/- 150 mils.

7 Reference

Data sheet, S25FL129P, 128-Mbit CMOS 3.0 Volt Flash Memory with 104-MHz SPI (Serial Peripheral Interface) Multi I/O Bus, Cypress.

Document History Page

Document Title: AN201383 - S25FL-P SPI Flash Family PCB Layout Guide Document Number: 002-01383				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	11/19/2009	Initial version
*A	4927860	MSWI	09/21/2015	Updated in Cypress template
*B	5798987	AESATMP8	07/06/2017	Updated logo and Copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709