AN202107

Migrating from S25FL204K to S25FL116K

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Associated Part Family: S25FL204K S25FL116K

Related Application Notes: None

AN202107 discusses the key differences that need to be considered when migrating from a S25FL204K to a S25FL116K. This application note explains how a S25FL116K is a replacement for a S25FL204K.

1 Introduction

S25FL116K, a 16-Mbit SPI Flash, is a replacement device for S25FL204K. The devices are identical in terms of pinout, package composition, and dimensions. This application note discusses the key differences between the devices that need to be considered when migrating from a S25FL204K to a S25FL116K.

2 Replacement Considerations

From a hardware point of view, the S25FL116K is a drop-in replacement for the S25FL204K. It is package and pinout compatible, and operates over the same temperature and voltage ranges.

One minor difference is that the S25FL116K has a higher maximum programming current. However, because the current requirement for erase is higher than for programming and since the programming current for both devices is the same, the power supply to the Flash is capable of supplying the required programming current.

From a software point of view, the command sets are similar. The S25FL116K supports several features that the S25FL204K doesn't including Security Registers, SFDP device identification, Wrapped bursts, Erase and Program Suspend and Resume, as well as Quad input/output. The opcodes for reading, programming and erasing are the same on the S25FL204K devices and the S25FL116K. However, the Sector Erase and Chip Erase opcodes can take longer to execute on the S25FL116K. Although the simple status register functions such as 'write enable' and 'write in progress' are compatible and the commands to access them are the same, other status register functions such as 'block protection' and locking the status register are different. The Write Status register opcode may take longer to complete on the S25FL116K. The device IDs are different for the devices.

Table 1 shows the compatibility chart of S25FL204K and S25FL116K. For a detailed comparison, see Table 3.

Table 1. Compatibility Chart

S25FL204K Feature or Spec	Is S25FL116K Compatible?
Package	Yes
Pinout	Yes
Temperature Range	Yes
Operating Voltage	Yes
Operating Current	No
Standby Current	Yes
Command Set	No
Signal Timing / Frequency	Yes
Data Retention	Yes
Endurance	Yes
Block Protection	No

3 Ordering Part Numbers

Table 2. Recommended Ordering Part Numbers for Migration

S25FL204K	S25FL116K
Ordering Part Number	**Ordering Part Number**
S255FL204K0TMFI01	S25FL116K0XMFI01
S255FL204K0TMFI04	S25FL116K0XMFI04

4 Comparison of S25FL204K and S25FL116K

Table 3 gives a detailed comparison of the devices.

Table 3. Detailed Comparison Table

		S25FL204K	S25FL116K	Comments
Package type		01, 04	01, 04	Identical RoHS compliant packages.
Pinout/package Outline		SOIC-8 (208 mil),SOIC-8 (150 mil)	SOIC-8 (208 mil),SOIC-8 (150 mil)	Identical pinout, outline and board footprint.
Temperature Range		–40 ºC to +85 ºC	–40 ºC to +85 ºC	Identical (S25FL116K is also available in Automotive and Extended temperature ranges)
Operating Voltage Range		2.7 V to 3.6 V	2.7 V to 3.6 V	Identical
Read Data[1 2] Current	**Typical**	10 mA @ 33 MHz	6 mA @ 33 MHz	Better
	Max	15 mA @ 33 MHz	9 mA @ 33 MHz	
	Max	25 mA @ 100 MHz	18 mA @ 108 MHz	
Dual Output Read Current[1 2]	**Typical**	12 mA @ 33 MHz	7 mA @ 33 MHz	Better
	Max	18 mA @ 33 MHz	10.5 mA @ 33 MHz	
	Max	25 mA @ 100 MHz	22 mA @ 108 MHz	
Page Program Current[3]	**Typical**	15 mA	20 mA	Different. See the Program Current section in Critical Considerations.
	Max	20 mA	25 mA	
Write Status Register Current[3]	**Typical**	10 mA	8 mA	Better
	Max	18 mA	12 mA	
Erase Current[3]	**Typical**	20 mA	20 mA	Identical
	Max	25 mA	25 mA	
Standby Current[4]	**Typical**	15 µA	15 µA	Identical
	Max	35 µA	35 µA	
Power-down	**Typical**	15 µA	2 µA	Better

[1] SCK = 0.1 V_{CC} / 0.9 V_{CC} DO= Open

[2] Checker Board Pattern

[3] CS# = V_{CC}

[4] CS# = V_{CC}, V_{IN} = GND or V_{CC}

		S25FL204K	S25FL116K	Comments
Current[4]	**Max**	32 µA	8 µA	
Command Set		3-byte addressing, opcodes	3- byte addressing, opcodes	Status Register command arguments are different. Additional commands supported. See the Command Set section in Critical Considerations.
Clock Frequency		85 MHz	108 MHz	Better
Data Retention		20-year data retention typical	20-year data retention Typical	Identical
Endurance (Program/Erase Cycles)		100k erase/program cycles typical	100K erase/program cycles minimum	Better
VCC (min) to CS# Low (t_{VSL})		10 µs Min	10 µs Min	Identical
Device ID	**ABh**	12h	14h	Different. See the Device ID section in Critical Considerations.
	90h	0112h	0114h	
	95h	014013h	014015h	
Write Status Register Time	**Typical**	10 ms	2 ms	Different. See the Status Register section in Critical Considerations.
	Max	15 ms	30 ms	
Byte Program Time (First Byte)	**Typical**	30 µs	15 µs	Better or Identical
	Max	50 µs	50 µs	
Additional Byte Program Time (After First Byte)	**Typical**	6 µs	2.5 µs	Better or Identical
	Max	12 µs	12 µs	
Page Program Time	**Typical**	1.5 ms	0.7ms	Better
	Max	5 ms	3 ms	
Sector Erase Time (4 kB)	**Typical**	50 ms	50 ms[5]	Different. See the Sector Erase section in Critical Considerations.
	Max	300 ms	450 ms[5]	
Block Erase Time (64 kB)	**Typical**	0.5 s	0.5 s[5]	Identical
	Max	2 s[6]	2 s[5]	
Chip Erase Time	**Typical**	3.5 s	11.2 s[5]	Different. See the Device Density section in Critical Considerations.
	Max	7 s[7]	64 s[5]	
Block Protection		See Table 6	See Table 7	Different. See the Block Protection section in Critical Considerations.
Number of Blocks (64K) / Sectors (4K)		8/128	32/512	Different. See the Device Density section in Critical Considerations.
Flash Array Size		524,288 bytes	2,095,152 bytes	Different. See the Device Density section in Critical Considerations.
Status Registers		1	3	Different. See the Status Register section in Critical Considerations.

[5] For the S25Fl116K all erase times are tested using a random pattern

[6] Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 5.3 s

[7] Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 8.4 s

5 Critical Considerations

You should consider all the parameter differences mentioned in Table 3 for the migration to S25FL116K. This section discusses the critical differences. System designers should also review the datasheet when migrating to the new part.

5.1 Program Current

The page program current of the S25FL116K is higher than that of the S25FL204K. The typical and worst-case page programming currents are 5 mA higher in the S25FL116K. This should not be an issue for most systems because these currents are the same as the erase currents of the S25FL204K, and the power supply is able to deliver the higher current required. Also, the page programing time for the S25FL116K is faster than the S25FL204K so less energy will be used.

5.2 Command Set

The S25FL116K supports all the commands that the S25FL204K does and adds some additional commands. With one exception, it also has the exact same arguments. The exception is the Write Status Register(s) (01h). On the S25FL204K this op code only takes eight bits of data. The S25FL116K version of the opcode takes 8, 16, or 24 bits of data depending on how many of the status registers you wish to write to. The table below details the command sets.

Table 4. Command Comparison

Command Name	Opcode	S25FL204K	S25FL116K
		Arguments	Arguments
Write Status Register(s)	01h	1-Byte	1,2, or 3-Bytes
Read Status Register-1	05h	None	None
Read Status Register-2[8]	35h	NA	None
Read Status Register-3[8]	33h	NA	None
Write Enable	06h	None	None
Write Enable for Volatile Status Register	50h	None	None
Write Disable	04h	None	None
Set Burst with Wrap[8]	77h	NA	3-Bytes Dummy 1-Byte Data
Page Program	02h	3-Bytes Address Up to 256-Bytes data	3-Bytes Address Up to 256-Bytes data
Sector Erase (4 kB)	20h	3-Bytes Address	3-Bytes Address
Block Erase (64 kB)	DBh	3-Bytes Address	3-Bytes Address
Chip Erase	C7h/60h	None	None
Erase / Program Suspend[8]	75h	NA	None
Erase / Program Resume[8]	7Ah	NA	None
Read Data	03h	3-Bytes Address	3-Bytes Address
Fast Read	0Bh	3-Bytes Address 1-Byte Dummy	3-Bytes Address 1-Byte Dummy
Fast Read Dual Output	3Bh	3-Bytes Address 1-Byte Dummy	3-Bytes Address 1-Byte Dummy
Fast Read Quad Output[8]	6Bh	NA	3-Bytes Address 1-Byte Dummy

[8] Not Supported on the S25FL204K

Command Name	Opcode	S25FL204K	S25FL116K
Fast Read Dual I/O[8]	BBh	NA	3-Bytes Address 1-Byte Mode
Fast Read Quad I/O[8]	EBh	NA	3-Bytes Address 1-Byte Mode
Software Reset Enable[8]	66h	NA	None
Software Reset[8]	99h	NA	None
Continuous Mode Reset[8]	FFh	NA	None
Deep Power Down	B9h	None	None
Release from Power Down/Device ID	ABh	3-Bytes Dummy	3-Bytes Dummy
Manufacturer / Device ID	90h	2-Bytes dummy 1-Byte 0	2-Bytes dummy 1-Byte 0
JEDEC ID	9Fh	None	None
Read SFDP Register / Read Unique ID[8]	5Ah	NA	2-Bytes 0 1-Byte Address 1-Byte Dummy
Read Security Registers[8]	48h	NA	3-Bytes Address 1-Byte Dummy
Erase Security Registers[8]	44h	NA	3-Bytes Address
Program Security Registers[8]	42h	NA	3-Bytes Address up to 256-Bytes data

5.3 Device ID

Table 5 shows the opcodes that can be used to retrieve the device ID from the flash and their values. Software that checks the device ID of the S25FL204K will need to be changed to recognize the device ID returned by the S25FL116K.

Table 5. Device ID Values

Opcode	S25FL204K Value	S25FL116K Value
ABh	12h	14h
90H	0112h	01014h
9FH	014013h	014015h

5.4 Status Register

5.4.1 Status Registers

The S25FL116K has three status registers where the S25FL204K has only one. The basic status bits Write In Progress (WIP) and Write Enable (WE) are in the same locations and accessed by the same opcodes. The protection bits are different and are detailed in the Block Protection section of this document. For more details about the two additional status registers in the S25FL116K, see the datasheet referred to in the Related Documents section.

5.4.2 Status Write Time

The write status register opcode takes longer on the S25FL116K than it does on the S25FL204K. Any software that uses a delay to determine when this operation is finished will need to have the delay lengthened or replaced with the polling of the WIP bit in the status register. When WIP = 0, the operation is complete. Software that already polls WIP will not require any changes.

5.4.3 Status Register Locking

The S25FL204K provides a method for locking the value of the Status Register. Setting bit 7 (Status Register Protect SRP) in the Status Register to 1 will cause Status Register writes to fail if the write protect signal (WP#) is held LOW. The S25FL116K provides the same functionality. In Status Register 1, bit 7 is the Status Register Protect 0 (SPR0), and in Status Register 2, bit 0 is Status Register Protect 1 (SPR1). If SPR1 is 0, its default value, then SPR0 provides the same functionality as the S25FL204K's SRP. If SPR1 is set to 1, then the protection is permanently locked if SR0 is 1, and locked until the next power cycle if SR0 is 0.

5.5 Sector Erase

The maximum sector erase time for the S25FL116K is longer than the maximum sector erase time for the S25FL204K. Software that uses the WIP bit in the Status Register will not have to be modified. If software uses a delay to determine when the operation is finished, the delay may need to be lengthened or replaced with polls for the WIP bit. When WIP = 0 the operation is complete.

5.6 Device Density

The fact that the S25FL116K has a higher density than the S25FL204K raises several issues that must be accounted for. The sections below detail these issues.

5.6.1 Chip Erase

Because the S25FL116K has a flash array that is four times the size of that in the S25FL204K, the time required to execute the Chip Erase (C7h/60h) opcode will be four times as long. Any software that uses time delays instead of checking the Write In Progress (WIP) bit in the status register may need to be modified to account for the longer chip erase time.

5.6.2 Addressable Flash Array

The flash array in the S25FL116K requires 21 bits (A0-A20) to have it completely addressed. It is necessary that migrated software control the additional address bits. If the additional address bits are not constant, it is possible that data will not be where it is expected to be.

5.7 Block Protection

The block protection mechanisms for the S25FL116K and the S25FL204K are different. The S25FL204K provides methods to protect blocks (64K) starting from the top of the address space and sectors (4K) starting at the bottom of the address space. The S25FL116K can be configured to protect blocks in the same way as the S25FL204K, but cannot duplicate the sector protection scheme. The next two sections detail how the device protection mechanisms work.

5.7.1 S25FL204K Block protection

On S25FL204K there are four nonvolatile bits that determine what portions of the device are protected. These bits are the BP0-3 bits in the Status Register (bits 2-5). The BP3 bit determines what type of regions are protected. If BP3 = 0, then 64K blocks are protected from the top of the address space. If BP3 = 1, then 4K blocks are protected from the bottom of the address space. The BP0-3 bits determine which sectors (4K) or blocks (64K) are protected. The table below summarizes the protection.

Table 6. S25FL204K Block Protection Details

Status Register Bit				S25FL204K
BP3	BP2	BP1	BP0	
0	0	0	0	None
0	0	0	1	Block 7 (070000h - 07FFFFh)
0	0	1	0	Blocks 6-7 (060000h-07FFFFh)
0	0	1	1	Blocks 4-7 (040000-07FFFFh)
0	1	0	0	Blocks 0-7 (000000h-07FFFFh)
0	1	0	1	Blocks 0-7 (000000h-07FFFFh)
0	1	1	0	Blocks 0-7 (000000h-07FFFFh)
0	1	1	1	Blocks 0-7 (000000h-07FFFFh)

Status Register Bit				S25FL204K
BP3	BP2	BP1	BP0	
1	0	0	0	None
1	0	0	1	Sectors 0-126 (000000h-07EFFFh)
1	0	1	0	Sectors 0-123 (000000h-07BFFFh)
1	0	1	1	Sectors 0-119 (000000h-076FFFh)
1	1	0	0	Sectors 0-111 (000000h-06FFFFh)
1	1	0	1	Sectors 0-95 (000000h-005FFFFh)
1	1	1	0	Sectors 0-63 (000000h-03FFFFh)
1	1	1	1	Sectors 0-127 (000000h-07FFFFh)

5.7.2 S25FL116K Block Protection

For the S25FL116K, there are six bits that determine the protection behavior in two status registers.

Block Protect bits 0-2 (BP0-2), which are bits 2-4 in Status Register 1 control which regions are protected.

The Top/Bottom Protect bit (TB), which is bit 5 in Status Register 1, controls whether protection is applied from the top or bottom of the address space. Note that this bit is in the same position as the BP3 bit of the S25FL204K, so care must be taken to ensure that migrated software does not accidently set this bit.

The Sector/Block Protect bit, which is bit 6 in status register 1, controls whether the regions protected are sectors (4K) or blocks (64K).

The Compliment Protect bit, which is bit 6 in Status Register 2, controls whether the regions defined by the BP0-2 bits are protected or available for modification.

All the protection bits are non-volatile.

The following tables summarize the protection behavior on the S25FL116K.

Table 7. S25FL116K Block Protection Details (CMP = 0)

Status Register Bit					S25FL116K Protected Region
SEC	TB	BP2	BP1	BP0	
X	X	0	0	0	None
0	0	0	0	1	Block 31 (1F0000h – 1FFFFFh)
0	0	0	1	0	Blocks 30-31 (1E0000h-1FFFFFh)
0	0	0	1	1	Blocks 28-31 (1C0000h-1FFFFFh)
0	0	1	0	0	Blocks 24-31 (180000h-1FFFFFh)
0	0	1	0	1	Blocks 16-31 (100000h-1FFFFFh)
0	1	0	0	1	Block 0 (000000h-00FFFFh)
0	1	0	1	0	Blocks 0-1 (000000h-01FFFFh)
0	1	0	1	1	Blocks 0-3 (000000h-03FFFFh)
0	1	1	0	0	Blocks 0-7 (000000h-07FFFFh)
0	1	1	0	1	Blocks 0-15 (000000h-0FFFFFh)
X	X	1	1	X	Blocks 0-31 (000000h-1FFFFFh)
1	0	0	0	1	Sectors 511 (1FF000h-1FFFFFh)
1	0	0	1	0	Sectors 510-511 (1FE000h-1FFFFFh)
1	0	0	1	1	Sectors 508-511 (1FC000h-1FFFFFh)

Status Register Bit					S25FL116K Protected Region
SEC	TB	BP2	BP1	BP0	
1	0	1	0	X	Sectors 504-511 (1F8000h-1FFFFFh)
1	1	0	0	1	Sector 0 (000000h-000FFFh)
1	1	0	1	0	Sectors 0-1 (000000h-001FFFh)
1	1	0	1	1	Sectors 0-3 (000000h-003FFFh)
1	1	1	0	X	Sectors 0-7 (000000h-007FFFh)

Table 8. S25FL116K Block Protection Details (CMP = 1)

Status Register Bit					S25FL116K Protected Region
SEC	TB	BP2	BP1	BP0	
X	X	0	0	0	All
0	0	0	0	1	Block 0-30 (000000h – 1EFFFFh)
0	0	0	1	0	Blocks 0-29 (000000h -1DFFFFh)
0	0	0	1	1	Blocks 0-27 (000000h -1BFFFFh)
0	0	1	0	0	Blocks 0-23 (000000h-17FFFFh)
0	0	1	0	1	Blocks 0-15 (000000h-0FFFFFh)
0	1	0	0	1	Block 1-31 (010000h-1FFFFFh)
0	1	0	1	0	Blocks 2-31 (020000h-1FFFFFh)
0	1	0	1	1	Blocks 4-31 (040000h-1FFFFFh)
0	1	1	0	0	Blocks 8-31 (080000h-1FFFFFh)
0	1	1	0	1	Blocks 16-31 (100000h-1FFFFFh)
X	X	1	1	X	None
1	0	0	0	1	Sectors 0-510 (000000h-1FEFFFh)
1	0	0	1	0	Sectors 0-509 (000000h-1FDFFFh)
1	0	0	1	1	Sectors 0-507 (000000h-1FBFFFh)
1	0	1	0	X	Sectors 0-503 (000000h-1F7FFFh)
1	1	0	0	1	Sector 1-511 (001000h-1FFFFFh)
1	1	0	1	0	Sectors 2-511 (002000h-1FFFFFh)
1	1	0	1	1	Sectors 4-511 (004000h-1FFFFFh)
1	1	1	0	X	Sectors 8-511 (008000h-1FFFFFh)

6 Summary

AN202107 discussed the differences between the S25FL204K and the S25FL116K that need to be considered during migration to the S25FL116K.

7 Related Documents

S25FL204K Datasheet

S25FL116K Datasheet

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4898721	AHCL	09/01/2015	New application note
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