AN2219

PSoC® 1 Selecting Analog Ground and Reference

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AN2219 describes the internal ground and reference structure in detail and outlines the applicability of each reference setting to typical system designs.

1 Introduction

Analog voltage measurement and signal processing applications in PSoC® require the use of a precision ground and voltage references. Selecting the correct analog ground and voltage reference is essential in establishing accurate system performance. The PSoC offers considerable flexibility in setting references.

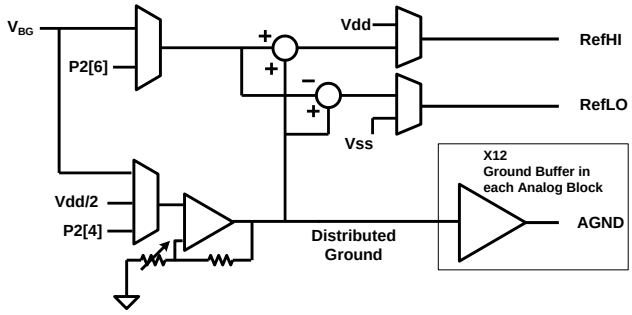
2 Analog Ground

The PSoC Programmable System-on-Chip operates on a single power supply between 3.0 and 5.25 volts. Analog signals in most systems are typically of both positive and negative polarity around some reference or ground. The PSoC only handles signals of positive polarity with respect to VSS. An artificial ground is constructed on the chip to provide a reference point for signals of both polarities; this reference is called Analog Ground.

The ground for analog circuits must be quiet and free from interaction between circuits connected to ground. In standard system designs, this is accomplished by using a dedicated ground plane in the PCB design, or at the very least, by using wide ground traces. Unfortunately, there is no solid copper ground plane in the PSoC chip. Routing a ground signal around the chip, with load currents into and out of each analog block results in the sum of the currents developing a noise voltage across the routing resistance. This noise is common to all signals. The ground noise could be so high as to make low-level signal processing difficult.

In order to take advantage of a common ground for all signals, the ground signal is routed to all analog blocks then buffered locally with an op-amp. The reference and ground structure is shown in Figure 1.

Figure 1.Ground and Reference Structure



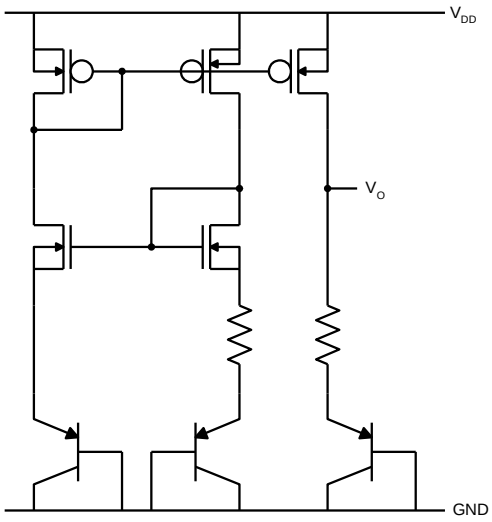
The analog ground voltage can be derived from a voltage divider connected to V_{dd}, the positive power supply, an external input, or a multiple of the on-chip bandgap reference. When the analog ground is derived from a multiple of the bandgap it is relatively immune to power supply variations.

3 What's a BandGap?

The term bandgap refers to the potential difference between the valence band and the conduction band in atomic structures. The operation of the bandgap reference is simple and discussed at great length in numerous semiconductor design references (see the Appendix for suggested reading). The voltage difference between two diodes is used to generate a current proportional to absolute temperature (PTAT) in a resistor.

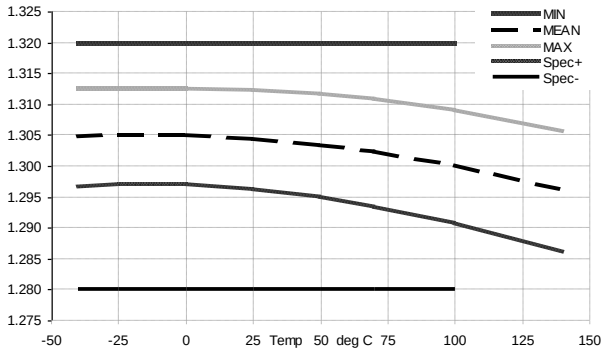
A current mirror is used to generate a voltage in a second resistor; this voltage is added to the voltage of one of the diodes. The diode voltage temperature coefficient is negative; the PTAT temperature coefficient is positive. The ratios of the diode sizes and resistor values are chosen so that the first order temperature dependence of the diode and the PTAT current cancel. The resulting voltage is quite stable and has parabolic temperature dependence. An example of a bandgap circuit is shown in Figure 2.

Figure 2. Example BandGap Circuit



The typical performance of the PSoC bandgap reference is shown in Figure 3.

Figure 3. Typical PSoC BandGap Performance



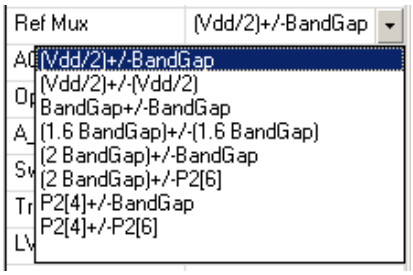
The excellent accuracy and stability of the PSoC bandgap reference are achieved by actively trimming the PTAT current source for magnitude and temperature performance in the wafer and final package test steps of the manufacturing process. The initial value at room temperature is set slightly above the nominal 1.300 volts so that temperature variations (always negative from the peak value) result in an average value close to the specification over the full operating temperature range.

4 Reference Structure

In addition to the analog ground, the reference generator forms signals RefHI, above analog ground, and RefLO, below analog ground. These are generated in the reference block by adding and subtracting the reference voltage from the analog ground signal using op-amps, as shown in Figure 1. The references are used primarily for setting ADC and DAC ranges.

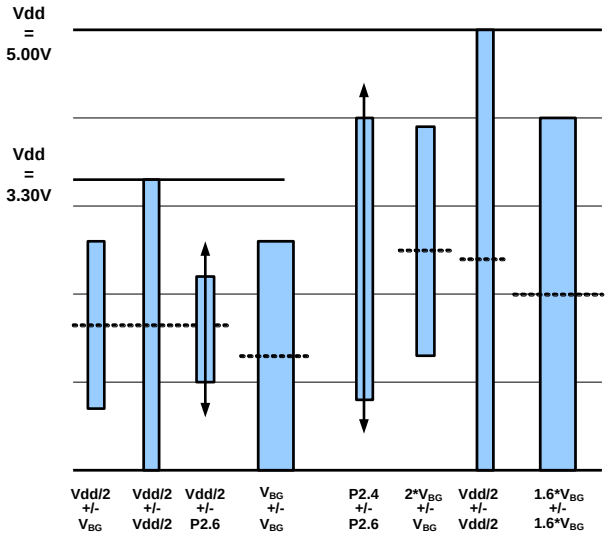
The analog ground and reference values are selected in the global resources window of PSoC Designer, as shown in Figure 4.

Figure 4. Reference Selections



These selections are shown in graphical form in Figure 5. Some ground and reference settings are suitable for use at both 3.3 and 5.0 volts. Other settings generate reference values out of range for 3.3 V systems.

Figure 5. Reference Ranges



The op-amps in the reference outputs require a certain amount of headroom, typically 0.3 volts from each supply rail. When the analog ground and reference are derived from external sources, the RefHI and RefLO signals must meet this requirement.

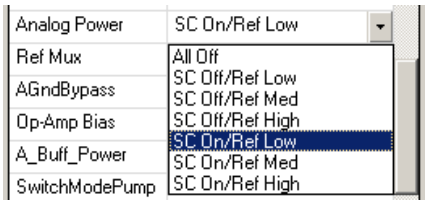
In cases where the reference is the supply rail (e.g., $V_{DD}/2$ +/- V_{DD} /2, RefHI = V_{DD}, RefLO = V_{SS}), the reference output op-amps are switched off and the reference is simply switched directly to the appropriate supply rail.

Digital-to-analog converter (DAC) outputs are scaled to the reference values. DAC outputs connected to external loads must go through the analog output buffers. The analog output buffers in the PSoC are not rail-to-rail, but typically reach 0.4 volts from V_{SS} and 0.6 volts from V_{DD}, so system designs must accommodate this output swing even if the reference outputs are set to V_{DD} or V_{SS}.

While the analog ground is buffered in each analog block, RefHI and RefLO are not. Load currents from the block are either very low and static in the continuous time blocks or dependent on clock speed in the switched capacitor blocks.

The RefHI and RefLO outputs must settle to their nominal values on every cycle of the analog column clock when loaded by analog user modules. The reference power level, shown in Figure 6, must be set to the same level as the highest power analog user module.

Figure 6. Reference Power Selection



Each analog ground and reference setting is suitable to a specific set of signal processing needs. Settings are listed in Table 1.

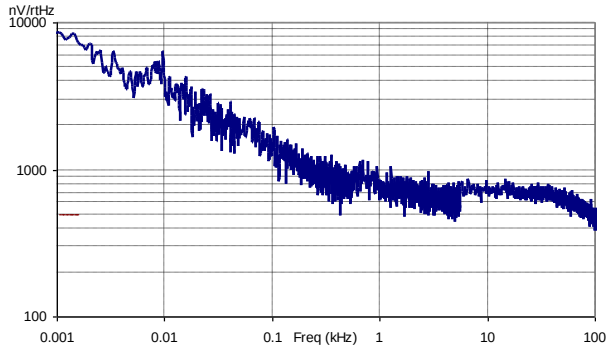
Table 1. Ground and Reference Selections

Selection	Voltage Range	Application
V_{DD}/2 +/- BandGap	1.2 V to 3.8 V for V_{DD} =5.0 V 0.35 V to 2.85 V for V_{DD} =3.3 V	Systems using differential sensors or AC coupled measurements where absolute voltages are measured. A good example is audio signal processing.
V_{DD} /2 +/- V_{DD} /2	0.0 V to 5.0 V for V_{DD} =5.0 V 0.0 V to 3.3 V for V_{DD} =3.3 V	Systems using sensors with outputs that are ratiometric to the power supply voltage and need analog-to-digital converters with input range tracking the supply voltage. V_{DD} connected pressure sensors are a good example.
BandGap +/- BandGap	0.0 V to 2.60 V for V_{DD} =5.0 V 0.0 V to 2.60 V for V_{DD} =3.3 V	Systems requiring measurements that are absolute (that is not ratiometric to the supply) effectively use this selection. Examples include battery measurement or system power supply monitoring.
1.6*BandGap +/- 1.6*BandGap	0 V to 4.16 V for V_{DD} =5.0 V Not valid for V_{DD} =3.3 V	This setting is used by systems requiring absolute measurements with wider range than 2*BandGap full scale. Note that 4.16 volts is very close to 1 mV per bit for 12-bit systems.
2*BandGap +/- BandGap	1.3 V to 3.9 V for V_{DD} =5.0 V Not valid for V_{DD} =3.3 V	Used for systems with limited range centered at a fixed voltage. Commonly used for resistance and thermistor temperature measurements as in AN2017.
2*BandGap +/- P2[6]	2.60-P2[6] to 2.60+P2[6] for V_{DD} =5.0 V Not valid for V_{DD} =3.3 V	Used for systems with absolute measurements with user-specific ADC input range, typically with higher sensitivity around the nominal analog ground. The limit in this case is the build-up of offset voltages in the reference generation; this limits the minimum value of user-supplied reference to greater than 0.5 V.
P2[4] +/- BandGap	P2[4]-1.30 V to P2[4]+1.30 V for V_{DD} =5.0V P2[4]-1.30 V to P2[4]+1.30 V for V_{DD} =3.3 V when P2[4]<1.8 V	Used for systems with absolute measurements with a user-specific analog ground value. This is typical of systems where the sensor also outputs a specific reference near mid-supply and this level is an essential part of system calibration.
P2[4] +/- P2[6]	0.3 V to 4.4 V for V_{DD} =5.0 V 0.4 V to 2.8 V for V_{DD} =3.3 V	Used for systems where the user supplies external values for both ground and reference. Typically, this is for systems where the analog ground is set at a specific offset and the user needs a limited range for ADC inputs with higher resolution. The resolution limit is set by the offset error contribution in the reference generator.

5 Noise Levels

Analog ground, as discussed earlier, is not zero, but a derived signal. As such, it can be expected to have a certain amount of noise. The bandgap noise is multiplied by the reference generator gain, so AGND=2*BandGap has twice the noise of AGND=BandGap. The analog ground voltage of 2*BandGap is approximately 700 nV/rtHz at 1.0 kHz. As with most CMOS linear circuits, the bandgap noise is proportional to 1/f as shown in Figure 7.

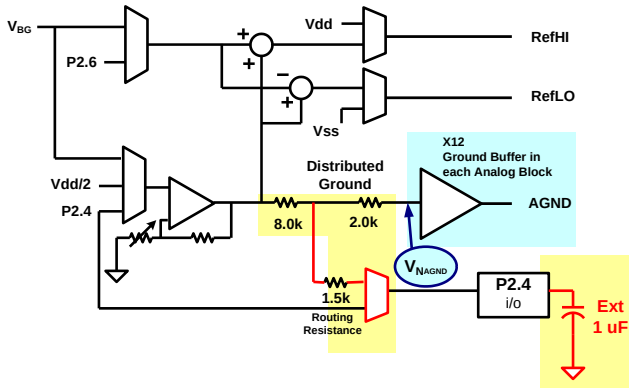
Figure 7. Analog Ground Noise AGND=2*BandGap



Analog ground based on the $V_{DD}/2$ signal generator is effectively a simple resistor divider. This ground has a noise level of about half of the level bandgap-derived analog ground. The noise level of analog ground is higher than the analog block op-amp noise level, which is approximately 100 nV/rtHz at 1.0.

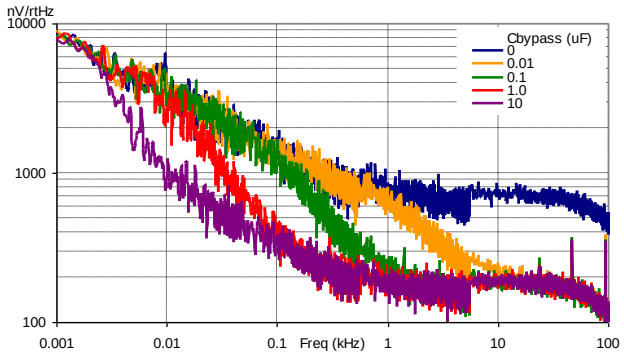
These ground noise levels are somewhat high for low noise signal processing. A feature is provided to route the internal analog ground signal to P2[4]. An external capacitor bypasses the analog ground noise to ground (V_{SS}) externally, as shown in Figure 8.

Figure 8. Analog Ground Bypass



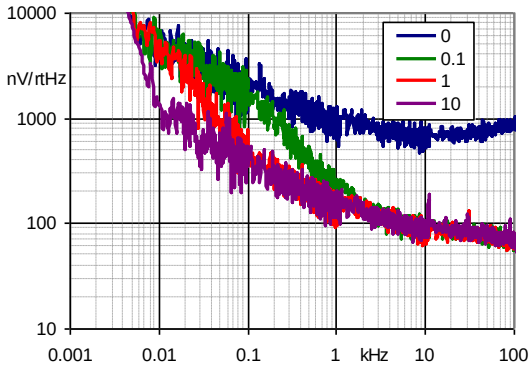
The distributed analog ground resistance (nominally 8.0 kΩ) and the external capacitor set the noise corner frequency. Figure 9 shows the noise level for several values of bypass capacitor. The noise reduction is limited by the voltage divider of the series resistance in the distributed ground path as well as the routing resistance of the multiplexer and I/O port, P2[4]. Note, the less-than-expected reduction at very low frequencies for the largest bypass capacitor is an artifact of the spectrum analyzer bandwidth used to make the measurements, not a function of circuit performance.

Figure 9. Analog Ground Noise, Bypassed CY8C24/27/29xxx



CY8C28xxx has reduced routing resistance in the path from the buffer on the output of the AGND buffer to P2.4 (the 1.5 k resistor in schematic Figure 8). As a result the noise above 3.0 kHz is significantly reduced as shown in Figure 10.

Figure 10. Analog Ground Noise, Bypassed CY8C28xxx



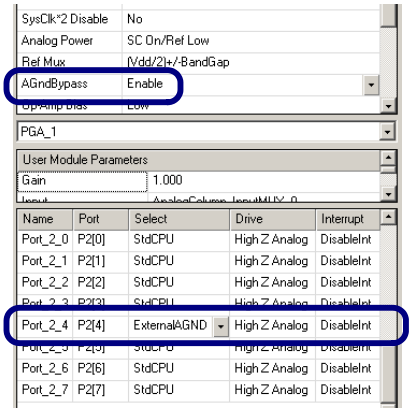
6 AGND Bypass Caveat

The Analog Ground Bypass terminal on P2.4 has a high DC output resistance. Any external resistive load will affect the value of this internalized signal. This pin can be used for an analog ground output if it is buffered with an external opamp.

7 Implementation in PSoC Designer

Selection of analog ground and reference values is done in the global resources and user module parameters windows of PSoC Designer, shown in Figure 11.

Figure 11. Global Resources and User Module Parameters Selections



The reference circuit is a small but continuous load to the bandgap circuit. Changing the analog ground and reference selection at run-time also changes the load on the bandgap. This may change the internal reference and influence the low voltage detection (LVD) comparator.

To prevent errant low voltage interrupts, simply disable the LVD interrupt prior to changing the ground and reference value, and then re-enable the LVD interrupt.

8 Summary

Single supply analog systems usually require an artificial analog ground, usually near mid-supply. The PSoC topology provides a number of possible analog grounds, both Vdd-based and using fixed references. These values are used for scaling ADCs, and DACs.

8.1 Appendix. Suggested BandGap References

1. Gray, Paul R., Meyer, Robert G. *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons, 1977.
2. Pease, Bob. *The design of Band-Gap Reference Circuits: Trials and Tribulations*, IEEE Proceedings of the 1990 Bipolar Circuit and Technology Meeting, September 17-18th, 1990.

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**	1505943	VED	10/08/2007	Recataloged Application Note
*A	3184941	SEG	03/01/2011	Update title, abstract, delete CY8C25/26 references.
*B	4308450	SEG	03/13/2014	Sunset update only, no change
*C	5718832	AESATMP9	05/24/2017	Updated logo and copyright.

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