Hardware design guidelines for WLC 50W transmitter

Applicable for WLC1150

About this document

Scope and purpose

This document provides design guidelines for the WLC1150-based power transmitter solution board for wireless charger (WLC) applications.

Intended audience

Wireless transmitter hardware designers using WLC1150 wireless transmitter with integrated USB Type-C PD controller.

Table of contents

1 About WLC1150

Wireless power transmission, based on loosely coupled inductive power transfer, is a widely used near-field power conversion topology. These power transfer systems are common in consumer appliances such as electric toothbrushes or cell phone chargers, medical devices (power supply and implantable devices), automotive applications (in-cabin charger), and industrial applications. The Qi wireless power topology utilizes series LC resonance tanks on both transmitter and receiver halves of the wireless power transfer system. The resonant topology offers low EMI along with ZVS turn-on of transmitter-side FETs and receiver-side rectifier FETs. The in-band communication between the transmitter and receiver sections offers a compact solution for wireless charging.

The WLC1150 is a highly integrated wireless transmitter controller with integrated USB Type-C power delivery (PD). While ideal for 50-W charging applications with the Infineon high power proprietary protocol, WLC1150 complies with the latest USB Type-C, WPC 1.3.x, and PD specifications. The WLC1150 supports variable frequency and phase angle control and has integrated gate drivers for inverter power stage MOSFETs. The WLC1150 also offers integrated gate drivers and control for an auxiliary power supply, which powers the fan and enables cooling of the interface surface during high power delivery. The single-chip solution provides system control and in-band communication (FSK modulation and ASK demodulation) with minimal external circuits. With a fully programmable MCU and analog and digital peripherals, the WLC1150 enables development of scalable wireless charging solutions.

1.1 WLC1150 features and applications

1.1.1 Typical applications

- Industrial wireless charging applications
- Smart phones
- Portable accessories
- Furniture and home goods
- Docking stations
- Power tools
- Robot and drones

1.1.2 Features

- Qi v1.3.x compliant transmitter (MP-A2 coil)
- Integrated USB-PD controller
  - Supports latest USB-PD 3.1 version
  - Programmable power supply (PPS) mode
  - Configurable resistors (RP, RD)
  - Support for USB-PD legacy charging protocols like QC 2.0/3.0 and AFC
- Integrated buck converter controller for fan supporting thermal management
- Integrated gate drivers for inverter stage MOSFETs
- Integrated Q factor detection
- Integrated FSK modulator
- Wide input voltage range: 4.5 to 24 V
- Communication ports: I^2C, UART

Protection
- Overcurrent protection (OCP), overvoltage protection (OVP)
- Supports overtemperature protection through integrated ADC circuit and internal temperature sensor

Temperature range: –40°C to +105°C extended industrial temperature range

Package: 68-pin QFN 8.0 x 8.0 x 0.65 mm LD68B 5.7 x 5.7 mm E-PAD

- Figure 1 shows the WLC1150 internal architecture in the form of a logic block diagram. See the datasheet [2] for more details.

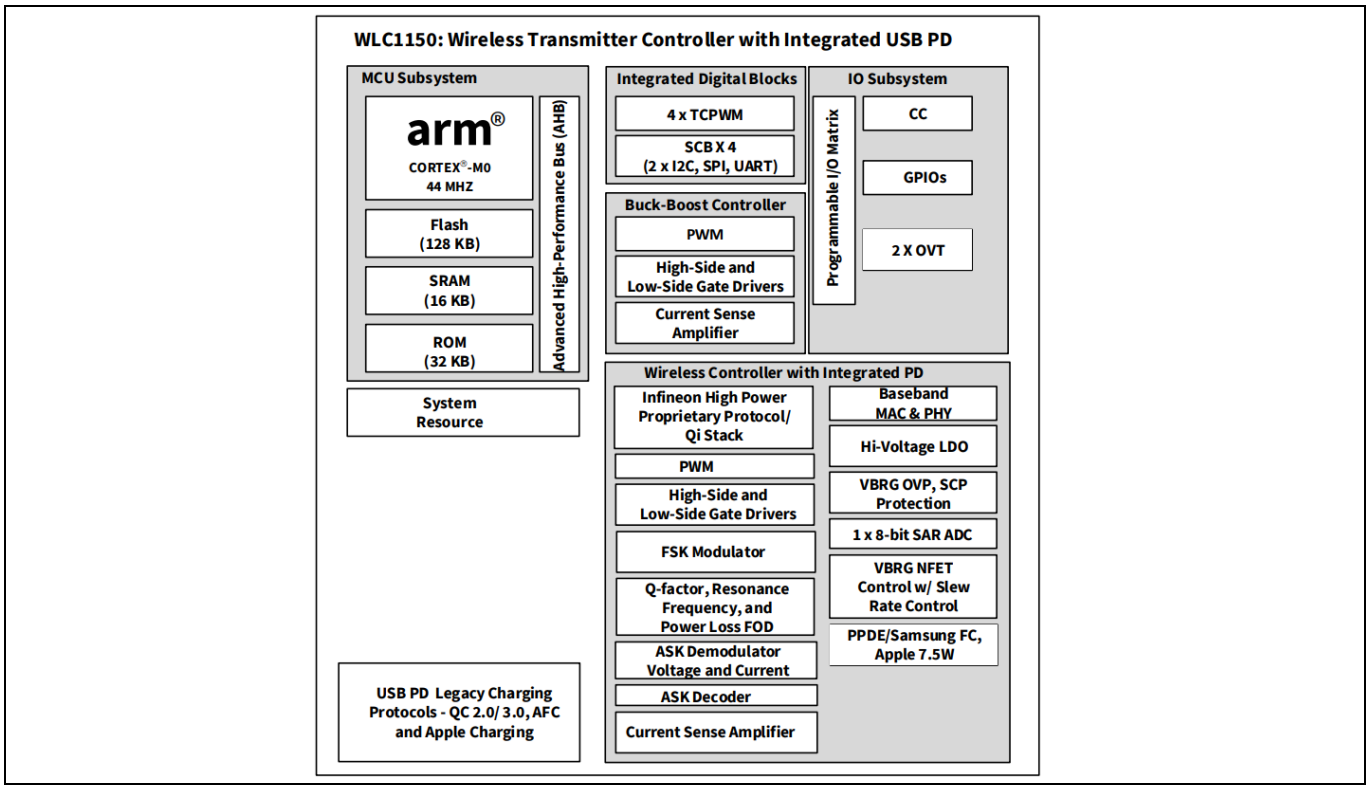

Figure 1 WLC1150 logic block diagram

1.2 WLC1150 in wireless transmitter application

A single stage wireless power transmitter unit with WLC1150, compliant with both Qi and Infineon high power proprietary protocol, is shown in Figure 2 for the MP-A2 coil. The MP-A2 coil-based transmitter system uses fixed input voltage, variable frequency and variable phase angle control for the inverter stage. The single stage architecture is attractive for low losses and low component count. The power supply to the transmitter unit uses a USB-C power adapter through the Type-C connector. For Qi compliant operation, the transmitter establishes 12 V contract with adaptor. For 50 W support with Infineon make wireless receiver, the contract is made for 20 V. With a USB-PD type input, the input voltage can be set to 5 V in idle mode reducing the standby power consumption.

An N-channel consumer FET on VBUS_IN provides inrush current protection for input power. The FET is directly driven from WLC1150 without any external gate drivers or turn ON/OFF speed control. For cooling of the transmitter interface surface and the receiver at high power, forced air cooling is required from the transmitter side. The cooling fan requires typically 2 W power, which requires an auxiliary power supply unit. WLC1150 offers the control and driving mechanism for the low-power buck converter for the fan power supply. A transmitter board with WLC1150 needs a minimal number of external components for system control. Some signal conditioning circuits and amplifier circuits are required for the PWM logic and in-band communication.

About WLC1150

An external authentication chip interfaced to the WLC1150 over I2C completes the requirements for the Qi 1.3.x standard.

For the purposes of implementing the protection features, the WLC1150 monitors the individual power stage currents and voltages. With an on-chip 32-bit Arm® Cortex®-M0 processor, 128 kB of flash memory, 16 kB of RAM, and 32 kB of ROM, the firmware supporting the complete Qi state machine logic or any other proprietary power transfer protocol for high power can be programmed onto the WLC1150.

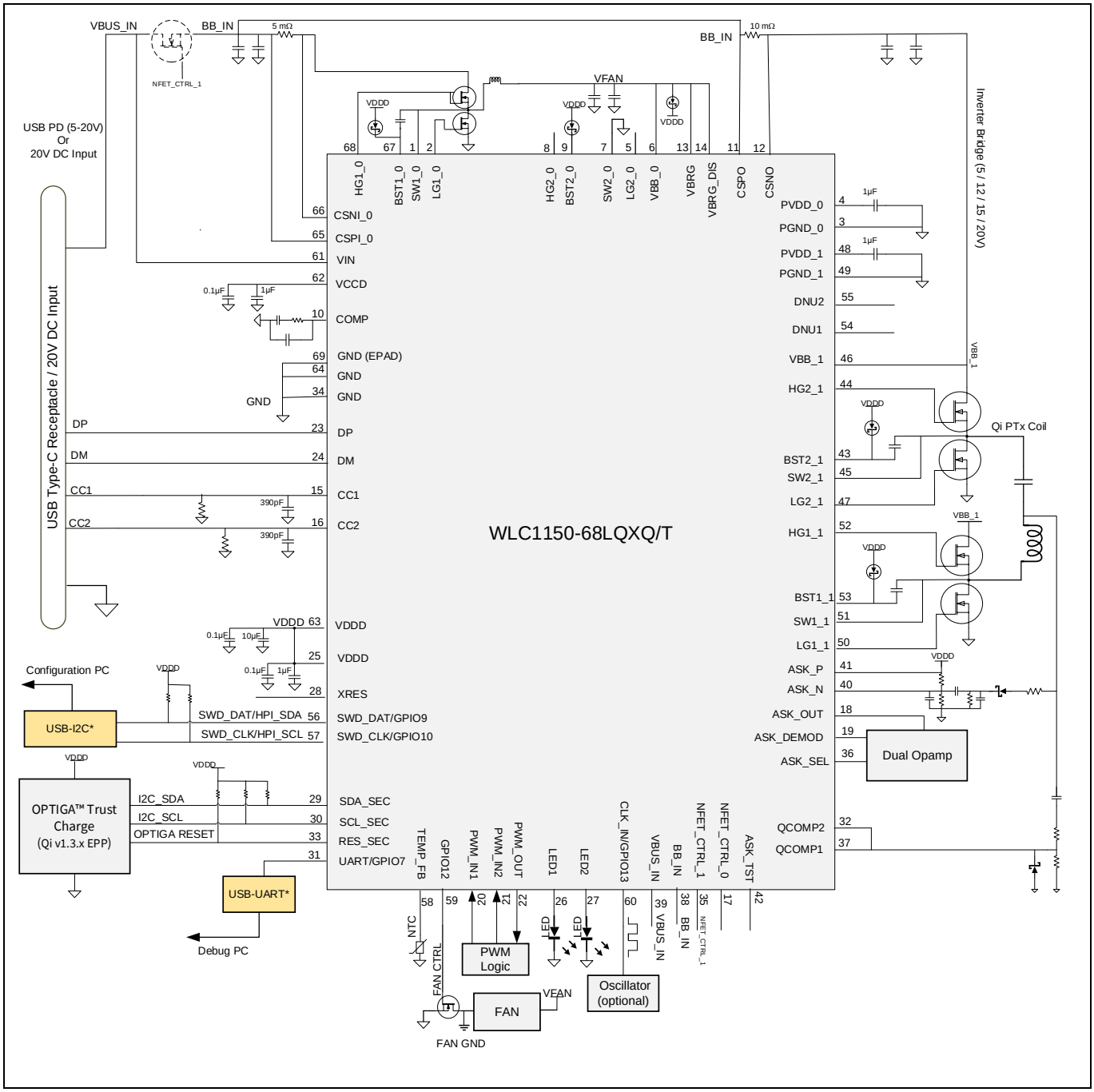

Figure 2 Single Stage wireless power transmitter system with WLC1150

About WLC1150

Figure 3 shows WLC1150 for a wireless transmitter with fixed DC input voltage. An input voltage ranging from 5 V to 20 V is supported for this configuration. The buck-boost stage regulates the VBRG or the inverter input voltage to 12 V or 20 V based on receiver type as identified during ping phase. The MP-A2 coil control requirements of fixed frequency and variable phase angle to regulate the power flow to the receiver is achieved through the WLC1150. For this configuration, an external switching regulator is required to power the cooling fan.

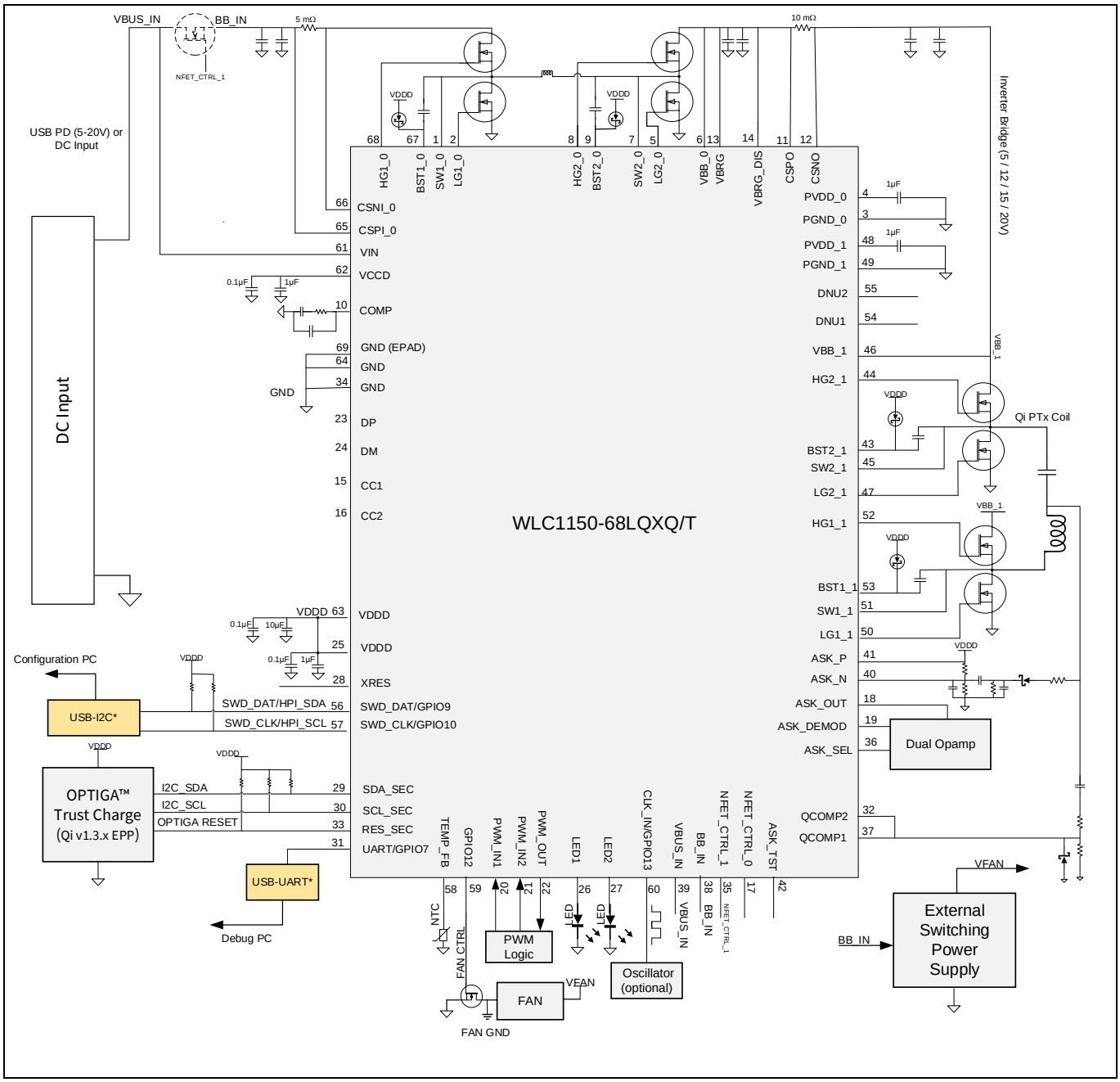

Figure 3 Dual stage wireless power transmitter system with WLC1150

1.3 MP A2 power transmitter board (REF_WLC_TX50W_N1)

REF_WLC_TX50W_N1 power transmitter board, based on WLC1150, is both high power compatible and Qi-compliant wireless power transmitter design with MP-A2 type transmitter coil. The transmitter unit works with an input from a Type-C USB-PD adaptor for Qi receivers and Infineon high power receiver. The fixed 20Vdc input compatibility is available for Infineon high power receiver only. The transmitter board offers the following value propositions:

- Low bill of materials (BOM) count, cost for 50 W power delivery, and Qi v1.3.2 compliance
- Single MCU system that handles USB-PD, inverter control, and Qi state machine
- Form factor comparable to off-the-shelf chargers
- CE/RE compliant design; ready-to-market layout
- Critical system-level parameters (foreign object detection (FOD) power loss threshold, inverter switching frequency, and so on.) are configurable using a utility

The transmitter board is developed on a compact four-layer PCB. The PCB area under the transmitter coil houses the cooling fan. The acrylics around the coil and the interface surface is designed in a way to direct the air on top of transmitter coil. It cools the receiver and the interface surface. The board top-side placement section with key sections is shown in Figure 4. The wireless charger transmitter board key specifications are listed in Table 2.

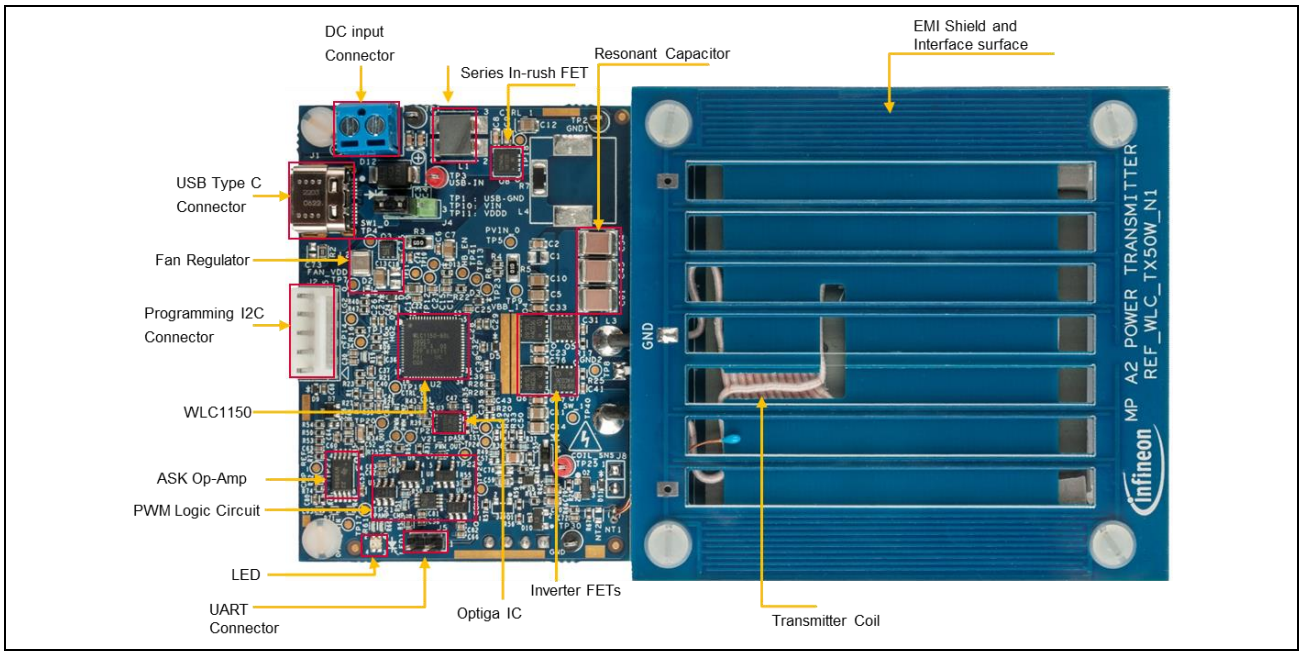

Figure 4 REF_WLC_TX50W_N1 MP-A2 50 W transmitter board key sections

Table 1 REF_WLC_TX50W_N1 operating modes

Mode	Input adaptor/supply	Rx max output	Qi/Proprietary
#1	20 V Fixed DC (65 W)	50 W (20 V, 2.5 A)	Proprietary
#2	20 V PDO or PPS (65 W)	50 W (20 V, 2.5 A)	Proprietary
#3	15 V PDO (30 W)	15 W	Qi EPP compatible
#4	12 V PPS (30 W)	15 W	Qi EPP compatible
#5	5 V – 16 V PPS	7.5 W	iPhone 7.5 W charging

Table 2 REF_WLC_TX50W_N1 power transmitter board brief specification <TBD>

Parameter	Value
Feature list	
Compatible transmitter coil	1-coil MP-A2
Input type/Connector	USB Type-C, Power supply 20 V
Input PDO voltage Fixed power supply	15 V/ 20 V 20V
Typical output power	50 W for High-power protocol mode 15 W for Qi protocol
Peak system efficiency	>89% with Infineon high power receiver (REF_WLC_RX50W_N1). >83% with test receiver WRM483265-10F5-12V-G
Inverter switching frequency	110 kHz to 145 kHz
Standby power	With PDO: 8 mA at 5 V i.e., 130 mW With power supply: 8 mA at 20 V i.e., 160 mW
ASK demodulator	AC voltage (coil voltage) based and DC current based
FSK modulator	Meets Qi v1.3.2 requirements
Foreign object detection	Based on power loss, Q-factor, and resonant frequency
Other Protections	OVP, UVP, OCP, short-circuit protection (SCP), OTP
Authentication	Compatible with Qi v1.3.2 requirements
PCB details	64 x 47 mm / 4 layers / 2-1-1-2 oz. copper
Operating temperature	0°C to +85°C
Storage temperature	–40°C to +125°C
Other features	Samsung proprietary extension, up to 7.5 W charging for iPhones
Compliance / Certification	
USB certification	USB-PD version 3.1
Qi Pre-compliance	Qi 1.3.2
Conducted and radiated emission pre-compliance	CISPR 32 Class B or equivalent

2 Hardware design

This section covers the requirements and design or selection criteria for the single-stage wireless transmitter board key components shown in Figure 5. The blocks in gray indicate the power stage components. The blocks in green are the circuit blocks for the control section of the WLC1150-based wireless transmitter design.

The buck-boost converter design is not included in this section for a dual-stage transmitter with the WLC1150. Contact Infineon for information on the buck-boost converter and interface with the WLC1150 for a dual-stage wireless transmitter.

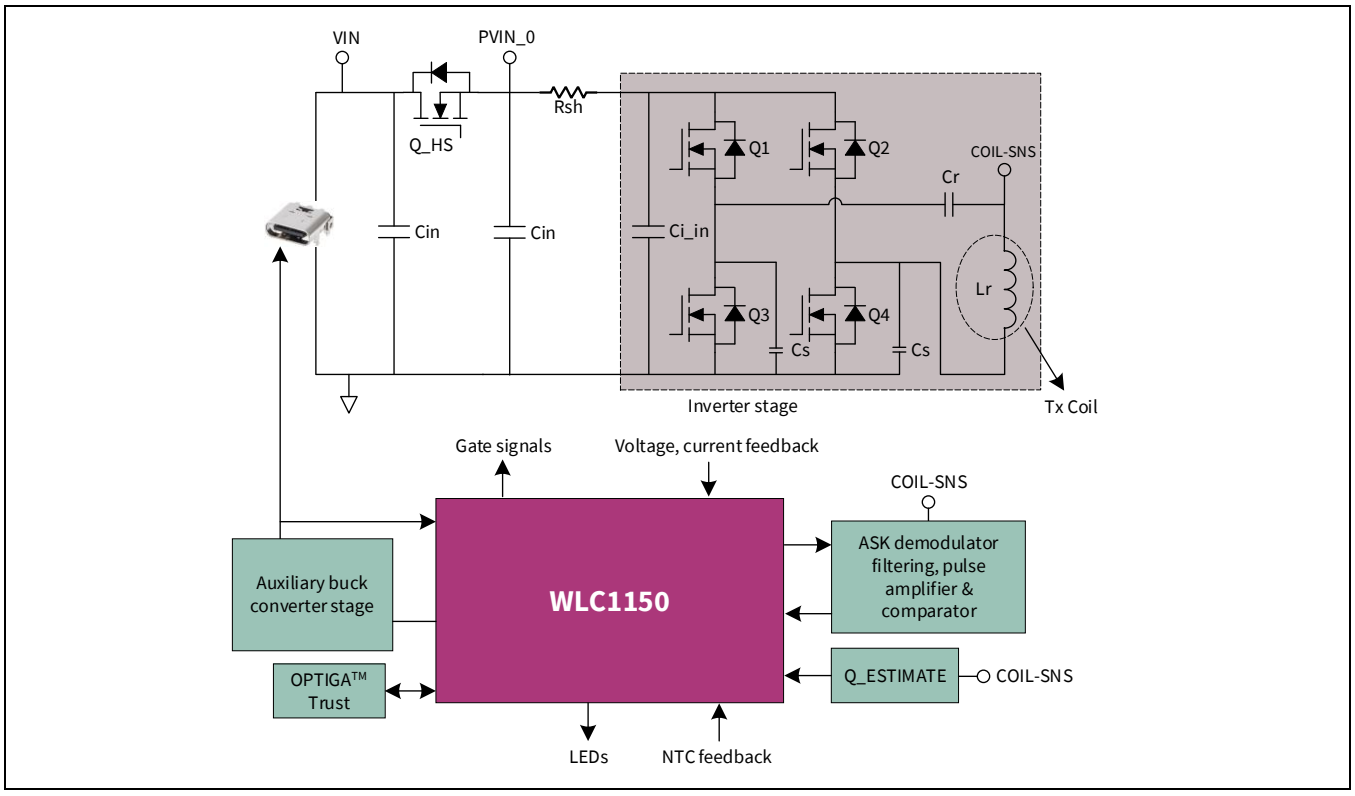

Figure 5 WLC1150-based single stage wireless transmitter board key components

2.1 Inrush current and input transient protection

The transmitter board needs protection elements on the power supply input to cater to the needs of input surges and inrush currents. The design can also include EMI filters based on measurements of emissions.

. The consumer NFET can decouple the transmitter board electronics from input in the case of sustained overvoltage events. However, for overvoltage from transient surges, the protection needs to be from passive methods like transient voltage suppressor (TVS) diodes.

Selecting the TVS diode for surge protection

1. The reverse working or standoff voltage rating of the diode should be more than the maximum operating input voltage of the system. The maximum reverse leakage current should also be lower (<0.5mA) so that the contribution of TVS diode to standby power is negligible.
2. The peak pulse current rating is higher than the surge current to be protected against.
3. The clamping voltage should be lower than the system withstanding voltage.

The WLC1150 has an integrated USB Type-C PD controller and complies with the latest USB Type-C and PD specifications. The bulk capacitance between the USB input (often referred to as VBUS) and ground results in a large inrush current. The USB-PD specifications mandate the sink to limit the input inrush current at attach. The bulk capacitance is required to minimize the switching ripple generated from inverter switching and cannot be minimized to bring down the inrush current. To comply with the inrush current requirements of the transmitter unit, the WLC1150 has an integrated high-voltage gate driver to drive a consumer NFET on VBUS. The gate driver has a slow turn-on feature that can be used to avoid a sudden inrush of current.

Consumer NFET selection and interface to WLC1150

1. The MOSFET should have a voltage rating higher than the maximum operating input voltage. The current rating should be higher than the maximum input current during overload.
2. Select a low $R_{DS(on)}$ MOSFET for low conduction losses. This MOSFET works as a load switch and will not have any switching losses.
3. Use the NFET_CTRL_1 pin of WLC1150 (pin 35) to drive the consumer NFET. There is no need for a gate resistance or gate-to-source pull-down resistance for this FET.

In addition to these components, the input section can have EMI filters. Note that the effective input capacitance before the consumer FET should not cross the requirements of USB-PD, which can result in an inrush current above the specifications.

2.2 Current sense resistor selection

WLC1150 uses an internal high-side current sense amplifier (CSA) for input current measurement. The amplifier can operate at a high common-mode voltage of up to 21.5 V. The current feedback in wireless charging is used for inverter power measurement for power loss calibration and FOD, along with overcurrent and short circuit protection. The feedback is also used for ASK demodulator through the current path.

For the CS resistor R_{sh} , WLC1150 requires a 10 mΩ CS resistor for a good sensing range and ADC resolution.

Sense resistor part selection

Sense resistor losses and ease of routing determine the selection of the resistor package. The resistor losses are:

$$P_{Rsh} = {I_{Rs}}^2 R_{Rsh}$$

$$I_{Rsh} = I_{in-avg}$$

The resistor package should be rated to handle the power dissipation of at least double the value of P_{Rsh}. It is also recommended to take the feedback traces from the sense resistor as Kelvin connection for accuracy of feedback. Considering the pitch between traces and pads, the 0805 or 1206 package is most suitable for CS resistors.

2.3 Inverter power stage

The inverter stage in REF_WLC_TX50W_N1 is shown in Figure 6. The power stage consists of a filter capacitor at input, and a full-bridge inverter power stage feeding a resonant tank made up of transmitter coil (Lr)and resonant capacitor (Cr). The four MOSFETs form a full-bridge inverter as recommended for the MP-A2 coil. When Q2 is held in OFF state and Q4 is held in ON state while Q1 and Q3 are switching, the inverter stage operates as half-bridge inverter. The snubber capacitors C_S aid in reducing dV/dt during MOSFET turn-on and turn-off on each switching node. With proper tuning of snubber capacitor and dead time, the ZVS turn-on of FETs with minimal body diode conduction can be achieved.

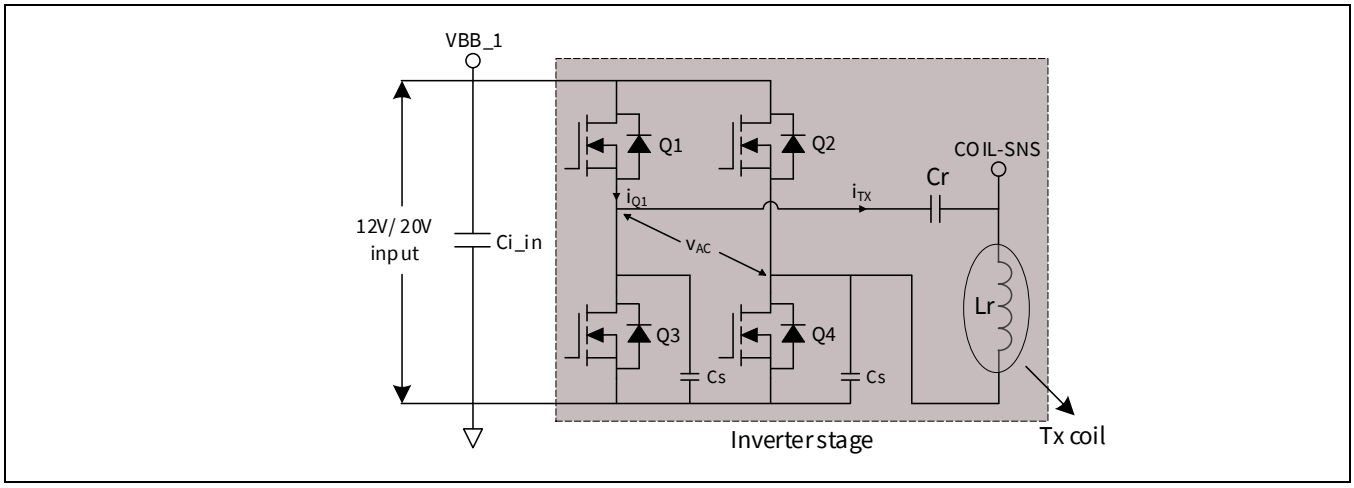

Figure 6 Inverter stage in REF_WLC_TX50W_N1

The steady-state waveforms for the inverter stage in full-bridge operation with 180° phase are shown in Figure 7. The waveforms represent the converter state in normal operating range, i.e., after the resonant peak in frequency characteristics. The impedance seen by the bridge is inductive; therefore, the tank current (i_{TX}) is lagging behind the tank voltage (V_{AC}).

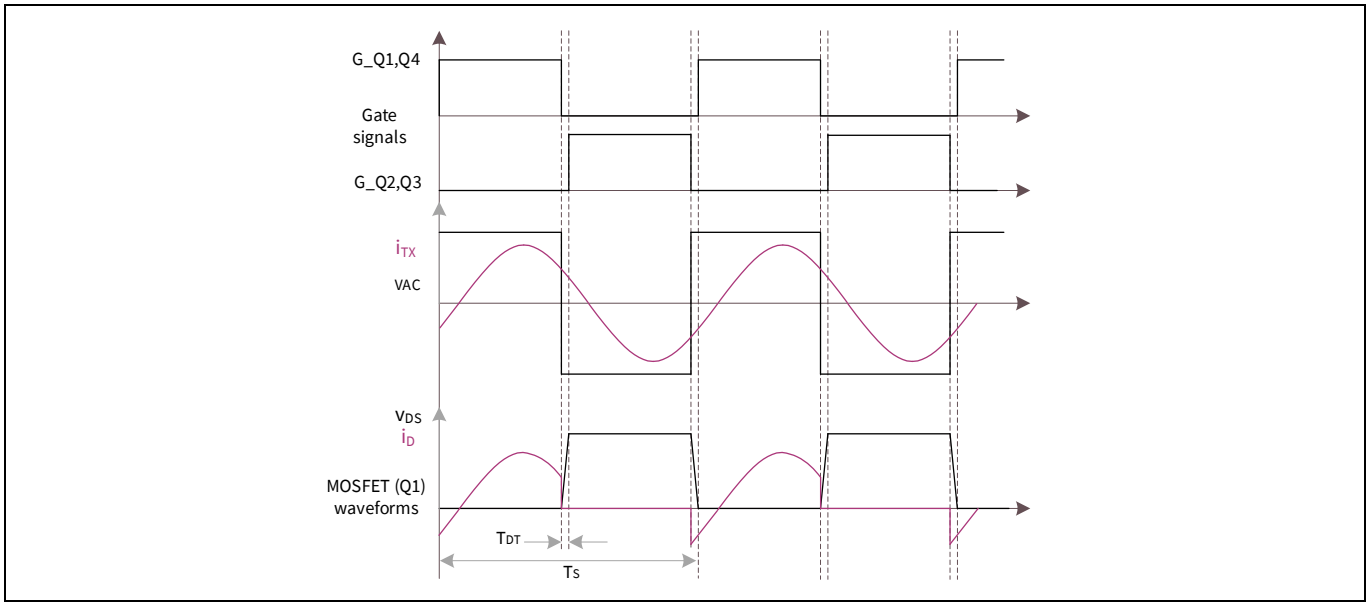

Figure 7 Inverter steady-state waveforms in full bridge operation

For regulation, the WLC1150 applies phase-angle control in full-bridge mode and duty control in half-bridge mode. For phase-angle control, the gate pulses have a fixed 50% duty, whereas the overlap between adjacent MOSFET gate pulses regulates the power flow to the receiver.

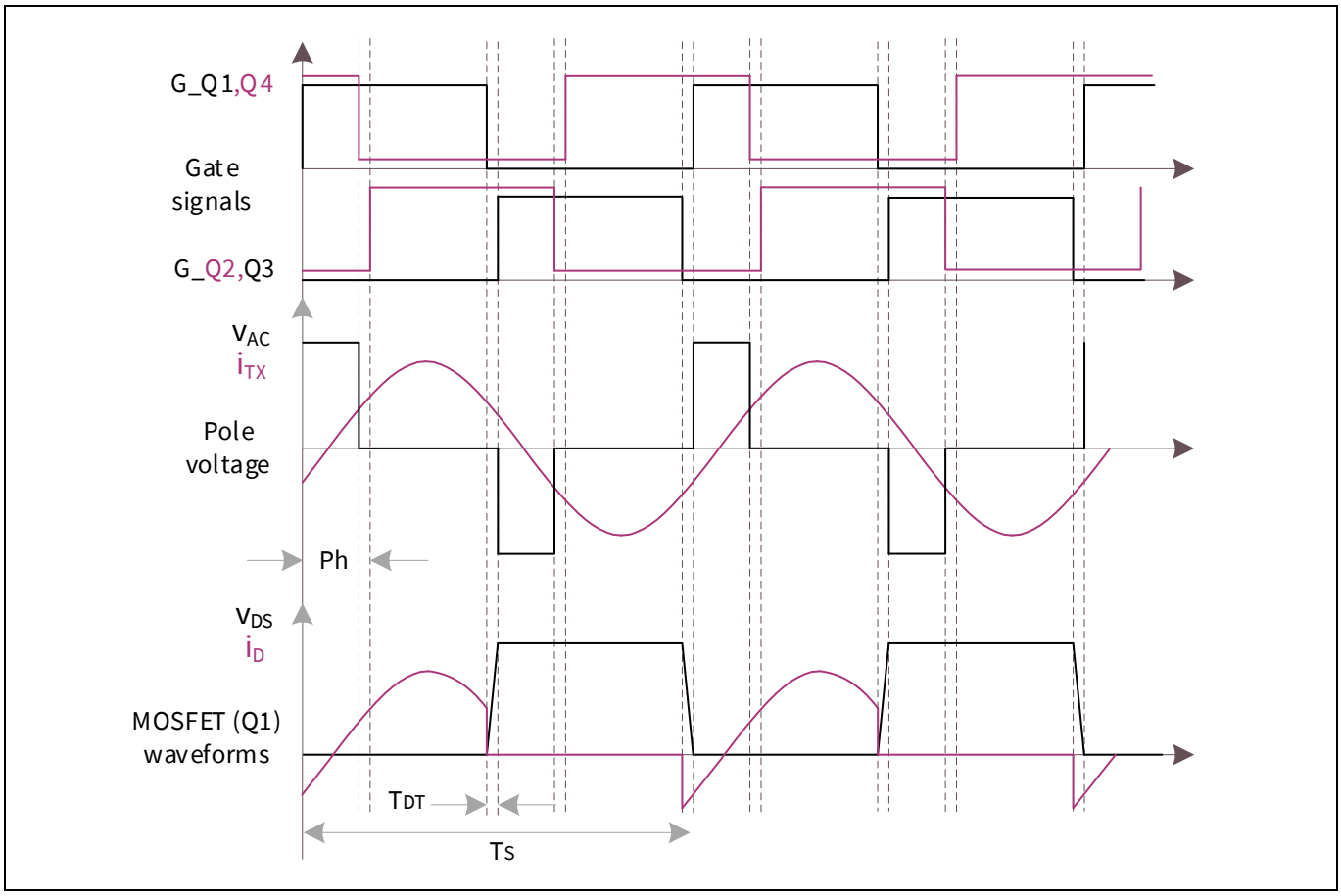

Figure 8 Inverter steady-state waveforms in full-bridge, phase-angle control operation

2.3.1 First harmonic approximation (FHA) analysis

In the design calculator worksheet, FHA analysis is used to compute the resonant tank performance with respect to frequency for the operating frequency range.

It computes the operating frequency, primary side current (rms and peak), and input current phase based on the design input of Input Voltage, Output Voltage, O/P power, Rx coil alignment, and TX coil alignment.

The equivalent circuit diagram is shown in Figure 9 for a loosely coupled WPT system.

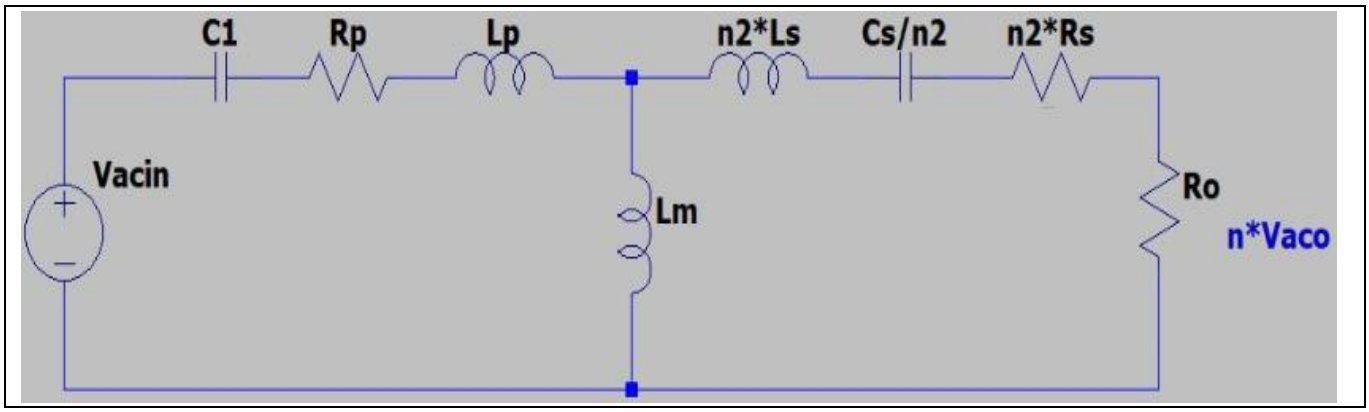

Figure 9 Inverter steady-state waveforms in full-bridge, phase-angle control operation

Where,

C1: Tx resonant capacitor

Cs: Rx resonant capacitor

$Lp = L'_{TX}(1-k)$

L'_{TX}: Tx coil inductance when Tx coil is mated with Rx coil

k: Coupling factor

$Ls = L'_{RX}(1-k)$

L'_{RX}: Rx coil inductance when Rx coil is mated Tx coil

N: Turn ratio of Tx coil and Rx coil

$Lm = L'_{TX} - Lp$

Rp: Tx side coil ac resistance (Rac)

Rs: Rx side coil ac resistance (Rac)

$$Ro = \frac{8 * n^2}{\pi^2} * R_L$$

Where, R_L is resistive load on Receiver.

System gain can be written as

$$V_{gain}(s) = \frac{Zm(s) * Ro}{\big(Zp(s) * Zs(s)\big) + \big(Zm(s) * (Zp(s) + Zs(s) + Ro)\big) + (Zp(s) * Ro)} * R_L$$

Where,

$$Zs(s) = Rs * n^2 + (s * Ls) + \left(\frac{1}{s * Cs}\right)$$

$$Zp(s) = Rp + (s * Lp) + \left(\frac{1}{s * C1}\right)$$

$$Zm(s) = s * Lm$$

Output power of Rx is a function of system gain, Input voltage, and R_L.

$$Pout_{Rx(freq)} = \frac{|Vgain(s)|^2}{Ro} * |V_{acin}|^2$$

Where, V_{acin} is first harmonic of input Tx supply voltage.

$$V_{acin} = \frac{4 * V_{dc}}{\pi}$$

V_{dc}: Input DC supply voltage to Tx.

The Tx operating frequency(fop) can be calculated for a given power by plotting the Power vs Frequency curve (see Figure 10) for a fixed input, R_L, and coupling factor.

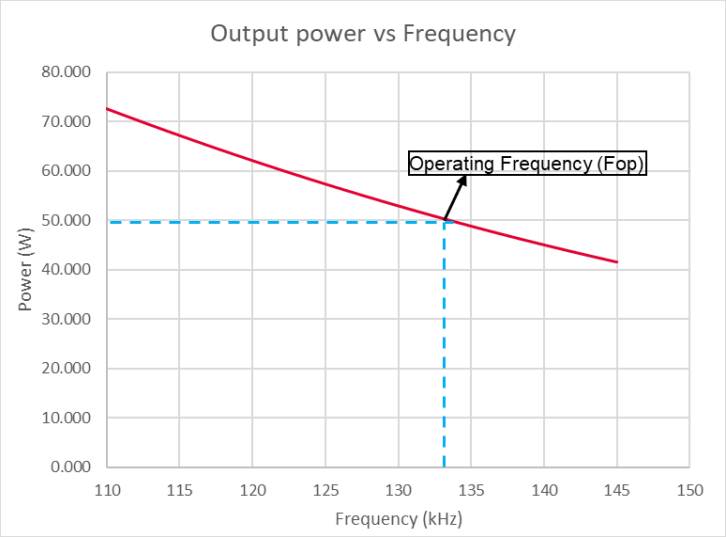

Figure 10 Receiver Power (Pout_rx) vs Frequency curve

After finding the Tx operating frequency (fop), other parameters can be computed.

Tx coil peak current at operating frequency (Fop) is calculated as,

$$I_{TX\_pk}(Fop) = \left|\frac{V_{acin}(s)}{Z_{in}(s)}\right|$$

Where, Z_{in} is the total input impedance at the Tx side and can be written as the following equation:

$$Z_{in}(s) = Zp(s) + \frac{Zm(s) * (Ro + Zs(s))}{Zm(s) + Ro + Zs(s)}$$

Tx Input DC current at operating frequency is calculated as,

$$I_{IN}(Fop) = \frac{2}{\pi} * \left|Re\left(\frac{V_{acin}(s)}{Z_{in}(s)}\right)\right|$$

Input current phase angle is calculated as,

$$\Phi_{in}(F_{op}) = (\pi - \measuredangle Z_{in}(F_{op}))$$

Note: The FHA is a modelling technique, used to analyze the performance of resonant power converters. The assumption is that only the first harmonic signals contribute to the power transfer. Especially for the commonly applied LLC resonant converter, the FHA modelling technique becomes inaccurate when operation of the converter is well below series resonance. This is mainly caused by the non-linearity of the output rectifiers, which is not taken into consideration in the FHA.

2.3.2 Inverter bridge decoupling capacitors

The inverter stage has decoupling capacitors on each half-bridge leg to reduce the switching power-loop inductance and the associated Vds turn OFF overshoots and ringing in the inverter stage MOSFETs. In addition, there are bulk capacitors after the buck output CS resistors and high-frequency noise-decoupling capacitors close to the inverter bridge.

The bulk capacitors ensure that the reactive current in the inverter bridge is contained within the inverter stage and is not seen by the buck output capacitors. In this way, the inverter bridge CS resistor sees only the active current drawn by the inverter. The capacitor rms current can be calculated as,

$$I_{C_{INrms}} = \sqrt{{I_{TXrms}}^2 - {I_{IN}}^2}$$

where I_{TXrms} is coil RMS current and I_{IN} is the average input current. The worst-case value will be obtained when the transmitter is delivering power in the least coupling position.

2.3.3 Transmitter coil selection

The transmitter coil parameters (inductance and ferrite shield construction) for the MP-A2 coil are from the Qi specifications. The parameters for the MP-A2 coil from [1] are summarized in Table 3.

Table 3 MP-A2 transmitter coil parameters

Parameter	Value	Tolerance
Self-inductance	10 µH	±10 percent
Coil outer diameter	48 mm	±0.5 mm
Coil inner diameter	19 mm	±0.5 mm
Number of turns	12	–
Number of layers	1	–
Ferrite shield thickness	1.5 mm	–
Coil to shield minimum gap	1.0 mm	–
Coil top surface to interface surface gap (dz)	3.0 mm	+0.5/–0.25 mm
Shield extension beyond coil	2.5 mm	–

While most of the parameters of the transmitter coil are already taken care of by the manufacturer, the dz gap must be set using the right combinations of spacers and acrylic. The coil assembly used in REF_WLC_TX50W_N1 is shown in Figure 11. The coil assembly is mounted on the coil PCB using double-sided tape. The interface surface is an acrylic sheet, and the gap between the sheet and coil is set using four nylon spacers. The spacer height is selected so that the dz gap is close to the Qi-recommended nominal value.

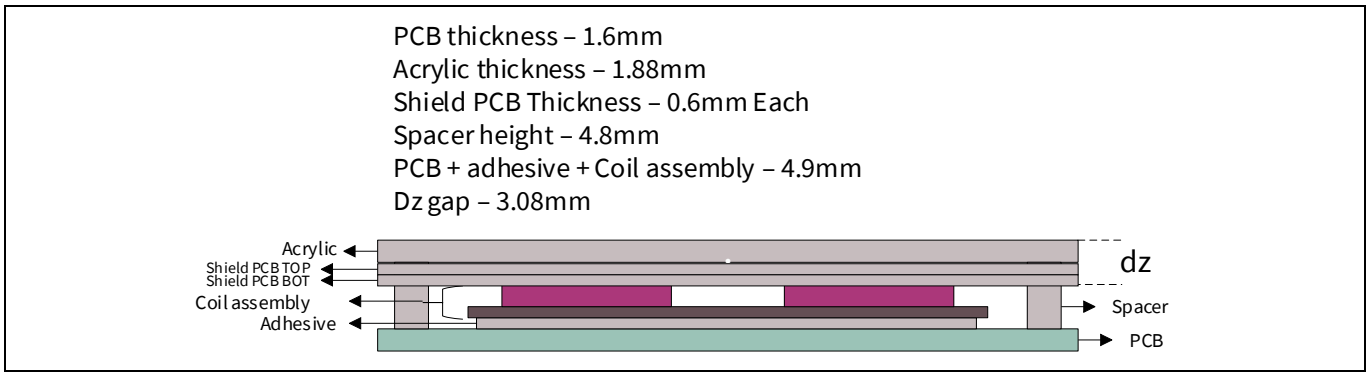

Figure 11 MP-A2 coil assembly and associated measurements in REF_WLC_TX50W_N1

2.3.3.1 Transmitter coil losses

The coil losses consist of conduction losses in the windings and core losses in the ferrite shield. For conduction losses, the coil resistance—both DC resistance and skin-effect-induced AC resistance—comes into the picture. To precisely predict the conduction losses, use the Q factor curve provided by the manufacturer and compute the total resistance at the operating frequency. Alternatively, use an impedance analyzer to obtain the total coil resistance at the operating frequency (see Figure 12).

$$P_{coil-cond} = {I_{TXrms}}^2 R_{total}$$

$$R_{total} = \frac{Q_{Fs-inv}}{2\pi F_{Sinv} L_{tx}}$$

Where, I_{TXrms} is coil RMS current and R_{total} is the sum of AC and DC resistance of the coil. The worst-case coil current can be estimated through the FHA analysis or through actual measurements. The maximum coil current will be observed when full power is delivered in a low coupling scenario. The current magnitude is higher due to the large reactive current component in it.

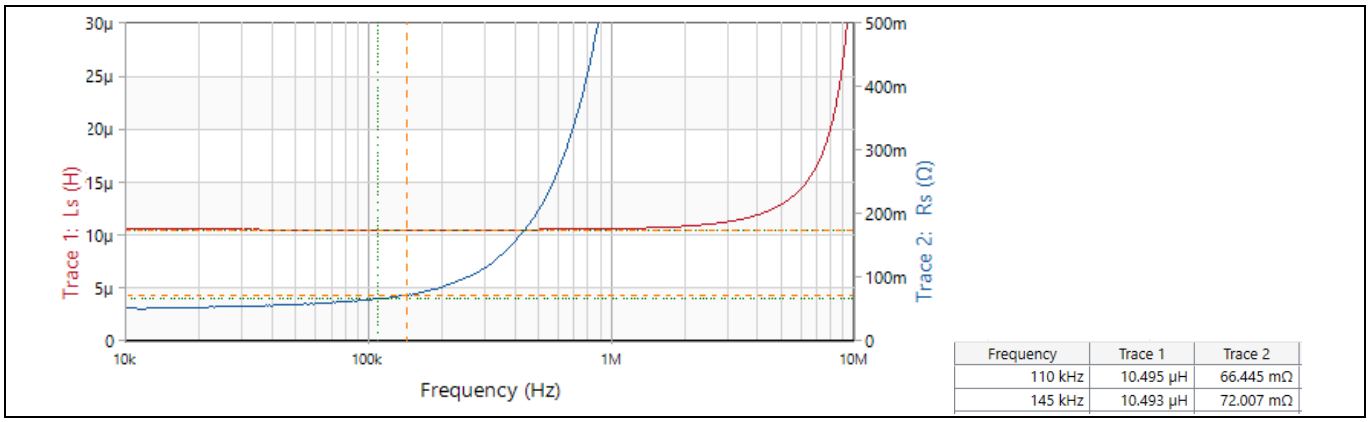

Figure 12 Inductance and Resistance measurements on MP-A2 coil used in REF_WLC_TX50W_N1

Qi recommends the use of a Ni-Zn or Mn-Zn ferrite core for shielding the coil. The ferrite core will have alternating magnetization, resulting in core losses. The core loss computation is similar to that of the buck inductor:

$$P_{Core} = C {F_{S-inv}}^{\alpha} {B_{pk}}^{\beta} V_e$$

$$B_{pk} = \frac{L_r I_{TX\_pk}}{N A_C}$$

Where, the constants C, α, and β are specified by the manufacturer:

V_e is the core material volume.

B_{pk} is the peak flux in the core.

A_C is the core cross-section area (product of the ferrite width and thickness).

2.3.3.2 Transmitter coil part selection guidelines

1. The selected part should match the Qi requirements for the MP-A2 coil (electrical design, ferrite shield design, and so on).
2. Inductance value tolerance should not be more than ±10%.
3. A high Q-factor coil (low total resistance for the 110 kHz to 145 kHz range) is favorable for low losses.

2.3.4 Resonant capacitor selection

The Qi-recommended resonant capacitor value to be used with the MP-A2 coil is 247 nF ±5%. The resonant capacitors can be realized using a single capacitor or through a capacitor bank. The resonant tank is a series LC tank and the capacitor currents are same as the coil currents. The losses in the capacitor are largely due to the capacitor rms alone.

The loss in resonant capacitor or capacitor bank is from the equivalent series resistance (ESR) capacitor:

$$P_{Cr} = {I_{TXrms}}^2 \frac{R_{Cr}}{N_{Cr}}$$

Where, R_{Cr} is the ESR of the individual capacitor and N_{Cr} is the number of capacitors in the bank.

2.3.4.1 Resonant capacitor part selection guidelines

1. The selected part should match the Qi requirements for the value and tolerance. The capacitance value should not vary throughout the operating frequency and voltage range. A capacitor with C0G-type dielectric or equivalent should be used.
2. The capacitor bank RMS current rating should not result in temperature rise beyond the capacitor rating.
3. The voltage rating of the resonant capacitor must ensure failsafe operation for all phases in the Qi state machine. During power transfer, the capacitor voltage is low. However, there are certain operating cases that can result in high-voltage across the resonant capacitor.
   a. A Sudden change in coupling when delivering power to a load can momentarily increase the load voltage, tank current, and hence the capacitor voltage. Though the control loop will eventually bring down the current, the capacitor should not fail during this momentary rise in voltage.
   b. The lowest operating frequency of the transmitter is close to the resonant frequency of the primary LC tank. If the receiver is removed from the interface surface when the power is being delivered at its lowest operating frequency, the primary LC tank will be left energized and close to resonance until a packet timeout shuts down the inverter. The operation close to resonance results in a large capacitor voltage, which the capacitor has to handle without failure. This voltage can be estimated using FHA for the primary tank alone, and the value for the 20-V input case needs to be considered.

To prevent capacitor failure from voltage stress, the recommended voltage rating is 200 V. This is in line with data in the Qi specification, where the capacitor voltage is predicted to reach 200 V pk-pk.

2.3.5 MOSFET selection for inverter stage

The MOSFET voltage rating should be higher than the maximum input voltage value, which includes the input OVP level. The current rating should be greater than the peak transmitter coil current value. The MOSFET current rating at the highest case temperature rating should be considered for reliable operation.

$$V_{ds-pk} = \max\left((1.5 \text{ x } V_{in}), \text{Input OVP level}\right)$$

$$I_{ds-pk} = I_{TX-pk}$$

Power loss in the MOSFET is another key parameter that governs the MOSFET part selection. As shown in Figure 7, the MOSFET current is negative during turn-on before applying the gate pulse, resulting in ZVS turn-on. However, the MOSFET turn-off is hard and is the dominant switching loss. Additionally, each MOSFET conducts for half of the switching period, based on which the MOSFET parameters for losses are as follows:

$$I_{Qrms} = \frac{I_{TX-pk}}{2}$$

$$P_{cond} = {I_{Qrms}}^2 R_{ds(on)}$$

$$P_{SW} = P_{SW-OFF} = \frac{1}{2} V_{in}\, I_{SW,off}\, t_{OFF}\, F_{op}$$

$$t_{OFF} = \left(R_{GOFF} C_{iss} \frac{V_{gp}}{V_{gth}}\right) + \left(\frac{R_{GOFF}}{V_{gp}} V_{in} C_{rss}\right)$$

Where,

R_{GOFF} is the gate resistance for falling gate voltage (sum of MOSFET internal gate resistance, driver pull-down resistance, and external gate resistance if any).

C_{iss} and C_{gd} are the MOSFET input and reverse transfer capacitances respectively.

V_{gth} and V_{gp} are MOSFET gate threshold and gate plateau voltages respectively specified in the datasheet [2].

The MOSFET capacitance C_{gd} is non-linear and it is difficult to incorporate the non-linearity in the loss computations. One method to include the non-linearity is to average out the C_{rss} as in [4].

$$C_{gd} = \frac{C_{rss}@0V + C_{rss}@V_{in}}{2}$$

The turn-off current $I_{SW,off}$ is the coil current at the instant when the bridge voltage changes polarity. See Figure 13 for the identification of MOSFET currents during turn-on and turn-off from the coil current. The current can also be predicted from the FHA model using the tank current magnitude and input current phase angle.

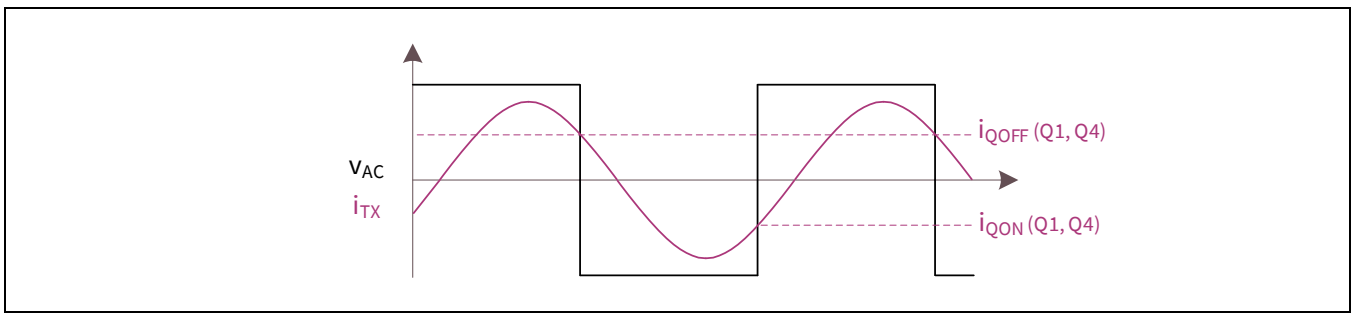

Figure 13 Identifying MOSFET turn-on and turn-off from coil voltage and current waveforms

2.3.5.1 Gate drive power

The gate charging and discharging consumes a certain amount of power, which is supplied from the gate driver supply. The gate power is a function of total gate charge and switching frequency:

$P_{GATE} = Q_G V_{DDD} F_S$

Where,

V_{DDD} is the driver supply voltage.

Q_G is the gate charge. The value is available in the datasheet [2] and must be selected for the V_{DDD} level.

2.3.5.2 MOSFET part selection guidelines

1. The selected part should be rated to handle for V_{ds-pk} and I_{ds-pk} over the entire operating temperature range specified in the datasheet.
2. For lower conduction losses, select a part with low $R_{DS(on)}$. For operation at low coupling, there will be large circulating current even at a light load, and a low $R_{DS(on)}$ helps in reducing light power losses.
3. The integrated gate drivers in WLC1150 drive the MOSFET gate with 5 V. The selected MOSFET part should be logic-level driven (should have the specified $R_{DS(on)}$ at gate voltage of 4.5 V).
4. MOSFETs with low C_{rss} and Q_G are preferred to keep switching losses to a minimum.
5. WLC1150 has integrated gate resistance, the value of which can be firmware-configured to up to 33 Ω, and internal pull-down resistors. There is no need for external gate resistors.
6. MOSFETs with SMD package are preferred. Avoid using a through-hole part because the lead inductance will add to switching losses and emissions.
7. The MOSFET package should be such that the thermal management is manageable with natural cooling, without occupying much PCB area. See section 4.4 for thermal management for MOSFETs.

2.3.5.3 Snubber capacitor for Inverter MOSFETs

The turn-on switching losses and C_{oss} losses are zero due to ZVS action. The time taken to discharge the MOSFET C_{oss} depends on the magnitude of the transmitter coil current at the instant of turn-off of the complementary MOSFET. The dV/dt will be dependent on the turn-off current and C_{oss} value.

$$\frac{dV}{dt} = \frac{I_{SW,off}}{C_{OSS}}$$

When the dead time is fixed, the $I_{SW,off}$ quickly discharges the device C_{oss} capacitance and the MOSFET body diode conduction starts. The MOSFET is turned on with ZVS when the gate signal is applied. The dead time between gate signals should be large enough to ensure that the drain voltage has completely discharged C_{oss} and initiate the body diode conduction.

If the minimum settable dead time is high relative to dV/dt, there will be a period where the body diode conducts for a short duration until the corresponding gate signal is asserted. There is a dead time loss in four MOSFETs, and for power levels like 50 W, the dead time loss has an impact on efficiency. A snubber capacitor (C_S) in parallel with one half-bridge device will slow down the dV/dt and ensure minimal body diode conduction, as illustrated in Figure 14.

The introduction of C_S has two advantages. It slows down the dV/dt of MOSFETs, thereby reducing emissions, and ensures a minimal body diode conduction period for good efficiency.

The snubber capacitor value is computed to bring the switch voltage to zero within the minimum settable dead time for the maximum turn-off current magnitude.

$$C_S = \frac{I_{SW,off-max}\, T_{DT}}{V_{IN}}$$

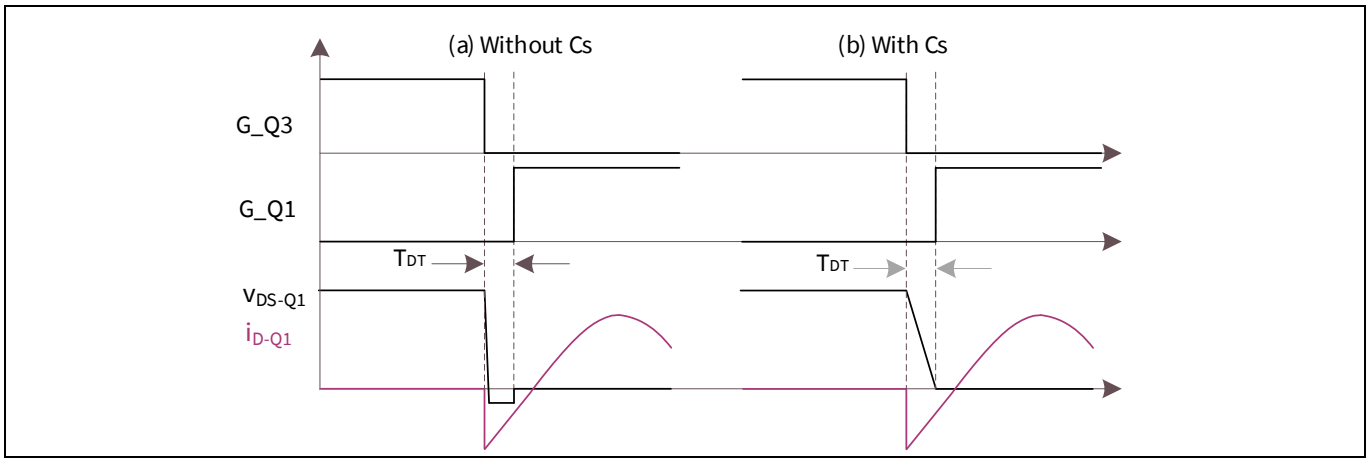

Figure 14 Impact of snubber capacitor (C_S) on switching performance

2.3.6 Bootstrap circuit

The buck stage FETs are driven using inbuilt gate drivers of WLC1150. The high-side MOSFET requires a voltage supply referenced at the switching node or source of Q_HS. A bootstrap circuit built using C_{boot} and D_{boot} is used (see Figure 15) to generate the supply for Q_HS.

The C_{boot} must be able to supply a charge (= 2*gate charge) and retain its full voltage. If that does not happen, there will be a significant amount of ripple on the Q_HS gate drive supply.

$$C_{boot} \gg 20C_g$$

$$C_g = \frac{Q_g}{\mathrm{VDDD} - V_{F-Dboot}}$$

$\mathrm{VDDD} = V_{dr}$ is the supply voltage and is the same as the Q_LS gate drive supply.

Q_g is the gate charge of the MOSFET.

$V_{F-Dboot}$ is the forward drop of bootstrap diode D_{boot}.

The chosen bootstrap capacitor (C_{boot}) should be able to withstand switch node voltage (SW1_0) + VDDD.

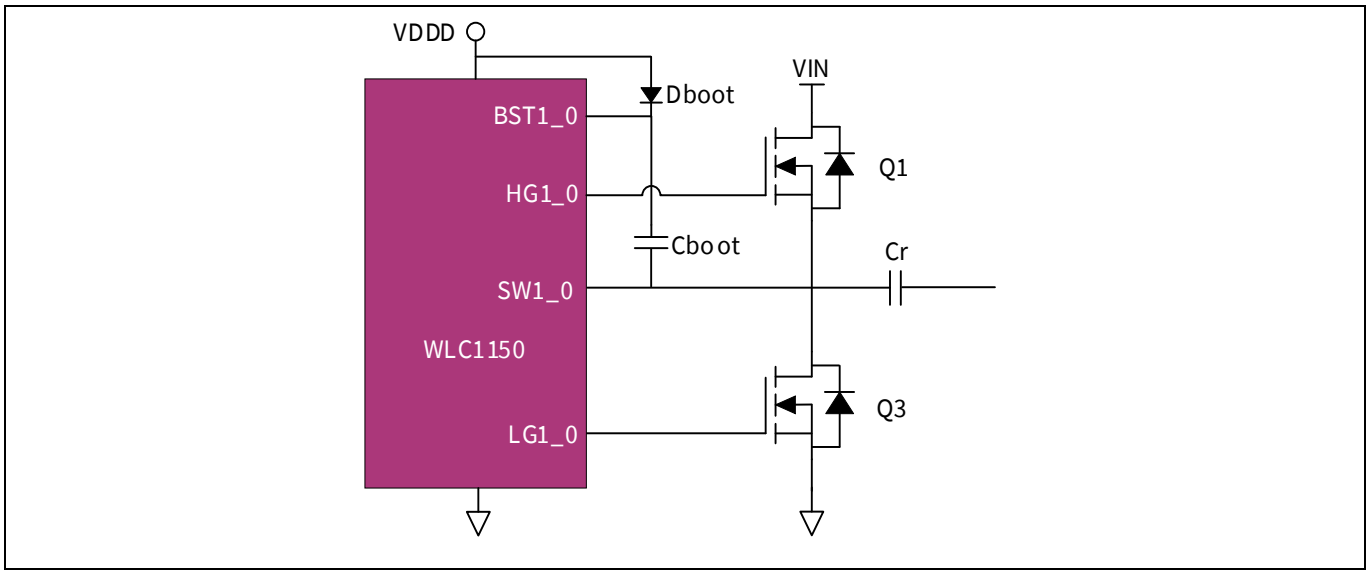

Figure 15 Bootstrap circuit

The bootstrap diode (D_{boot}) needs to be able to block the full-power rail voltage, which is seen when the high-side MOSFET (S1) is switched on. It must be a fast recovery diode to minimize the amount of charge fed back from the bootstrap capacitor (C_{boot}) into the VDDD supply, and similarly the high temperature reverse leakage current will be important if the capacitor must store charge for long periods of time. The current rating of the bootstrap diode is the average gate current:

$$I_{Dboot} = \frac{P_{GATE}}{\mathrm{VDDD}} = Q_G F_S$$

2.4 Control section

WLC1150 in the wireless transmitter application for MP-A2 requires minimum external circuitry. In the control section, signal conditioning circuits are required for Q factor estimation and the ASK demodulator, along with coil temperature measurement. The WLC1150 requires a standard decoupling capacitor network and bootstrapped circuit components to drive the power stage.

2.4.1 Q factor estimation with WLC1150

WLC1150 uses the coil voltage information to compute the coil Q factor. The presence of Rx, FO, or a combination of both before power transfer is reflected in the form of lower Q factor and change in resonance frequency. The primary resonant tank is excited with few pulses, and the Q factor and resonant frequency are estimated using the decaying coil voltage waveform, as shown in Figure 16. The coil voltage after excitation decays more slowly in the case of no Rx than in the case of Rx or FO present on the interface surface.

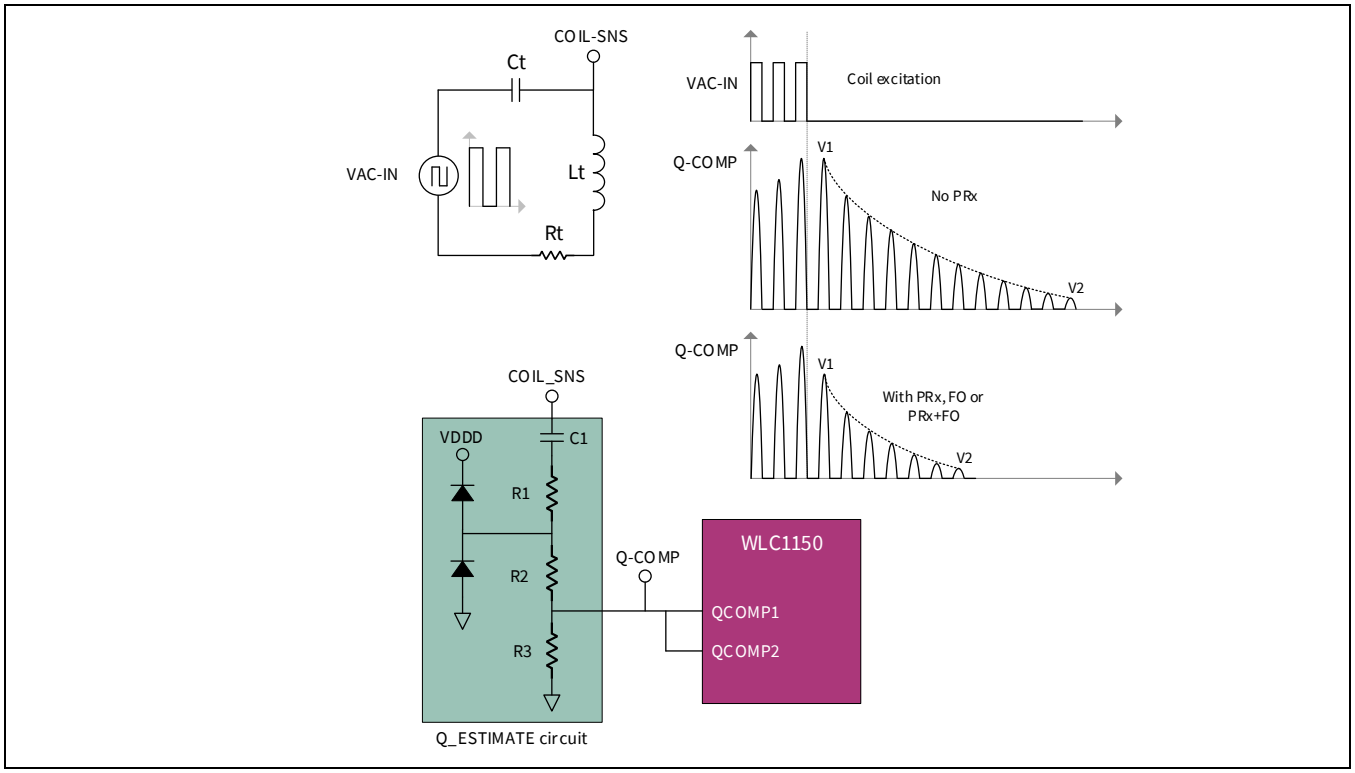

Figure 16 Q factor estimation using WLC1150

The Q factor is calculated from the decaying voltage waveform as:

$$Q = \frac{\pi\,(t_2 - t_1)\,F_r}{\ln\left(\frac{V_1}{V_2}\right)} = \frac{\pi\,N}{\ln\left(\frac{V_1}{V_2}\right)}$$

N is the number of cycles of the decaying waveform between intervals t_1 and t_2, where V_1 and V_2 are captured, and F_r is the resonant frequency of the primary tank under the influence of the receiver or FO, or both.

See the REF_WLC_TX50W_N1 schematics for the Q factor estimation circuit recommended for use with the WLC1150. The selection criteria for the components of the Q factor estimation circuit are as follows:

1. The clamping diodes should be of low leakage and low forward drop type. The leakage current of less than 100 nA at the highest operating ambient temperature is ideal. Standard recovery-type diodes rated for more than 100 V suit the application.
2. The diode clamping clamps the entire negative half of the coil voltage. The clamping current flows through the diode and R1. Set R1 to have less than 1 mA at the highest operating coil voltage for a low-loss circuit.
3. The WLC1150 has an internal pull-down resistor that is disabled only during analog ping and enabled for the rest of the duration.
4. R3 value should be approximately half of (R1 + R2).
5. R2 value should be slightly lower than (R3 || R_D).
6. C1 along with R1, R2 and (R3||R_D) forms a high-pass filter. Filter bandwidth should be less than the natural resonant frequency of primary LC tank.

2.4.2 ASK demodulator

The ASK demodulator circuit makes use of coil voltage and inverter bridge input current to demodulate the data from the receiver. The bridge input current feedback is routed to WLC1150 for current measurement. The information from the coil voltage, taken to WLC1150, is derived through some signal conditioning. The demodulated information from both paths is processed through a gain stage followed by a comparator to generate digital data. The configuration used in REF_WLC_TX50W_N1 is shown in Figure 17.

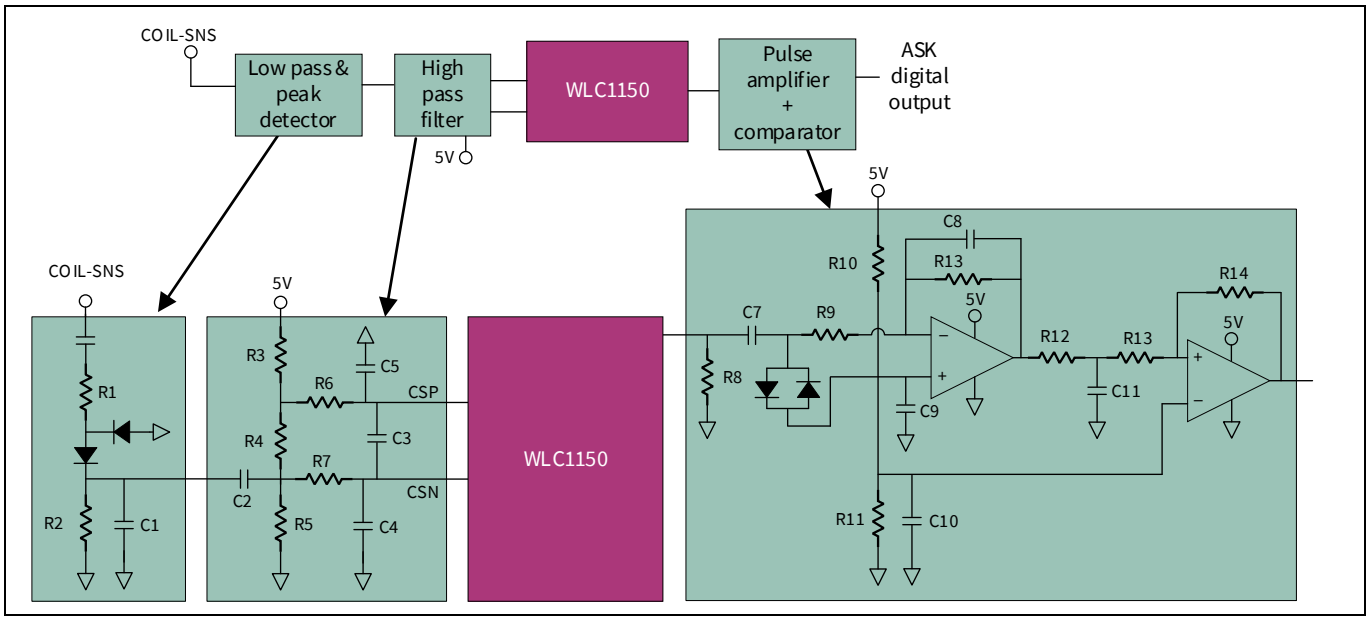

Figure 17 ASK demodulator circuit using WLC1150

The component values are tuned with the following considerations for REF_WLC_TX50W_N1 and are recommended for use with WLC1150:

1. Front-end low-pass filter and peak detector
   a. The negative blocking diode should be rated for the same voltage as the capacitor voltage rating; in addition, the diode should be of the fast recovery type.
   b. The dc blocking and peak charge hold capacitor should also be rated for 100 V.
2. High-pass filter
   a. The DC blocking capacitor C2 forms a high-pass filter with R5|| (R3+R4), and the filter bandwidth should be much lower than the ASK communication rate (2 kHz).
   b. Resistor ladder R3, R4, and R5 are selected to ensure >3 V at the CSP and CSN pins.
   c. The differential voltage across R4 should be greater than 5 mV.
   d. The differential filter formed by (R6 + R7) and C3 should have a bandwidth lower than the switching frequency.
3. WLC1150 gain settings
   a. For bridge current, the gain is set at 100.
   b. For voltage path, gain options range from 40 to 110; set the gain such that the input to amplifier stage is at (VDDD/2) which gives enough headroom for ASK-related swing.
4. Pulse amplifier and comparator stage
   a. R8 and C6 forms a low-pass filter; the bandwidth should be less than inverter switching frequency but greater than ASK communication frequency.
   b. Amplifier gain is set by R9 and R13.
   c. Offset to the gain output is set across C9 using R10 and R11; the offset value should be well within the common mode range of the op-amp.
   d. R12 and C11 form a low pass filter for amplifier output. Set the bandwidth slightly above 2kHz and well below the lowest inverter switching frequency.
   e. The reference to comparator across C10 is also set using R10 and R11; the reference should be slightly lower than the offset added to the gain stage output, which reduces toggles in comparator output when there is no modulation happening for ASK.
   f. The comparator hysteresis is set using R14 and R13 to minimize the chatter at comparator output between the data packets.

2.4.3 WLC1150-related circuitry

The WLC1150 is a highly integrated controller with built-in peripheral and programming flexibility to implement the Qi wireless power transmitter design along with USB-PD compatibility. The controller also has a built-in low-dropout (LDO) regulator to generate the logic supply (VDDD) and core supply (VCCD), eliminating the need for an auxiliary power supply unit.

Detailed pin descriptions and external requirements for each pin are listed in the datasheet [2].

2.4.4 NTC feedback

The NTC monitors the transmitter unit temperature and is placed close to the coil. The NTC, when mounted on the interface surface, can be used to detect temperature rise in the interface surface from the heat radiated from the FO. The NTC feedback interface to the WLC1150 ADC is a simple divider network with a filter, as shown in Figure 18. The NTC resistance is a function of temperature, and the accurate NTC resistance temperature characteristics are provided by the manufacturer (the characteristics can also be generated from NTC parameters, but the manufacturer-provided values account for non-linearities). The feedback to WLC1150 for the REF_WLC_TX50W_N1 is shown in Figure 18.

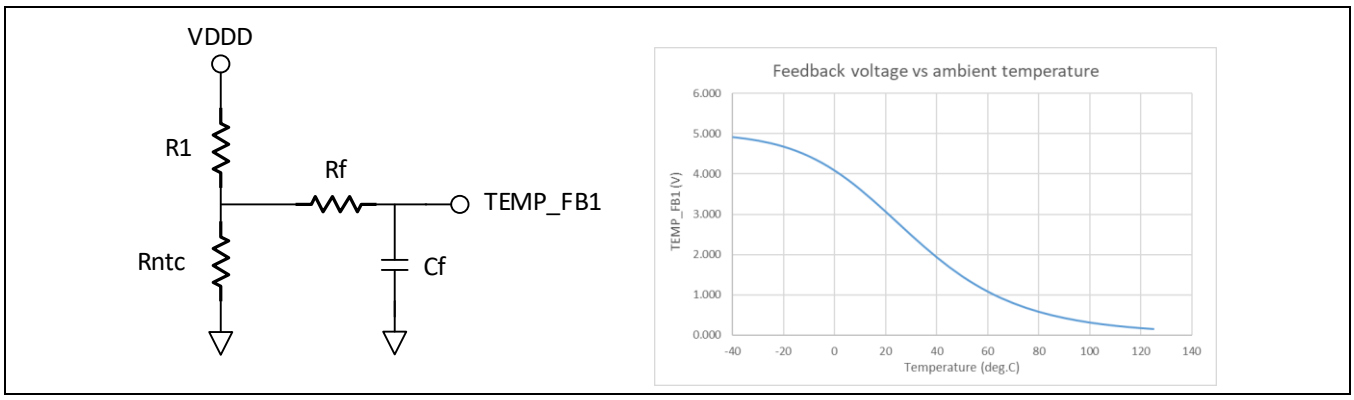

Figure 18 NTC interface to WLC1150 and NTC feedback value with temperature for REF_WLC_TX50W_N1

Design considerations:

1. The series resistor should ensure that the current in NTC at any temperature does not lead to a power loss greater than NTC's specified value.
2. The low-pass filter in the feedback path should have bandwidth low enough to discard the switching noise and ASK modulator frequency.
3. Good resolution in feedback around required trip and recovery points.

2.4.5 Other circuits

The authentication requirements for Qi v1.3.2 is realized using a security controller from Infineon. The OPTIGA™ Trust comes with full system integration for simple and cost-effective deployment of authentication. The OPTIGA™ Trust (U2) interface with the WLC1150 is through the I^2C protocol (see Figure 19), along with a control line for OPTIGA™ chip reset. The SCL and SDA have pull-up resistors for the I^2C lines.

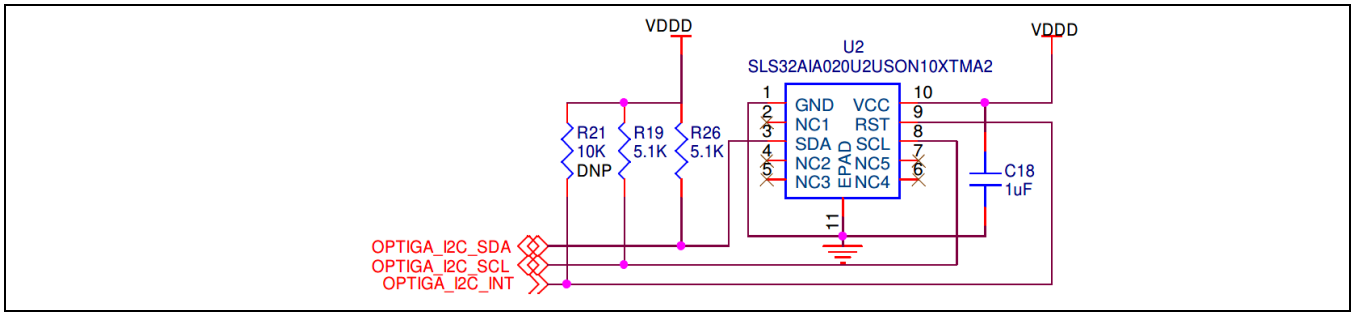

Figure 19 Authentication IC interface

2.5 Auxiliary buck converter for fan power

WLC1150 offers the drivers and control functionality required for an auxiliary buck converter, which derives power from input. The auxiliary power converter is used for powering up the cooling fan, which is critical for thermal management, especially at high power. This auxiliary buck converter needs the buck power stage (MOSFETs, an inductor and a capacitor). The control within the WLC1150 for this converter is with peak current mode control (PCMC); therefore, it utilizes a current sense resistor.

Auxiliary buck converter design guidelines with WLC1150

1. The current sense resistor for the auxiliary buck stage should be 5 mΩ. WLC1150 has an internal high-side CSA for amplification of the sense signal and is best suited with a 5 mΩ sense resistor.
2. The converter is switched at 400 kHz. The recommended inductance for the buck stage is 10µH, and output capacitance is 22 µF.
3. The gate driver for high-side FET need a bootstrapped power supply with a diode and 100-nF capacitor.
4. A half bridge type MOSFET array with a low $R_{SD(on)}$ and 5-V drive is recommended. The half-bridge package yields a small power loop.
5. Place a low-value decoupling capacitor close to the half bridge to keep the switching loop area as small as possible.

2.6 EMI-EMC shield

One of the challenges in wireless power transfer (WPT) for high-power transfer applications is EMI-EMC. Therefore, shielding provisions are required to shield the strong EMFs.

For more details on EMI-EMC shield, contact Infineon technical support.

3 Design example – 50 W transmitter board

This section presents a design example for the 50-W wireless charger transmitter board, the specifications of which match the REF_WLC_TX50W_N1.

The design is to be done for 50-W power delivery. The key specifications of the power stage are as follows:

- Input voltage: 20 V during power delivery; 5 V during ping stage
- Auxiliary buck converter power: Up to 2 W
- Receiver output power: 50 W with Infineon high power receiver
- Inverter stage switching frequency range: 120 kHz to 145 kHz
- Rx and TX coil alignment: 3 mm Z axis shift

The system transformer parameters depend on the Rx and Tx coil alignments, which are measured for a 3 mm Z axis shift. These parameters are as follows:

When the PTx coil is coupled with PRx coil, its inductance L'_{TX} = 12.07.

When the PRx coil is coupled with PTx coil, its inductance L'_{RX} = 9.84.

The coupling factor between the Tx and Rx coils, k = 0.523.

As per FHA analysis in section 2.3.1 , for given operating inputs, the operating frequency of inverter calculated as $F_{op=}$ 124.5 kHz.

Input current parameters which are calculated for operating frequency $F_{op} = 124.5\ kHz$, are as follows:

- Tx input peak current, $I_{TX-pk} = 7.16\ A$
- Tx Average input DC current, $I_{IN} = 2.71\ A$
- Tx input current phase angle, $\Phi_{in}\left(F_{op}\right) = 53.5°$

The inverter power stage components calculation is listed in Table 4. Based on the computed values, the BOM for key components is listed in Table 6. For the Q factor estimation and ASK demodulator circuit, see the component values from the REF_WLC_TX50W_N1 schematics in [2].

Table 4 Inverter power stage parameter value and component selection calculation

Parameter	Formula	Calculated value	Remarks
Tx coil rms current	$I_{Txrms} = \frac{I_{TX-pk}}{\sqrt{2}}$	5.06 A	
MOSFET current at switch off	$I_{SW,off} = I_{TX-pk} * Sin(\Phi_{in}\ (F_{op})$	5.76 A	
Inverter bridge capacitor	$I_{C_{INrms}} = \sqrt{{I_{TXrms}}^2 - {I_{IN}}^2}$	4.27 A	This is total current in inverter bridge capacitor. If there is N capacitor in parallel, then current in a capacitor will be $\frac{I_{CIN_{rms}}}{N}$.
Input CS shunt	$R_{sh_{in}} = 0.010\ \Omega$ $P_{Rsh_{in}} = {I_{IN}}^2\ R_{sh_{in}}$	$P_{Rsh_{in}} = 0.074\ W$	Shunt value as per WLC1150 requirement

Parameter	Formula	Calculated value	Remarks
			Computed loss is the worst-case value across the operating points
Transmitter coil	$L_{tx} = 10uH$	$I_{TXrms} = 7.07$ A	Inductance and capacitance values as per Qi Standard [1]
Resonant cap	$C_r = 247nF$	$Vcr_{pk\_pk} = 76$ V	
Inverter stage MOSFETs	$V_{ds-pk} = (1.5 \text{ x } V_{in})$ $I_{ds-pk} = I_{TX-pk}$	$V_{ds-pk} = 30$ V $I_{ds-pk} = 7.16\ A$	
Snubber capacitors	$C_S = \frac{I_{SW,off-max}\ T_{DT}}{V_{in}}$	$C_S = 11.5\ nF$	

Table 4 sets out the values and requirements for the power stage components. The selection of parts depends on factors such as performance, losses, cost, and so on, and might also need a few iterations. As an example, part selection for inverter stage MOSFETs is shown in Table 5. Based on a similar approach for other components, a high-level BOM for the design example is captured in Table 6.

Table 5 Part selection example – Inverter Stage MOSFETs

MOSFET requirements	Voltage rating – 30 V Current rating – 5 A
Option 1	BSZ0910LSATMA1 Rating – 30 V, 40 A, 5.7 mΩ Power loss (from equations in sections 2.3.5) for 20 V input 50 W load on receiver output with Infineon high power receiver MOSFET losses (worst case) – 632 mW (inclusive of conduction and switching and recovery)
Option 2	IRFHM830PbF Rating – 30 V, 21 A, 6.0 mΩ Power loss (from equations in sections 2.3.5) for 20 V input 50 W load on receiver output with Infineon high-power receiver MOSFET losses – 1008 mW (inclusive of conduction and switching and recovery)
Selected part	BSZ0910LSATMA1 – considering the losses, which is a key aspect for System loss/efficiency

Table 6 Key components BOM for the design example

Function	Qty	Description	Part number	Manufacturer
Wireless controller	1	Wireless transmitter with integrated USB Type-C PD controller 68-pin QFN	WLC1150-68LQXQ	Infineon Technologies
Inverter stage MOSFETs	4	N-channel 30 V 18 A (T_a), 40 A (T_c) 2.1 W (T_a), 37 W (T_c) surface-mount PG-TDSON-8 FL	BSZ0910LSATMA1	Infineon Technologies
Consumer side NFET	1	N-Channel 40 V 21 A (T_a), 40 A (T_c), 2.1 W (T_a), 63 W (T_c) surface mount PG-TSDSON-8-FL	BSZ028N04LS	Infineon Technologies
Bridge current sense	1	Resistor 0.01 Ω 1% 1 W 1206	LVT12R0100FER	Ohmite
Inverter input bulk capacitors	4	Ceramic capacitor 22 µF 25 V X5R 0805	CL21A226MAYNNNE	Samsung Electro-Mechanics
Transmitter coil	1	1 coil, 1 layer 10 µH wireless charging coil transmitter 55 mΩ max.	760308103102	Würth Elektronik
Resonant capacitors	2	Ceramic capacitor 0.1 µF 200 V C0G 1812	C1812X104J2GACTU	KEMET
Resonant capacitors	1	Ceramic capacitor 0.047 µF 200 V C0G 1812	C1812X473J2GACTU	KEMET
Inverter MOSFET snubber capacitor	2	Ceramic capacitor 10000 pF 25 V X7R 0402	04023C103KAT2A	KYOCERA AVX
Op-amp in amplifier and comparator	1	IC opamp GP 2 circuit 8-VSSOP	LMV358QPWR	Texas Instruments
Authentication IC for Qi v1.3.2 support	1	Enhanced wireless charging authentication solution	SLS32AIA020U2USON10XTMA2	Infineon Technologies
NTC	1	NTC thermistor 100k	NXFT15WF104FEAB021	Murata Electronics
Auxiliary buck MOSFETs	1	Mosfet Array 2 N-Channel (Dual) 30 V 3.6 A 1.5 W Surface Mount 6-PQFN (2x2)	IRLHS6376TRPBF	Infineon Technologies
Auxiliary buck inductor	1	10 µH Shielded Drum Core, Wirewound Inductor 900 mA 420 mΩ Max 1210	1277AS-H-100M=P2	Murata Electronics

4 PCB layout guidelines

This section explains the schematic and layout design requirements of the WLC1150 solution based on the reference board REF_WLC_TX50W_N1.

The WLC1150 wireless power transmitter consists of power circuits, digital circuits, an Arm® Cortex®-M0 CPU, and analog circuitry. The mixed-signal system solution requires special attention when placing and routing the design to maximize the performance of all functions. In Figure 20, the dashed circles in red represent the power sections, those in green indicate precision analog components, and those in purple cover the digital section of the application. When designing an Infineon WLC1150-based EPP Tx, the following order of block-level component placement should be followed:

- Power section: Inverter auxiliary buck and gate drivers
- Analog section: Demodulator, current sensing, and Q factor
- Digital section: USB communication, OPTIGA™ Trust, GPIOs, and external clock (optional)

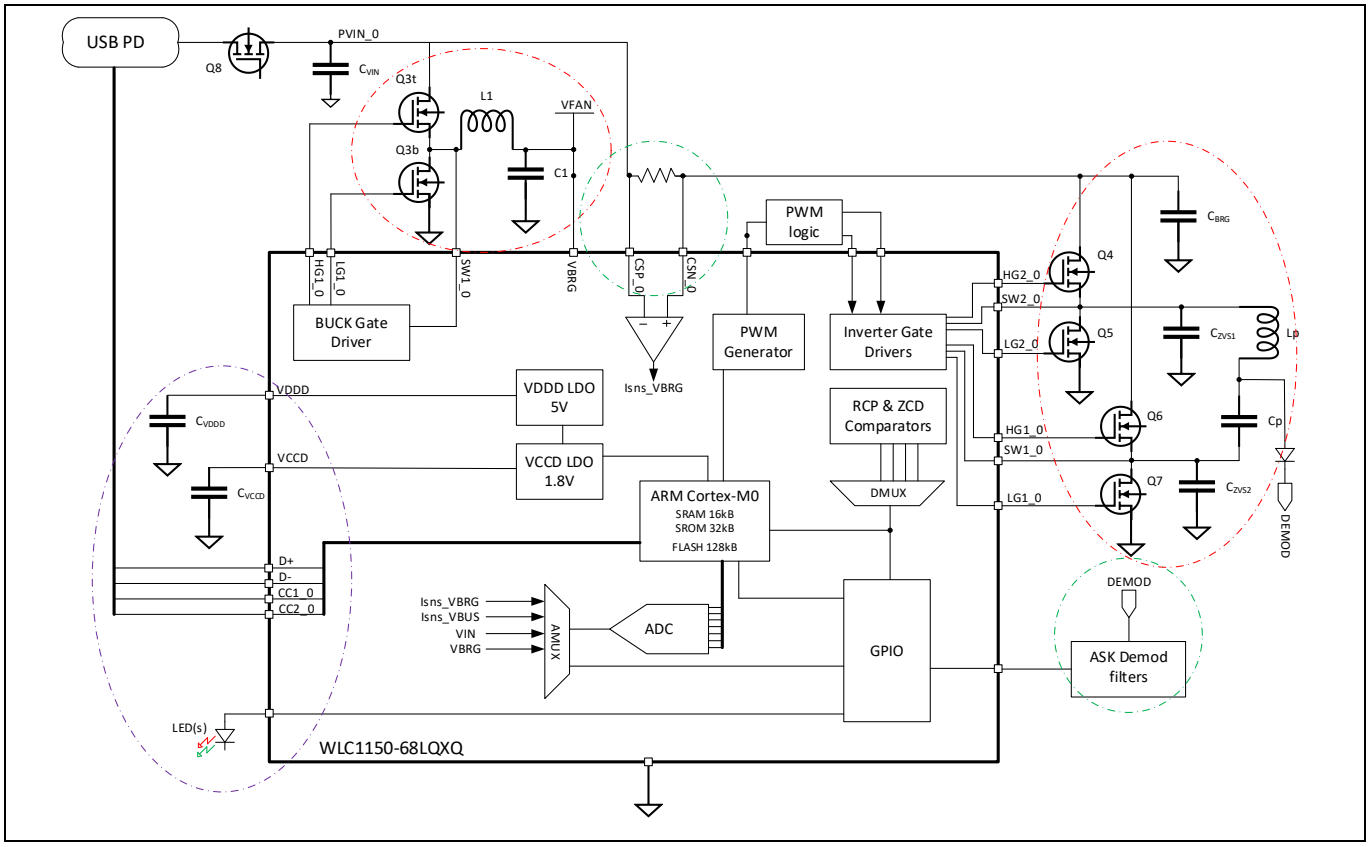

Figure 20 WLC1150 wireless power Tx simplified diagram

4.1 Power section

The power section is the most critical for maintaining high efficiency, providing sufficient thermal management, and reducing EMI. Consideration of the power path should be the first decision, followed by the location of the USB connector, Tx coil location, and inverter MOSFETs. The critical power circuits are the inverter bypass capacitors, bootstrap capacitors, and ZVS capacitors.

The power path can be described as the main current path from the input connector to the Tx coil and the GND return current back to the USB connector. The optimal design is to minimize this path length to reduce conduction losses and the current loop area.

In Figure 21, the positive current path is highlighted by the blue arrows and drawn on the PCB top layer; the main GND return path is shown in green. The power path is intentionally placed and routed such that the high currents do not need to pass under the WLC1150 (U2) controller IC to supply power to the Tx coil and back. A second path should exist from the WLC1150 IC to the common mode choke output for the controller quiescent currents (shown by the thinner arrows).

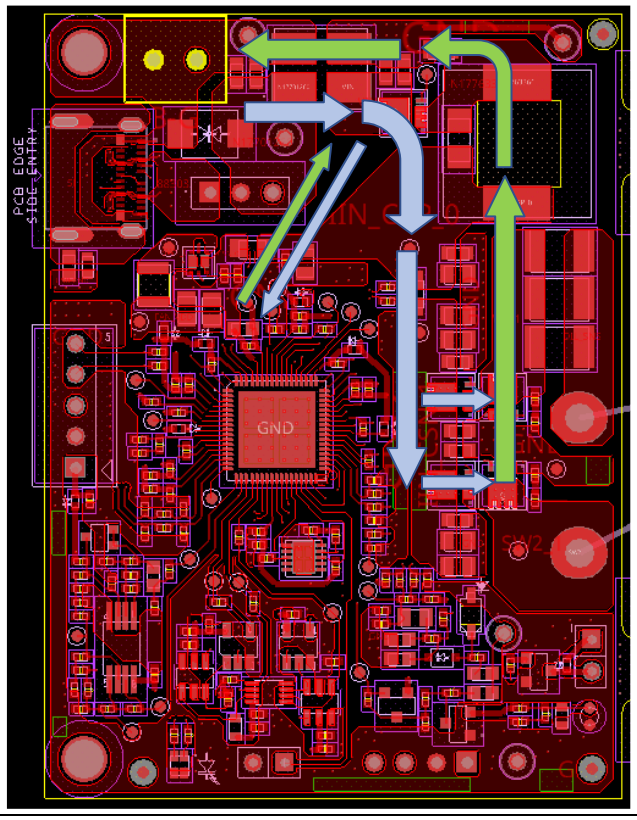

Figure 21 MP-A2 reference design wireless power current paths

4.1.1 Inverter

The full-bridge inverter is the next power section that will be examined in detail. Figure 22 and Figure 23 show the reference schematic and layout snippets for the inverter.

The placement of bypass capacitors (C23, C33, C76, and C77) is critical to performance. The switching nodes (SW2_1 and SW1_1) should be routed widely to reduce the impedance and skin effects and improve heat dissipation. The ZVS components (C41, R25, C31, and R17) should be next to the respective MOSFETs (Q7 and Q5). The BST capacitors (C32 and C25) should be placed next to the WLC1150 IC (U2). Use of multiple vias (six to eight, at least) for layer transitions is required for all connections.

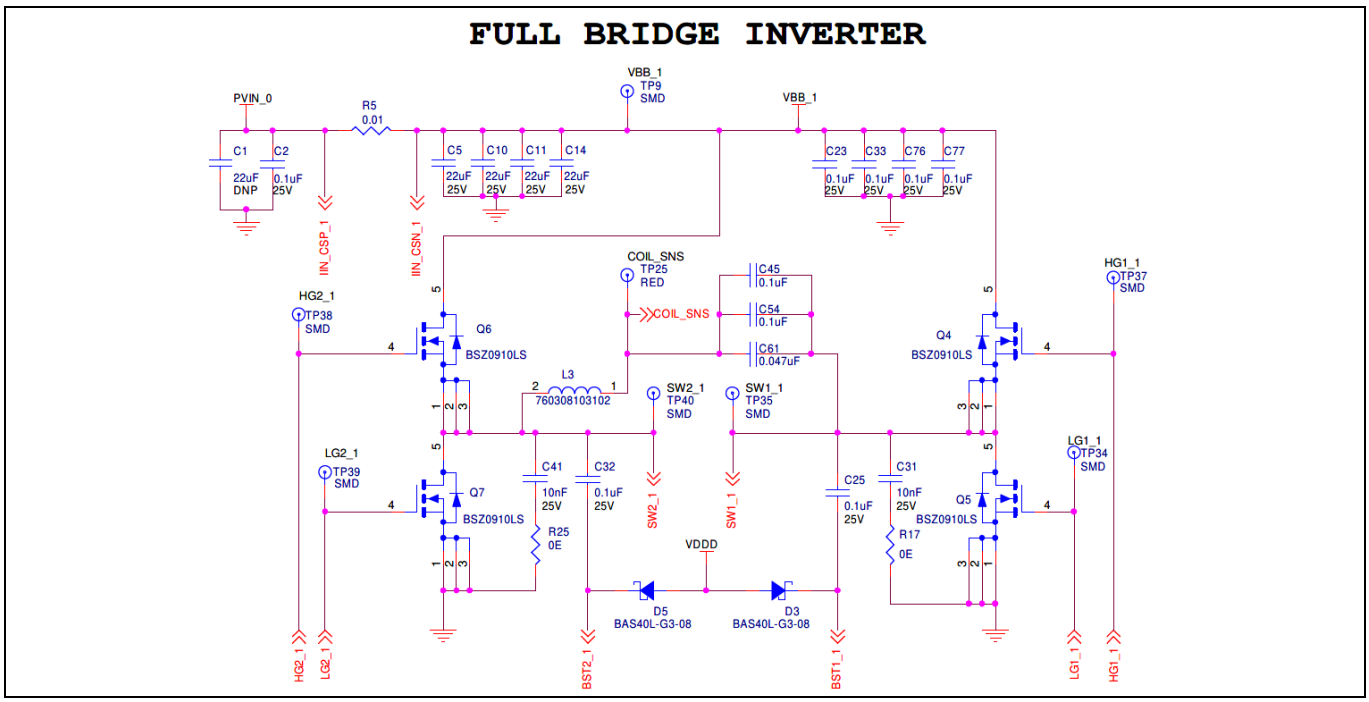

Figure 22 Inverter stage schematic

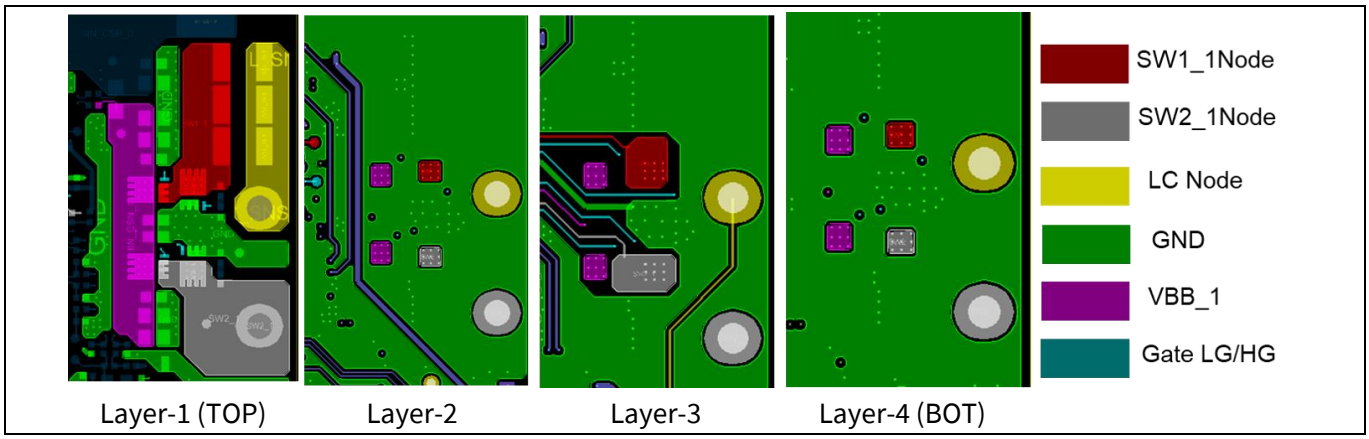

Figure 23 Inverter placement and layout (top and bottom layers)

4.1.2 Gate drivers, BST, bypass capacitors

The connection to the gates and the switching nodes (SW1_1 and SW2_1) to the WLC1150 (see Figure 24) should be at least 20 mil wide and routed as directly as possible. In addition, a GND signal returns the gate drive current to the device. Use of two vias for each connection layer transition is recommended. The BST capacitors should be located next to U2 and placed so they straddle the respective SW and BST pins.

The following are the minimum number of power-related components necessary for proper operation of the WLC1150 IC (U2): These should all be placed next to U2 (see Figure 25).

- BST capacitors (C25, C32)
- Bypass capacitors
  - VIN (C15, C17)
  - VDDD (C19, C22, C26, C27, C28, C29)
  - VCCD (C21)
  - VBRG (C37, C40)

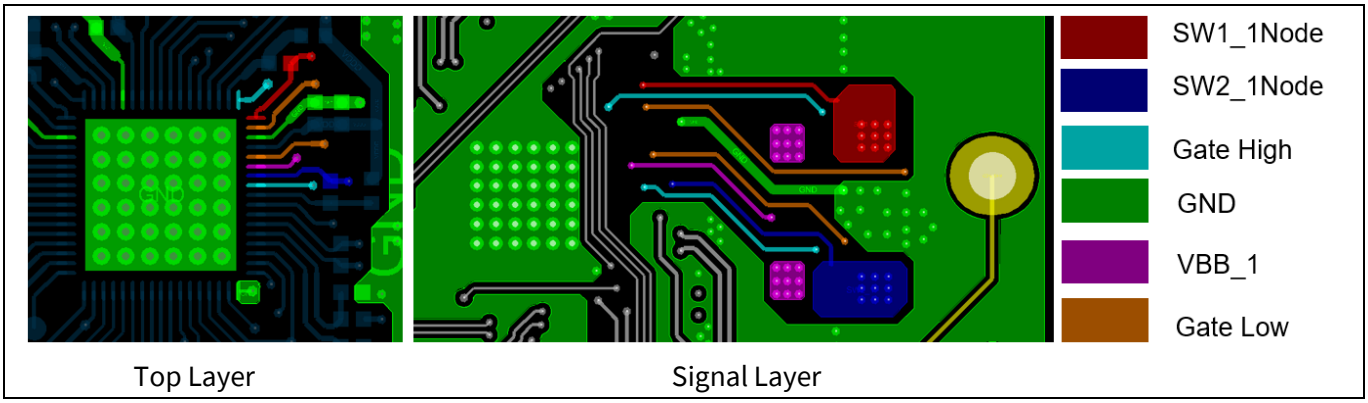

Figure 24 Routing from the WLC1150 device to the inverter gates and SWx nodes

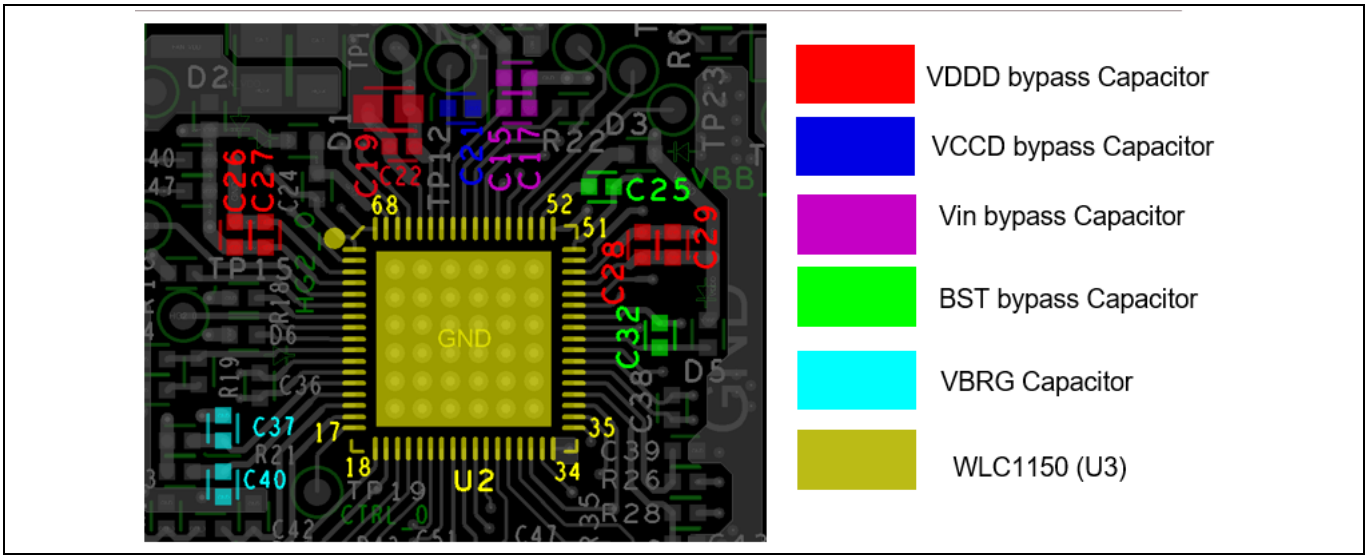

Figure 25 WLC1150 bypass and BST capacitors placement

4.2 Analog section

The precision analog circuits are composed of the DEMOD filter, the buck compensation network, the CS filters and the Q factor circuit. In addition, a thermistor input should be considered in the analog domain; this would need filtering before being digitized by the ADC.

4.2.1 Demodulator (voltage path and gain stage)

It is important to avoid the ground connections for each DEMOD component being in the main return path. as shown in Figure 26, after component D4 and D8, the voltage sensing path becomes relatively high-impedance; therefore, it should not run in parallel with either AC node when being routed unless there is a GND shielding plane between the nets. Both the voltage and current DEMOD sense filters should have a direct GND connection for each reference to the E-PAD of the WLC1150 IC.

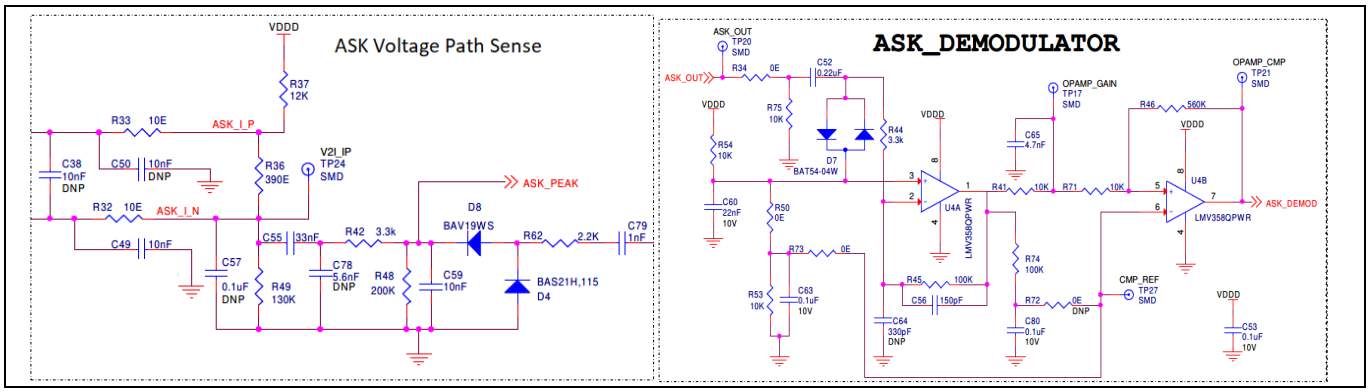

Figure 26 WLC1150 ASK voltage path and ASK Demodulator

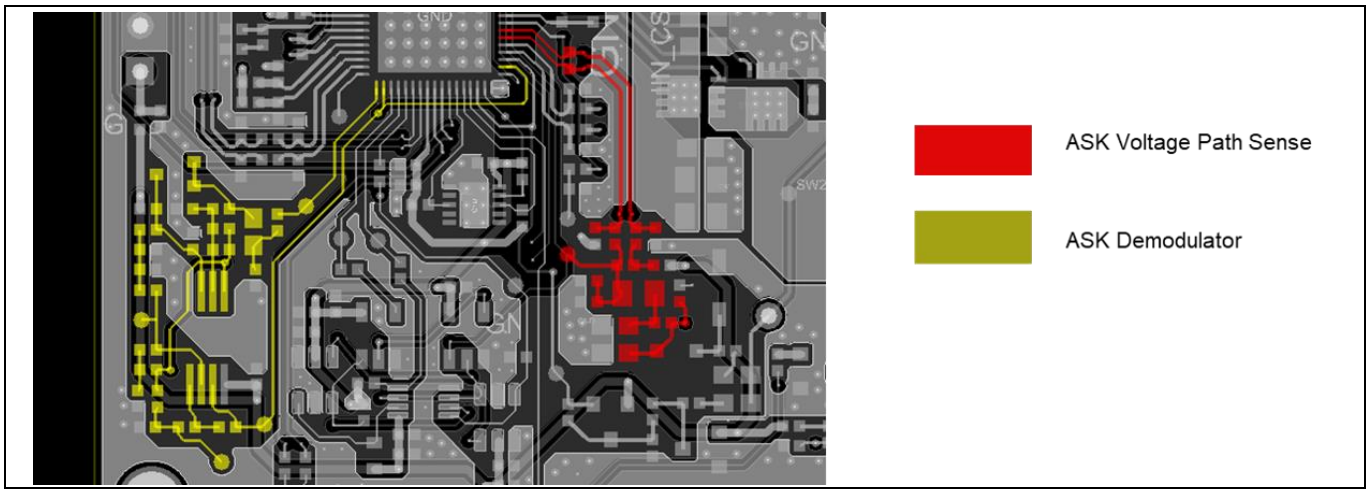

Figure 27 ASK Voltage path sense and ASK Demodulator filter component placement and routing

4.2.2 Current sensing

Current sensing (see Figure 28) must use Kelvin sense connections to properly detect the voltage drop across each CS resistor. The inverter input current is measured for current fault protection and Tx power for FOD comparison. The Aux buck input current sense is used to control the Buck control.

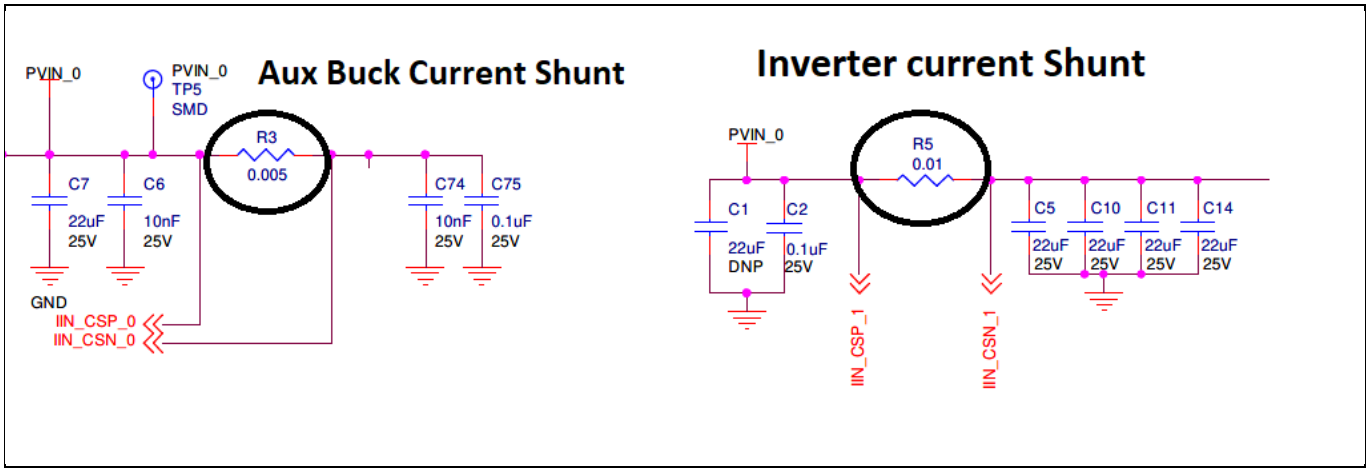

Figure 28 WLC1150 CS resistors schematic

In Figure 29, note that the Aux buck input and inverter input CS resistors are Kelvin-sensed from the inside of the component pads. In addition, the CSN and CSP lines are routed from the CS resistors to the WLC1150 IC as a differential pair to avoid common-mode noise being picked up by the signals. Capacitor C36 should be placed next to the WLC1150 IC, straddling pins 11 and 12:

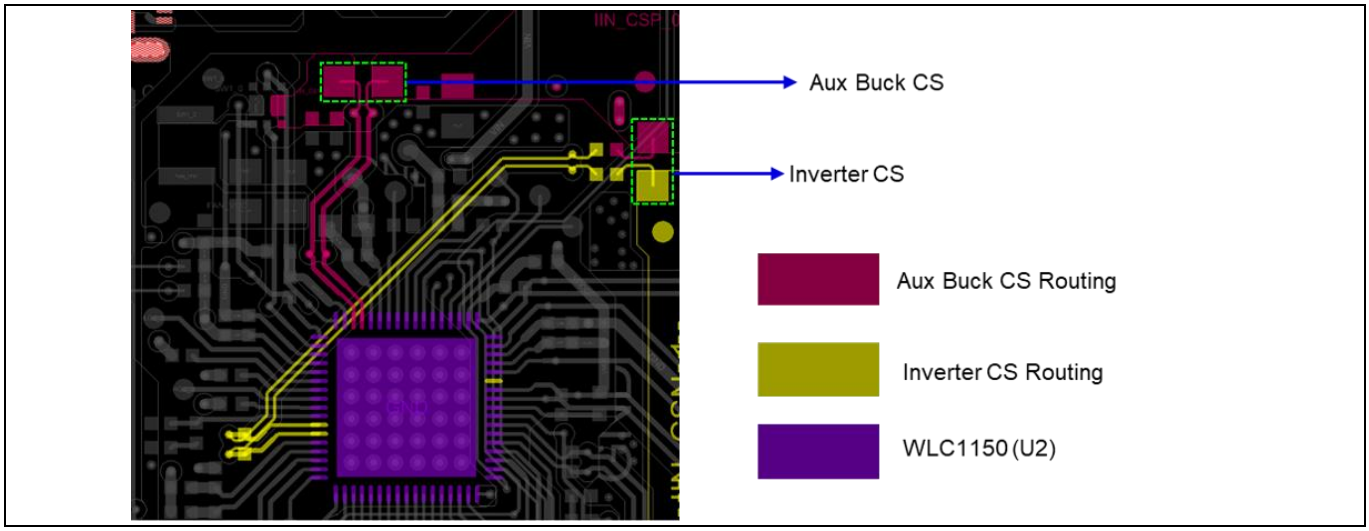

Figure 29 CS resistor connections and routing

4.2.3 Q factor and buck compensation

The Q factor circuit is necessary for EPP-compliant designs and uses the LC decay of the resonance tank to measure the quality factor of the LC tank (wireless Tx coil (L3) and resonance capacitors (C45, C54, C61)). The common node between these components is often referred to as the “COIL_SNS”; together they make up the LC tank. The Q factor component should be placed near the WLC1150 IC and outside the main power path. They should be placed after the previously mentioned components, and signal routing to U2 should be done with enough clearance from high frequency power path.

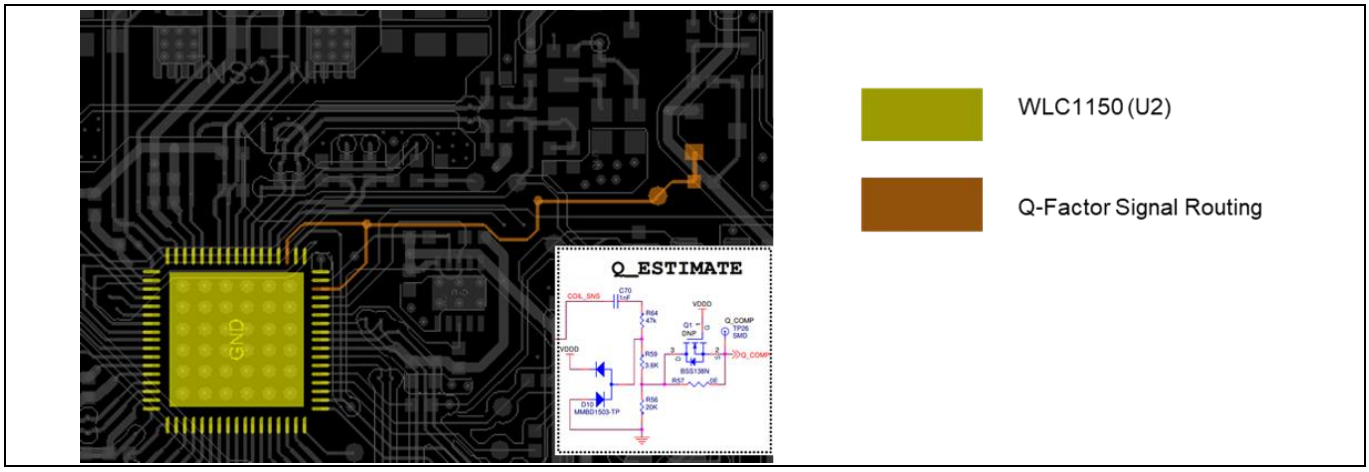

Figure 30 Q factor measurement circuit schematic, placement and routing

4.3 Digital section

GPIOs, the clock, OPTIGA™ Trust IC, and the USB communication lines (D+, D-, CC1, and CC2) are considered to be the digital section. Any GPIOs not mentioned here are low power and relatively low frequency; they are not considered critical and may be routed as convenient. The GPIOs are powered by the VDDD 5 V supply for the digital logic-level reference.

The OPTIGA™ Trust IC is necessary for Qi v1.3.2 authentication. It is recommended to place this component near the WLC1150 wireless controller IC and route the I^2C lines on the inner layers if possible.

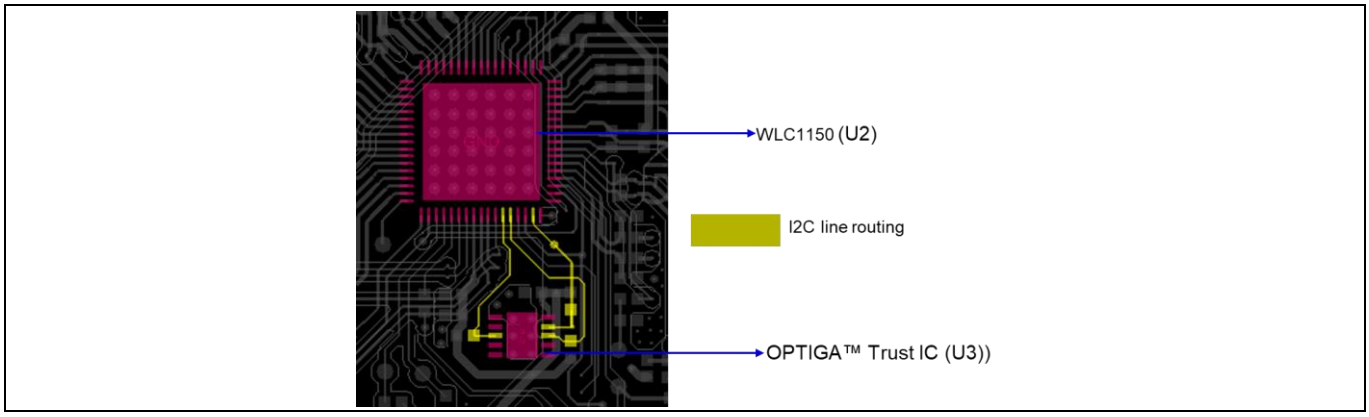

Figure 31 OPTIGA™ Trust memory IC (U3) placement and I2C line routing

The D+_0, D-_0, CC1_0, and CC2_0 lines should be routed as directly as possible to the USB Type-C connector; they should be routed together similar to differential pairs to reduce the noise interference from coupling or distortion. Avoid routing the traces under the buck or inverter portions of the PCB (if necessary, be sure to use a solid GND plane to shield these from any switching regulator). The D+ and D- and the CC1 and CC2 traces should be routed next to each other, respectively, and should be of the same length to within 5 mm. Avoid unnecessary layer transitions and vias when routing these lines.

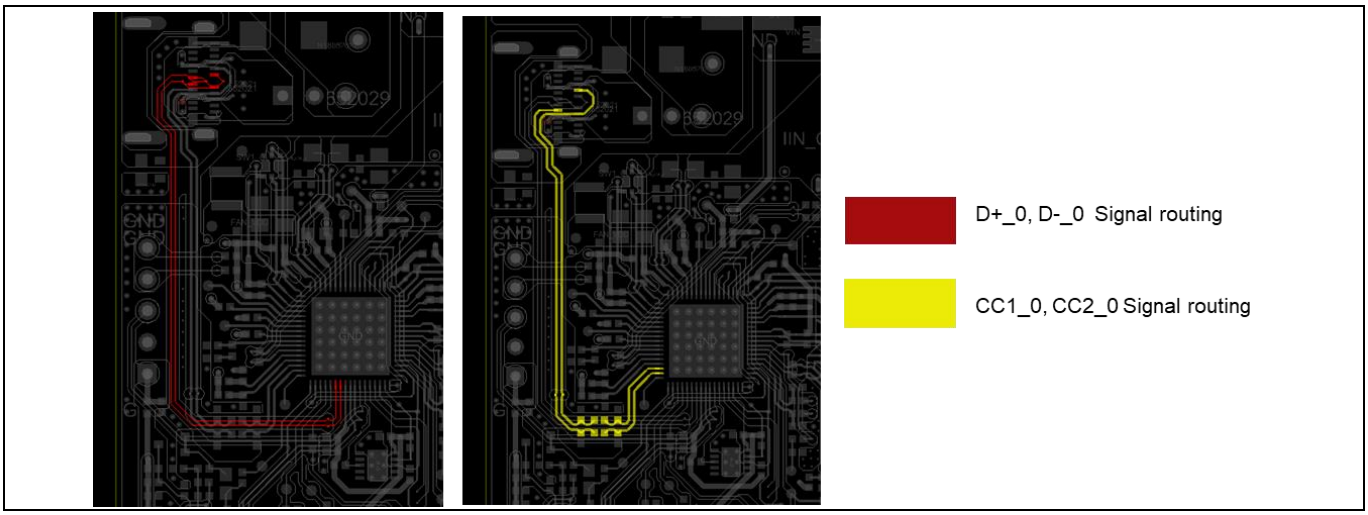

Figure 32 WLC1150 USB routing (D+ and D-, CC1 and CC2)

4.4 Thermal management

Thermal management of the solution is critical for high performance and reasonable operating temperatures. To improve thermal performance, the use of multiple vias and large surface areas in the form of copper planes are highly recommended. The critical components for adding thermal management provisions are the inverter FETs (M13, M14, M15, and M16) and WLC1150 controller IC (U2).

The WLC1150 IC needs to have at least 15 thermal vias in the E-PAD and should have direct GND plane access for electrical and thermal conduction. Thermal performance is improved by using multiple layers with multiple vias to transfer heat between layers, using heavier copper foil weights, and making thinner PCBs. Large, continuous planes connected directly to heat sources are the most effective method to reduce the operating temperature of power management components.

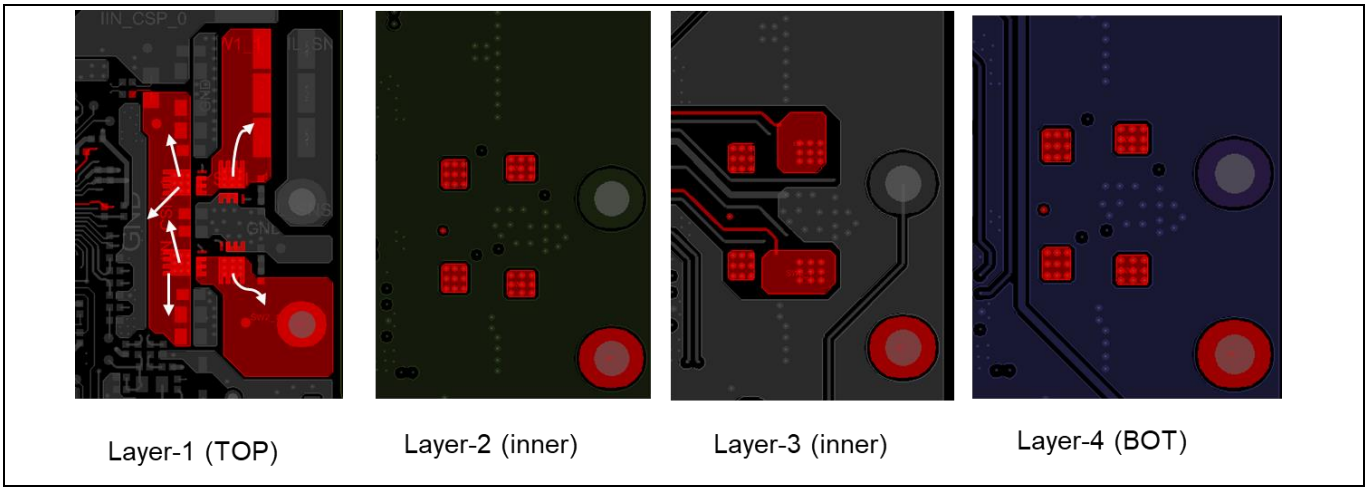

Figure 33 Inverter thermal planes and heat flow (top and bottom layers)

When using parallel planes add vias evenly spaced across each surface for maximum heat transfer to each plane to achieve the lowest possible operating temperature.

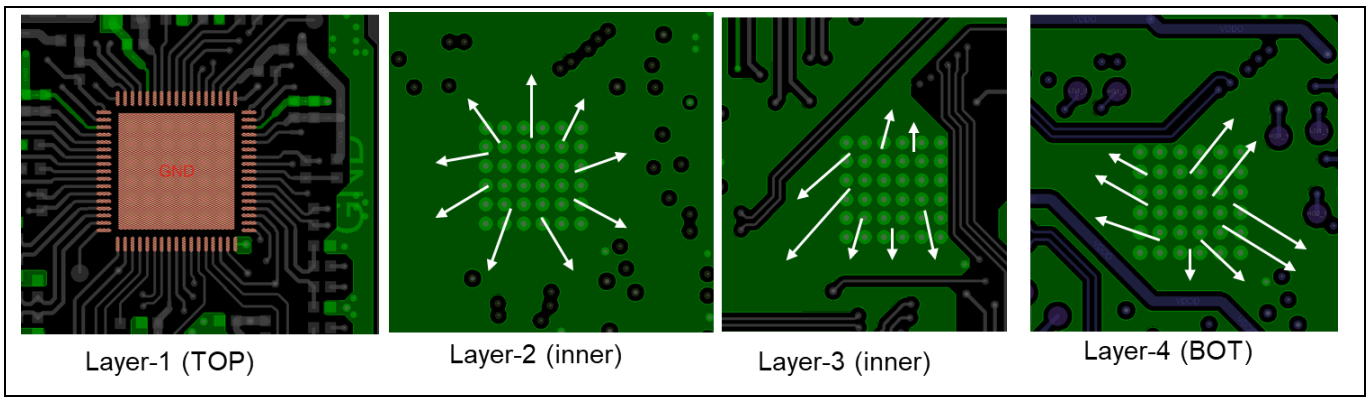

Figure 34 WLC1150 thermal paths and heat flow and thermal vias in E-PAD

4.5 Package footprint design guidelines

For the exact package dimensions, refer to the WLC1150 datasheet [2]. For proper operation, at least 15 thermal vias should be spread across the E-PAD. The solder mask should extend at least 2.5 mils beyond each copper pad opening and the paste mask should be the same dimension as each pin. Designing to the typical dimension is sufficient for proper installation.

5 Schematic and PCB layout review checklist

The schematic entry checklist is captured in Table 7, including the component selection guidelines in section 2.

Table 7 Schematic checklist

Priority	Item	Yes/No/NA
1	The components are well derated for the required operating temperature	
2	The selected MOSFET current ratings are within the calculated peak current value even at case temperature of 100°C	
3	The MOSFETs are logic-level type, the gate threshold voltages are below 5 V and low $R_{DS(on)}$ is achievable with 5 V gate drive	
4	The transmitter coil part has inductance as specified by Qi	
5	The transmitter coil Q factor is high or the effective coil resistance at inverter operating frequency is less than 80 mΩ	
6	The resonant capacitor part in the inverter stage meets Qi recommendations for the MP-A2 coil	
7	The capacitor part for the resonance capacitor has a stable capacitance over its operating voltage and temperature range (C0G or NP0-type dielectric)	
8	The capacitor voltage rating covers Qi recommendations for peak voltage	
9	The Type-C USB connector at input has the necessary pins for power, CC lines and D+ and D- lines	
10	Any common-mode filter at input, if used, has a DCR less than 20 mΩ	
11	There is 5.1 kΩ pull-down and 330 pF capacitor-to-ground for both CC lines	
12	The CC1, CC2 connections and D+, D- connections are correctly mapped at the USB connector pins and the WLC1150 pins	
13	The CS resistors for buck stage input and output side have a tolerance no less than 1% and the temperature coefficient ≤50 ppm	
14	There are low-value (less than 100 nF) low-ESL type decoupling capacitors placed close to the two inverter switching legs.	
15	The WLC1150 VIN pin has decoupling capacitors as per datasheet recommendations	
16	The VDDD and VCCD pins have decoupling capacitors as per WLC1150 recommendations and the effective capacitance of these capacitors at 5 V yields the recommended capacitance value	
17	The WLC1150 pins where pin voltage is expected to go beyond absolute maximum value (during transients or faults) have necessary clamping	
18	The diodes used for clamping of QCOMP1 and QCOMP2 pins have low leakage (less than 100 nA) at 5 V operation	
19	The CSPO and CSNO pins have filter capacitors	
20	The I^2C lines used for interface with the authentication IC have the necessary pull-up to VDDD	
21	The VBRG, VBRG_DIS, and VBUS_IN pins have 0.1 µF decoupling capacitors close to WLC1150	
22	The unused pins of WLC1150 are terminated as recommended in the WLC1150 datasheet	

Priority	Item	Yes/No/NA
23	The VTARG pin of the programming connector is connected to VDDD with a series diode as in the REF_WLC_TX50W_N1 schematic	
24	The op-amp part used in the ASK demodulator section is of rail-to-rail output type with a slew rate less than 1 V/µs	
25	The bootstrap capacitor has 0.1 µF capacitance at the maximum input voltage	
26	The chosen bootstrap diode forward voltage is small to ensure lower conduction losses	
27	The mechanical accessories used around the transmitter coil (spacers, acrylic, tapes) do not contain any metallic elements	
28	The chosen combinations of tapes, spacers and acrylic for coil mounting gives a dz height as recommended by Qi (see Figure 11)	
29	The chosen NTC has an operating range of at least -20°C to +100°C	
30	The chosen NTC for coil temperature measurement has a long lead for placement of the sensing element near the coil and soldering of leads on the PCB	
31	The NTC feedback to WLC1150 has a low-pass filter with bandwidth lower than ASK modulation frequency	
32	Decoupling Capacitors of 100n and 10n should be placed at each logic gate IC between VSS and GND in PWM logic circuit.	
33	The series resistance with NTC ensures that the current in NTC results in a power loss lower than the NCT-rated value even at the highest NTC-rated temperature	
35	The schematic is identical to the schematic of REF_WLC_TX50W_N1 in [2]	

Table 8 Layout checklist

Priority	Item	Yes/No/NA
1	The power path is direct from the input power connector to the Tx coil with wide copper and direct GND connection	
7	Inverter input bypass capacitors are placed next to each half-bridge and straddle VBRG to GND	
8	Inverter ZVS capacitors are placed next to the LS MOSFETs and switch node (but not blocking the power path)	
9	Additional copper and vias are added for heat dissipation near all MOSFETs and under WLC1150 E-PAD	
10	All BST capacitors are placed next to the WLC1150 device	
11	All PVDD, VDDD, VCCD and VBRG bypass capacitors shown in Figure 25 are placed next to the WLC1150 device	
12	The bootstrap capacitor and diodes are placed close to WLC1150	
13	DEMOD filters are placed outside the power path and near the WLC1150 device	
14	CS resistors are Kelvin-sense connected and routed to the WLC1150 device as differential pairs	
15	The CC lines and DP, DM lines are routed differentially for most of the trace lengths, do not overlap with any high-frequency nodes and are guarded with GND on either side	
16	Routing length of PWM-IN1 and PWM-IN2 signal to WLC1150 should be less than 25 mm.	

The following guidance should be used when routing the following nets from the evaluation board. These are minimum values and routing wider than listed is recommended when space permits.

Table 9 Minimum routing guide

Net name	Minimum routing width*
VBRG, SW0, SW1_0, SW1_1, SW2_1, COIL_SNS (Tx coil to resonance capacitors only)	2.54 mm (100 mils)
VIN	2 mm (78 mils)
VDDD, VCCD	0.75 mm (30 mils)
BST nodes, gate drive lines	0.5 mm (20 mils)
COIL_SNS (to ASK filter and Q factor circuit)	0.2 mm (8 mils)
CS signals (CSP_N, CSN_N), routed as differential pairs	0.127 mm (5 mils)
GPIOs, I^2C, interrupts, ASK DEMOD, clock	0.127 mm (5 mils)
PWM_IN1, PWM_IN2	0.127 mm (5 mils)

* - Using 1-oz copper

Acronyms/abbreviations

Table 10 Acronyms/abbreviations

Acronym/abbreviation	Definition
ADC	Analog-to-digital converter
Arm®	Advance RISC machine, a CPU architecture
ASK	Amplitude shift keying
BOM	Bill of materials
BPP	Baseline power profile
CC	Configuration channel
CPU	Central processing unit
CSA	Current sense amplifier
CSN	Current sense negative
CSP	Current sense positive
DCR	Direct current resistance
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EPP	Extended power profile
ESR	Equivalent series resistance
FOD	Foreign object detection
FSK	Frequency shift keying
GPIO	General-purpose input/output
IC	Integrated circuit
IDE	Integrated development environment
I^2C	Inter-integrated circuit, a communication protocol
I/O	Input/output
LDO	Low-dropout regulator
MCU	Microcontroller unit
MOSFET	Metal oxide semiconductor field-effect transistor
NC	No connect
OCP	Overcurrent protection
OTP	Overtemperature protection
OVP	Overvoltage protection
PCB	Printed circuit board
PD	Power delivery
PDO	Power delivery objects
PPS	Programmable power supply
POR	Power-on-reset
PCMC	Peak current mode control
PWM	Pulse-width modulator

Acronyms/abbreviations

Acronym/abbreviation	Definition
QFN	Quad-flat no-lead, a type of IC packaging
Qi	Pronounced “chee”
RAM	Random access memory
ROM	Read-only memory
R_D	Pull-down resistor on Type-C CC lines
R_P	Pull-up resistor on Type-C CC lines
Rx	Receiver
SCB	Serial communication block
SCL	I^2C serial clock
SCP	Short-circuit protection
SDA	I^2C serial data
SMD	Surface-mount device
SPI	Serial peripheral interface, a communication protocol
TA	Travel adaptor
TCPWM	Timer/counter pulse-width modulator
Tx	Transmitter
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
ZVS	Zero voltage switching

References

[1] Qi specifications, WPC knowledge base; https://www.wirelesspowerconsortium.com/knowledge-base/specifications/download-the-qi-specifications.html

[2] Datasheet, 002-36311: WLC1150, Wireless charging IC (WLC) – Transmitter 50W with integrated USB Type-C PD controller

[3] REF_WLC_TX50W_N1 design files

[4] D. Graovac, et al., MOSFET power losses calculation using the datasheet parameters/Infineon Application Note 2006-07 V1.1 – Infineon Technologies AG

[5] Alan Huang, Hard commutation of power MOSFET OptiMOS™ FD 200 V/250 V/Infineon Application Note 2014-03 V1.0 – Infineon Technologies AG

[6] SangCheol Moon, et al., “Analysis and design of a wireless power transfer system with an intermediate coil for high efficiency”, IEEE Transactions on Industrial Electronics, Vol. 61, No. 11, Nov. 2014

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