AN98475

Migration from Winbond W25Q16DV to S25FL116K SPI Flash Family

AN98475 provides conversion guidelines for migrating from the Winbond® W25Q16DV SPI series to the Cypress S25FL116K SPI Flash Family, and discusses the specification differences.

Contents

1 Introduction

Cypress S25FL1-K flash is a feature rich and cost-optimized serial peripheral interface (SPI) non-volatile NOR flash family manufactured on a 90 nm 3-volt floating gate process technology node. This application note provides conversion guidelines for migrating from the Winbond® W25Q16DV SPI series to the Cypress S25FL116K SPI Flash Family.

This application note is based on information available to date from data sheets and other application notes publicly available from Cypress and Winbond. Please refer also to the latest relevant specifications. The document discusses the specification differences when migrating from W25Q16DV to S25FL116K.

2 Feature Comparison and Differences

Winbond W25Q16DV products are well suited for migration to Cypress S25FL116K products. Some of the reasons are compatible pinouts, packages, command set, and 4-kB sector structure.

Both Cypress S25FL116K and Winbond W25Q16DV devices support Single (Standard) I/O, Dual I/O, and Quad I/O modes.

The main differences between Cypress S25FL116K and Winbond W25Q16DV are:

- Data program scheme (See *Program Method* on page 4.)
- Status register structure (See *Status Registers* on page 4.)
- Block protection scheme (See *Block Protection Scheme* on page 5.)
- Unique ID (See *Unique ID* on page 7.)

Table 1. High Level Feature Support Comparison

Feature / Parameter	S25FL116K	W25Q16DV
Single (Standard) IO Operations	√	√
Dual IO Operations	√	√
Quad IO Operations	√	√
Standard Normal Read SCK Frequency (max)	50 MHz	50 MHz
Standard Fast Read SCK Frequency (max)	108 MHz	104 MHz
Dual Fast Read SCK Frequency (max)	108 MHz	104 MHz
Quad Fast Read SCK Frequency (max)	108 MHz	104 MHz
Wrapped Read Modes	√	√
Program Page Size	256 Bytes	256 Bytes
Program Suspend and Resume	√	√
Erase Suspend and Resume	√	√
Quad Page-Program	—	√
4 kB, 64 kB, and Chip Erase	√	√
32-kB Block Erase	—	√
Write Protection	√	√
Volatile Configuration	√	√
Software Reset	√	√
One Time Programmable Region(s)	3 x 256 Bytes	3 x 256 Bytes
Temperature Range Option	-40°C to +85°C -40°C to +105°C -40°C to +125°C	-40°C to +85°C

2.1 Hardware Package

The pinouts of S25FL116K and W25Q16DV are identical.

Figure 1 shows the SOIC packages and pinouts.

Figure 2 shows the TFBGA 8 x 6 mm packages and pinouts.

Refer to the data sheets for detailed package information.

Figure 1. SOIC 150 / 208 / 300 mil Package and Pinout (16-Pin and 8-Pin Versions)

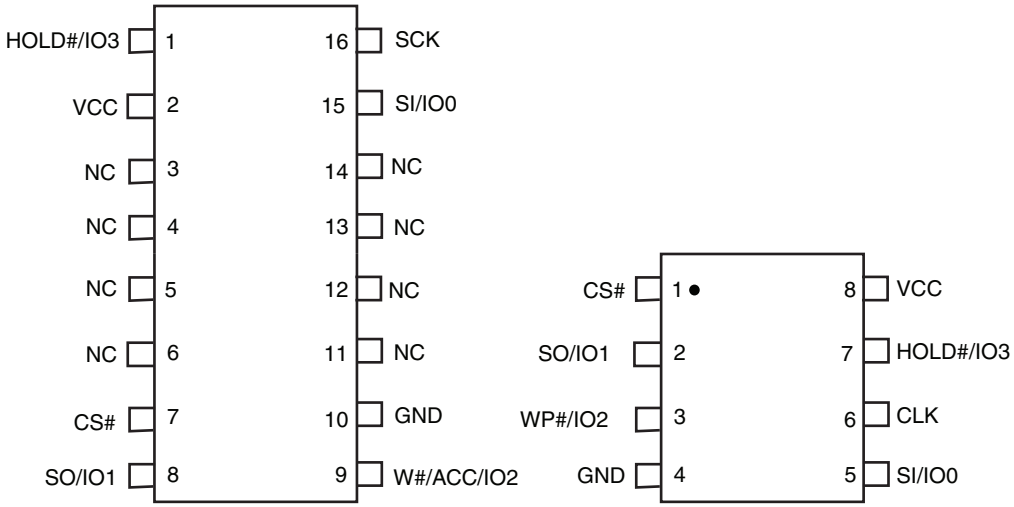


Figure 2. Ball Configuration TFBGA 8 x 6 mm Package and Pinout (Package Code TB or TC)

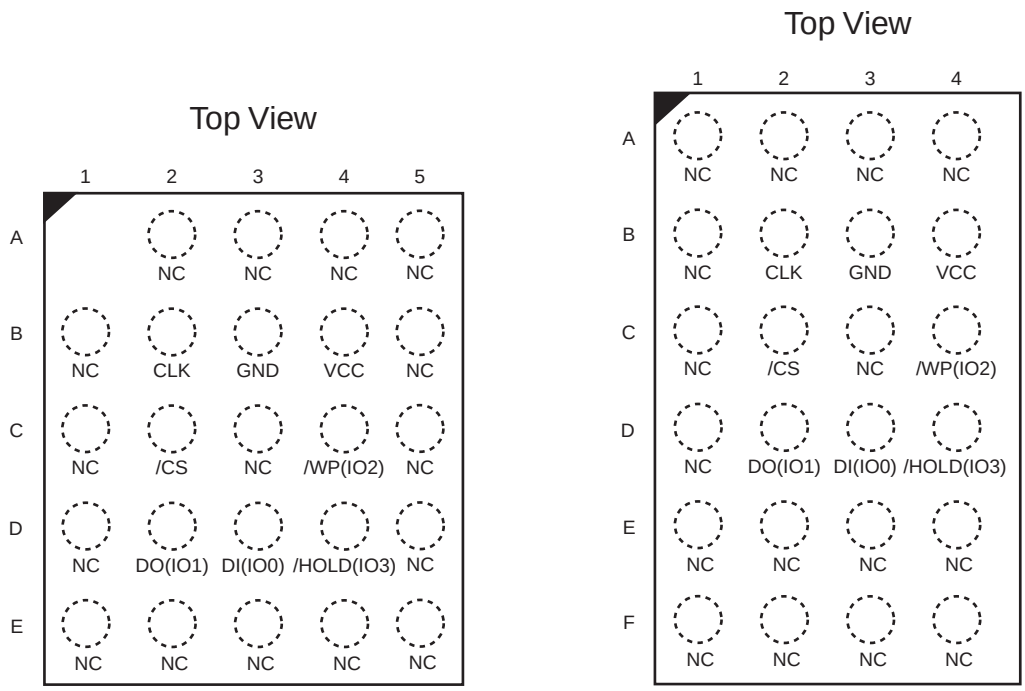


Table 2 summarize the available packages from Cypress and Winbond.

Table 2. Cypress and Winbond Available Packages

	S25FL116K	W25Q16DV
SOIC8 150 mil	√	√
SOIC8 208 mil	√	√
SOIC16 300 mil	—	√
PDIP 300 mil	—	√
WSON 5x6	√	√
24-ball BGA 6 x 8 mm (6 x 4 / 5 x 5 ball array)	√	√
KGD / KGW	√	√

2.2 Block Structure

Both Winbond W25Q16DV and Cypress S25FL116K support 4-kB sector erase in any sector.

Winbond W25Q16DV supports both 32-kB block erase and 64-kB block erase, while Cypress S25FL116K supports 64-kB block erase only.

2.3 Program Method

Both Winbond W25Q16DV and Cypress S25FL116K support page program with program length from 1 to 256 bytes.

W25Q16DV supports Quad Page-Program, while S25FL116K does not.

2.4 Multi-I/O Operation

W25Q16DV and S25F116K support dual output read, dual I/O read, quad output read, and quad I/O.

W25Q16DV supports Word Read Quad I/O and Octal Word Read Quad I/O, while S25FL116K does not.

2.5 Status Registers

Both W25Q16DV and W25Q16DV have two status registers: SR1 and SR2.

The S25FL116K has one additional status register (SR3), which can be used to provide status on additional device features and to configure the burst wrap feature. The Write Status Register instruction allows the three status registers to be written in one command sequence. Only non-volatile status register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 through 2 of Status Register-1), CMP, LB3, LB2, LB1, LB0, QE, SRP1 (bits 6 through 0 of Status Register-2), and W6, W5, W4, and LC (bits 6 through 0 of Status Register-3) can be written. All other status register bit locations are read-only and will not be affected by the Write Status Register instruction.

Table 3 illustrates the Status Register bit assignments for Winbond W25Q16DV and Cypress S25FL116K.

Table 3. Status Register Bit Assignments for W25Q16DV and S25FL116K

Bits	Cypress S25FL116K		Winbond W25Q16DV	
	Name	Function	Name	Function
SR1[7]	SRP0	Status Register Protect0	SRP0	Status Register Protect0
SR1[6]	SEC	Sector / Block Protect	SEC	Sector / Block Protect
SR1[5]	TB	Top / Bottom Protect	TB	Top / Bottom Protect
SR1[4]	BP2	Block Protect Bits	BP2	Block Protect Bits
SR1[3]	BP1		BP1	
SR1[2]	BP0		BP0	
SR1[1]	WEL	Write Enable Latch	WEL	Write Enable Latch
SR1[0]	BUSY	Embedded Operation Status	BUSY	Embedded Operation Status
SR2[7]	SUS	Suspend Status	SUS	Suspend Status
SR2[6]	CMP	Complement Protect	CMP	Complement Protect
SR2[5]	LB3	Security Register Lock Bits	LB3	Security Register Lock Bits
SR2[4]	LB2		LB2	
SR2[3]	LB1		LB1	
SR2[2]	LB0		R	Reserved
SR2[1]	QE	Quad Enable	QE	Quad Enable
SR2[0]	SRP1	Status Register Protect1	SRP1	Status Register Protect1
SR3[7]	RFU	Reserved	—	—
SR3[6]	W6	Burst Wrap Length	—	—
SR3[5]	W5		—	—
SR3[4]	W4	Burst Wrap Enable	—	—
SR3[3]	Latency Control (LC)	Variable Read Latency Control	—	—
SR3[2]			—	—
SR3[1]			—	—
SR3[0]			—	—

2.6 Block Protection Scheme

Both S25FL116K and W25Q16DV have the same Block Protection Scheme. They allow all, none, or a portion of the memory array to be protected from Program and Erase instructions by way of the status register.

The Block Protect Bits (BP2-0) provide Write Protection control and status. The factory default setting for the Block Protect Bits is 0 (none of the array is protected). The non-volatile Top/Bottom bit (TB) controls whether the Block Protect Bits (BP2-0) protect from the Top (TB=0) or the Bottom (TB=1) of the array. The non-volatile Sector/Block Protect bit (SEC) selects whether the Block Protect Bits (BP2-0) protect 4-kB Sectors (SEC=1) or 64-kB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array.

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register. It is used in conjunction with SEC, TB, and BP2-0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 will be reversed.

Refer to the data sheet for the valid combinations. Table 4 and Table 5 show Block Protection.

Table 4. Block Protection (CMP = 0)

Status Register					Protected Portion	Protected Addresses
SEC	TB	BP2	BP1	BP0		
x	x	0	0	0	None	None
0	0	0	0	1	Upper 1/32	1F0000h - 1FFFFFH
0	0	0	1	0	Upper 1/16	1E0000h - 1FFFFFH
0	0	0	1	1	Upper 1/8	1C0000h - 1FFFFFH
0	0	1	0	0	Upper 1/4	180000h - 1FFFFFH
0	0	1	0	1	Upper 1/2	100000h - 1FFFFFH
0	1	0	0	1	Lower 1/32	000000h - 00FFFFH
0	1	0	1	0	Lower 1/16	000000h - 01FFFFH
0	1	0	1	1	Lower 1/8	000000h - 03FFFFH
0	1	1	0	0	Lower 1/4	000000h - 07FFFFH
0	1	1	0	1	Lower 1/2	000000h - 0FFFFFH
x	x	1	1	x	All	000000h - 1FFFFFH
1	0	0	0	1	Upper 1/512	1FF000h - 1FFFFFH
1	0	0	1	0	Upper 1/256	1FE000h - 1FFFFFH
1	0	0	1	1	Upper 1/128	1FC000h - 1FFFFFH
1	0	1	0	x	Upper 1/64	1F8000h - 1FFFFFH
1	1	0	0	1	Lower 1/512	000000h - 000FFFH
1	1	0	1	0	Lower 1/256	000000h - 001FFFH
1	1	0	1	1	Lower 1/128	000000h - 003FFFH
1	1	1	0	x	Lower 1/64	000000h - 007FFFH

Table 5. Block Protection (CMP = 1)

Status Register					Protected Portion	Protected Addresses
SEC	TB	BP2	BP1	BP0		
x	x	0	0	0	All	000000h - 1FFFFFH
0	0	0	0	1	Lower 31/32	000000h - 1EFFFFH
0	0	0	1	0	Lower 15/16	000000h - 1DFFFFH
0	0	0	1	1	Lower 7/8	000000h - 1BFFFFH
0	0	1	0	0	Lower 3/4	000000h - 17FFFFH
0	0	1	0	1	Lower 1/2	000000h - 0FFFFFH
0	1	0	0	1	Upper 31/32	010000h - 1FFFFFH
0	1	0	1	0	Upper 15/16	020000h - 1FFFFFH
0	1	0	1	1	Upper 7/8	040000h - 1FFFFFH
0	1	1	0	0	Upper 3/4	080000h - 1FFFFFH
0	1	1	0	1	Lower 1/2	100000h - 1FFFFFH
x	x	1	1	x	None	None
1	0	0	0	1	Lower 511/512	000000h - 1FEFFFH
1	0	0	1	0	Lower 255/156	000000h - 1FDFFFH
1	0	0	1	1	Lower 127/128	000000h - 1FBFFFH
1	0	1	0	x	Lower 63/64	000000h - 1F7FFFH
1	1	0	0	1	Upper 511/512	001000h - 1FFFFFH
1	1	0	1	0	Upper 255/256	002000h - 1FFFFFH

Table 5. Block Protection (CMP = 1) (Continued)

Status Register					Protected Portion	Protected Addresses
SEC	TB	BP2	BP1	BP0		
1	1	0	1	1	Upper 127/128	004000h - 1FFFFFH
1	1	1	0	x	Upper 63/64	008000h - 1FFFFFH

2.7 Variable Latency

Cypress S25FL116K adds support for variable latency read timing. You can use the default latency code value when migrating from Winbond products to S25FL116K without any change in read timing. Or you can set latency code (SR3[3-0]) and change read timing to enable faster initial access time or higher clock rate read commands. See full feature details in the S25FL116K data sheet.

2.8 Burst Read Mode

Both W25Q16DV and S25FL116K support Set Burst with Wrap command (77H) preceding the Fast Read Quad I/O command. See full feature details in data sheet.

Cypress S25FL116K supports Fast Read Quad I/O (EBh) in Burst with Wrap mode. Status Register-3 provides a bit (SR3[4]) to enable a read with wrap option for the Read Quad I/O command. To set burst length, Status Register-3 provides bits (SR3[6:5]) to select the alignment boundary. Burst wrap length can be aligned on 8-, 16-, 32-, or 64-byte boundaries.

2.9 OTP (One-Time Program) Area

Both S25FL116K and W25Q16DV provide three 256-byte Security Registers. Each security register can be read (opcode 48h), programmed (opcode 42h), erased (opcode 44h), and permanently locked by setting Status Register bits LB1, LB2, and LB3 to 1.

2.10 Reset Operations

Both S25FL116K and W25Q16DV support software reset operation. It is used to put the device in normal operating ready mode. This operation consists of two commands: Enable Reset (66h) and Reset (99h).

S25FL116K does not have a hardware Reset pin. If the host system memory controller resets without a complete power down and power up sequence, while S25FL116K is set to Continuous Mode Read, S25FL116K will not recognize any initial standard SPI commands from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset (FFFFh) command as the first command after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI commands to be recognized.

If Burst Wrap Mode is used, it is also recommended to issue a Set Burst with Wrap (77h) command that sets the W4 bit to one as the second command after a system Reset. Doing so will release the device from the Burst Wrap Mode and allow standard sequential read SPI command operation.

Issuing these commands immediately after a non-power-cycle (warm) system reset ensures the device operation is consistent with the power-on default device operation.

2.11 Unique ID

Both S25FL116K and W25Q16DV provide 8-byte unique ID. This is a factory-set read-only number that is unique to each device. The S25FL116K uses command 5Ah to access Read Unique ID Number, and access flow is: opcode 5A -> offset F8h to FFh -> 1 dummy byte -> 64bit unique ID.

W25Q16DV uses command 4Bh to access Unique ID Number, and access flow is: opcode 4B -> 4 dummy bytes -> 64-bit unique ID.

3 Command Set Comparison

W25Q16DV and S25FL116K share similar instructions (op-codes) in their command-set, which determine a compatible set of internal algorithms. Nevertheless, not all commands are supported when comparing one product family with the other.

Table 6 shows a comparison summary of the command set of a Cypress S25FL116K and Winbond W25Q16DV.

Table 6. Command Set of S25FL116K and W25Q16DV

Command Description	S25FL116 Opcode	W25Q16DV Opcode
Configuration, Status, Erase, and Program Commands		
Read Status Register-1	05h	05h
Read Status Register-2	35h	35h
Read Status Register-3	33h	—
Write Enable	06h	06h
Write Enable for Volatile Status Register	50h	50h
Write Disable	04h	04h
Write Status Registers	01h	01h
Set Burst with Wrap	77h	77h
Page Program	02h	02h
Quad Page Program	—	32h
Sector Erase (4 kB)	20h	20h
Block Erase (32 kB)	—	52h
Block Erase (64 kB)	D8h	D8h
Chip Erase	C7h / 60h	C7h / 60h
Suspends Program / Erase	75h	75h
Resumes Program / Erase	7Ah	7Ah
Read Data	03h	03h
Fast Read	0Bh	0Bh
Fast Read Dual Output	3Bh	3Bh
Fast Read Quad Output	6Bh	6Bh
Fast Read Dual I/O	BBh	BBh
Fast Read Quad I/O	EBh	EBh
Continuous Read Mode Reset	FFh	FFh
Word Read Quad I/O	—	E7h
Octal Word Read Quad I/O	—	E3h
ID, Security, and Other Commands		
Deep Power-Down	B9h	B9h
Release Power-Down / Device ID	ABh	ABh
Manufacturer / Device ID	90h	90h
JEDEC ID Read	9Fh	9Fh
Dual I/O JEDEC ID Read	—	92h
Quad I/O JEDEC ID Read	—	94h
Read SFDP Register	5Ah	5Ah
Read Security Registers	48h	48h
Erase Security Registers	44h	44h
Program Security Registers	42h	42h
Read Unique ID	5Ah	4Bh
Enable Reset	66h	66h
Reset	99h	99h

4 Timing Considerations

4.1 Power-Up Timing

One of the most sensitive electrical specifications is the power-up timing needed to correctly initialize the device. Table 7 and Figure 3 show the power-up characteristics of S25FL116K and W25Q16DV. Figure 4 show the power-down characteristics of S25FL116K.

Table 7. Power-Up Timing Requirement

Parameter	Symbol	S25FL116K		W25Q16DV		Unit
		Min	Max	Min	Max	
$V_{CC(min)}$ to CS# Low	t_{VSL}	10		20		µs
Time Delay Before Write Command	t_{PUW}		10	5		ms
Write Inhibit Threshold Voltage	V_{WI}	2.4		1.0	2.0	V
Power-Down Time	t_{PD}	10		x	x	µs
V_{CC} Power-Down Reset Threshold Voltage	V_{CC} Low	1.0		x	x	V

Figure 3. Power-Up Timing and Voltage Levels

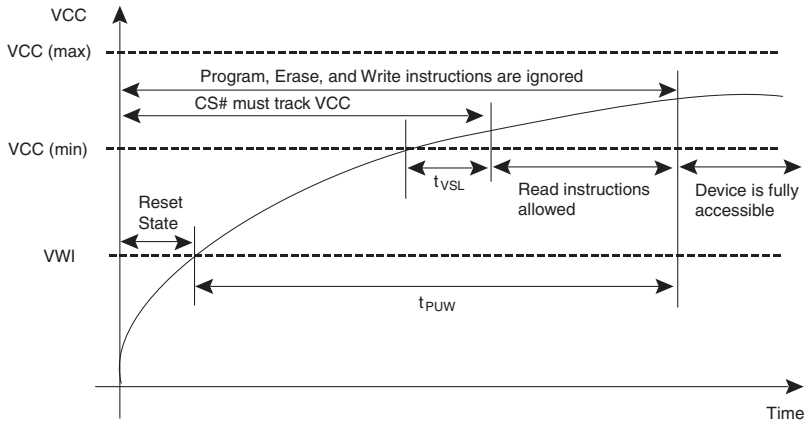
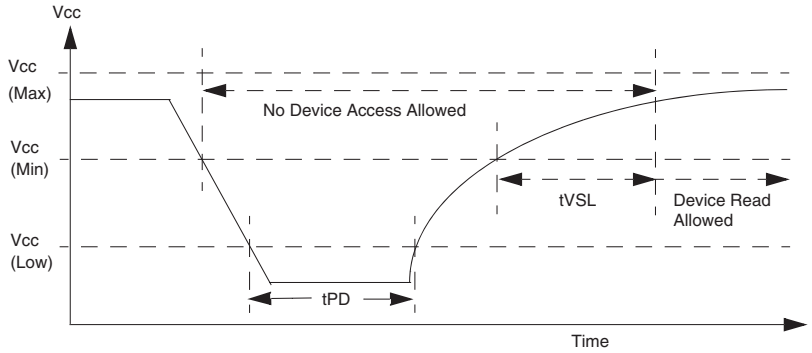


Figure 4. Power-Down and Voltage Drop



4.2 Data In Setup/Hold Time

Two AC timing parameters that are critical in SPI designs are Data-In Setup Time and Data-In Hold Time. They specify how long data needs to be valid before and after the rising edge of the clock signal, respectively. The minor different requirement should not be an issue in the design but may just need to be verified. Table 8 shows the Data-In Setup / Hold timing characteristics for both S25FL116K and Winbond devices.

Table 8. Data-In Setup / Hold Timing Characteristics Comparison

Parameter	S25FL116K	W25Q16DV	Unit
	Min		
Data-In Setup Time	2	2	ns
Data-In Hold Time	5	3	ns

4.3 Further Timing Comparison

In general, the timing characteristics of both Winbond and Cypress flash families are almost identical with just a little deviation.

One difference is that the S25FL116K family has a faster CS# deselect time than W25Q16DV. There is no need to do any changes but it's important to note that read performance of the application can be increased easily here.

When SPI clock frequency is 80 MHz, CS# deselect time for read after writes of W25Q16DV is 12.5 ns minimum. The minor different requirement should not be an issue in the design but may just need to be verified when migrating from W25Q16DV to S25FL116K.

Table 9 shows a comparison between S25FL116K and W25Q16DV with regards to the various CS# deselect times.

Table 9. CS# Deselect Timing Characteristics Comparison

Parameter	S25FL116K	W25Q16DV	Unit
	Min		
CS# deselect time between Reads	7	10	ns
CS# deselect time for Read after Writes	40	50	ns

5 Conclusion

Migrating from Winbond W25Q16DV to the Cypress S25FL116K is straightforward and requires minimal accommodation in regards to either system software or hardware.

Additionally, once accommodations are made, if required, S25FL116K flash will enable access to a wider range of SPI flash features and superior read throughput up to 54 Mbytes/s using Quad bit data path.

Document History Page

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**	-	-	06/09/2014	New Cypress version.
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