# Configuring S25FS128S and S25FS256S SPI Sector Architecture

## About this document

### Scope and purpose

AN98539 discusses the considerations for configuring the S25FS128S and S25FS256S SPI Sector Architecture devices.

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# 1 Introduction

The S25FS-S 1.8 Volt Serial Peripheral Interface (SPI) Multi-I/O Flash Memory family has a flexible hybrid sector architecture with parameter sectors located at either the bottom (default) or top of the memory address space. For the 128-Mbit S25FS128S and the 256-Mbit S25FS256S devices, the hybrid sectors consist of eight (8) 4-kbyte parameter sectors and one (1) adjacent 32-kbyte sector with all remaining sectors of 64-kbytes. The group of 4-kbyte parameter sectors replaces the respective bottom or top 32-kbyte of the lowest or highest address uniform sector. The Parameter Sector Erase commands (20h or 21h) must be used to erase the 4-kB sectors individually. The Sector (uniform block) Erase commands (D8h or DCh) must be used to erase any of the remaining sectors, including the 32-kbyte portion of highest or lowest address sector that is not overlaid by the parameter sectors. The uniform block erase command has no effect on parameter sectors. Uniform Sector Erase commands may also be configured to erase 256-kB logical blocks rather than individual 64-kB physical sectors.

# 2 Sector Configuration Options

In addition to the default bottom configuration, S25FS-S devices can configure the 4-kbyte parameter sectors at the top of the memory space or remove the 4-kbyte (4-kB) parameter sectors from the address map.

## 2.1 Parameter Sector Location

The location of the parameter sectors is controlled by Configuration Register 1 non-volatile bit 2 (CR1NV[2]) also referenced as the TBPARM_O field. Since TBPARM_O is set to 0 (CR1NV[2] = 0) by factory default, the parameter sectors are located at the bottom of the memory address space. When the OTP (One-Time Programmable) TBPARM_O is programmed to 1 (CR1NV[2] = 1), the parameter sectors are located at the top of the memory address space. However, once TBPARM_O is programmed to 1, writing the bit with a 0 does not change the value or set the Status Register 1 Volatile Program Error bit 6 (P_ERR in SR1V[6]) since it is OTP.

The desired state of TBPARM_O must be selected at the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPARM_O must not be programmed after programming or erasing is done in the main flash array since this could result in data loss.

## 2.2 Disabling the 4-kB Parameter Sectors

The state of 4-kbyte parameter sectors is controlled by Configuration Register 3 Non-Volatile bit 3 (CR3NV[3]) also referenced as the 20h_NV field. Since 20h_NV is set to 0 (CR3NV[3] = 0) by factory default, the 4-kbyte parameter sectors are enabled in the Hybrid Sector Architecture.

When the OTP (One-Time Programmable) 20h_NV is programmed to 1 (CR3NV[3] = 1), the 4-kbyte parameter sectors are disabled in the Uniform Sector Architecture. Once 20h_NV is programmed to 1, writing the bit with a 0 does not change the value or set the Status Register 1 Volatile Program Error bit 6 (P_ERR in SR1V[6]) since it is OTP.

When the memory array is configured as uniform sectors, the TBPARM_O bit is Reserved for Future Use (RFU) and has no effect because all sectors are of uniform size.

The desired state of 20h_NV must be selected at the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. 20h_NV must not be programmed after programming or erasing is done in the main flash array since this could result in data loss.

# 3 Sector Erase Size Configuration

Both the S25FS128S and S25FS256S devices may configure the uniform Sector Erase commands to erase 256-kB logical blocks rather than individual 64-kB physical sectors.

This configuration option (CR3V[1]=1) allows lower density devices to emulate the same sector erase behavior as higher density members of the family that use 256-kB physical sectors. This can simplify software migration to the higher density members of the S25FS-S family.

The Sector Erase Size is controlled by Configuration Register 3 Non-Volatile bit 1 (CR3NV[1]) also referenced as the D8h_NV field. Since D8h_NV is set to 0 (CR3NV[1] = 0) by factory default, 64-kbyte is the sector erase size for D8h or DCh sector erase commands. When the OTP (One-Time Programmable) D8h_NV is programmed to 1 (CR3NV[1] = 1), the Sector Erase Size for D8h or DCh sector erase commands is set to 256-kbyte.

Once D8h_NV is programmed to 1, writing the bit with a 0 does not change the value or set the Status Register 1 Volatile Program Error bit 6 (P_ERR in SR1V[6]) since it is OTP. However, Configuration Register 3 Volatile bit 1 (CR3V[1]) can be used to override the OTP D8h_NV setting to erase 64-kbyte sectors for testing or other purposes.

# 4 Programming OTP Bits

Programming the OTP bits for fields such as TBPARM_O, 20h_NV, or D8h_NV requires creating a Configuration Register Non-Volatile bit field mask, programming the bit field mask to the Configuration Register Non-Volatile, and checking the device status to ensure the programming operation has completed.

## 4.1 Pseudo Code Example

Here is a pseudo code example for programming OTP field 20h_NV to 1 (CR3NV[3] = 1) to disable the 4-kbyte parameter sectors of the S25FS-S family.

```
RDAR 65h Read Any Register CR3NV to CR3NVmask
If CR3NVmask[3]=1, then return (done)  /* already set */


Set CR3NVmask[3] = 1
WREN 06h
WRAR 71h Write Any Register: address 0x00000004 (CR3NV) data CR3NVmask
```

*Note: The register address length should correspond to Configuration Register 2 Non-Volatile bit 7 (CR2V[7]) also referenced as the AL_NV field. 3-byte addresses are the default.*

```
RDSR1 05h Read Status Register 1 until WIP Write-In-Progress bit = 0 (SR1V[0]
= 0)
If P_ERR =1 (SR1V[6] = 1) then return (error)    /* check for programming
error */
RSTEN 66h           /* Software Reset Enable */
RST 99h             /* Software Reset             */
```

Upon OTP bit program completion, a POR (Power-On Reset), hardware reset, or software reset command sequence is recommended as a best practice. This ensures the Configuration Register Non-Volatile OTP bit programming is reflected in the volatile version of the Configuration Register and sector configuration changes take effect.

## 4.2 SPI Low Level Driver Based Code Example

The following code snippet leverages the SPI Low Level Driver (SLLD) functions to disable the 4-kbyte parameter sectors of the S25FS-S family. The slld_WRAR_Op function encapsulates all the steps required to write to Configuration Register 3 Non-Volatile including SPI commands WREN Write Enable and WRAR Write Any Register followed by checking for the completion of the register write operation.

```
#include "slld.h"
#define CR3NV_20h_NV B3_MASK


    BYTE CR3NVmask = 0x00;
    SLLD_STATUS status = SLLD_OK;
    DEVSTATUS dstatus;
```

...

### Programming OTP Bits

```
    status = slld_RDARCmd (CR3NV , &CR3NVmask); /* CR3NV defined as address
0x00000004 */


    if (status == SLLD_OK)
    {

        if (CR3NVmask & CR3NV_20h_NV) return(SLLD_OK); /* already set */
    }
    else
    {
        return(status);
    }


    CR3NVmask = CR3NVmask | CR3NV_20h_NV; /* create CR3NV register mask */


    if (slld_WRAR_Op (CR3NV, &CR3NVmask, &dstatus) == SLLD_OK) /* write mask
to CR3NV register */
    {
        /* issue software reset command sequence */
        slld_RSTENCmd();          /* Software Reset Enable */
        slld_RSTCmd();               /* Software Reset             */
    }
    else
    {
        return(SLLD_ERROR);
    }
```

The SPI Low Level Driver (SLLD) is available for download from the **website**.

# 5 Summary

Using Configuration Register Non-Volatile OTP bits, the S25FS128S and S25FS256S devices can configure the 4-kB parameter sectors at the top of the memory space or remove the 4-kB parameter sectors from the address map. In addition, Uniform Sector Erase commands may be configured to erase 256-kB logical blocks rather than individual 64-kB physical sectors to future proof migrations to higher density S25FS-S family devices.

## References

[1] **S25FS-S Family Datasheet**

[2] **SPI Low Level Driver**

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| ** | 2015-01-19 | Initial version |
| *A | 2015- 09-22 | Updated to template |
| *B | 2017-07-18 | Updated logo and Copyright |
| *C | 2017-12-06 | Sunset Review |
| *D | 2021-19-03 | Updated to Infineon template |

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