Designing a Serial Peripheral Interface

Author: Eric Lin

AN98542 introduces the basic features of an SPI interface. It also describes Cypress SPI flash bus protocol, command set, and power cycle.

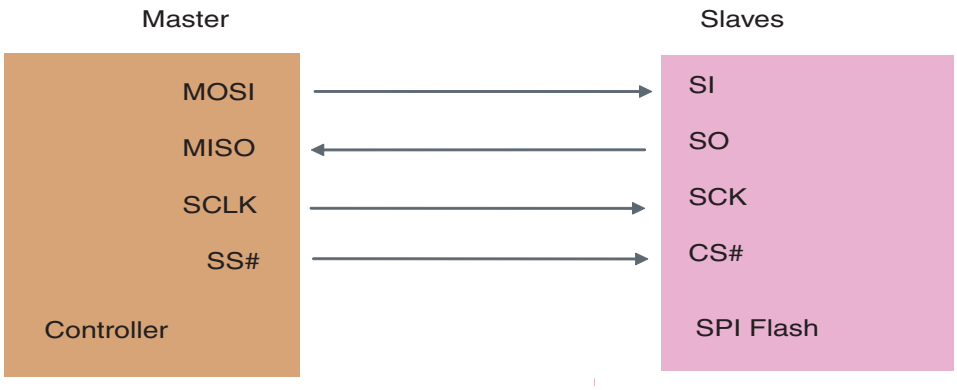
1 What is a Serial Peripheral Interface (SPI)?

A serial peripheral interface (SPI) has a simple 4-wire synchronous interface protocol that enables controllers and peripheral devices to intercommunicate.

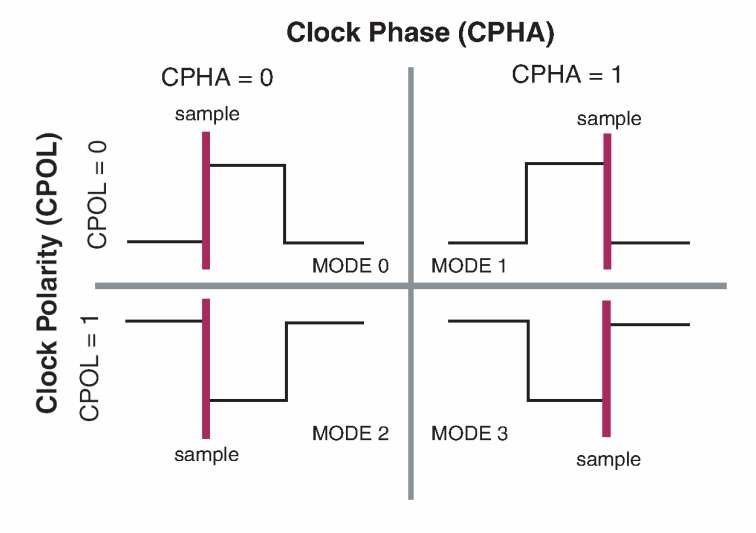
An SPI Bus consists of 4 signal wires. See Figure 1.

1. Master Out Slave In (MOSI) — MOSI signal is generated by Master, recipient is the Slave.
2. Master In Slave Out (MISO) — MISO signals are generated by Slaves, recipient is the Master.
3. Serial Clock (SCLK or SCK) — SCLK signal is generated by the Master to synchronize data transfers.
4. Slave Select (SS#) from master to Chip Select (CS#) of slave — SS# signal is generated by Master to select individual Slave devices.

Figure 1. SPI Bus



2 SPI Bus Modes



CPHA = Clock Phase

CPOL = Clock Polarity

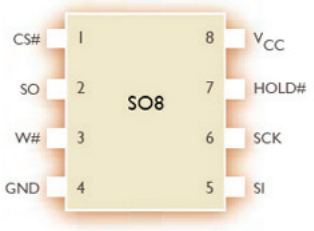
The following values define how the serial SPI bits are latched.

SPI Mode	CPHAS	CPOL	Description
0	0	0	When CPOL is inactive low, rising edge latches SPI data
1	1	0	When CPOL is inactive low, falling edge latches SPI data
2	0	1	When CPOL is inactive high, falling edge latches SPI data
3	1	1	When CPOL is inactive high, rising edge latches SPI data

Cypress SPI Flash supports SPI Mode 0 and Mode 3.

3 Cypress® SPI Product Input/Output Description

SCK	Serial Clock Input (always driven by the master)
SI	Serial Data Input (used to transfer data into the SPI device)
SO	Serial Data Output (used to transfer data out of the SPI device)
CS#	Chip Select Input (for enabling device operation)
W#	Write Protect Input (used to guard against program/erase instructions)
HOLD#	Hold Input (to pause SPI transaction)
Vcc	Supply Voltage
GND	Ground



SOIC - 8

SOIC - 16

USON - 8 (0.5mm height)
WSON - 8 (0.75mm height)

4 Cypress SPI Flash Command Set

Table 1. SPI Flash Command Set

Instruction	Description	One-Byte Instruction Code	Address Bytes	Dummy Bytes	Data Bytes	Total Bytes
Status Register Operations						
WREN	Write Enable	06h (0000 0110)	0	0	0	1
WRDI	Write Disable	04h (0000 0100)	0	0	0	1
WRSR	Write to Status Register	01h (0000 0001)	0	0	1	2
RDSR	Read from Status Register	05h (0000 0101)	0	0	1 to Infinity	2+
Read Operations						
READ	Read	03h (0000 0011)	3	0	1 to Infinity	5+
FAST_READ	Fast Read	0Bh (0000 1011)	3	1	1 to Infinity	6+
RDID(1)	Manuf & Device ID Read	9Fh (1001 1111)	0	0	1 to 3	2+
Erase Operations						
SE	Sector Erase	D8h (1101 1000)	3	0	0	4
BE	Bulk(Chip) Erase	C7h (1100 0111)	0	0	0	1
Program Operations						
PP	Page Program	02h (0000 0010)	3	0	1 to 256	5+
Power Savings Mode Operations						
DP	Deep Power Down	B9h (1011 1001)	0	0	0	1
RES	Release from DP	ABh (1010 1011)	0	0	0	1
	Release from DP and Read Electronic Signature	ABh (1010 1011)	0	3	1 to Infinity	5+

Note:

1. *All instructions, addresses and data are shifted in and out of the device, MSB first. SI is sampled on the 1st rising edge of SCK after CS# is driven low. Then, the 1-byte instruction opcode is shifted into the device via SI, MSB first.*

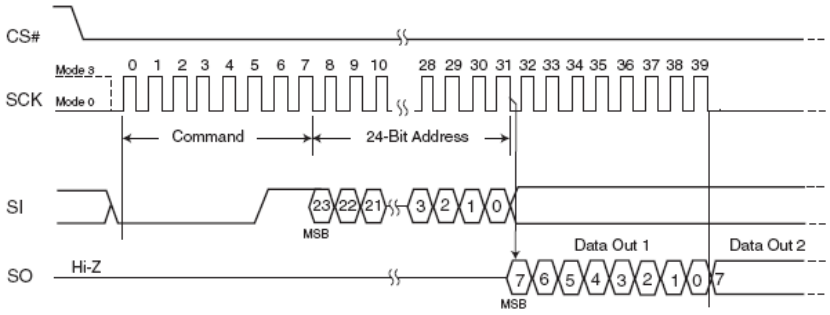
5 Cypress SPI Flash Operations

5.1 Normal Read Operation

Normal Read command (0x03h) enables data to be read from the memory array at the SCK (maximum 33 MHz).

1. The host system must first select the device by driving CS# to active low.
2. The READ command (0x03h) is written to SI, followed by a 3-byte address (A23-A0) and can be at any location of the device.
3. The device automatically increments to the next higher address after each byte of data is outputted.
4. The device allows single-byte read sequence and can continue data output, indefinitely.
5. The READ command is terminated by driving CS# high at any time during data output.

6. The device rejects any READ command issued while it is executing a program, erase, or Write Status Register operation, and continues the operation uninterrupted.

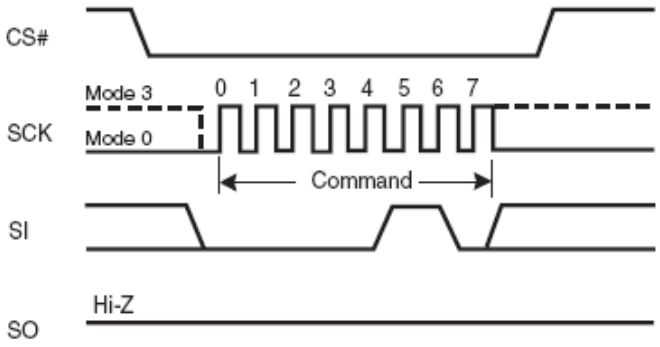


5.2 Page Program Operation and How to Check Status

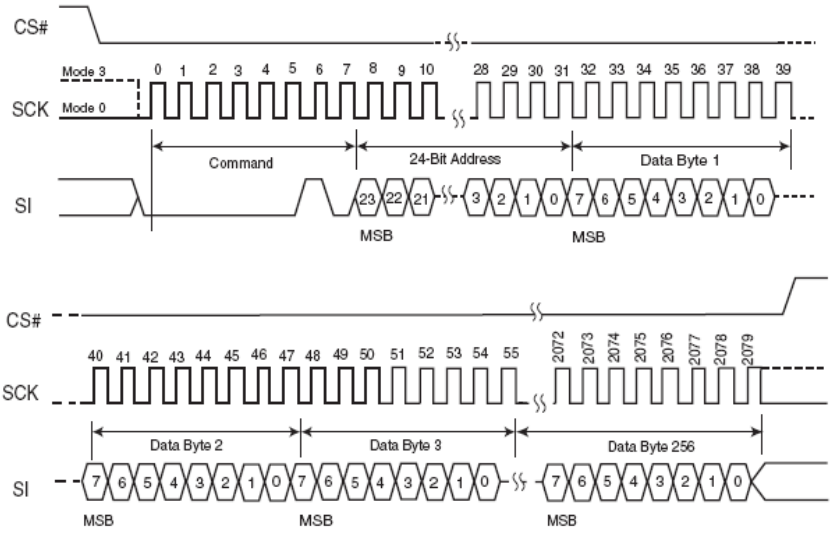
Page Program (PP) command (0x02h) enables memory array data to be programmed from 1 to 0.

1. The host system must first select the device by driving CS# to low.
2. A WREN command (0x06h) is required prior to writing the PP command.

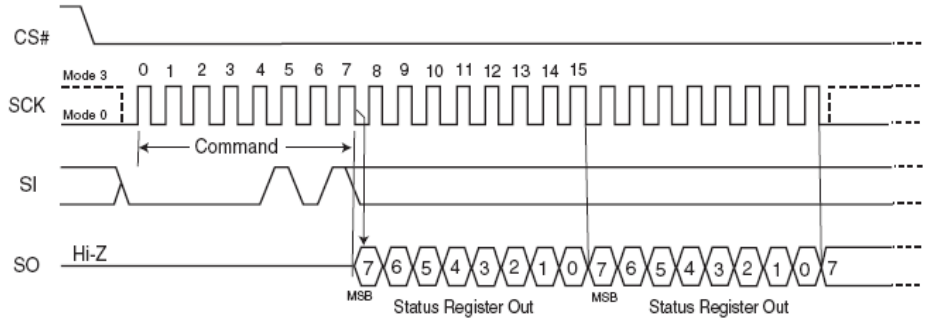
   The Write Enable (WREN) command (shown below) sets the Write Enable Latch (WEL) bit to a 1, which enables the device to accept a Write Status Register, program, or erase command. The WEL bit must be set prior to every Page Program (PP), Erase (SE or BE) and Write Status Register (WRSR) command.



3. The PP command (0x02h) (shown below) is written to SI, followed by three address bytes, and at least one data byte written to SI.
4. The device programs only the last 256 data bytes sent to the device.
5. The host system must drive CS# high after the device has latched the 8th bit of the data byte.



6. Use Read Status Register command (0x05h) (shown below) to check the value of the Write In Progress (WIP) bit while the PP operation is in progress.



7. The WIP bit is 1 during the PP operation, and is 0 when the operation is completed.

Table 2 highlights the 8 bits that are part of the SPI Status register.

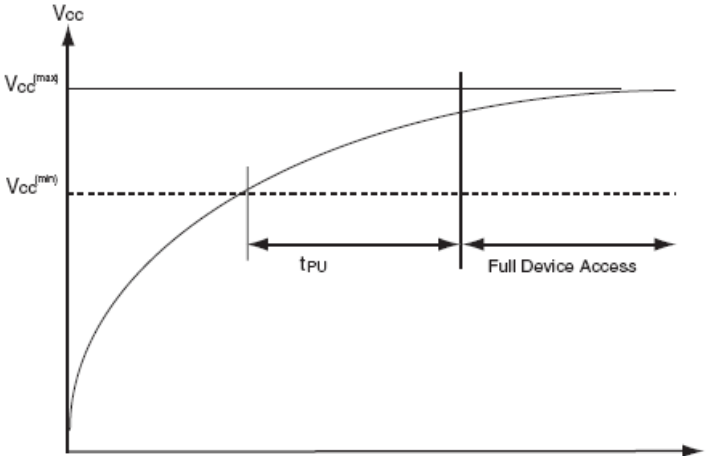
Table 2. SPI Status Register Bits

Bit	Status Register Bit	Bit Function	Description
7	SRWD	Status Register Write Disable	1 = Protects when W# is low 0 = No protection, even when W# is low
6	—	—	Not used
5	—	—	Not used
4	BP2	Block Protect	Protected memory size starting from upper most address: 000 = none, 001 = 1/64, 010 = 1/32, 011 = 1/16, 100 = 1/8, 101= 1/4, 110 = 1/2, 111 = all
3	BP1		
2	BP0		
1	WEL	Write Enable Latch	1 = Device accepts Write Status Register, program, or erase commands 0 = Ignores Write Status Register, program, or erase commands
0	WIP	Write in Progress	1 = Device Busy. A Write Status Register, program, or erase operation is in progress 0 = Ready. Device is in standby mode and can accept commands.

6 Power-Up

During power-up certain conditions must be observed.

1. CS# must follow the voltage applied on V_{CC}, and must not be driven low to select the device until V_{CC} reaches the allowable values as follows
2. No Write Status Register, program, or erase command should be sent to the device until V_{CC} rises to the V_{CC}(min), and then to a further delay of t_{PU}
3. At power-up, the device is in standby mode and the WEL bit is reset (0).



Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC}(minimum)	2.7		V
t_{PU}	V_{CC}(min) to device operations	10		ms

Document History Page

Document Title: AN98542 - Designing a Serial Peripheral Interface Document Number: 001-98542				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	03/04/2008	Initial version
*A	4943347	MSWI	10/01/2015	Updated in Cypress template
*B	5803538	AESATMP8	07/07/2017	Updated logo and Copyright.

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