AN98574

Migration from S25FL-K to S25FL1-K SPI Flash Memories

AN98574 discusses the specification differences that must be considered when migrating to S25FL1-K from a like-density S25FL-K.

1 Introduction

Cypress S25FL1-K flash is a feature rich and cost-optimized serial peripheral interface (SPI) non-volatile NOR flash family manufactured on a 90 nm 3-volt floating gate process technology node. The S25FL1-K family is composed of three members:

- S25FL116K16 Mbit (2 MB)
- S25FL132K32 Mbit (4 MB)
- S25FL164K64 Mbit (8 MB)

S25FL1-K flash can replace legacy S25FL-K flash in most applications without hardware or software modification. This application note discusses the specification differences that must be considered when migrating to S25FL1-K from a like density S25FL-K.

2 Feature Comparison and Differences

The S25FL1-K supports a subset of features that are supported by S25FL-K. Table 1 summarizes the feature similarities and differences between S25FL-K and S25FL1-K.

Table 1. High Level Feature Support Comparison (Sheet 1 of 2)

Feature / Parameter (1)	FL-K	FL1-K
16-Mbit, 32-Mbit, 64-Mbit Density Options	√	√
4-Mbit, 8-Mbit, 128-Mbit Density Options	√	—
Single (Standard)/Dual/Quad IO Operations	√	√
Standard Normal Read SCK Frequency (max)	50 MHz	50 MHz
Standard/Dual/Quad Fast Read SCK Frequency (max)	80/104 MHz	108 MHz
Continuous and Wrapped Read Modes	√	√
Quad IO Word and Octal Burst Read	√	—
Variable Read Latency	—	√
256B Program Page	√	√
Quad IO Page Programming	√	—
Program and Erase Suspend/Resume Functions	√	√ (2)
4 kB, 64 kB, and Chip Erase Granularity	√	√
32-kB Block Erase Granularity	√	—
Fractional Block Protection (BP)	√	√
Complement Block Protection	√	√
Pointer-based Block Protection	—	√ (3)
Serial Flash Discoverable Parameter (SFDP) Register	√	√
Volatile Configuration (4)	—	√
Unique Serial Number	√	—
One Time Programmable Region(s)	3 x 256B	3 x 256B

Table 1. High Level Feature Support Comparison (Sheet 2 of 2)

Feature / Parameter (1)	FL-K	FL1-K
Deep Power-Down Mode	√	√
8-lead SOIC (150 and 208mil) Package Options (5)(6)	√	√
16-lead SOIC Package Option (7)	√	√
KGD, USON, and BGA Package Options	—	√
-40° to +85°C Temperature Range Option	√	√
-40° to +105°C Temperature Range Option	—	√

Notes:

1. *Comparisons apply to operation while V_{CC} = 2.7 to 3.6V and temperature = -40° to +85°C.*
2. *For S25FL116K only, support for Program and Erase Suspend functions varies by ordering part number (see data sheet or contact Cypress Sales for clarification).*
3. *Pointer-based Block Protection supported by S25FL132K and S25FL164K only.*
4. *In addition to legacy non-volatile configuration.*
5. *8-lead SOIC (150 mil) Package available on FL004K, FL008K, FL016K, FL116K, and FL132K devices.*
6. *8-lead SOIC (208 mil) Package available on FL004K, FL008K, FL016K, FL032K, FL064K, FL116K, FL132K, and FL164K devices.*
7. *16-lead SOIC Package available on FL064K, FL128K, and FL164K devices.*

2.1 Command Differences

S25FL1-K supports the vast majority of the read, program, erase, identification and mode control commands that are supported by S25FL-K. Table 2 summarizes the commands supported by either S25FL-K or S25FL1-K.

Table 2. Supported Commands (Sheet 1 of 2)

Command Description	Opcode	FL-K	FL1-K
Array Read Operations			
Standard Read (READ)	03h	√	√
Fast Standard Read (FAST_READ)	0Bh	√	√
Fast Dual Output Read (DOR)	3Bh	√	√
Fast Quad Output Read (QOR)	6Bh	√	√
Fast Dual I/O High Read (DIOR)	BBh	√	√
Fast Quad I/O High Read (QIOR)	EBh	√	√
Quad I/O Octal Word Read	E3h	√	—
Quad I/O Word Read	E7h	√	—
Set Burst with Wrap	77h	√	√
Continuous Read Mode Reset	FFh	√	√
Array Program and Erase Operations			
Page Program (PP)	02h	√	√
Quad Page Programming (QPP)	32h	√	—
4-kB Sector Erase (P4E)	20h	√	√
32-kB Block Erase	52h	√	—
64-kB Block Erase (SE)	D8h	√	√
Bulk Erase (BE)	60h / C7h	√	√
Program/Erase Suspend	75h	√	√ (1)
Program/Erase Resume	7Ah	√	√ (1)
Write Control			
Write Disable (WRDI)	04h	√	√
Write Enable (WREN)	06h	√	√
Write Enable for Volatile Status Register	50h	√	√
Status Register Operations			
Write Status Register (WRR)	01h	√	√
Read Status Register 1 - SR1[7:0] (RDSR)	05h	√	√
Read Status Register 2 - SR2[7:0] (RDSR)	35h	√	√

Table 2. Supported Commands (Sheet 2 of 2)

Command Description	Opcode	FL-K	FL1-K
Read Status Register 3 - SR3[7:0] (RDSR)	33h	—	√
ID and Security			
Deep Power-Down (DP)	B9h	√	√
Release from Deep Power-Down and Read Electronic Signature (RES)	ABh	√	√
Read Manufacturer and Device Identification (READ_ID)	90h	√	√
Read Identification - JEDEC ID (RDID)	9Fh	√	√
Read Identification by Dual I/O	92h	√	—
Read Identification by Quad I/O	94h	√	—
Read Unique ID	4Bh	√	—
Read SFDP Mode	5Ah	√	√
Read Security Registers	48h	√	√
Program Security Registers	42h	√	√
Erase Security Registers	44h	√	√
Set Pointer Value	39h	— (2)	√

Notes:

1. *For S25FL116K only, support for Program and Erase Suspend functions varies by ordering part number (see data sheet or contact Cypress Sales for clarification).*
2. *Pointer-based Block Protection supported by S25FL132K and S25FL164K only.*

Migration from S25FL-K to S25FL1-K requires driver modification if the existing application utilizes any of the seven S25FL-K specific opcodes listed in Table 2 (32h, 4Bh, 52h, 92h, 94h, E3h, E7h).

2.2 Modes of Operation

The S25FL1-K and S25FL-K support the standard SPI Mode 0 (0,0) and Mode 3 (1,1) modes of operation utilizing a single IO. See data sheet for full details of supported modes of operation and related commands.

2.2.1 Standard (Single IO) Modes

S25FL-K and S25FL1-K support Standard (Single IO) modes of operation, including Read (opcode 03h), Fast Read (opcode 0Bh), and Page Program (opcode 02h). For the S25FL1-K, all commands that query or manipulate configuration, status or security registers, or that manipulate the main array, use the Standard (Single IO) mode only.

Unlike the S25FL-K, the S25FL1-K does not support erasing in 32 kB blocks (opcode 52h). The S25FL1-K supports full chip erasure (opcodes 60h and C7h) and erasure in 4 kB and 64 kB increments (opcodes 20h and D8h, respectively).

The S25FL1-K adds support for variable latency read timing to enable faster initial access time or higher clock rate read commands. Use of this feature is optional, see full feature details in the S25FL1-K data sheet.

2.2.2 Dual Modes

Both the S25FL-K and S25FL1-K support Fast Dual Output Read (opcode 3Bh) and Fast Dual IO High Read (opcode BBh) modes. Neither the S25FL-K nor S25FL1-K support programming in Dual IO mode.

2.2.3 Quad Mode

Both the S25FL-K and S25FL1-K support Fast Quad Output Read (opcode 6Bh) and Fast Quad IO High Read (opcode EBh) modes. Unlike the S25FL-K, the S25FL1-K does not support Quad IO Octal Word Read (opcode E3h), Quad IO Word Read (opcode E7h) or Quad Page Programming (opcode 32h).

The S25FL-K and S25FL1-K support Fast Quad IO High Read (opcode EBh) in standard continuous mode and in Burst with Wrap mode. Both support the use of the Set Burst with Wrap command (opcode 77h) preceding the Fast Quad IO High Read command. The S25FL1-K has an additional method for enabling Burst with Wrap mode by using the S25FL1-K exclusive Status Register bits W4, W5, W6 (SR3[4:6]).

2.3 Device Identification

The S25FL-K and S25FL1-K support Standard mode (Single IO) READ-ID (90h), RDID (9Fh) and RES (ABh) device identification command methods, as shown in Table 3 through Table 5, respectively. Unlike the S25FL-K, the S25FL1-K does not support Dual or Quad mode Read Identification commands (opcodes 92h and 94h, respectively).

The Manufacturer ID byte is different for S25FL-K and S25FL1-K, the latter using Cypress's standard 01h value.

The S25FL1-K uses the same identification data convention as employed in S25FL-K, e.g. S25FL116K provides the same returned values as the S25FL016K for Device ID.

Table 3. Product Identification - READ-ID (Opcode 90h)

Device	READ-ID Manufacturer ID Byte 0 (MF7-MF0)	READ-ID Device ID Byte 1 (ID7-ID0)
S25FL016K	EFh	14h
S25FL032K	EFh	15h
S25FL064K	EFh	16h
S25FL116K	01h	14h
S25FL132K	01h	15h
S25FL164K	01h	16h

Table 4. Product Identification - Read JEDEC ID (Opcode 9Fh)

Device	Read JEDEC ID Manufacturer ID Byte 0 (MF7-MF0)	Read JEDEC ID Memory Type Byte 1 (ID15-ID8)	Read JEDEC ID Capacity Byte 2 (ID7-ID0)
S25FL016K	EFh	40h	15h
S25FL032K	EFh	40h	16h
S25FL064K	EFh	40h	17h
S25FL116K	01h	40h	15h
S25FL132K	01h	40h	16h
S25FL164K	01h	40h	17h

Table 5. Product Identification - Read Electronic Signature RES (Opcode ABh)

Device	Read Electronic Signature Device ID Byte 0 (ID7-ID0)
S25FL016K	14h
S25FL032K	15h
S25FL064K	16h
S25FL116K	14h
S25FL132K	15h
S25FL164K	16h

The S25FL-K and S25FL1-K support the Serial Flash Discoverable Parameter (SFDP) register for run-time driver configuration. Unlike the S25FL-K, S25FL1-K does not contain a unique factory programmed serial number and does not support the Read Unique ID command (opcode 4Bh).

2.4 Status Register

The S25FL-K has a 2-byte Status Register, S0-S15, with 15 defined bits. The S25FL1-K has a 3-byte Status Register, SR1[0-7], SR2[0-7], SR3[0-7], with 23 defined bits. Table 6 illustrates the Status Register bit assignments for S25FL-K and S25FL1-K. The function of the defined S25FL-K Status Register bits, S0-S9 and S11-S15, are identical to the corresponding bit locations in the lower two bytes of the S25FL1-K Status Register,

SR1[0-7], SR2[0-1] and SR2[3-7]. The functions of the six defined bits in the upper byte of the S25FL1-K Status Register, SR3[0-6], are unique. Please refer to the flash data sheet for complete definition and usage of the Status Register bits, including the new burst wrap length, variable latency and volatile Status Register features of the S25FL1-K.

Table 6. Status Register Comparison

S25FL-K				Functionally Compatible	S25FL1-K			
Reg Bit	Default	Bit Name	Bit Function		Reg Bit	Default	Bit Name	Bit Function
S0	0	BUSY	Erase/Write in Progress	Yes	SR1[0]	0	BUSY	Erase/Write in Progress
S1	0	WEL	Write Enable Latch	Yes	SR1[1]	0	WEL	Write Enable Latch
S2	0	BP0	Block Protect Bit	Yes	SR1[2]	0	BP0	Block Protect Bit
S3	0	BP1	Block Protect Bit	Yes	SR1[3]	0	BP1	Block Protect Bit
S4	0	BP2	Block Protect Bit	Yes	SR1[4]	0	BP2	Block Protect Bit
S5	0	TB	Top/Bottom Protect	Yes	SR1[5]	0	TB	Top/Bottom Protect
S6	0	SEC	Sector/Block Protect	Yes	SR1[6]	0	SEC	Sector/Block Protect
S7	0	SRP0	Status Reg. Protect 0	Yes	SR1[7]	0	SRP0	Status Reg. Protect 0
S8	0	SRP1	Status Reg. Protect 1	Yes	SR2[0]	0	SRP1	Status Reg. Protect 1
S9	0	QE	Quad Enable	Yes	SR2[1]	0	QE	Quad Enable
S10	0	R	Reserved	No	SR2[2]	1	LB0	Security Reg Lock Bit 0
S11	0	LB1	Security Reg Lock Bit 1	Yes	SR2[3]	0	LB1	Security Reg Lock Bit 1
S12	0	LB2	Security Reg Lock Bit 2	Yes	SR2[4]	0	LB2	Security Reg Lock Bit 2
S13	0	LB3	Security Reg Lock Bit 3	Yes	SR2[5]	0	LB3	Security Reg Lock Bit 3
S14	0	CMP	Complement Protect	Yes	SR2[6]	0	CMP	Complement Protect
S15	0	SUS	Suspend Status	Yes	SR2[7]	0	SUS	Suspend Status
—	—	—	—	No	SR3[0]	0	LC	Variable Read Latency
—	—	—	—	No	SR3[1]	0	LC	Variable Read Latency
—	—	—	—	No	SR3[2]	0	LC	Variable Read Latency
—	—	—	—	No	SR3[3]	0	LC	Variable Read Latency
—	—	—	—	No	SR3[4]	1	W4	Burst Wrap Enable
—	—	—	—	No	SR3[5]	1	W5	Burst Wrap Length
—	—	—	—	No	SR3[6]	1	W6	Burst Wrap Length
—	—	—	—	No	SR3[7]	0	RFU	Reserved

The S25FL-K and S25FL1-K use opcode 05h to read the lower byte of their Status Registers (Status Register 1) and opcode 35h to read the second byte of their Status Registers (Status Register 2). The S25FL1-K uses opcode 33h to read the third byte of its Status Register (Status Register 3) as well as the Pointer value utilized by the optional pointer based sector protection scheme supported by the S25FL132K and S25FL164K. Use of the third byte of the S25FL1-K Status Register (or Status Register 3) is optional so its existence does not create an incompatibility when migrating from S25FL-K.

The default values of the lower byte of the S25FL-K and S25FL1-K Status Registers (Status Register 1) are identical with all bits being 0. The default values of the second byte of the S25FL-K and S25FL1-K (Status Register 2) are not identical, with all bits being 0 for S25FL-K and all bits except bit 2 being 0 for S25FL1-K. This difference may require software modification when migrating from S25FL-K to S25FL1-K if the existing driver did not mask out the reserved S10 bit during opcode 35h returned value queries.

Both the S25FL-K and S25FL1K use the Write Enable command (opcode 06h) followed by the Write Status Registers command (opcode 01h) to modify the Status Register bits. The Write Enable command sets the WEL bit (S1 or SR1[1]) and the Write Status Registers command modifies those bits that can be modified, e.g. non-volatile bits SRP0, SEC, TB, BP2, BP1, BP0, CMP, LB3, LB2, LB1, LB0, QE and SRP1 and the S25FL1-K only volatile bits SR3[0:6]. The Write Status Register command must end with a CS# transition to high after the eighth bit of a data byte, e.g. CS# set to 1 after the 8th, 16th or 24th data bit is entered. Writing to the third byte of the S25FL1-K Status Register is optional so its presence does not create an incompatibility when migrating from the S25FL-K.

Both the S25FL-K and S25FL1-K support the use of the Write Disable command (opcode 04h) to reset the Status Register WEL bit to 0.

2.5 Security and Write Protection

The S25FL-K and S25FL1-K have three 256B security registers which can be read (opcode 48h), programmed (opcode 42h), erased (opcode 44h), and permanently locked by setting Status Register bits LB1, LB2 and LB3 to 1.

The S25FL-K and S25FL1-K support identical variable size block protection by use of Status Register bits BP0, BP1, BP2, TB, SEC, and CMP. Please see specific protection options in the product data sheet.

The S25FL132K and S25FL164K support an additional pointer-based sector protection scheme that allows securing a range of sectors from the top or bottom of the array to any 4-kB sector boundary within the array. Op code 39h is used to enable and configure this sector protection scheme and opcode 33h functionality has been extended to enable reading of the pointer value following output of SR3. Please refer to the data sheet for specific implementation details. Use of this pointer based sector protection scheme is optional and this feature does not need to be accommodated when migrating from S25FL032K or S25FL064K.

2.6 DC and AC Parameter

The S25FL-K and S25FL1-K have largely compatible DC and AC parameter specifications. Table 7 highlights the minor differences in DC parameters for S25FL-K and S25FL1-K, none of which should cause issues when migrating from S25FL-K.

Table 7. DC Parameter Differences

DC Parameter	Type	Units	S25FL-K	S25FL1-K
V_{IOT}: Transient Voltage on Any Pin	Max	V	V_{CC} + 2.0	6
V_{CC}: Operating Range Core Source Voltage	Min / Max	V	2.7 / 3.6 (1)	2.7 / 3.6
I_{CC1}: Standby Current	Typ / Max	µA	10 / 25	20 / TBD
I_{CC2}: Power Down Current	Typ / Max	µA	1 / 5	2 / TBD
I_{CC4}: Write Status Register Current	Max	mA	15	12

Note:

1. *S25FL-K orderable with V_{CC} operating range of either 2.7-3.6V or 3.0-3.6V.*

Table 8 highlights the AC parameter differences for S25FL-K and S25FL1-K. While most parameter differences should not cause performance issues when migrating from S25FL-K, it is highly recommended that the user carefully review all parameter differences for potential impact.

Table 8. AC Parameter Differences

Parameter (1)	Type	Units	S25FL004K	S25FL104K
f_R: SCK Frequency - Read Data Instruction (03h)	Max	MHz	33	50
F_R: SCK Frequency - All Other Commands	Max	MHz	80/104	108
t_{CLH}, t_{CLL}: Clock High/Low Time –– except Read (03h) and Fast Read	Min	ns	4.5/6	3.3
t_{CLH}, t_{CLL}: Clock High/Low Time –– Fast Read	Min	ns	6	4.3
t_{CRLH}, t_{CRLL}: Clock High/Low Time –– Read (03h)	Min	ns	8	6
t_{CSH}, t_{CS1}: CS# High Time Between Read Instructions	Min	ns	10	7
t_{CSH}, t_{CS2}: CS# High Time Between Erase/Program and Status Read	Min	ns	50	40
t_{HO}: Output Hold Time	Min	ns	0	2
t_{BP1}: Byte Program Time (1st byte)	Typ	ns	20/30	15
t_{SE}: Sector Erase Time (4 kB)	Typ / Max	ms	30 / 400	70 / 450
t_{BE}: Block Erase Time (64 kB)	Typ / Max	s	0.15 / 1	0.35 / 2

Note:

1. *All specifications for V_{CC} = 2.7 to 3.6V operation and C_L = 30 pF.*

3 Conclusion

Migration from the S25FL-K to the S25FL1-K is straightforward and can be accomplished with minimal firmware and/or software modifications. Additionally, new features and higher performance of S25FL1-K can bring benefits to systems and applications currently using S25FL-K.

Document History Page

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**	-	-	01/14/2013	Initial version
*A	-	-	02/11/2013	Added S25FL116K specific note to Table 2.1: High Level Feature Support Comparison and Table 2.2: Supported Commands
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