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Spec Title: AN98575 - MIGRATION FROM S25FL-K TO S25FL2-K SPI FLASH MEMORIES

Replaced by: NONE

AN98575

Migration from S25FL-K to S25FL2-K SPI Flash Memories

AN98575 discusses the specification differences that must be considered when migrating to S25FL2-K from a like density S25FL-K.

1 Introduction

Cypress S25FL2-K flash is a cost-optimized serial peripheral interface (SPI) non-volatile NOR flash family manufactured on a 90 nm floating gate process technology node. The S25FL2-K family is composed of three members:

- S25FL204K 512 kB (4 Mbit)
- S25FL208K 1 MB (8 Mbit)
- S25FL216K 2 MB (16 Mbit)

S25FL2-K flash can replace legacy S25FL-K flash in many applications. Certain features and performance attributes supported by the S25FL-K are not supported by the S25FL2-K. This application note discusses the specification differences that must be considered when migrating to S25FL2-K from a like density S25FL-K.

2 Feature Comparison

The S25FL2-K supports a subset of features that are supported by S25FL-K. Table 1 summarizes the feature similarities and differences between S25FL-K and S25FL2-K. The principal feature differences are related to Quad IO support, identification, and security options. Differences are discussed in more detail in later sections.

Table 1. Feature Comparison between Cypress S25FL-K and S25FL2-K

Feature / Parameter (1)	FL-K	FL2-K
4-Mbit, 8-Mbit, 16-Mbit Density Options	Yes	Yes
32+ Mbit Density Options	Yes	No
Standard Single IO Operation	Yes	Yes
Dual Output Operation	Yes	Yes
Dual/Quad IO Operation	Yes	No
Burst Read with Wrap	Yes	No
256B Program Page Buffer Depth	Yes	Yes
4-kB Sector Erase Granularity	Yes	Yes
32-kB Block Erase Granularity	Yes	No
64-kB Block Erase Granularity	Yes	Yes
HOLD# and WP# Inputs	Yes	Yes
Single IO Normal Read SCK Frequency (max)	50 MHz	44 MHz
Single/Dual Fast Read SCK Frequency (max)	80 MHz	65+ MHz (2)
Program and Erase Suspend/Resume Function	Yes	No
SFDP Register	Yes	No
Fractional Block Protection (BP)	Yes	Yes
Complement Block Protection	Yes	No
Unique Serial Number	Yes	No
One Time Programmable Region(s)	Yes	No

Table 1. Feature Comparison between Cypress S25FL-K and S25FL2-K (Continued)

Feature / Parameter (1)	FL-K	FL2-K
Deep Power Down Mode	Yes	Yes
SOIC 8 (150- and 208-mil) Package Options	Yes	Yes

Notes:

1. *Comparisons apply to operation while V_{CC} = 2.7 to 3.6V and temperature = -40 to +85°C.*
2. *Single and Dual Output Fast Read maximum frequency varies by density: S25FL204K - 85 MHz, S25FL208K - 76 MHz, S25FL216K - 65 MHz.*

2.1 Commands

The S25FL2-K supports all basic read, program, erase, identification, and mode control commands that are supported by the S25FL-K. Table 2 summarizes the commands supported by both S25FL2-K and S25FL-K. Table 3 lists the commands that are supported by the S25FL-K but not the S25FL2-K. Migration from S25FL-K to S25FL2-K can only be accomplished without driver changes provided none of the opcodes listed in Table 3 are used by existing drivers.

Table 2. Commands Supported by Both S25FL2-K and S25FL-K

Command	Description	Opcode
Read Operations		
READ	Read Data Bytes	03h
FAST_READ	Read Data Bytes at Higher Speed	0Bh
DOR	Dual Output Read	3Bh
READ_ID	Read Manufacturer and Device Identification	90h
RDID	Read Identification JEDEC	9Fh
Write Control		
WRDI	Write Disable	04h
WREN	Write Enable	06h
Program and Erase Operations		
PP	Page Program	02h
P4E	4-kB Sector Erase	20h
BE	Bulk Erase	60h / C7h
SE	64-kB Block Erase	D8h
Power Saving Mode		
RES	Release from Deep Power-Down and Read Electronic Signature	ABh
DP	Deep Power Down	B9h
Status and Configuration Register Operations		
WRR	Write (Status and Configuration) Register	01h
RDSR	Read Status Register	05h

Table 3. S25FL-K Commands Not Supported by S25FL2-K

Command	Description	Opcode
Read Operations		
QOR	Quad Output Read	6Bh
	Set Burst with Wrap	77h
	Read Identification by Dual I/O	92h
	Read Identification by Quad I/O	94h
DIOR	Dual I/O High Performance Read	BBh
	Quad I/O Octal Word Read	E3h
	Quad I/O Word Read	E7h
QIOR	Quad I/O High Performance Read	EBh
	Continuous Read Mode Reset	FFh
Write Control		
	Write Enable for Volatile Status Register	50h
Program and Erase Operations		
QPP	Quad Page Programming	32h
	32-kB Block Erase	52h
	Program/Erase Suspend	75h
	Program/Erase Resume	7Ah
Status and Configuration Register Operations		
	Read Status Register-2	35h
OTP Operations		
	Program Security Registers	42h
	Erase Security Registers	44h
	Read Security Registers	48h
	Read SFDP Register	48h, 5Ah
Others		
ABRD	Read Unique ID	4Bh

2.2 Modes of Operation

The S25FL2-K and S25FL-K support the standard SPI Mode 0 (0,0) and Mode 3 (1,1) modes of operation utilizing a single IO. See data sheets for full details of supported modes of operation and related commands.

2.2.1 Dual Output / Dual IO Mode

The S25FL2-K and S25FL-K support Dual Output mode and the Fast Read Dual Output (3Bh) command (3Bh opcode), which uses single IO channel for both command and address input. Unlike the S25FL-K, the S25FL2-K does not support Dual IO mode and the Fast Read Dual I/O command (BBh opcode), which uses single IO channel for command input and dual I/O channels for address input.

2.2.2 Quad Output / Quad IO Mode

Unlike the S25FL-K, the S25FL2-K does not support Quad Output or Quad IO modes of operation. The S25FL2-K will ignore any Quad mode command.

2.3 Device Identification

The S25FL2-K supports standard READ-ID (90h), RDID (9Fh), and RES (ABh) device identification command methods, as shown in Table 4 through Table 6, respectively. The Manufacturer ID byte is different for S25FL-K and S25FL2-K, the latter using Cypress's standard 01h value. The S25FL2-K uses the same identification data convention as employed in S25FL-K, e.g. The S25FL204K provides the same returned values as the S25FL004K for Device ID.

Table 4. Product Identification - READ-ID (Opcode 90h)

Device	READ-ID Manufacturer ID Byte 0 (MF7-MF0)	READ-ID Device ID Byte 1 (ID7-ID0)
S25FL004K	EFh	12h
S25FL008K	EFh	13h
S25FL016K	EFh	14h
S25FL204K	01h	12h
S25FL208K	01h	13h
S25FL216K	01h	14h

Table 5. Product Identification - Read JEDEC ID (Opcode 9Fh)

Device	Read JEDEC ID Manufacturer ID Byte 0 (MF7-MF0)	Read JEDEC ID Memory Type Byte 1 (ID15-ID8)	Read JEDEC ID Capacity Byte 2 (ID7-ID0)
S25FL004K	EFh	40h	13h
S25FL008K	EFh	40h	14h
S25FL016K	EFh	40h	15h
S25FL204K	01h	40h	13h
S25FL208K	01h	40h	14h
S25FL216K	01h	40h	15h

Table 6. Product Identification - Read Electronic Signature RES (Opcode ABh)

Device	Read Electronic Signature Device ID Byte 0 (ID7-ID0)
S25FL004K	12h
S25FL008K	13h
S25FL016K	14h
S25FL204K	12h
S25FL208K	13h
S25FL216K	14h

The S25FL2-K does not support the Serial Flash Discoverable Parameter (SFDP) register. Applications that must use SFDP parameters for driver configuration cannot use the S25FL2-K.

2.4 Status Register

The S25FL2-K has an 8-bit Status Register (R0-R7), which is read accessed using the Read Status Register command (05h opcode), and write accessed using the Write Enable command (06h opcode) and the Write Status Register command (01h opcode).

In comparison, the S25FL-K has a 16-bit Status Register (S0-S15). Read access to the lower byte (S0-S7) is by the same Read Status Register command (05h opcode) used by the S25FL2-K. Read access to the upper byte (S8-S15) is via the Read Status Register 2 command (35h opcode). Write access to the Status Register uses the same Write Enable command (06h opcode) and the Write Status Register command (05h opcode) used by S25FL2-K; however, the Write Status Register command for S25FL-K has three bytes inputs: Command Opcode, followed by Status Register Lower Byte (S7-S0), followed by Status Register Upper Byte (S15-S8). Additionally, the S25FL-K supports the Write Status Register Volatile command (50h opcode), which allows the normally non-volatile Status Register bits to be written as volatile bits. This feature is not supported by the S25FL2-K.

The S25FL2-K Status Register is not functionally compatible with the Status Register Lower Byte of the S25FL-K. Table 7 highlights the differences in Status Register bit definitions. Only the WIP (R0/S0 bit), WEL (R1/S1 bit), and SRP/SRP0 (R7/S7 bit) have identical functionality. Driver changes will be required when migrating from S25FL-K to S25FL2-K in those applications that implement the embedded operation suspend and/or sector and/or block protection features.

Table 7. Status Register Comparison

S25FL-K			Functionally Compatible	S25FL2-K		
Reg Bit	Bit Name	Bit Function		Reg Bit	Bit Name	Bit Function
S0	WIP	Erase/Write in Progress	Yes	R0	WIP	Erase/Write in Progress
S1	WEL	Write Enable Latch	Yes	R1	WEL	Write Enable Latch
S2	BP0	Block Protect Bit	No	R2	BP0	Block Protect Bit
S3	BP1	Block Protect Bit	No	R3	BP1	Block Protect Bit
S4	BP2	Block Protect Bit	No	R4	BP2	Block Protect Bit
S5	TB	Top/Bottom Protect	No	R5	BP3	Block Protect Bit
S6	SEC	Sector Protect	No	R6	Reserved	Undefined
S7	SRP0	Status Reg Protect	Yes	R7	SRP	Status Reg Protect
S8	SRP1	Status Reg Protect	No	—	—	—
S9	QE	Quad Enable	No	—	—	—
S10	Reserved	Undefined	No	—	—	—
S11	LB1	Security Reg Lock Bit	No	—	—	—
S12	LB2	Security Reg Lock Bit	No	—	—	—
S13	LB3	Security Reg Lock Bit	No	—	—	—
S14	CMP	Complement Protect	No	—	—	—
S15	SUS	Suspend Status	No	—	—	—

2.5 Security and Write Protection

The S25FL2-K has a limited security feature set. It does support standard write protection features, such as the need to set WEL bit in the Status Register prior to array or Status Register changes and the need for all commands that change data to conclude with the correct byte oriented clock cycles.

2.5.1 Block Protection

The S25FL2-K supports a reduced number of options to set the granularity and location of array read-only protection compared to the S25FL-K. The S25FL2-K uses four Block Protection bits (BP3-BP0) to define which portions of the array are erase/write protected in Software Protected Mode (SPM) and Hardware Protected Mode (HPM). Table 8 provides the mapping of BP3-BP0 bits to the limited set of protected address range options for S25FL2-K.

Table 8. S25FL2-K Block Protection Options (Sheet 1 of 2)

BP[3:0]	S25FL204K		S25FL208K		S25FL216K	
	Protected Addresses	Protected Size	Protected Addresses	Protected Size	Protected Addresses	Protected Size
0000b	None	0 kB	None	0 kB	None	0 kB
0001b	070000h-07FFFFh	64 kB	0F0000h-0FFFFFh	64 kB	1F0000h-1FFFFFh	64 kB
0010b	060000h-07FFFFh	128 kB	0E0000h-0FFFFFh	128 kB	1E0000h-1FFFFFh	128 kB
0011b	040000h-07FFFFh	256 kB	0C0000h-0FFFFFh	256 kB	1C0000h-1FFFFFh	256 kB
0100b	000000h-07FFFFh	512 kB	080000h-0FFFFFh	512 kB	180000h-1FFFFFh	512 kB
0101b	000000h-07FFFFh	512 kB	000000h-0FFFFFh	1024 kB	100000h-0FFFFFh	1024 kB
0110b	000000h-07FFFFh	512 kB	000000h-0FFFFFh	1024 kB	000000h-0FFFFFh	2048 kB
0111b	000000h-07FFFFh	512 kB	000000h-0FFFFFh	1024 kB	000000h-0FFFFFh	2048 kB
1000b	None	0 kB	None	0 kB	000000h-0FFFFFh	2048 kB
1001b	000000h-07EFFFh	504 kB	000000h-07EFFFh	1016 kB	000000h-0FFFFFh	2048 kB

Table 8. S25FL2-K Block Protection Options (Sheet 2 of 2)

BP[3:0]	S25FL204K		S25FL208K		S25FL216K	
	Protected Addresses	Protected Size	Protected Addresses	Protected Size	Protected Addresses	Protected Size
1010b	000000h-07DFFFh	496 kB	000000h-07DFFFh	1008 kB	000000h-0FFFFFh	1024 kB
1011b	000000h-07BFFFh	480 kB	000000h-07BFFFh	992 kB	000000h-16FFFFh	1472 kB
1100b	000000h-077FFFh	448 kB	000000h-077FFFh	960 kB	000000h-1AFFFFh	1792 kB
1101b	000000h-05FFFFh	384 kB	000000h-05FFFFh	896 kB	000000h-1CFFFFh	1920 kB
1110b	000000h-03FFFFh	256 kB	000000h-03FFFFh	768 kB	000000h-1EFFFFh	1984 kB
1111b	000000h-07FFFFh	512 kB	000000h-07FFFFh	1024 kB	000000h-1FFFFFh	2048 kB

2.5.2 Other Security Options

Unlike the S25FL-K, the S25FL2-K does not have a Unique ID (serial number) feature. It also does not have an One Time Programmable (OTP) region feature, and as such, the S25FL2-K does not have the Security Register feature found in the S25FL-K.

2.6 DC and AC Parameter

Table 9 provides a comparison of DC parameters for the S25FL-K and the S25FL2-K. Table 10, Table 11, and Table 12 provide comparisons of AC parameters for the S25FL-K and the S25FL2-K by density. While most parameter differences should not cause performance issues when migrating from the S25FL-K to the S25FL2-K, it is highly recommended that the user carefully review all parameter differences for potential impact.

Table 9. DC Parameter Differences

DC Parameter	Type	Units	S25FL004K S25FL008K	S25FL016K	S25FL2-K
V_{CC}: Core Source Voltage	Min / Max	V	2.7 / 3.6 (1)	2.7 / 3.6 (1)	2.7 / 3.6
V_{IL}: Input Low Voltage	Min / Max	V	-0.6 / 0.3 x V_{CC}	-0.6 / 0.3 x V_{CC}	-0.5 / 0.3 x V_{CC}
V_{OL}: Output Low Voltage	Max	V	0	0	0.4
I_{CC1}: Standby Current	Typ / Max	µA	25 / 50	10 / 25	15 / 35
I_{CC2}: Power Down Current	Typ / Max	µA	1 / 5	1 / 5	15 / 32
I_{CC3}: Read Data Current - Single IO, 33 MHz	Typ / Max	mA	6 / 9	6 / 9	10 / 15
I_{CC3}: Read Data Current - Dual IO, 33 MHz	Typ / Max	mA	7 / 10.5	7 / 10.5	12 / 18
I_{CC3}: Read Data Current - Single IO, Fsck_max (2)	Max	mA	15	15	25
I_{CC3}: Read Data Current - Dual IO, Fsck_max (2)	Max	mA	16.5	16.5	25
$I_{CC4/5}$: Write Status Register Current	Typ / Max	mA	8 / 12	10 / 15	10 / 18
$I_{CC5/4}$: Page Program Current	Typ / Max	mA	20 / 25	20 / 25	15 / 20

Notes:

1. *S25FL-K specified with V_{CC} operating range options of 2.7-3.6V or 3.0-3.6V.*
2. *S25FL-K Fsck_max = 80 MHz; S25FL204K Fsck_max = 85 MHz, S25FL208K Fsck_max = 76 MHz, S25FL216K Fsck_max = 65 MHz.*

Table 10. AC Parameter Differences – 4-Mbit Density (Sheet 1 of 2)

Parameter	Type	Units	S25FL004K	S25FL204K
$f_{SCK,R}$: SCK Frequency - Read Data Instruction (03h) (1)	Max	MHz	50	44
$f_{SCK,R}$: SCK Frequency - All Other Commands (1)	Max	MHz	80	85
t_{CLH}, t_{CLL}, t_{CRLH}, t_{CRLL}: Clock High/Low Time - Read (03h)	Min	ns	8	4
t_{WH}, t_{CH}, t_{WL}, t_{CL}: Clock High/Low Time - All Other Commands	Min	ns	6	4
t_{SU-DAT}: Data Input Setup to SCK	Min	ns	2	4
t_{CS}: CS# High Time Between Read Instructions	Min	ns	10	50
t_{CS}: CS# High Time Between Erase/Program and Status Read	Min	ns	50	100
t_{DIS}: Output Disable Time	Max	ns	7	6

Table 10. AC Parameter Differences – 4-Mbit Density (Sheet 2 of 2)

Parameter	Type	Units	S25FL004K	S25FL204K
t_V: SCK low to Output Valid - Except Read ID Commands	Max	ns	7	10
t_{V2}: SCK low to Output Valid - Read ID Commands	Max	ns	7.5	10
t_{PP}: Page Program Time	Typ / Max	ms	0.7 / 3	1.5 / 5
t_{SE}: Sector Erase Time (4 kB)	Typ / Max	ms	30 / 200	50 / 300
t_{BE}: Block Erase Time (64 kB)	Typ / Max	s	0.15 / 1	0.5 / 2

Note:

1. *Comparisons apply to operation while V_{CC} = 2.7 to 3.6V and temperature = -40 to +85°C.*

Table 11. AC Parameter Differences – 8-Mbit Density

Parameter	Type	Units	S25FL008K	S25FL208K
$f_{SCK,R}$: SCK Frequency - Read Data Instruction (03h) (1)	Max	MHz	50	44
$f_{SCK,R}$: SCK Frequency - All Other Commands (1)	Max	MHz	80	76
t_{CLH}, t_{CLL}, t_{CRLH}, t_{CRLL}: Clock High/Low Time - Read (03h)	Min	ns	8	4
t_{SU-DAT}: Data Input Setup to SCK	Min	ns	2	4
t_{CSH}: CS# Active Hold from SCK	Min	ns	5	3
t_{CS}: CS# High Time Between Read Instructions	Min	ns	10	50
t_{CS}: CS# High Time Between Erase/Program and Status Read	Min	ns	50	100
t_{DIS}: Output Disable Time	Max	ns	7	6
t_V: SCK low to Output Valid - Except Read ID Commands	Max	ns	7	10
t_{V2}: SCK low to Output Valid - Read ID Commands	Max	ns	8.5	10
t_{PP}: Page Program Time	Typ / Max	ms	0.7 / 3	1.5 / 5
t_{SE}: Sector Erase Time (4 kB)	Typ / Max	ms	30 / 200	50 / 300
t_{BE}: Block Erase Time (64 kB)	Typ / Max	s	0.15 / 1	0.5 / 2

Note:

1. *Comparisons apply to operation while V_{CC} = 2.7 to 3.6V and temperature = -40 to +85°C.*

Table 12. AC Parameter Differences – 16-Mbit Density

Parameter	Type	Units	S25FL016K	S25FL216K
$f_{SCK,R}$: SCK Frequency - Read Data Instruction (03h) (1)	Max	MHz	50	44
$f_{SCK,R}$: SCK Frequency - All Other Commands (1)	Max	MHz	80	65
t_{CLH}, t_{CLL}, t_{CRLH}, t_{CRLL}: Clock High/Low Time - Read (03h)	Min	ns	8	4
t_{WH}, t_{CH}, t_{WL}, t_{CL}: Clock High/Low Time - All Other Commands	Min	ns	6	4
t_{SU-DAT}: Data Input Setup to SCK	Min	ns	2	4
t_{CSH}: CS# Active Hold from SCK	Min	ns	5	3
t_{CS}: CS# High Time Between Read Instructions	Min	ns	10	50
t_{CS}: CS# High Time Between Erase/Program and Status Read	Min	ns	50	100
t_{DIS}: Output Disable Time	Max	ns	7	6
t_V: SCK low to Output Valid - Except Read ID Commands	Max	ns	7	14
t_{V2}: SCK low to Output Valid - Read ID Commands	Max	ns	8.5	14
t_W: WRR Write Time	Max	ms	15	5
t_{PP}: Page Program Time	Typ / Max	ms	0.7 / 3	1.6 / 5
t_{SE}: Sector Erase Time (4 kB)	Typ / Max	ms	30 / 200	45 / 200
t_{BE}: Block Erase Time (64 kB)	Typ / Max	s	0.15 / 1	0.45 / 1.5
t_{CE}: Chip Erase Time	Typ / Max	s	3 / 10	12 / 25

Note:

1. *Comparisons apply to operation while V_{CC} = 2.7 to 3.6V and temperature = -40 to +85°C.*

3 Conclusion

Migration from the S25FL-K to the S25FL2-K is straightforward for those applications that do not operate at high frequency, do not utilize Quad IO modes, and do not require elaborate security.

Document History Page

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*A	-	-	08/22/2012	Corrected other minor typos Changed BUSY signal to WIP In Feature Comparison section, Changed table title and modified note 2 In DC and AC Parameters, modified tables and notes
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