Migration from S70FL256P to S25FL256S

About this document

Scope and purpose

AN98592 discusses the minimum changes required to migrate existing designs based on S70FL256P MirrorBit™ SPI Multi-I/O Flash Memory to the 65-nm MirrorBit process S25FL256S SPI flash device.

Table of contents

1 Introduction

The minimum changes required to migrate existing S70FL256P MirrorBit<Superscript>® SPI Multi-I/O Flash Memory based designs to the 65 nm MirrorBit process S25FL256S SPI flash device are discussed in this application note.

The S70FL256P is a Dual Die Package (DDP) device consisting of two 128 Mbit density S25FL129P die, each controlled independently by a dedicated chip select input and with all other input and output signals shared.

By contrast, the monolithic 256-Mbit density Single Die Package (SDP) S25FL256S has a single chip select input and requires a different addressing methodology to access its full 32-MB (Megabyte) array, compared to the pair of lower density S25FL129P devices within the S70FL256P DDP.

Software and potentially hardware changes are required to migrate from the S70FL256P to the S25FL256S. The **Migration from FL-P to FL-S Family SPI Interface Flash** application note should also be referenced as required.

2 Migration Design Considerations

The key S70FL256P migration considerations revolve around the SPI flash memory 24-bit or 3-byte addressing limit. SPI flash memory densities 128 Mbit (16 Mbyte) and below could be addressed by 24-bit addresses to byte granularity. In order to support 256 Mbit (32 Mbyte) and higher SPI flash memory densities, the de facto SPI specification has evolved to support 32-bit or 4-byte extended addressing.

2.1 Chip Select

The S70FL256P device straddled the transition from processors and chipsets with 24-bit SPI addressing support only to those with both 24-bit and 32-bit SPI extended addressing capability. The S70FL256P combines two 24-bit address aware S25FL129P SPI flash devices each selectable via dedicated chip select inputs as shown in **Figure 1**.

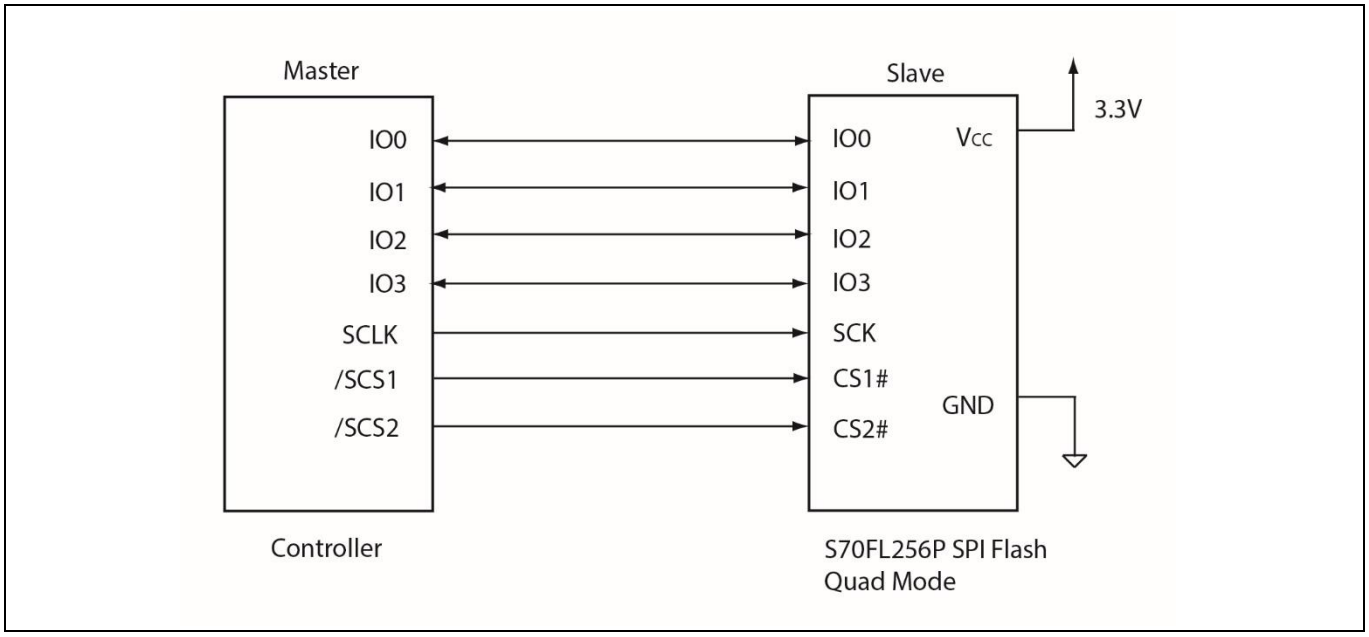

Figure 1 S70FL256P System Implementation

The second chip select CS2# is non-standard for SPI flash memory and is not supported in the S25FL256S. In order to migrate the S70FL256P design shown in **Figure 1** to the S25FL256S, the two system controller chip select outputs need to be combined into a single chip select connected to the same SPI flash input as CS1#. The S25FL256S has only one chip select CS# and is pinout compatible with the S70FL256P CS1# while the unused CS2# input location is not connected internally to the S25FL256S so any electrical activity on this input will be ignored. Therefore, if the system chip selects can be combined via software or hardware changes onto CS1#, the PCB connection to CS2# does not require modification.

If the system chip selects cannot be combined via changes internal to the controller, an external logical AND of the system chip select outputs onto CS1# could achieve the same result but would require validation versus all of the S25FL256S SPI AC timing specifications.

In **Connection Diagrams**, side-by-side comparisons of the S70FL256P and S25FL256S package pinouts illustrate the commonality between the CS1# and CS# chip select inputs respectively.

2.2 Extended Addressing

Combining the SPI chip selects only solves part of the S70FL256P migration to the S25FL256S. In order to address the full S25FL256S 32-MB array, one of three new 32-bit extended addressing modes must be used. As described in Section 2.2 Extended Addressing of the **Migration from FL-P to FL-S Family SPI Interface Flash** application note, extended 32-bit addressing is enabled using three methods in conjunction with the new Bank Address Register:

- Extended address mode – a bank address register bit that changes all legacy commands to expect 32 bits of address supplied from the host system.
- New commands – that perform both legacy and new functions, which expect 32-bit address.
- Bank address register – a software (command) loadable internal register that supplies the high order bits of address when legacy 24-bit addresses are in use.

The Bank Address Register is defined in **Table 1**. At power-up and after reset, the Bank Address Register defaults to zeros and the extended address mode is set to 24-bit addressing for legacy software compatible access to the first 128 Mbits of the S25FL256S device.

Table 1 Bank Address Register (BAR)

Bits	Field Name	Function	Type	Default State	Description
7	EXTADD	Extended Address Enable	Volatile	0b	1 = 4-byte (32-bits) addressing required from command. 0 = 3-byte (24-bits) addressing from command + Bank Address
6 to 1	RFU	Reserved	Volatile	00000b	Reserved for Future Use
0	BA24	Bank Address	Volatile	0	A24 for 256-Mbit device, RFU for lower density device

Selection of the extended addressing method is determined by the capabilities of the system controller. If the system controller's SPI interface only supports 24-bit addressing, using existing instructions with the Bank Address Register is the only option. However, if the system controller's SPI interface supports both 24-bit and 32-bit addressing, any of the three options can be employed depending on the system design implementation.

2.2.1 24-bit Addressing Example

In S70FL256P applications, the system design was implemented with 24-bit SPI addressing regardless of the system controller capabilities. Therefore, using existing instructions with the Bank Address Register of the S25FL256S will often be the simplest migration option to minimize software changes.

In this extended addressing mode, the volatile Bank Address Register is used to provide the 4th byte of the address to allow switching between the two 16-MB banks of the S25FL256S flash array. Specifically, BAR[0] equates to S25FL256S address bit A24. The 3-byte address selects an address within the Bank selected by BAR[0] for read, erase, and program commands. BAR[7] cleared to zero (EXTADD = 0) selects the 3 byte + bank address extended addressing method. At power up and hardware reset, the default is BAR cleared to zero, selecting this addressing method and Bank 0, which limits initial access to the lowest 16 MB of the flash array. For Read operations, the device will continuously transfer out data until the end of the array starting from the address provided in the read command, regardless of which bank it is in.

Migration Design Considerations

The S25FL256S supports three new commands for accessing and modifying the Bank Address Register: Bank Register Read (BRRD), Bank Register Write (BRWR), and Bank Register Access (BRAC) as described in Section 2.2.4 New Commands to Support Bank Address Register of the **Migration from FL-P to FL-S Family SPI Interface Flash** application note.

The BRWR command (opcode 17h) is used to write address bits above A23 into the Bank Address Register (BAR[0]). The command is also used to write the Extended address control (EXTADD) bit in the Bank Address Register (BAR[7]). This command does not require use of a preceding WREN command. The BRWR command consists of CS# assertion, followed by input of the single opcode byte 17h, followed by input of the single data byte BAR[7:0], followed by CS# negation.

The BRAC command (opcode B9h) provides an alternative method to modify the BAR to enable accesses to higher 16-MB array banks while using legacy 3-byte addressing. This method is necessary in systems that cannot support the new BRRD and BRWR commands due to SPI memory controllers with fixed instruction code libraries. However, this alternative command sequence has no effect on the value of EXTADD (BAR[7]).

2.3 Device Identification

Section 2.1 Device Identification of the **Migration from FL-P to FL-S Family SPI Interface Flash** application note describes the standard READ-ID (90h), RDID (9Fh), and RES (ABh) device identification command methods in detail.

2.4 Block Protection

If the existing S70FL256P design uses the SPI Block Protection feature, Section 2.6 Block Protection of the **Migration from FL-P to FL-S Family SPI Interface Flash** application note illustrates BP[2:0] settings to achieve equivalent Block Protection in S70FL256P and S25FL256S.

2.5 DC and AC Parameters

Section 2.4 DC and AC Parameter of the **Migration from FL-P to FL-S Family SPI Interface Flash** application note provides comparisons of the DC and AC parameters for the S70FL256P and the S25FL256S devices. These parameter differences should be reviewed for potential impact on the system design.

3 Packaging and Pinout

Table 2 provides the recommended migration S25FL256S ordering part numbers for each of the S70FL256P devices.

Table 2 Recommended Migration Ordering Part Numbers

S70FL256P Ordering Part Number	Recommended Migration Ordering Part Number
S70FL256P0XMFI00	S25FL256SAGMFI00
S70FL256P0XMFI01	S25FL256SAGMFI01
S70FL256P0XBHI20	S25FL256SAGBHI20
S70FL256P0XBHI21	S25FL256SAGBHI21

3.1 Connection Diagrams

The side-by-side comparison of the S70FL256P and S25FL256S 16-Lead SOIC package connection diagrams is show in Figure 2. The S70FL256P CS1# chip select input pin 7 corresponds to the same physical input pin 7 as the S25FL256S CS# chip select. S25FL256S pin 6, corresponding to the S70FL256P CS2# chip select, is not connected internally so any electrical activity on this input will be ignored. However, it is recommended not to use the RFU pin 6 for PCB routing channels.

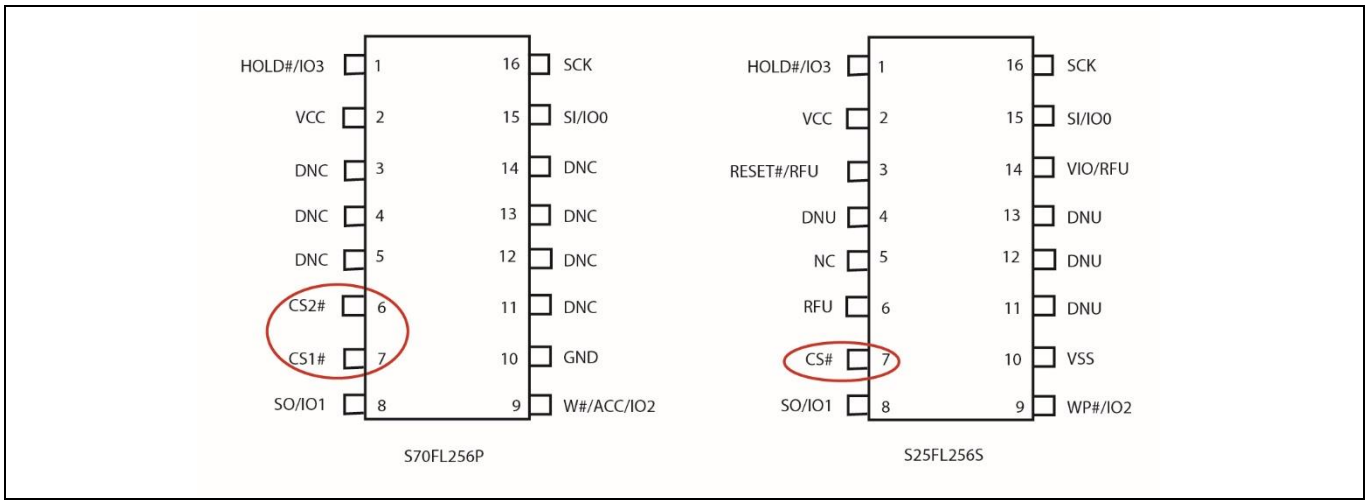

Figure 2 16-Lead SOIC Package, Top View

The side-by-side comparison of the S70FL256P and S25FL256S 24-Ball BGA (FAB024) package connection diagrams is shown in 24-ball BGA, 5 x 5 Ball Footprint (FAB024), Top View. The S70FL256P CS1# chip select input C2 corresponds to the same physical input ball C2 as the S25FL256S CS# chip select. S25FL256S ball C3, corresponding to the S70FL256P CS2# chip select, is not connected internally so any electrical activity on this input will be ignored. However, it is recommended not to use the RFU pin 6 for PCB routing channels.

Packaging and Pinout

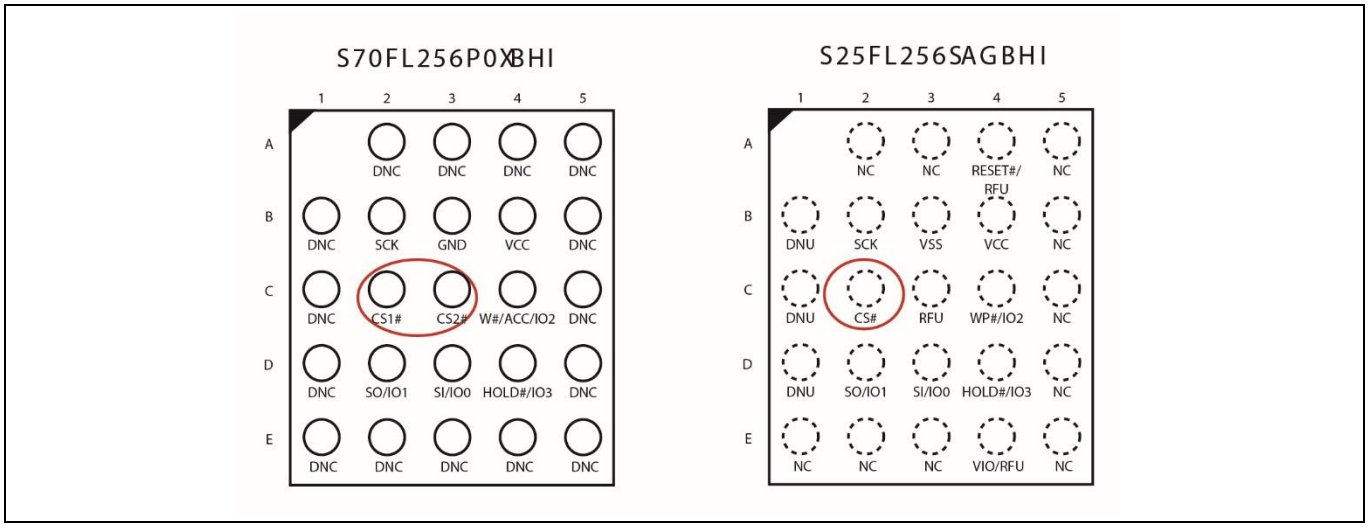

Figure 3 24-ball BGA, 5 x 5 Ball Footprint (FAB024), Top View

4 Summary

Software and potentially hardware changes are required to migrate from the S70FL256P to the S25FL256S SPI Flash. The key S70FL256P migration considerations concern combining the two dedicated system chip selects and selecting the best 32-bit extended addressing mode to address the full S25FL256S 32MB array.

References

[1] **S25FL129P Datasheet**

[2] **S70FL256P Datasheet**

[3] **S25FL128S and S25FL256S Datasheet**

[4] **Migration from FL-P to FL-S Family SPI Interface Flash Application Note**

Revision history

Document version	Date of release	Description of changes
**	2012-03-27	Initial version
*A	2015-09-21	Updated in template
*B	2017-07-19	Updated logo and Copyright
*C	2018-03-22	Sunset review; no content updates
*D	2021-03-29	Updated to Infineon template

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