AN99111

Parallel NOR Flash Memory: An Overview

AN99111 gives an overview of how Cypress Parallel NOR Flash Memory is used in embedded systems.

1 Introduction

All computer-based systems contain memory. Memory is where information is stored while waiting to be operated on by the Central Processing Unit (CPU) of the computer. There are two types of memory: volatile memory and nonvolatile memory. Volatile memory retains its information only while power is applied to the memory device. The contents of this memory type may be easily and quickly changed. Nonvolatile memory retains its information even when no power is applied to the memory device. Although the information in most nonvolatile memories may be changed, the process involved is much slower than for volatile memory.

1.1 Volatile Memory

Volatile memory loses its contents when the device loses power. Random Access Memory (RAM) is the traditional name used for volatile memory. The name refers to the ability to access any location of the memory quickly with no particular order of accesses needed. Static RAM (SRAM) and Dynamic RAM (DRAM) are two examples of volatile memories that have this characteristic.

SRAM typically uses six transistors for each memory bit (cell) to retain data as long as power is being supplied. This makes each memory cell relatively large and limits SRAM to use in lower density memories. SRAM can provide faster access to data, use less standby power, and tends to be more expensive than DRAM.

DRAM uses a single transistor and a small capacitor for each bit of memory. Since capacitors do not hold a charge indefinitely, DRAM cells must be frequently recharged (refreshed) to avoid losing the contents. These smaller memory cells allow DRAM to be used for high density, low cost memories, but are typically slower than SRAM.

1.2 Nonvolatile Memory

Nonvolatile memory is memory that retains its contents even if the power is lost. Nonvolatile memory was originally called Read Only Memory (ROM) because its contents were loaded during the manufacturing process and could be read, but never erased or reprogrammed. Over time, the ability to erase and reprogram ROM was added in different ways and referred to as Electrically Programmable ROM (EPROM), Electrically Erasable and Programmable ROM (EEPROM), and Flash EEPROM, commonly referred to simply as flash memory.

ROM memory is programmed by the way it is manufactured and stores permanent code and data that is generally used to initialize and operate a computer system.

EPROM can be electrically programmed one byte at a time but is not electrically erasable. It has to be exposed to ultraviolet (UV) light for about twenty minutes in order to erase all bits in the memory array. EPROM uses a single transistor for each data bit and can be used in relatively high density memories.

EEPROM is electrically erasable and programmable in-system, one byte at a time, but the memory cells use more transistors and are larger than those in EPROMs, thus EEPROM has higher costs and lower density (generally less than 1 Mb).

Flash EEPROM memory can be electrically programmed a single byte or word at a time, but a large group of bytes or words—called a block, sector, or page—are electrically erased at the same time. Due to the erase operation being much faster than the prior EPROM or EEPROM devices, these devices came to be called flash erase EEPROM, or simply flash memories. The flash memory cell uses a single transistor to store one or more bits of information. Flash technology combines the high density of EPROM with the electrical in-system erase and programmability of EEPROMs. Flash memory has become the dominant type of nonvolatile memory in use.

Table 1 compares the fundamental features of flash memory with those of the other memory technologies discussed earlier. The remainder of the application note will cover only flash memory.

Table 1. Comparison Flash Memory with Other Memory Technologies

	Non volatile	High Density	Low Power	One Transistor Per Cell	In-System Rewriteable	Fully Bit-Alterable	High-Performance Read
Flash Memory	x	x	x	x	x	–	x
SRAM	–	–	–	–	x	x	x
DRAM	–	x	–	x	x	x	x
EPROM	x	x	x	x	–	–	x
EEPROM	x	–	x	–	x	x	x

2 Flash Memory Architectures

The two main architectures dominate the flash memory: they are NOR and NAND.

NOR is typically used for code storage and execution. NOR allows quick random access to any location in the memory array, 100% known good bits for the life of the part, and code execution directly from NOR Flash memory.

NAND is used for data storage. NAND flash requires a relatively long initial read access to the memory array, 98% good bits when shipped with additional bit failure over the life of the part (ECC highly recommended), program/erase times are much faster than NOR and NAND cost less per bit than NOR.

Table 2. Difference Between NOR and NAND

Parameter	NOR	NAND
Density	1 Mbit – 1 Gbit	64 Mbit - 1 6Gbit
Read initial access	55 ns	10,000 ns
Read sequential access	9 ns	50 ns
Program	0.3 Mbytes/s	2.6 Mbytes/s
Erase	0.2 Mbytes/s	8.2 Mbytes/s
Access Method	Random	Sequential

3 Cypress Flash Memory

Cypress is the world's leading supplier of NOR flash memory. Cypress flash memory products include a broad spectrum of densities and features to support a wide range of customer specific markets such as hand-held/mobile electronics, computer, set-top boxes and automotive applications. Cypress primarily uses two flash memory technologies, Floating Gate and MirrorBit®.

Floating Gate technology was first introduced in the early 1990s. It offered fast access times, and high program/erase endurance cycles. This technology allowed the storage of only one data bit per cell. However, with the introduction of MirrorBit technology in 2001, Cypress is able to offer a more cost-effective solution to customers, while still maintaining fast access times and high endurance cycles. The cost-effective solution is the design of the MirrorBit storage cell, which can store two data bits per cell, instead of just one data bit. This design enables manufacturing costs to be significantly lower than that of Floating Gate technology. MirrorBit technology definitely has a clear economical, as well as a technological advantage over Floating Gate technology.

3.1 Distinctive Features

Cypress flash memory offers many distinctive features that help designers build feature-rich, cost-effective systems. Key distinctive characteristics include:

- Secured Silicon (SecSi) Sector
- ACC
- WP#
- VI/O
- CFI
- Write Buffer
- Advanced Sector Protection
- Page Mode
- Burst Mode
- Simultaneous Read/Write

SecSi (Secured Silicon) feature enables permanent part identification through an Electronic Serial Number (ESN). The SecSi sector provides a 128 Bytes to 64 Kbytes area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur. SecSi Sector Indicator Bit (DQ7) is used to determine whether or not the SecSi sector is protected. Cypress offers the device with the SecSi sector either as customer-lockable or as factory-locked. The customer-lockable version is shipped with the SecSi sector unprotected and has the SecSi Sector Indicator Bit permanently set to a "0." The factory- locked version is always protected and has the SecSi Sector Indicator Bit permanently set to a "1."

ACC (Accelerated Program Operation) is an input pin which allows for faster programming or erases operation when raised to a specified voltage (12 V or 9 V).

WP# (Write Protect) is a hardware method for protecting boot sectors using standard control logic signals.

$V_{I/O}$ is a feature that allows the signal interface voltage levels to be determined by the $V_{I/O}$ power supply.

CFI is a feature which provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices. The device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can also write the CFI Query command when the device is in the Autoselect mode.

Write Buffer allows the system to write up to 32 words in one programming operation. It is implemented to speed up programming operations. A Write Buffer is a set of registers used to hold several words that are to be programmed as a group.

Advanced Sector Protection provides command-controlled rather than voltage-controlled protection to any sector against inadvertent or malicious program or erase operations. Refer to the datasheet for detailed information.

Page Mode allows high-speed random read access to memory addresses near the initial access address.

Burst Mode allows high-speed sequential reading of the flash without the need to update the address lines.

Simultaneous Read/Write allows the flash to be read from at the same time a program or erase operation is being performed.

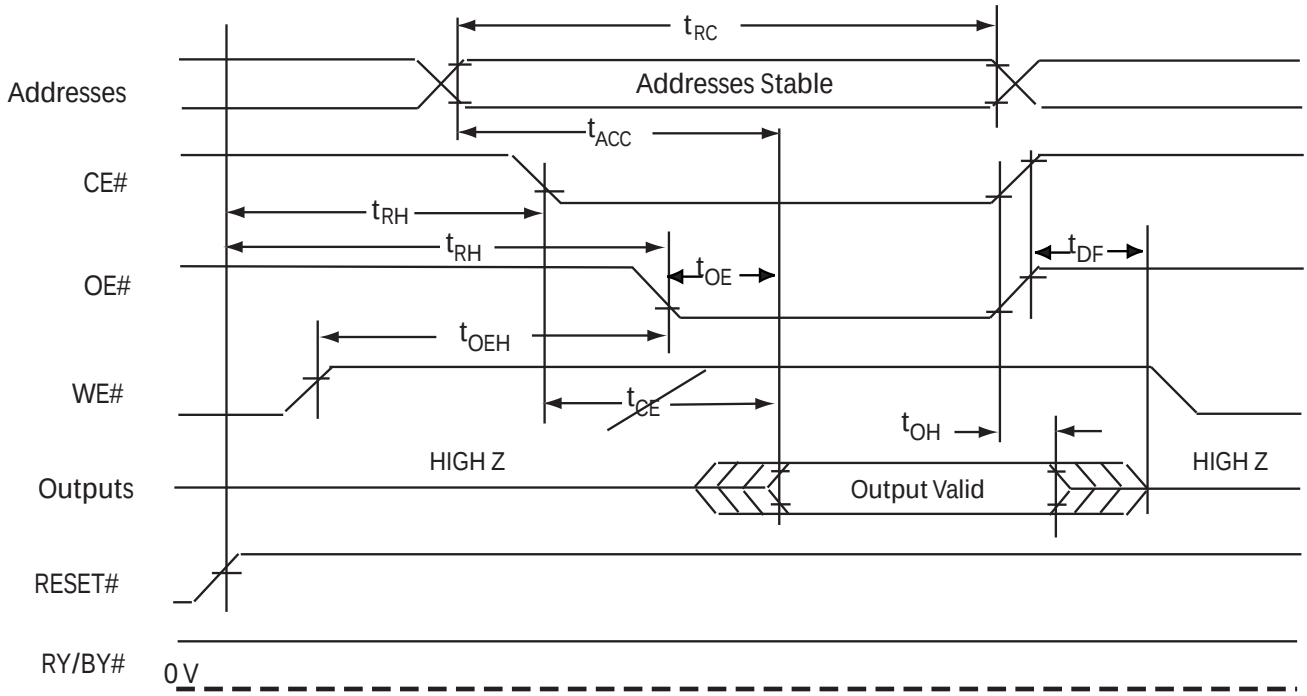
3.2 Basic Operation

There are three basic operations in a flash memory: read (a byte or a word), program (a byte or a word), and erase (one or more sectors).

3.2.1 Read

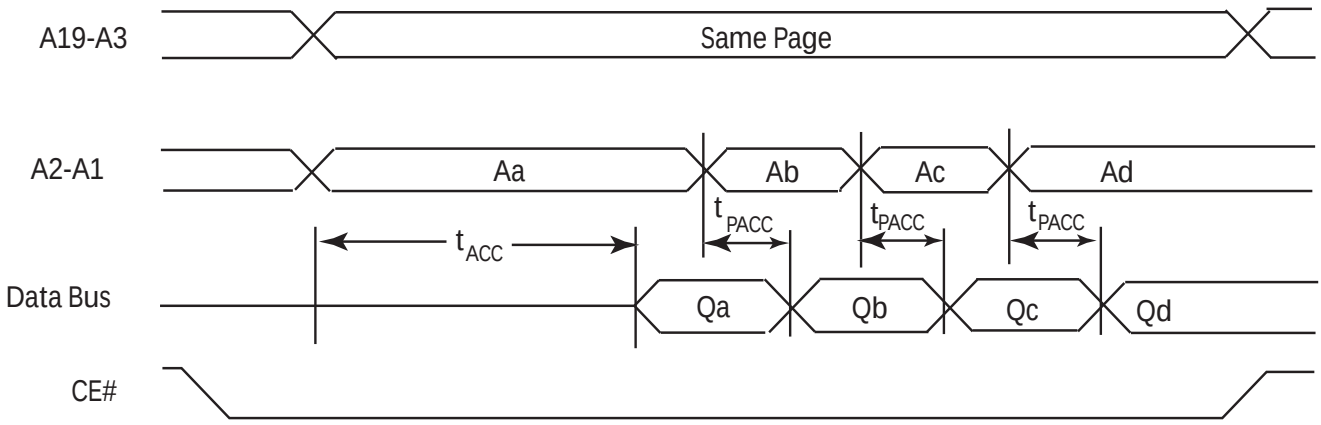
Cypress provides three types of read operations: asynchronous read, asynchronous page read, and synchronous burst read. Asynchronous read is a read not occurring at predetermined or regular intervals (not dependent on a clock). Typical read access time is 55 to 120 ns. Figure 1 shows the timing diagram.

Figure 1. Asynchronous Read Operation Timing



Asynchronous page read is an asynchronous read operation of several words, in which the first word of the group takes a longer initial access time, and subsequent words in the group take less “page” access time to be read. The page size of the page mode devices is either four words or eight words, with the page being selected by the least significant two or three bits of address. Page mode interface provides faster read access speed for random locations within a page. Initial access time is typically 70 to 120 ns. Access time within a page is typically 25 ns. Figure 2 shows the page read timing diagram.

Figure 2. Page Read Timing



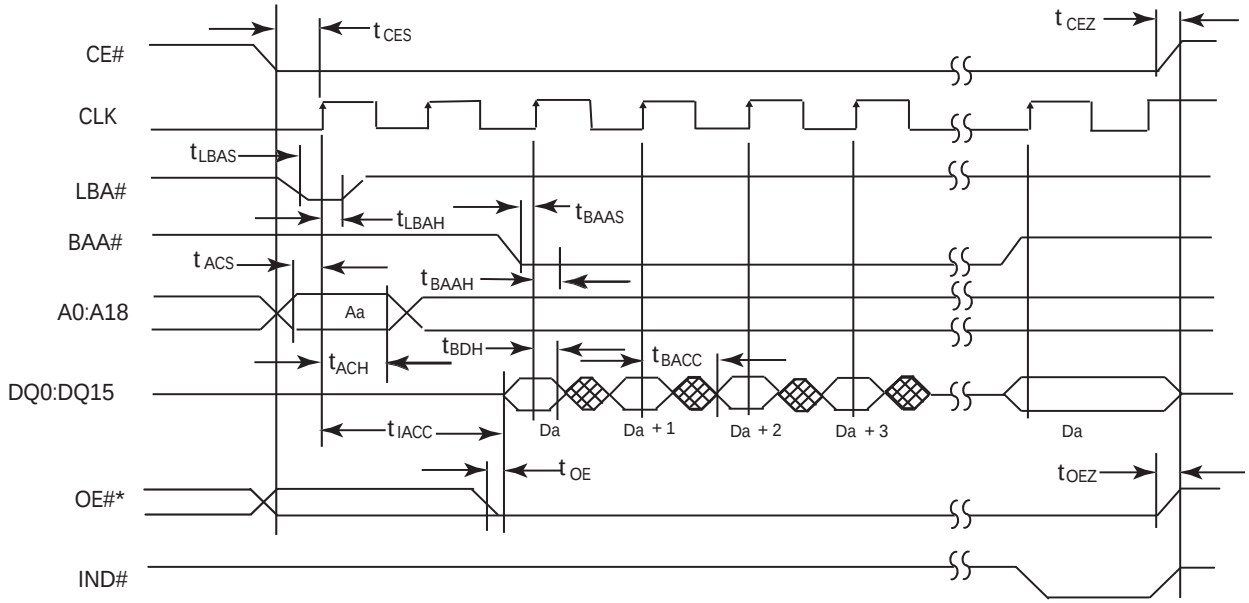
Synchronous burst read is a read occurring at regular intervals dependent on a clock edge. Burst mode devices require three extra control pins to perform burst read. They are Clock, Load Burst Address (LBA#) or Address Valid (ADV#), and Burst Address Advance (BAA#) or RDY.

When the burst device first powers up, it is enabled for asynchronous read operation. To enable synchronous burst read, the system must issue the burst mode enable command sequence. The initial address of an access is loaded by the clock edge when LBA# or AVD# is low. The first data word is available after the initial access time delay. Sequential words are available on each following clock edge after the burst access time delay. Typical initial access time is 50 to 70 ns. Burst accesses can continue with a 50- to 80-MHz clock.

Depending on the specific device, Cypress burst mode flash offers a number of read modes to interface with a wide range of microprocessors. They are linear burst, interleaved burst, and continuous sequential burst. In the linear and interleaved burst modes, the device delivers a stream of words from a 4, 8, 16, or 32 word aligned

block. (For the S29CD family, the burst is 32-bit double words.) If the initial address is not at the beginning of the block, the sequence of words following the initial access will wrap from the end to the beginning of the block. In continuous sequential burst mode, the device reads sequentially through the entire address range. Refer to a specific burst device datasheet for detailed information. Figure 3 shows burst read mode.

Figure 3. Burst Read Timing



3.2.2 Program

The unprogrammed state of a flash memory cell is a high signal level or logical one. Changing a flash memory cell (or bit) to a low voltage level or zero is called programming. Programming on Cypress Floating Gate flash is generally done one byte or word at a time. MirrorBit technology uses a write buffer to program one byte to as many as 32 bytes.

One key point to note is that programming only changes ones to zeros. Programming is initiated by a series of write accesses that form a program command. The required sequence of write accesses prevents unintended changes to stored data.

3.3 Erase

Erasure of a flash device is done through multiple write accesses that form an erase command. The erase completion time is dependent upon the sector size and technology. The erase command sequence initiates the embedded erase algorithm – an internal algorithm that automatically preprograms the memory array (if it is not already programmed) before executing the erase operation simultaneously on all bits of the sector.

One key point to note is that chip or sector erasing only changes zeros to ones. During erase, the device automatically times the erase pulse widths and verifies the proper cell margin.

3.4 Temperature Ranges

Cypress flash memory devices are available in various temperature ranges.

Table 3. Various Temperature Options (Sheet 1 of 2)

Code	Name	Description
C	Commercial	0 - +70ºC
W	Wireless	-25 - +85ºC
I	Industrial	-40 - +85ºC
V	Automotive-In cabin	-40- +105ºC

Table 3. Various Temperature Options (Sheet 2 of 2)

Code	Name	Description
N	Extended	-40 - +125ºC
H	Hot	-40 - +145ºC

3.5 Cypress Product Families

Table 4. Cypress Product Families

	Architecture	Density	Voltage
F	Standard Interface Flash Memory	1 Mb – 32 Mb	5.0 V
DL	Simultaneous Read/Write, Low Voltage Flash Memory	4 Mb – 128 Mb	3.0 V
BL	High Performance Burst Mode Flash Memory	8Mb and 16Mb	3.0 V
PL	Parallel Page Mode, Simultaneous Read/Write Flash Memory	32 Mb - 128 Mb	3.0 V
AL	Universal Footprint Standard Interface Flash Memory	8 Mb - 16 Mb	3.0 V
AS	Standard Interface Flash Memory	8 Mb - 16 Mb	1.8 V
CD/CL	x32 Burst Mode, Simultaneous Read/Write Flash Memory	16 Mb – 32 Mb	2.5 V-3.0 V
GL	MirrorBit Technology, High Performance, Parallel Page Mode Flash Memory	32 Mb - 2 Gb	3.0V
NS-VS-XS	Burst Mode, Simultaneous Read/Write Flash Memory	64 Mb - 512 Mb	1.8 V
WS	Burst Mode, Simultaneous Read/Write Flash Memory	64 Mb – 512 Mb	1.8 V
JL	Simultaneous Read/Write Flash Memory	32 Mb - 128 Mb	3.0 V

4 Conclusion

Cypress flash memory provides a compact, easy to use, nonvolatile code and data storage solution for electronic products. Cypress provides a broad portfolio of flash memories to suit a wide range of applications. The memory size, voltage, speed, and package, can be selected to suit the application.

Document History Page

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