S25FL1-K SPI Power-Up Timing and Reset

AN99199 discusses the considerations for ensuring strict adherence to Power-Up Timing and Voltage Levels specified in the data sheet for Cypress S25FL1-K SPI Multi-I/O Flash Memory family devices.

1 Introduction

The S25FL1-K Serial Peripheral Interface (SPI) Multi-I/O Flash Memory family requires strict adherence to Power-Up Timing and Voltage Levels specified in the data sheet.

2 Power-On (Cold) Reset

S25FL1-K devices execute a Power-On Reset (POR) process until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the VWI threshold as shown in Figure 1. The device must not be selected until after t_{VSL} since Chip Select (CS#) must to go high with V_{CC}, i.e. no commands may be sent to the device until the end of t_{VSL}. Program, Erase, and Write instructions will be ignored until after t_{PUW}. Power-Up Timing and Voltage Level parameters are shown in Table 1. CS# should not be held low during the POR.

Figure 1. Power-Up Timing and Voltage Levels

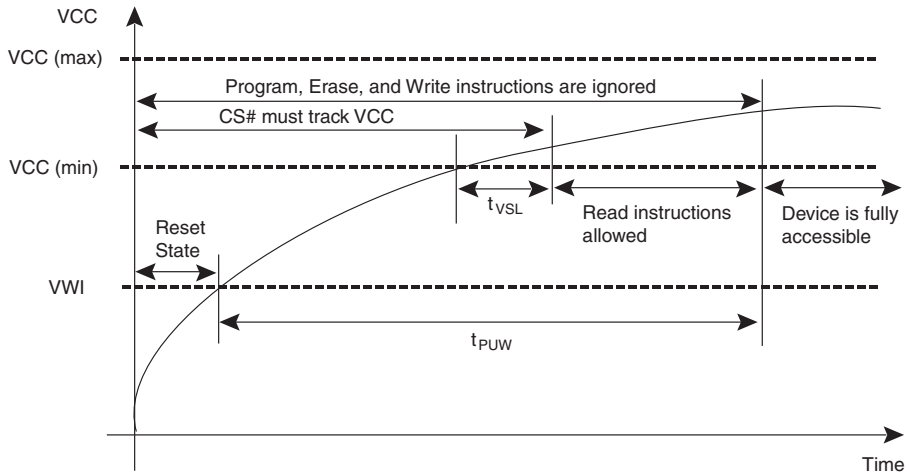

Table 1. Power-Up Timing and Voltage Levels

Parameter	Symbol	Spec		Unit
		Min	Max	
V_{CC} (min) to CS# Low	t_{VSL}	10		µs
Power-Up to Write — Time Delay Before Write Command	t_{PUW}		10	ms
Write Inhibit Threshold Voltage	V_{WI}	2.4		V
Power-Down Time	t_{PD}	10.0		µs
V_{CC} Power-Down Reset Threshold Voltage	V_{CC} Low	1.0		V

Note:

1. *These parameters are characterized only.*

3 Software Reset Command

After a Power-On (Cold) Reset or Power-Down and Voltage Drop, issuing the Software Reset command is recommended as a best practice. The Software controlled Reset command restores the device to its initial power up state by reloading volatile registers from non-volatile default values.

A Software Reset is initiated by the Software Reset Enable command (66h) followed by the Software Reset command (99h) and then executed when CS# is brought high after t_{RCH} time at the end of the Software Reset instruction and requires an additional t_{RST} time before executing the next Instruction after the Software Reset as shown in Figure 2 and Table 2.

Figure 2. Software Reset Command Timing

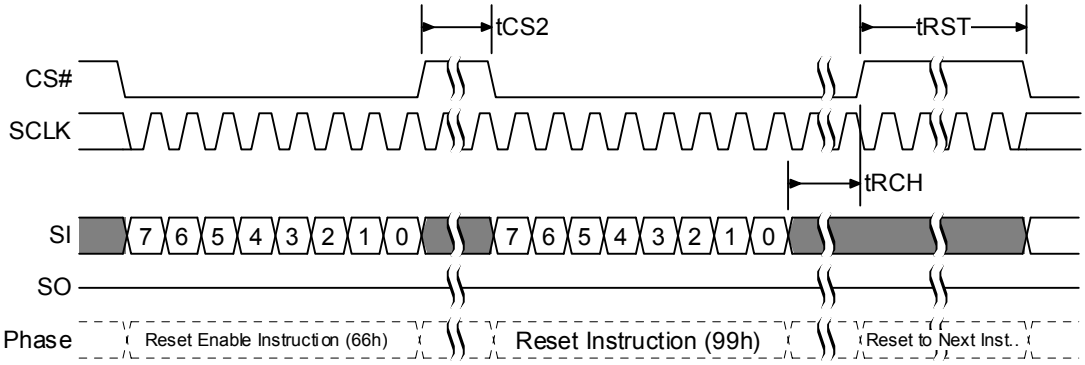

Table 2. Software Reset Timing

Parameter	Symbol	Spec		Unit
		Min	Max	
End of Reset Instruction to CE# High	t_{RCH}	40		ns
CE# High to Next Instruction after Reset	t_{RST}	1.5		µs

If a Software Reset is initiated during a Erase, Program or Register write operation, the data in that Sector, Page, or Register is unknown, and the operation needs to be initiated again.

When the device is in Deep Power Down mode, the software reset commands are ignored and have no effect. To reset the device send the Release Power down command (ABh) and after the time duration of CS# High to Standby Mode without Electronic Signature Read t_{RES1}, the device will resume normal operation and the Software reset commands will be accepted.

4 Summary

The Power-Up Timing and Voltage Levels specified in the S25FL1-K device family data sheet should be strictly adhered to during the Power-On Reset (POR) process, and, in particular, Chip Select CS# should not be held low during the POR. Furthermore, issuing the Software Reset command after the Power-On (Cold) Reset or Power-Down and Voltage Drop is recommended as a best practice.

Document History Page

Document Title: AN99199 - S25FL1-K SPI Power-Up Timing and Reset Document Number: 001-99199				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	09/04/2014	Initial version
*A	4929456	MSWI	09/22/2015	Updated in Cypress template
*B	5866800	AESATMP8	08/29/2017	Updated logo and Copyright.

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