AN INFINEON TECHNOLOGIES COMPANY

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S25FL129P Programming Guide

About this document

Scope and purpose

Every flash device supports three fundamental operations: Read, Erase, and Program. The Read operation enables access to digital data contents of the flash memory array. The Erase operation converts bits from '0' (programmed) to '1' (erased) and are performed on a sector basis. The Programming operation sets a bit or group of bits from '1' (erased) to '0' (programmed). The S25FL (032/064/129) P Flash Family offers both Single and Multi I/O read and write access modes which provides access bandwidths (BW) up to 40 Mbytes/s. The S25FL129P supports standard Page Programming and Quad Page Programming operations. This document investigates the S25FL-P standard Page Programming and Quad Programming performance and highlights recommended programming practices and verification methods.

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1 S25FL129P SPI Flash

SPI Flash supports the fundamental flash Read, Erase, and Program operations. The S25FL-P Multi I/O SPI Family supports standard SPI features and provides additional features like increased read and write BW accesses speeds up to 40 Mbytes/s. The S25FL-P faster read and write speeds BW provide for an expanded command set including an enhanced Quad Page Program (QPP) command. The QPP allows the flash input buffer to be filled much faster than standard Page Programming. The next sections compare the S25FL-P standard Page Programming and Quad Programming performance along with recommended programming practices and verification.

1.1 Page Programming vs. Quad Programming

As previously stated a programming operation sets a bit or group of bits from '1' (erased state) to '0' (programmed state). A complete program operation has multiple steps consisting of sending the program command sequence including program address, filling the input buffer with program data, and performing the internal flash program operation. The following investigates these program steps for the S25FL129P both PP and QPP operations.

1.1.1 S25FL129P Programming

- Performs programming on a full page or partial page basis (Page: 256 bytes)
- Page Programming (PP) and Quad Page Programming (QQP)
  - PP fills input page buffer a single bit of data/Clock cycle (PP 2079 clock cycles)
  - QPP fills input page buffer with 4 bits of data/Clock cycle (QPP 543 clock cycles)
- Typical Page program time is 1.5 ms for PP and QPP operations

Table 1 Comparison of Page and Quad Page Buffer Fill Times (8 MByte File: 32K Pages)

SPI Clk	Single Buffer Fill		32K Buffer Fills (8 MB) ([1], [2])		Cell Programming (s) [2]	Buffer Fill + Prog (s)		Time Delta (s)	Comment
	PP (s)	QPP (s)	PP (s)	QPP (s)	PP/ QPP (s)	PP (s)	QPP (s)		
1	2.1E-03	5.4E-04	66.53	17.38	~48	114.53	65.38	49.15	Time deltas decrease as SPI Clock increases
5	4.2E-04	1.1E-04	13.31	3.48		61.31	51.48	9.83	
10	2.1E-04	5.4E-05	6.65	1.74		54.65	49.74	4.92	
20	1.0E-04	2.7E-05	3.33	0.87		51.33	48.87	2.46	
40	5.2E-05	1.4E-05	1.66	0.43		49.66	48.43	1.23	
80	2.6E-05	6.8E-06	0.83	0.22		48.83	48.22	0.61	

This example shows that QPP improves overall program performance. However, systems with faster clock speed will not realize as much benefit for the QPP instruction since the internal page program time is greater than the time it takes to clock data into the input buffer.

1 SPI Clock Cycles to fill buffer: PP 2079 clock cycles and QPP 543 clock cycles.

2 The flash internal Page program time is the same for PP and QPP operations.

1.2 Programming Recommendations and Verification

1.2.1 Efficient Programming

The most efficient flash programming is achieved when writing full 256 Byte pages, once per page. It is recommended to program 256 bytes at a time, aligned on 256 byte boundaries. Programming data in full, aligned pages is the most efficient method to store data. Using misaligned buffer can force alignment at some level of software or firmware, which can slow down some systems. Please consult the processors documentation to understand any impact on your platform. Some applications require writes that are less than 256 bytes. In this case, the recommended program size is at least 16 bytes aligned on a 16 byte boundary.

Manufacturing environments enable additional efficiencies where production programmers can access multiple flash devices in parallel. This avoids bus contention by only allowing access to a single device at a time. Note accelerated programming is typically used in production environments to further reduce programming times.

1.2.2 Flash Operating Environment

Infineon recommends a flash V_{CC} be maintained within the flash data sheet specification to ensure reliable flash operations. Many times V_{CC} Bias noise can be reduced via characterization and optimization of the module's signal integrity and power delivery network. These type investigations should be part of the early design planning and validation to ensure the power and ground voltage fluctuations are within an IC's V_{CC} specification across all operating conditions.

1.2.3 Flash Usage Model

Another topic related to flash programming is the flash usage model and product life expectancy. The following two application notes address flash programming and erasure operations as they relate understanding flash endurance, data retention, and system level tools to extend reliable flash operation if required.

- Practical Guide to Endurance and Data Retention

http://www.cypress.com/documentation/application-notes/an99121-practical-guide-endurance-and-data-retention

- Wear Leveling

http://www.cypress.com/documentation/application-notes/an98521-wear-leveling

1.2.4 Programming Verification

The following addresses another important aspect of programming; Programming Verification.

Programming validation starts with an assessment of the flash Read access integrity. Read access assessment is completed by performing basic Read Identification / Read ID check to determine if the system controller is communicating with the flash device correctly. Performing these tests enables first level verification that basic continuity, write timing, and voltage interface do not exhibit any major issues. If the flash Device fails Read assessment, it is highly recommended to re-verify these basic Read operations on a reference system such as an industry standard flash programmer and determine if the reference system can successfully access the flash device. If these first basic reads fail on both systems, the flash is exhibiting gross operational failures and should be examined for signs of mechanical stress or electrical over stress.

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Once the device is shown to have good read integrity it is essential to understand the system programming algorithm, any block protection, and software time out constraints. Is the system using an auto timer with no periodic register polling for program operation status?

After sending a program command sequence it is recommended to read the Status Register WIP bit to confirm the device successfully accepted the programming command. To verify successful programming operation completions, it is useful to monitor the status register. The WIP and P_ERR bits provide status if the Program Operation completed successfully or there was an error. In instances where P_ERR = 1 (Program Error) is observed during a program operation it is an indication that there is a device fault. Once the program operation is successfully completed it is recommended to perform a 2x read verify operation at high and low flash V_{CC} range. Note a partially or incompletely programmed device/cell will typically fail read verification against its master pattern.

Please consult the device data sheet to ensure your flash hardware and software adhere to the specified requirements and note the **www.cypress.com** website can be accessed to obtain SW Driver, flash File Systems, along with numerous applications notes. If you have further questions about using SPI devices, please contact Infineon support.

2 Summary

This document shows the S25FL-P Multi I/O SPI Family supports standard SPI features and additional features like increased read and write BW access speeds up to 40 Mbytes/s, which enables programming option to improve the devices overall programming efficiency. Also highlighted was the concept that full Page programming is more efficient than word programming. To provide reliable flash operation, the designer should characterize the module design to provide an operating environment that at least meets or is better than the flash data sheet recommended operating conditions.

References

[1] S25FL129P datasheet

Revision history

Document version	Date of release	Description of changes
**	2010-07-09	Initial release.
*A	2018-07-18	Updated to Cypress template. Completing Sunset Review.
*B	2021-04-23	Updated to Infineon template.
*C	2021-07-27	Obsolete document. Completing Sunset Review.

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