THIS SPEC IS OBSOLETE

Spec No: 001-99494

Spec Title: AN99494 - MIGRATING FROM S25FL204K TO S25FL208K

Replaced by: NONE

AN99494

Migrating from S25FL204K to S25FL208K

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Associated Part Family: S25FL204K S25FL208K
Associated Code Examples: None
Related Application Notes: None

AN99494 discusses the key differences that need to be considered when migrating from S25FL204K to S25FL208K. This application note explains how S25FL208K is a replacement for S25FL204K.

1 Introduction

S25FL208K, an 8-Mbit SPI Flash, is a replacement device for S25FL204K. The two devices are identical in terms of pinout, package composition and dimensions, and command set. This application note discusses the key differences between the two devices that need to be considered when migrating from the S25FL204K to the S25FL208K.

2 Drop-In Replacement or Not?

From a hardware point of view, the S25FL204K operates at clock speeds up to 85MHz and the S25FL208K is only able to operate up to 76MHz. From a software point of view, the command sets are identical; the device ID, Block protection features, and Chip Erase times are different. Thus, in many cases, a S25FL208K is a drop-in replacement for a S25FL204K. See Critical Considerations for more details.

Table 1 shows the compatibility chart of S25FL204K and S25FL208K. For a detailed comparison, see Table 3.

Table 1. Compatibility Chart

S25FL204K Feature or Spec	Is S25FL208K Compatible?
Package	Yes
Pinout	Yes
Temperature Range	Yes
Operating Voltage	Yes
Operating Current	Yes
Standby Current	Yes
Command Set	Yes
Timing / Frequency	No
Data Retention	Yes
Endurance	Yes
Block Protection	No

3 Ordering Part Numbers

Table 2. Recommended Ordering Part Numbers for Migration

S25FL204K	S25FL208K	Comments
Ordering Part Number	Ordering Part Number	
S255FL204K0TMFI01	S25FL208K0RMFI01	Clocks above 76 MHz not supported. Software change required for Device ID update and Block protection.
S255FL204K0TMFI04	S25FL208K0RMFI04	

4 Comparison of S25FL204K and S25FL208K

Table 3. Detailed Comparison Table

		S25FL204K	S25FL208K	Comments
Package Type		01, 04	01, 04	Identical RoHS-compliant packages.
Pinout/package Outline		SOIC-8 (208 mil),SOIC-8 (150 mil)	SOIC-8 (208 mil),SOIC-8 (150 mil)	Identical pinout, outline, and board footprint.
Temperature Range		–40 ºC to +85 ºC	–40 ºC to +85 ºC	Identical
Operating Voltage Range		2.7 V to 3.6 V	2.7 V to 3.6 V	Identical
Read Data Current[1 2]	**Typical**	10 mA @ 33 MHz	10 mA @ 33 MHz	Identical
	Max	15 mA @ 33 MHz	15 mA @ 33 MHz	
	Max	25 mA @ 100 MHz	25 mA @ 100 MHz	
Dual Output Read Current[1 2]	**Typical**	12 mA @ 33 MHz	12 mA @ 33 MHz	Identical
	Max	18 mA @ 33 MHz	18 mA @ 33 MHz	
	Max	25 mA @ 100 MHz	25 mA @ 100 MHz	
Page Program Current[3]	**Typical**	15 mA	15 mA	Identical
	Max	20 mA	20mA	
Write Status Register Current[3]	**Typical**	10 mA	10 mA	Identical
	Max	18 mA	18 mA	
Erase Current[3]	**Typical**	20 mA	20 mA	Identical
	Max	25 mA	25 mA	
Standby Current[4]	**Typical**	15 µA	15 µA	Identical
	Max	35 µA	35 µA	
Power-Down Current[4]	**Typical**	15 µA	15 µA	Identical
	Max	32 µA	32 µA	
Command Set		3-byte addressing, opcodes	3-byte addressing, opcodes	Identical

[1]SCK = 0.1 VCC / 0.9 VCC DO= Open

[2]Checker Board Pattern

[3] CS# = VCC

[4] CS# = VCC, VIN = GND or VCC

		S25FL204K	S25FL208K	Comments
Clock Frequency		85 MHz	76 MHz	Different. See the Clock Speed section in Critical Considerations.
Data Retention		20-year data retention typical	20-year data retention typical	Identical
Endurance (Program/Erase Cycles)		100k erase/program cycles typical	100k erase/program cycles typical	Identical
VCC (min) to CS# Low (t_{VSL})		10 µs Min	10 µs Min	Identical
Time Delay Before Write Instruction (t_{PUW})	**Typical**	1 ms	1 ms	Identical
	Max	10 ms	10 ms	
Write Inhibit Threshold Voltage (V_{WI})	**Typical**	1 V	1 V	Identical
	Max	2 V	2 V	
Device ID	**ABh**	12h	13h	Different. See the Device ID section in Critical Considerations.
	90h	0112h	0113h	
	9Fh	014013h	014014h	
Write Status Register Time	**Typical**	10 ms	10 ms	Identical
	Max	15 ms	15 ms	
Byte Program Time (First Byte)	**Typical**	30 µs	30 µs	Identical
	Max	50 µs	50 µs	
Additional Byte Program Time (After First Byte)	**Typical**	6 µs	6 µs	Identical
	Max	12 µs	12 µs	
Page Program Time	**Typical**	1.5 ms	1.5ms	Identical
	Max	5 ms	5 ms	
Sector Erase Time (4 kB)	**Typical**	50 ms	50 ms	Identical
	Max	300 ms	300 ms	
Block Erase Time (64 kB)	**Typical**	0.5 s	0.5 s	Identical
	Max[5]	2 s	2 s	
Chip Erase Time	**Typical**	3.5 s	7 s	Different. See the Device Density section in Critical Considerations.
	Max	7 s[6]	15 s[7]	
Block Protection		See Table 5	See Table 5	Different. See the Device Density section in Critical Considerations.
Number of Blocks (64K) / Sectors (4K)		8/128	16/256	Different. See the Device Density section in Critical Considerations.
Flash Array Size		524,288 bytes	1,048,576 bytes	Different. See the Device Density section in Critical Considerations.

[5]Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 5.3 s

[6] Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 8.4 s

[7] Max value shown is for less than 10k cycles. For greater than 10k cycles, max value is 18 s.

5 Critical Considerations

You should consider all the parameter differences mentioned in Table 3 during the migration to S25FL208K. This section discusses the critical differences. System designers should also review the datasheet when migrating to the new part.

5.1 Clock Speed

The S25FL204K operates at a maximum clock rate of 85 MHz. The S25FL208K operates at a maximum clock rate of 76 MHz. If the system being migrated operates at more than 76 MHz, the clock rate will need to be reduced so that it is 76 MHz or less. If it is not possible to change the clock rate, contact Cypress for other migration options.

5.2 Device ID

Table 4 lists the opcodes that could be used to retrieve the device ID from the flash device and their values. Software that checks the device ID of the S25FL204K will need to be changed to recognize the device ID returned by the S25FL208K.

Table 4. Device ID Values

Opcode	S25FL204K Value	S25FL208K Value
ABh	12h	13h
90H	0112h	0113h
9FH	014013h	014014h

5.3 Device Density

The fact that the S25FL208K has a higher density than the S25FL204K raises several issues that must be accounted for. The sections below detail these issues.

5.3.1 Chip Erase

Because the S25FL208K has a flash array that is twice as large as the S25FL204K, the time required to execute the Chip Erase (C7h) opcode will be twice as long. Any software that uses time delays instead of checking the Write In Progress (WIP) bit in the status register will need to be modified to account for the longer chip erase time.

5.3.2 Block Protection

The S25FL208K has twice as many blocks (64K) and sectors (4K) as the S25FL204K. The behavior of the Block Protection bits in the Status register is different. Table 5 summarizes the differences.

Table 5. Block Protection Details

Status Register Bit				S25FL204K	S25FL208K
BP3	BP2	BP1	BP0		
0	0	0	0	None	None
0	0	0	1	Block 7 (070000h - 07FFFFh)	Block 15 (0F0000h-0FFFFFh)
0	0	1	0	Blocks 6-7 (060000h-07FFFFh)	Blocks 14-15 (0E0000h-0FFFFFh)
0	0	1	1	Blocks 4-7 (040000-07FFFFh)	Blocks 12-15 (0C0000h-0FFFFFh)
0	1	0	0	Blocks 0-7 (000000h-07FFFFh)	Blocks 8-15 (080000h-0FFFFFh)
0	1	0	1	Blocks 0-7 (000000h-07FFFFh)	Blocks 0-15 (000000h-0FFFFFh)
0	1	1	0	Blocks 0-7 (000000h-07FFFFh)	Blocks 0-15 (000000h-0FFFFFh)
0	1	1	1	Blocks 0-7 (000000h-07FFFFh)	Blocks 0-15 (000000h-0FFFFFh)
1	0	0	0	None	None
1	0	0	1	Sectors 0-126 (000000h-07EFFFh)	Sectors 0-254 (000000h-0FEFFFh)
1	0	1	0	Sectors 0-123 (000000h-07BFFFh)	Sectors 0-252 (000000h-0FCFFFh)

Status Register Bit				S25FL204K	S25FL208K
BP3	BP2	BP1	BP0		
1	0	1	1	Sectors 0-119 (000000h-076FFFh)	Sectors 0-247 (000000h-0F6FFFh)
1	1	0	0	Sectors 0-111 (000000h-06FFFFh)	Sectors 0-239 (000000h-0EFFFh)
1	1	0	1	Sectors 0-95 (000000h-005FFFFh)	Sectors 0-223 (000000h-0DFFFFh)
1	1	1	0	Sectors 0-63 (000000h-03FFFFh)	Sectors 0-191 (000000h-0BFFFFh)
1	1	1	1	Sectors 0-127 (000000h-07FFFFh)	Sectors 0-255 (000000-0FFFFFh)

5.3.3 Addressable Flash Array

The flash array in the S25FL208K is twice as large as the one in the S25FL204K so it requires one extra address bit to address it (A19). Migrated software must control address bit A19. If A19 is not constant (either 0 or 1), it is possible that data will not be where it is expected to be.

6 Summary

AN99494 discussed the differences between S25FL204K and S25FL208K that need to be considered during migration to the S25Fl208K.

7 Related Documents

S25FL204K Datasheet

S25FL208K Datasheet

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4898638	AHCL	08/27/2015	New application note.
*A	5866782	AESATMP8	08/29/2017	Updated logo and Copyright.
*B	6351987	BWHA	10/16/2018	Obsolete document. Completing Sunset Review.

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