

AURIX™ TC36x

About this document

Scope and purpose

The Appendix supplies information specific for the TC36x supplementing the family documentation.

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Revision history RevisionHistory-1

Introduction

1 Introduction

For Introduction, block diagrams and feature set consult the family document.
For Pinning consult the Data Sheet.

Memory Maps (MEMMAP)

2 Memory Maps (MEMMAP)

This is the automatically generated memory map of the TC36x.

2.1 Overview

The memory map describes the address locations and access possibilities for the units, memories, and reserved areas as “seen” from the different on-chip buses’ point of view.

2.2 Functional Description

The bus-specific address maps describe how the different bus master devices react on accesses to on-chip memories and modules, and which address ranges are valid or invalid for the corresponding buses.

The detailed address mapping of e.g. control registers, SRAM blocks or flash banks/sectors within a module is described in the related module chapter.

The SFI is an uni-directional bridge for access from SPB to SRI and therefore not mentioned here as an SRI master in the Address Map. The SFI is fully transparent and does not include an address translation mechanism.

Note: In addition to the here described system address map, each TriCore has a TriCore IP internal access to its PSPR via C000_0000_H and an internal access to its DSPR via D000_0000_H. This additional/private view to the local scratch pad SRAMs is described in the CPU chapter.

Table 1 defines the acronyms and other terms that are used in the address maps.

Table 1 Definition of Acronyms and Terms

Term	Description
BE	A bus access is terminated with a bus error.
ok	A bus access is allowed and is executed.
16	A bus access with width 16 and 32 bits is allowed and executed.
32	A bus access with width 32 bits is allowed and executed.
Access	A bus access is allowed and is executed.

2.2.1 Segments

This section summarizes the contents of the segments.

Segments 0 and 2

These memory segments are reserved.

Segments 1 and 3-7

These memory segments allow access to the CPUs Program and Data Scratch Pad SRAM (PSPR, DSPR), Program and Data Cache SRAMs (PCACHE, DCACHE) as well as TAG SRAMs related to Program and Data Cache (PTAG SRAM¹⁾ and DTAG SRAM¹⁾.

Where DCACHE is supported, DCACHE and DTAG SRAM¹⁾ can be only accessed if the Data Cache is disabled.

PCACHE and PTAG SRAMs¹⁾ can be only accessed if the related Program Cache is disabled.

1) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address.

Memory Maps (MEMMAP)

The attribute of these segments (cached / non-cached) can be partially configured¹⁾ for each CPUs data and program side individually (see CPU chapter: Physical Memory Attribute Registers, PMAx).

Segment 8

This memory segment allows cached access to PFlash and BROM.

Segment 9

This memory segment allows cached access to LMU and to EMEM.

Segment 10

This memory segment allows non-cached access to PFlash, DFlash and BROM.

Segment 11

This memory segment allows non-cached access to LMU and to EMEM.

Segment 12

This memory segment is reserved.

Segment 13

This memory segment is reserved.

Segment 14

This memory segment is reserved.

Segment 15

The lower 128 Mbyte is SPB address space and the upper 128 Mbyte is SRI address space.

2.3 Bus Fabric SRI

This is the merged view of all SRI Bus Segments as used in the TC36x.

Table 2 Address Map as seen by Bus Masters on Bus SRI

Address Range		Size	Unit	Access Type	
from	to			Read	Write
00000000 _H	5FFFFFFF _H	-	Reserved	BE	BE
60000000 _H	6002FFFF _H	192 Kbyte	Data ScratchPad RAM (CPU1)	ok	ok
60030000 _H	60033FFF _H	16 Kbyte	Data Cache RAM (CPU1)	ok	ok
60034000 _H	600BFFFF _H	-	Reserved	BE	BE
600C0000 _H	600C17FF _H	6 Kbyte	Data Cache Tag RAM (CPU1)	ok	ok
600C1800 _H	600FFFFFF _H	-	Reserved	BE	BE
60100000 _H	60107FFF _H	32 Kbyte	Program ScratchPad RAM (CPU1)	ok	ok
60108000 _H	6010FFFF _H	32 Kbyte	Program Cache RAM (CPU1)	ok	ok
60110000 _H	601BFFFF _H	-	Reserved	BE	BE

1) Mapping of Cache and TAG SRAMs is controlled via the MTU register MTU_MEMMAP.

Memory Maps (MEMMAP)

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
601C0000 _H	601C2FFF _H	12 Kbyte	Program Cache TAG RAM (CPU1)	ok	ok
601C3000 _H	6FFFFFFF _H	-	Reserved	BE	BE
70000000 _H	7002FFFF _H	192 Kbyte	Data ScratchPad RAM (CPU0)	ok	ok
70030000 _H	70033FFF _H	16 Kbyte	Data Cache RAM (CPU0)	ok	ok
70034000 _H	700BFFFF _H	-	Reserved	BE	BE
700C0000 _H	700C17FF _H	6 Kbyte	Data Cache Tag RAM (CPU0)	ok	ok
700C1800 _H	700FFFFFF _H	-	Reserved	BE	BE
70100000 _H	70107FFF _H	32 Kbyte	Program ScratchPad RAM (CPU0)	ok	ok
70108000 _H	7010FFFF _H	32 Kbyte	Program Cache RAM (CPU0)	ok	ok
70110000 _H	701BFFFF _H	-	Reserved	BE	BE
701C0000 _H	701C2FFF _H	12 Kbyte	Program Cache TAG RAM (CPU0)	ok	ok
701C3000 _H	7FFFFFFF _H	-	Reserved	BE	BE
80000000 _H	801FFFFFF _H	2 Mbyte	Program Flash (PFI0)	ok	ok
80200000 _H	802FFFFFF _H	-	Reserved	BE	BE
80300000 _H	804FFFFFF _H	2 Mbyte	Program Flash (PFI1)	ok	ok
80500000 _H	8FDFFFFFF _H	-	Reserved	BE	BE
8FE00000 _H	8FE7FFFF _H	512 Kbyte	Online Data Acquisition (OLDA) (DOM0)	BE	ok
8FE80000 _H	8FFEFFFF _H	-	Reserved	BE	BE
8FFF0000 _H	8FFFFFFF _H	64 Kbyte	Boot ROM (BROM) (DMU)	ok	ok
90000000 _H	9000FFFF _H	64 Kbyte	DLMU RAM (CPU0)	ok	ok
90010000 _H	9001FFFF _H	64 Kbyte	DLMU RAM (CPU1)	ok	ok
90020000 _H	9FFFFFFF _H	-	Reserved	BE	BE
A0000000 _H	A01FFFFFF _H	2 Mbyte	Program Flash (PFI0_NC)	ok	ok
A0200000 _H	A02FFFFFF _H	-	Reserved	BE	BE
A0300000 _H	A04FFFFFF _H	2 Mbyte	Program Flash (PFI1_NC)	ok	ok
A0500000 _H	A7FFFFFF _H	-	Reserved	BE	BE
A8000000 _H	A8003FFF _H	16 Kbyte	Erase Counter (PFI0)	ok	ok
A8004000 _H	A807FFFF _H	-	Reserved	BE	BE
A8080000 _H	A80FFFFFF _H	512 Kbyte	Register address space (PFI0)	ok	ok
A8100000 _H	A82FFFFFF _H	-	Reserved	BE	BE
A8300000 _H	A8303FFF _H	16 Kbyte	Erase Counter (PFI1)	ok	ok
A8304000 _H	A837FFFF _H	-	Reserved	BE	BE
A8380000 _H	A83FFFFFF _H	512 Kbyte	Register address space (PFI1)	ok	ok
A8400000 _H	AFFFFFFF _H	-	Reserved	BE	BE
AF000000 _H	AF01FFFF _H	128 Kbyte	Data Flash 0 EEPROM (DF0) and Host Command Sequence Interpreter (DMU)	ok	ok
AF020000 _H	AF3FFFFFF _H	-	Reserved	BE	BE

Memory Maps (MEMMAP)

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
AF400000 _H	AF405FFF _H	24 Kbyte	UCB_BMHD0_ORIG (UCB)	ok	ok
			UCB_BMHD1_ORIG (UCB)	ok	ok
			UCB_BMHD2_ORIG (UCB)	ok	ok
			UCB_BMHD3_ORIG (UCB)	ok	ok
			UCB_SSW (UCB)	ok	ok
			UCB_USER (UCB)	ok	ok
			UCB_TEST (UCB)	ok	ok
			UCB_HSMCFG (UCB)	ok	ok
			UCB_BMHD0_COPY (UCB)	ok	ok
			UCB_BMHD1_COPY (UCB)	ok	ok
			UCB_BMHD2_COPY (UCB)	ok	ok
			UCB_BMHD3_COPY (UCB)	ok	ok
			UCB_REDSEC (UCB)	ok	ok
			Reserved (UCB)	ok	ok
			Reserved (UCB)	ok	ok
			UCB_RETEST (UCB)	ok	ok
			UCB_PFLASH_ORIG (UCB)	ok	ok
			UCB_DFLASH_ORIG (UCB)	ok	ok
			UCB_DBG_ORIG (UCB)	ok	ok
			UCB_HSM_ORIG (UCB)	ok	ok
			UCB_HSMCOTP0_ORIG (UCB)	ok	ok
			UCB_HSMCOTP1_ORIG (UCB)	ok	ok
			UCB_ECPRIO_ORIG (UCB)	ok	ok
			UCB_SWAP_ORIG (UCB)	ok	ok
			UCB_PFLASH_COPY (UCB)	ok	ok
			UCB_DFLASH_COPY (UCB)	ok	ok
			UCB_DBG_COPY (UCB)	ok	ok
			UCB_HSM_COPY (UCB)	ok	ok
			UCB_HSMCOTP0_COPY (UCB)	ok	ok
			UCB_HSMCOTP1_COPY (UCB)	ok	ok
			UCB_ECPRIO_COPY (UCB)	ok	ok
			UCB_SWAP_COPY (UCB)	ok	ok

Memory Maps (MEMMAP)

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
cont'd			UCB_OTP0_ORIG (UCB)	ok	ok
			UCB_OTP1_ORIG (UCB)	ok	ok
			UCB_OTP2_ORIG (UCB)	ok	ok
			UCB_OTP3_ORIG (UCB)	ok	ok
			UCB_OTP4_ORIG (UCB)	ok	ok
			UCB_OTP5_ORIG (UCB)	ok	ok
			UCB_OTP6_ORIG (UCB)	ok	ok
			UCB_OTP7_ORIG (UCB)	ok	ok
			UCB_OTP0_COPY (UCB)	ok	ok
			UCB_OPT1_COPY (UCB)	ok	ok
			UCB_OPT2_COPY (UCB)	ok	ok
			UCB_OPT3_COPY (UCB)	ok	ok
			UCB_OPT4_COPY (UCB)	ok	ok
			UCB_OPT5_COPY (UCB)	ok	ok
			UCB_OPT6_COPY (UCB)	ok	ok
			UCB_OPT7_COPY (UCB)	ok	ok
AF406000 _H	AF7FFFFFF _H	-	Reserved	BE	BE
AF800000 _H	AF80FFFF _H	64 Kbyte	Configuration Sector Layout (CFS)	ok	ok
AF810000 _H	AFBFFFFFF _H	-	Reserved	BE	BE
AFC00000 _H	AFC1FFFF _H	128 Kbyte	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter (DMU)	ok	ok
AFC20000 _H	AFDFFFFFF _H	-	Reserved	BE	BE
AFE00000 _H	AFE7FFFF _H	512 Kbyte	Online Data Acquisition (OLDA) (DOM0_NC)	BE	ok
AFE80000 _H	AFFEFFFF _H	-	Reserved	BE	BE
AFFF0000 _H	AFFFFFFF _H	64 Kbyte	Boot ROM (BROM) (DMU)	ok	ok
B0000000 _H	B000FFFF _H	64 Kbyte	DLMU RAM (CPU0_NC)	ok	ok
B0010000 _H	B001FFFF _H	64 Kbyte	DLMU RAM (CPU1_NC)	ok	ok
B0020000 _H	F801FFFF _H	-	Reserved	BE	BE
F8020000 _H	F8027FFF _H	32 Kbyte	sri slave interface (FSIRAM)	ok	ok
F8028000 _H	F802FFFF _H	-	Reserved	BE	BE
F8030000 _H	F80300FF _H	256 byte	sri slave interface (FSI)	ok	ok
F8030100 _H	F8037FFF _H	-	Reserved	BE	BE
F8038000 _H	F803FFFF _H	32 Kbyte	sri slave interface (PMU)	ok	ok
F8040000 _H	F807FFFF _H	256 Kbyte	sri slave interface (DMU)	ok	ok
F8080000 _H	F86FFFFFF _H	-	Reserved	BE	BE
F8700000 _H	F870FFFF _H	64 Kbyte	sri slave interface (DOM0)	ok	ok
F8710000 _H	F87FFFFFF _H	-	Reserved	BE	BE

Memory Maps (MEMMAP)

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
F8800000 _H	F881FFFF _H	128 Kbyte	Safety Memory Protection Register (CPU0) DLMU Safety Memory Protection registers (CPU0) Safety register protection registers (CPU0) Kernel Reset registers (CPU0) Flash Configuration registers (CPU0) Overlay Block Control registers (CPU0) Memory Integrity Registers (CPU0) Core Special Function Registers (CPU0) General Purpose Registers (CPU0) Memory Protection Registers (CPU0) Temporal Protection System registers (CPU0) Floating point register (CPU0) Core Debug Performance Counter registers (CPU0) Data Memory Interface registers (CPU0) Program Memory Interface registers (CPU0)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F8820000 _H	F883FFFF _H	128 Kbyte	Safety Memory Protection Register (CPU1) DLMU Safety Memory Protection registers (CPU1) Safety register protection registers (CPU1) Kernel Reset registers (CPU1) Flash Configuration registers (CPU1) Overlay Block Control registers (CPU1) Memory Integrity Registers (CPU1) Core Special Function Registers (CPU1) General Purpose Registers (CPU1) Memory Protection Registers (CPU1) Temporal Protection System registers (CPU1) Floating point register (CPU1) Core Debug Performance Counter registers (CPU1) Data Memory Interface registers (CPU1) Program Memory Interface registers (CPU1)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok
F8840000 _H	FFBFFFFFF _H	-	Reserved	BE	BE
FFC00000 _H	FFC1FFFF _H	128 Kbyte	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter (DMU)	ok	ok
FFC20000 _H	FFFFFFFF _H	-	Reserved	BE	BE

2.4 Bus Instance SPB

Table 3 Address Map as seen by Bus Masters on Bus SPB

Address Range		Size	Unit	Access Type	
from	to			Read	Write
00000000 _H	0FFFFFFF _H	-	Reserved	BE	BE
10000000 _H	FFFFFFFF _H	3584 Mbyte	Redirection of SRI ranges (SFIBRIDGE1) Bridge to Bus Segment 00 of SRI (SFIBRIDGE1)	ok	ok

Memory Maps (MEMMAP)

Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
F0000000 _H	F00001FF _H	512 byte	FPI slave interface (FCE)	ok	ok
F0000200 _H	F00003FF _H	-	Reserved	BE	BE
F0000400 _H	F00005FF _H	512 byte	FPI slave interface (CBS)	ok	ok
F0000600 _H	F00006FF _H	256 byte	FPI slave interface (ASCLIN0)	ok	ok
F0000700 _H	F00007FF _H	256 byte	FPI slave interface (ASCLIN1)	ok	ok
F0000800 _H	F00008FF _H	256 byte	FPI slave interface (ASCLIN2)	ok	ok
F0000900 _H	F00009FF _H	256 byte	FPI slave interface (ASCLIN3)	ok	ok
F0000A00 _H	F0000AFF _H	256 byte	FPI slave interface (ASCLIN4)	ok	ok
F0000B00 _H	F0000BFF _H	256 byte	FPI slave interface (ASCLIN5)	ok	ok
F0000C00 _H	F0000CFF _H	256 byte	FPI slave interface (ASCLIN6)	ok	ok
F0000D00 _H	F0000DFF _H	256 byte	FPI slave interface (ASCLIN7)	ok	ok
F0000E00 _H	F0000EFF _H	256 byte	FPI slave interface (ASCLIN8)	ok	ok
F0000F00 _H	F0000FFF _H	256 byte	FPI slave interface (ASCLIN9)	ok	ok
F0001000 _H	F00010FF _H	256 byte	FPI slave interface (STM0)	ok	ok
F0001100 _H	F00011FF _H	256 byte	FPI slave interface (STM1)	ok	ok
F0001200 _H	F00017FF _H	-	Reserved	BE	BE
F0001800 _H	F00018FF _H	256 byte	FPI slave interface (GPT120)	ok	ok
F0001900 _H	F0001BFF _H	-	Reserved	BE	BE
F0001C00 _H	F0001CFF _H	256 byte	Register block QSPI0 (QSPI0)	ok	ok
F0001D00 _H	F0001DFF _H	256 byte	Register block QSPI1 (QSPI1)	ok	ok
F0001E00 _H	F0001EFF _H	256 byte	Register block QSPI2 (QSPI2)	ok	ok
F0001F00 _H	F0001FFF _H	256 byte	Register block QSPI3 (QSPI3)	ok	ok
F0002000 _H	F00025FF _H	-	Reserved	BE	BE
F0002600 _H	F00026FF _H	256 byte	FPI slave interface (MSC0)	ok	ok
F0002700 _H	F00029FF _H	-	Reserved	BE	BE
F0002A00 _H	F0002AFF _H	256 byte	FPI slave interface (CCU60)	ok	ok
F0002B00 _H	F0002BFF _H	256 byte	FPI slave interface (CCU61)	ok	ok
F0002C00 _H	F0002FFF _H	-	Reserved	BE	BE
F0003000 _H	F0003AFF _H	2.7 Kbyte	FPI slave interface (SENT)	ok	ok
F0003B00 _H	F0004FFF _H	-	Reserved	BE	BE
F0005000 _H	F0005AFF _H	2.7 Kbyte	FPI slave interface (PSI5) FPI slave interface (PSI5)	ok ok	ok ok
F0005B00 _H	F0006FFF _H	-	Reserved	BE	BE
F0007000 _H	F0007FFF _H	4 Kbyte	FPI slave interface (PSI5S)	ok	ok
F0008000 _H	F000FFFF _H	-	Reserved	BE	BE
F0010000 _H	F0013FFF _H	16 Kbyte	FPI slave interface (DMA)	ok	ok
F0014000 _H	F001BFFF _H	-	Reserved	BE	BE

Memory Maps (MEMMAP)

Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
F001C000 _H	F001CFFF _H	4 Kbyte	FPI slave interface (ERAY0) ERAY RAM (ERAY0)	ok ok	ok ok
F001D000 _H	F001F0FF _H	8.2 Kbyte	FPI bus interface (GETH) FPI bus interface (GETH)	ok ok	ok ok
F001F100 _H	F001FFFF _H	-	Reserved	BE	BE
F0020000 _H	F0023FFF _H	16 Kbyte	FPI slave interface (EVADC)	ok	ok
F0024000 _H	F0024FFF _H	4 Kbyte	FPI slave interface (EDSADC)	ok	ok
F0025000 _H	F00250FF _H	256 byte	FPI slave interface (CONVCTRL)	ok	ok
F0025100 _H	F002FFFF _H	-	Reserved	BE	BE
F0030000 _H	F00300FF _H	256 byte	BCU Registers (SBCU)	ok	ok
F0030100 _H	F0034FFF _H	-	Reserved	BE	BE
F0035000 _H	F00351FF _H	512 byte	FPI slave interface (IOM)	ok	ok
F0035200 _H	F0035FFF _H	-	Reserved	BE	BE
F0036000 _H	F00363FF _H	1 Kbyte	SCU: Connections to FPI/BPI bus (SCU) Clocking System Registers (SCU) Power Management Registers (SCU)	ok ok ok	ok ok ok
F0036400 _H	F00367FF _H	-	Reserved	BE	BE
F0036800 _H	F0036FFF _H	2 Kbyte	FPI slave interface (SMU)	ok	ok
F0037000 _H	F0037FFF _H	4 Kbyte	IR Status and Control Registers (INT)	ok	ok
F0038000 _H	F0039FFF _H	8 Kbyte	IR Service Request Control Registers (SRC) (SRC)	ok	ok
F003A000 _H	F003A0FF _H	256 byte	SPB bus slave interface (P00)	ok	ok
F003A100 _H	F003A1FF _H	-	Reserved	BE	BE
F003A200 _H	F003A2FF _H	256 byte	SPB bus slave interface (P02)	ok	ok
F003A300 _H	F003A9FF _H	-	Reserved	BE	BE
F003AA00 _H	F003AAFF _H	256 byte	SPB bus slave interface (P10)	ok	ok
F003AB00 _H	F003ABFF _H	256 byte	SPB bus slave interface (P11)	ok	ok
F003AC00 _H	F003ACFF _H	256 byte	SPB bus slave interface (P12)	ok	ok
F003AD00 _H	F003ADFF _H	256 byte	SPB bus slave interface (P13)	ok	ok
F003AE00 _H	F003AEFF _H	256 byte	SPB bus slave interface (P14)	ok	ok
F003AF00 _H	F003AFFF _H	256 byte	SPB bus slave interface (P15)	ok	ok
F003B000 _H	F003B3FF _H	-	Reserved	BE	BE
F003B400 _H	F003B4FF _H	256 byte	SPB bus slave interface (P20)	ok	ok
F003B500 _H	F003B5FF _H	256 byte	SPB bus slave interface (P21)	ok	ok
F003B600 _H	F003B6FF _H	256 byte	SPB bus slave interface (P22)	ok	ok
F003B700 _H	F003B7FF _H	256 byte	SPB bus slave interface (P23)	ok	ok
F003B800 _H	F003BFFF _H	-	Reserved	BE	BE
F003C000 _H	F003C0FF _H	256 byte	SPB bus slave interface (P32)	ok	ok
F003C100 _H	F003C1FF _H	256 byte	SPB bus slave interface (P33)	ok	ok

Memory Maps (MEMMAP)

Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
F003C200 _H	F003C7FF _H	-	Reserved	BE	BE
F003C800 _H	F003C8FF _H	256 byte	SPB bus slave interface (P40)	ok	ok
F003C900 _H	F003FFFF _H	-	Reserved	BE	BE
F0040000 _H	F005FFFF _H	128 Kbyte	System Registers (HSM) Debug Registers (HSM) Communication Registers (HSM) HSM Reset (HSM)	32 32 32 32	32 32 32 32
F0060000 _H	F006FFFF _H	64 Kbyte	FPI slave interface (MTU) FPI slave interface (MTU)	ok ok	ok ok
F0070000 _H	F007FFFF _H	-	Reserved	BE	BE
F0080000 _H	F00803FF _H	1 Kbyte	FPI slave interface (HSSL0)	ok	ok
F0080400 _H	F008FFFF _H	-	Reserved	BE	BE
F0090000 _H	F009FFFF _H	64 Kbyte	FPI slave interface (HSCT0)	ok	ok
F00A0000 _H	F00BFFFF _H	-	Reserved	BE	BE
F00C0000 _H	F00D00FF _H	64.2 Kbyte	FPI slave interface (I2C0) FPI slave interface (I2C0)	ok ok	ok ok
F00D0100 _H	F00FFFFF _H	-	Reserved	BE	BE
F0100000 _H	F01FFFFF _H	1 Mbyte	FPI slave interface (GTM) FPI slave interface (GTM) Mapped RAMs (GTM) Embedded DPLL RAM 2 (GTM)	ok	ok
F0200000 _H	F0208FFF _H	36 Kbyte	RAM Area (CAN0) Register Area (CAN0)	ok ok	ok ok
F0209000 _H	F020FFFF _H	-	Reserved	BE	BE
F0210000 _H	F0218FFF _H	36 Kbyte	RAM Area (CAN1) Register Area (CAN1)	ok ok	ok ok
F0219000 _H	F023FFFF _H	-	Reserved	BE	BE
F0240000 _H	F0241FFF _H	8 Kbyte	Standby Controller XRAM (PMS)	ok	ok
F0242000 _H	F0247FFF _H	-	Reserved	BE	BE
F0248000 _H	F02481FF _H	512 byte	FPI slave interface (PMS) SMU registers in Standby power domain (PMS)	ok ok	ok ok
F0248200 _H	F02C09FF _H	-	Reserved	BE	BE
F02C0A00 _H	F02C0AFF _H	256 byte	FPI slave interface (ASCLIN10)	ok	ok
F02C0B00 _H	F02C0BFF _H	256 byte	FPI slave interface (ASCLIN11)	ok	ok
F02C0C00 _H	F7FFFFFF _H	-	Reserved	BE	BE
F8000000 _H	FFFFFFFF _H	128 Mbyte	Redirection of SRI ranges (SFIBRIDGE1)	ok	ok

Memory Maps (MEMMAP)

2.5 Revision History

Table 4 Revision History

Reference	Change to Previous Version	Comment
V0.1.12		
-	Formal change: for some memory ranges (e.g. "PFI0") the name was changed by appending "_NC" to "PFI0_NC" to ensure that derived tool files contain different symbols for cached and non-cached memory ranges.	-
-	Changed description of range starting at F0240000 from "SCR XRAM (PMS)" to "Standby Controller XRAM (PMS)" and corrected its Access Type to "ok/ok".	-
-	Corrected size of Program Flash PFI0 and PFI1 from 3 MByte to 2 MByte at base addresses 80000000 (PFI0), A0000000 (PFI0_NC), 80300000 (PFI1), A0300000F (PFI1_NC).	-
V0.1.13		
-	No changes. Only version number changed to keep alignment with family address map.	-
V0.1.14		
-	No changes. Only version number changed to keep alignment with family address map.	-
V0.1.15		
Page 2	DF0 size in SRI Address Map table has changed from 256 Kbyte to 128 Kbyte.	
V0.1.16		
Page 2	Re-added entry for UCB_SWAP_COPY.	-
Page 2	Corrected access type of DMU range starting at F804 0000 from BE/BE to ok/ok.	-
V0.1.17		
-	No changes. Only version number changed to keep alignment with family address map.	-
V0.1.18		
-	No changes. Only version number changed to keep alignment with family address map.	-
V0.1.19		
-	No changes. Only version number changed to keep alignment with family address map.	
V0.1.20		
-	No changes. Only version number changed to keep alignment with family address map.	
V0.1.21		
Page 6	In bus instance SPB several address ranges corrected to "BE".	
Page 2	Table row at AF400000 - AF405FFF splitted in two parts.	

TC36x Firmware

3 TC36x Firmware

This chapter supplements the family documentation with device specific information for TC36x devices.

3.1 Checker Software exit information for ALL CHECKS PASSED

Below the SCU_STMEM3...SCU_STMEM6 registers' content corresponding to "ALL CHECKS PASSED" result from Checker Software (CHSW) upon different device reset types is shown.

Table 5 "ALL CHECKS PASSED" indication by CHSW for TC36x

Reset type	Additional conditions	SCU_STMEM3	SCU_STMEM4	SCU_STMEM5	SCU_STMEM6
Cold power-on ¹⁾	--	A030FB1F _H	00000001 _H	A030FB1F _H	A030FB1F _H
Warm power-on	--	A020F82F _H	00000001 _H	A020F82F _H	A020F82F _H
System reset	--	2020B84F _H	00000001 _H	2020B84F _H	2020B84F _H
Application reset	CCUCON5.GETHDIV<>0	2020088F _H	00000001 _H	2020088F _H	2020088F _H
	CCUCON5.GETHDIV=0	2020088F _H	00200001 _H	2000088F _H	2020088F _H

1) Device start-up after LBIST execution is handled by AURIX™ TC3xx Firmware as cold power-on, therefore the SCU_STMEMx values in this row apply also in such a case (after LBIST).

Note: The result from some check(s) depends on additional conditions as follows:

- The check for Gigabit Ethernet MAC module(s) calibration will fail after application reset, if the application software has not enabled GETH clock (in SCU_CCUCON5.GETHDIV register) after the previous power-on/system reset(s) - meaning if the module is not used by application - therefore in such use-case anyway the check for this' module calibration is not relevant.*

3.2 Revision History

Table 6 Revision History

Reference	Change to Previous Version	Comment
V1.1.0.1.14...V1.1.0.1.16		
	No change	
V1.1.0.1.17		
Table 5	Footnote added, explaining FW handling after LBIST execution (documentation improvement only, no change in implementation)	
V1.1.0.1.18		
-	No functional changes	

On-Chip System Connectivity {and Bridges}

4 On-Chip System Connectivity {and Bridges}

Text with reference to family spec.

4.1 TC36x Specific IP Configuration

Table 7 TC36x specific configuration of DOM

Parameter	DOM0
Application Reset	Application Reset
Access only when any Endinit (SCU_WDTCPUxCON0.EI = 0 for any CPUx)	ENDINIT
Access only when Safety Endinit (SCU_SEICON.EI = 0)	Safety ENDINIT
Access only from HSM Master or HSM debug (or FPRO.PROINHSMCFG=0)	HSM Access
Access only when PSW = Supervisor Mode	Supervisor Mode
Access only when PSW = User Mode 0 or 1	User Mode
Access only when OCDS enabled	Debug Mode
Access only from Master x (when MOD_ACCEN0.ENx = 1 or MOD_ACCEN1.ENx = 1)	Valid Master
Access only from Master x (when MOD_ACCEN0.ENx = 1)	Valid Master (0)
Access only from Master x (when MOD_ACCEN1.ENx = 1)	Valid Master (1)
Number of SCI interfaces	16
sri base address	F8700000 _H
sri address range	10000 _H
OLDA base address	8FE00000 _H
OLDA range	80000 _H
OLDA base address (non-cached)	AFE00000 _H
OLDA range (non-cached)	80000 _H

On-Chip System Connectivity {and Bridges}

4.2 TC36x Specific Register Set

Register Address Space Table

Table 8 Register Address Space - DOM

Module	Base Address	End Address	Note
(DOM0)	8FE00000 _H	8FE7FFFF _H	Online Data Acquisition (OLDA)
	AFE00000 _H	AFE7FFFF _H	Online Data Acquisition (OLDA)
DOM0	F8700000 _H	F870FFFF _H	sri slave interface

Register Overview Table

Table 9 Register Overview - DOM0 (ascending Offset Address)

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
DOM0_PCONx (x=0-15)	Protocol Error Control Register x	00000 _H + x*20 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_PRIORIT Yx (x=0-15)	SCIx Arbiter Priority Register	00008 _H + x*20 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_ERRADD Rx (x=0-15)	SCI x Error Address Capture Register	00010 _H + x*20 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_ERRx (x=0-15)	SCI x Error Capture Register	00018 _H + x*20 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_ID	Identification Register	00408 _H	32,U,SV	BE	See Family Spec
DOM0_PESTAT	Protocol Error Status Register	00410 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_TIDSTAT	Transaction ID Status Register	00418 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_TIDEN	Transaction ID Enable Register	00420 _H	32,U,SV	32,P,SV	See Family Spec
DOM0_BRCON	Domain 0 Bridge Control Register	00430 _H	32,U,SV	32,P,SV	4

On-Chip System Connectivity {and Bridges}**Table 9 Register Overview - DOM0 (ascending Offset Address) (cont'd)**

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
DOM0_ACCEN0	Access Enable Register 0	004F0 _H	32,U,SV	32,SV,SE	See Family Spec
DOM0_ACCEN1	Access Enable Register 1	004F8 _H	32,U,SV	32,SV,SE	See Family Spec

On-Chip System Connectivity {and Bridges}

4.3 TC36x Specific Registers

4.3.1 sri slave interface

Domain 0 Bridge Control Register

DOM0_BRCON

Domain 0 Bridge Control Register

(00430_H)

Application Reset Value: 0000 0200_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											0				
r											rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		0		0		1		0		0		0			OLDAEN
rw		r		rw		rw		r		rw		r			rw

Field	Bits	Type	Description
OLDAEN	0	rw	Online Data Acquisition Enable This bit is used to control trap generated for write accesses to the OLDA address range associated with this domain. 0 _B Trap generated on a write access to the OLDA memory range. 1 _B No trap generated on a write access to the OLDA memory range.
0	5:1, 8:7, 12:11, 31:20	r	Reserved Read as 0; shall be written with 0.
0	6, 10, 19:13	rw	Reserved Read as 0; shall be written with 0.
1	9	rw	Reserved Read as 1; shall be written with 1.

4.4 Connectivity

No connections in TC36x

4.5 Interconnection Matrices

4.5.1 Domain 0 Interconnection Matrix

By default the crossbar connects MCIs to SCIs. The following connectivity matrix highlights (in red and yellow) the MCI to SCI interconnects that are non-standard in the TC36x. The unimplemented connections are redundant as they would not be useful (illegal or trapping) therefore do not restrict the functionality.

On-Chip System Connectivity {and Bridges}

		DMU	CPU0P	CPU0S	CPU1P	CPU1S	Default Slave
		SCI1	SCI3	SCI4	SCI5	SCI6	SCI15
r/w	MCI has read write connectivity to SCI						
r.o	MCI has only read connectivity to SCI						
x	MCI has no connectivity to SCI						
DMA MIF0	MCI0	r/w	r.o	r/w	r.o	r/w	r/w
SFI F2S	MCI1	r/w	r.o	r/w	r.o	r/w	r/w
CPU0	MCI2	r/w	r.o	r/w	r.o	r/w	r/w
CPU1	MCI3	r/w	r.o	r/w	r.o	r/w	r/w
HSSLO	MCI8	r/w	r.o	r/w	r.o	r/w	r/w
GETH	MCI9	r/w	r.o	r/w	r.o	r/w	r/w

Figure 1 TC36x Domain0 Connectivity Matrix

4.6 Revision History

Table 10 Revision History

Reference	Change to Previous Version	Comment
V1.1.13		
Page 4	Updated BRCON bitfield to show that bit 9 while reserved will read as 1 and should be updated to 1 (The bitfield was incorrectly showing value 0 previously). Restored correct access permission (r/w) for bit fields which are not intended for customer function.	
V1.1.14		
	No change.	
V1.1.15		
	No change.	
V1.1.16		
	No change.	
V1.1.17		
	No change.	

4.7 FPI Bus Control Units (SBCU)

This chapter supplements the family documentation with device specific information for TC36x.

4.7.1 TC36x Specific IP Configuration

The TC36x includes one FPI Bus instance. Each FPI Bus instance has its dedicated Bus Control Unit:

Table 11 Register Address Space - BCU

Module	Base Address	End Address	Note
(SBCU)	F0000000 _H	F7FFFFFF _H	FPI default slave
SBCU	F0030000 _H	F00300FF _H	BCU Registers

- System Peripheral Bus (SPB) -> SBCU. The SBCU registers are described in [Chapter 4.7.2](#)

4.7.2 SBCU Control Unit Registers

Figure 2 and Table 12 are showing the address maps with all registers of the System Bus Control Unit (SBCU) module.

SBCU Control Registers Overview

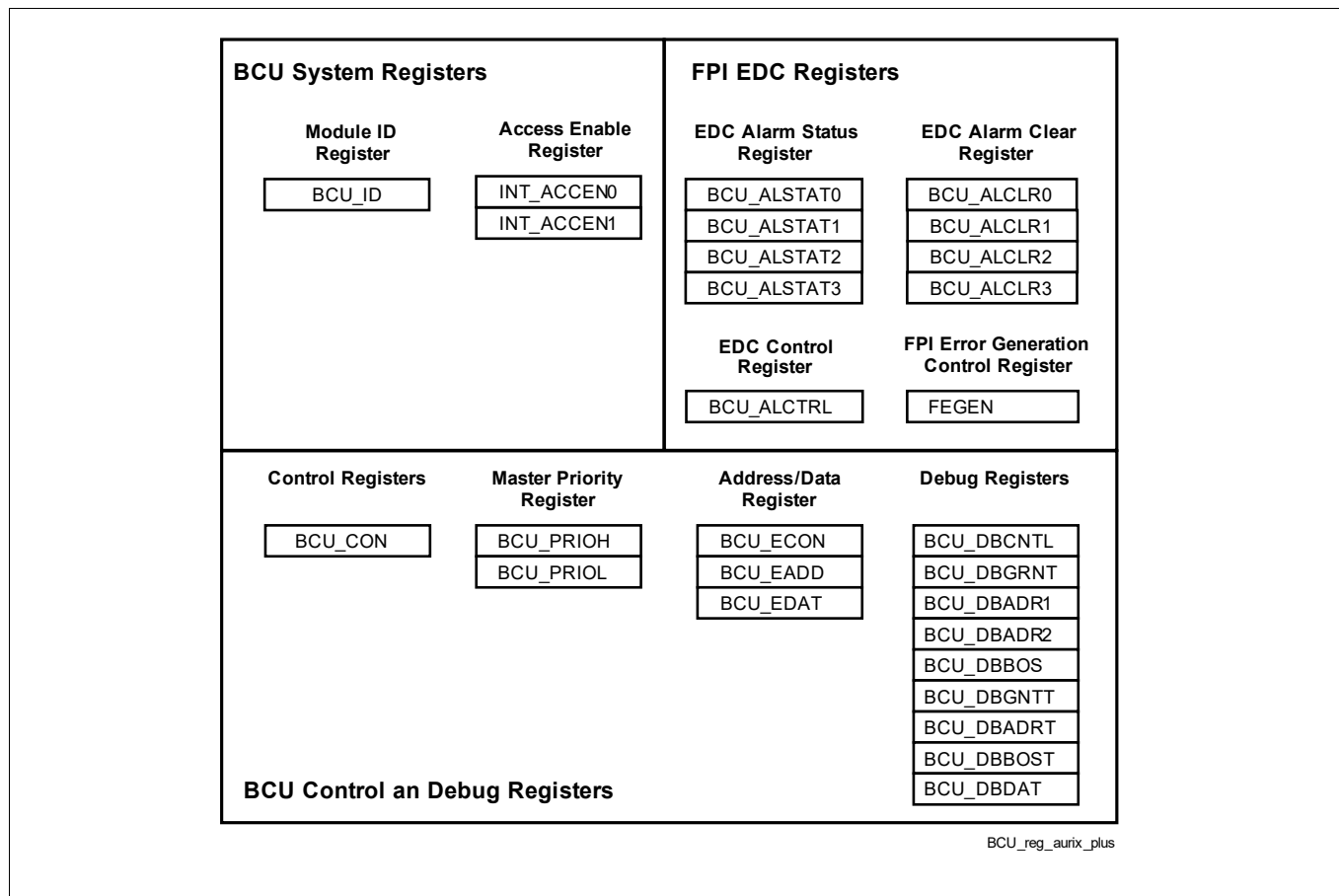


Figure 2 SBCU Registers

Table 12 Register Overview - SBCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_ID	Module Identification Register	0008 _H	U,SV	BE	Application Reset	See Family Spec
SBCU_CON	BCU Control Register	0010 _H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_PRIOH	Arbiter Priority Register High	0014 _H	U,SV	SV,E,P	Application Reset	10
SBCU_PRIOL	Arbiter Priority Register Low	0018 _H	U,SV	SV,E,P	Application Reset	10

Table 12 Register Overview - SBCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_ECON	BCU Error Control Capture Register	0020 _H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_EADD	BCU Error Address Capture Register	0024 _H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_EDAT	BCU Error Data Capture Register	0028 _H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_DBCNTL	BCU Debug Control Register	0030 _H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBGRNT	SBCU Debug Grant Mask Register	0034 _H	U,SV	SV,P	Debug Reset	12
SBCU_DBADR1	BCU Debug Address 1 Register	0038 _H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBADR2	BCU Debug Address 2 Register	003C _H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBBOS	BCU Debug Bus Operation Signals Register	0040 _H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBGNTT	SBCU Debug Trapped Master Register	0044 _H	U,SV	BE	Debug Reset	13
SBCU_DBADRT	BCU Debug Trapped Address Register	0048 _H	U,SV	BE	Debug Reset	See Family Spec
SBCU_DBBOST	BCU Debug Trapped Bus Operation Signals Register	004C _H	U,SV	BE	Debug Reset	See Family Spec
SBCU_DBDAT	BCU Debug Data Status Register	0050 _H	U,SV	BE	Debug Reset	See Family Spec
SBCU_ALSTATx (x=0-3)	BCU EDC Alarm Status Register x	0060 _H +x *4	U,SV	SV,P	Application Reset	14
SBCU_ALCLR _x (x=0-3)	BCU EDC Alarm Clear Register x	0070 _H +x *4	U,SV	SV,P	Application Reset	See Family Spec
SBCU_ALCTRL	BCU EDC Alarm Control Register	0080 _H	U,SV	SV,P	Application Reset	See Family Spec

Table 12 Register Overview - SBCU (ascending Offset Address) (cont'd)

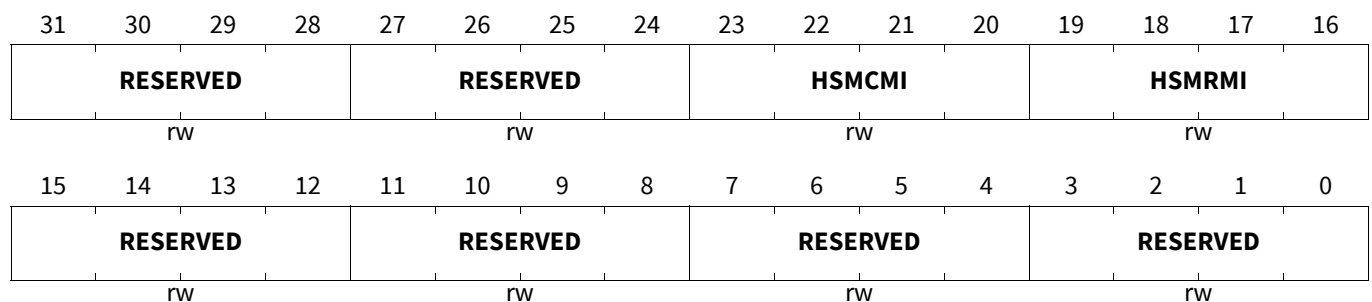
Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_FEGEN	FPI Error Generation Control Register	0084 _H	U,SV	SV,SE	Application Reset	See Family Spec
SBCU_ACCEN1	Access Enable Register 1	00F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
SBCU_ACCEN0	Access Enable Register 0	00FC _H	U,SV	SV,SE	Application Reset	See Family Spec

4.7.2.1 SBCU Control Registers Descriptions

Note: For all PRIOH / PRIOL bit fields, a lower number has a higher priority in the arbitration round than a higher one.

Arbiter Priority Register High

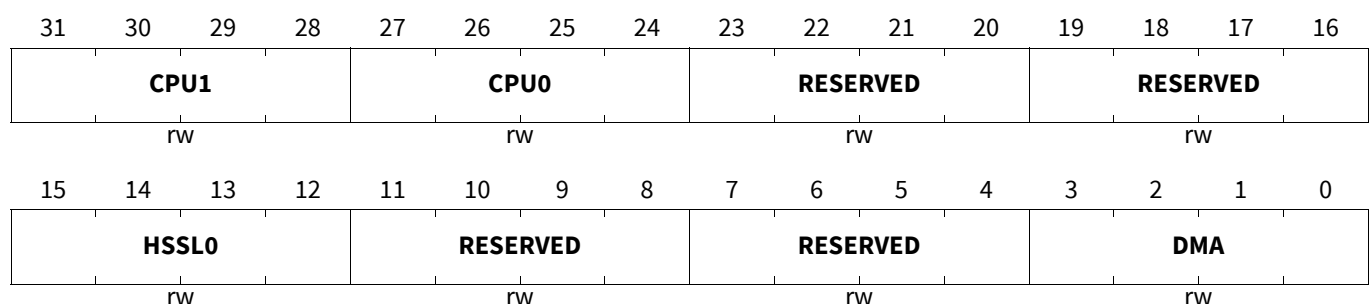
SBCU_PRIOH
Arbiter Priority Register High (0014_H) **Application Reset Value: FEDC 8888_H**



Field	Bits	Type	Description
RESERVED	3:0, 7:4, 11:8, 15:12, 27:24, 31:28	rw	Reserved Read as reset value or last written value; should be written with 0.
HSMRMI	19:16	rw	HSMRMI Priority (Index 12) This bit field defines the priority on the SPB for HSMRMI access to the SPB.
HSMCMI	23:20	rw	HSMCMI Priority (Index 13) This bit field defines the priority on the SPB for HSMCMI access to the SPB.

Arbiter Priority Register Low

SBCU_PRIOL
Arbiter Priority Register Low (0018_H) **Application Reset Value: 8854 3210_H**



Field	Bits	Type	Description
DMA	3:0	rw	DMA / Cerberus Priority (Index 0) This bit field defines the priority on the SPB for DMA and Cerberus access to the SPB.
RESERVED	7:4, 11:8, 19:16, 23:20	rw	Reserved Read as reset value or last written value; should be written with 0.
HSSL0	15:12	rw	HSSL0 Priority (Index 3) This bit field defines the priority on the SPB for HSSL0 access to the SPB.
CPU0	27:24	rw	CPU0 Priority (Index 6) This bit field defines the priority on the SPB for CPU0 access to the SPB.
CPU1	31:28	rw	CPU1 Priority (Index 7) This bit field defines the priority on the SPB for CPU1 access to the SPB.

4.7.2.2 SBCU OCDS Registers Descriptions

SBCU Debug Grant Mask Register

SBCU_DBG RNT

SBCU Debug Grant Mask Register

(0034_H)

Debug Reset Value: 0000 FFFF_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	HSMC MI	HSMR MI	1	1	1	1	CPU1	CPU0	1	1	HSSL0	1	1	DMA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

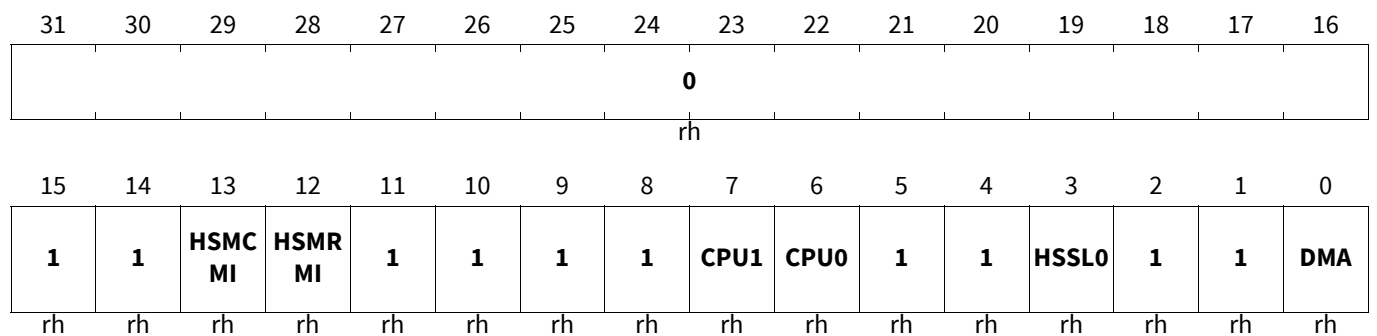
Field	Bits	Type	Description
DMA	0	rw	DMA / Cerberus Trigger Enable 0 _B FPI Bus transactions with DMA / Cerberus as bus master are enabled for grant trigger event generation. 1 _B FPI Bus transactions with DMA / Cerberus as bus master are disabled for grant trigger event generation.
HSSL0	3	rw	HSSL0 Trigger Enable 0 _B FPI Bus transactions with HSSL0 as bus master are enabled for grant trigger event generation. 1 _B FPI Bus transactions with HSSL0 as bus master are disabled for grant trigger event generation.
CPU0	6	rw	CPU0 Grant Trigger Enable 0 _B FPI Bus transactions with CPU0 as bus master are enabled for grant trigger event generation. 1 _B FPI Bus transactions with CPU as bus master are disabled for grant trigger event generation.
CPU1	7	rw	CPU1 Grant Trigger Enable 0 _B FPI Bus transactions with CPU1 as bus master are enabled for grant trigger event generation. 1 _B FPI Bus transactions with CPU1 as bus master are disabled for grant trigger event generation.
HSMRMI	12	rw	HSM Register Master Interface Grant Trigger Enable 0 _B FPI Bus transactions requested by the HSM bus master are enabled for grant trigger event generation. 1 _B FPI Bus transactions requested by the HSM bus master are disabled for grant trigger event generation.
HSMCMI	13	rw	HSM Cache Master Interface Grant Trigger Enable 0 _B FPI Bus transactions requested by the HSM bus master are enabled for grant trigger event generation. 1 _B FPI Bus transactions requested by the HSM bus master are disabled for grant trigger event generation.

Field	Bits	Type	Description
1	1, 2, 4, 5, 8, 9, 10, 11, 14, 15	rw	Reserved Read as 1 after reset; reading these bits will return the value last written.
0	31:16	r	Reserved Read as 0; should be written with 0.

SBCU Debug Trapped Master Register

SBCU_DBGNTT

SBCU Debug Trapped Master Register (0044_H) **Debug Reset Value: 0000 FFFF_H**



Field	Bits	Type	Description
DMA	0	rh	DMA / Cerberus FPI Bus Master Status 0 _B The DMA or Cerberus was the FPI bus master. 1 _B Neither DMA nor Cerberus was the FPI Bus master.
HSSL0	3	rh	HSSL 0 FPI Bus Master Status This bit indicates whether the HSSL 0 was FPI Bus master when the break trigger event occurred. 0 _B The HSSL0 was the FPI bus master. 1 _B The HSSL0 was not the FPI Bus master.
CPU0	6	rh	CPU0 FPI Bus Master Status This bit indicates whether the CPU0 was FPI Bus master when the break trigger event occurred. 0 _B The CPU0 was the FPI Bus master. 1 _B The CPU0 was not the FPI Bus master.
CPU1	7	rh	CPU1 FPI Bus Master Status This bit indicates whether the CPU1 was FPI Bus master when the break trigger event occurred. 0 _B The CPU1 was the FPI Bus master. 1 _B The CPU1 was not the FPI Bus master.

Field	Bits	Type	Description
HSMRMI	12	rh	HSM Register FPI Bus Master Interface Status This bit indicates whether the HSM was FPI Bus master when the break trigger event occurred. 0 _B HSMRMI was the FPI bus master. 1 _B HSMRMI was not the FPI Bus master.
HSMCMI	13	rh	HSM Cache FPI Bus Master Interface Status This bit indicates whether the HSM was FPI Bus master when the break trigger event occurred. 0 _B HSMCMI was the FPI bus master. 1 _B HSMCMI was not the FPI Bus master.
1	1, 2, 4, 5, 8, 9, 10, 11, 14, 15	rh	Reserved Read as 1 after reset; reading these bits will return the value last written.
0	31:16	rh	Reserved Read as 1 after reset; reading these bits will return the value last written.

BCU EDC Alarm Status Register x

The BCU provides one Alarm Status Register bit for each implemented FPI master and FPI slave.
Register bits without constant definition are reserved in this product.

SBCU_ALSTATx (x=0)

BCU EDC Alarm Status Register x (0060_H+x*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	AL30	AL29	AL28	AL27	AL26	AL25	AL24	AL23	AL22	AL21	AL20	AL19	AL18	AL17	AL16
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	AL14	AL13	AL12	AL11	AL10	AL09	AL08	AL07	AL06	AL05	AL04	AL03	AL02	AL01	AL00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	Alarm y 1 _B SBCU_S , an EDC error was detected in an active phase of the SBCU Slave Interface.
ALy (y=01)	y	rh	Alarm y 1 _B DMA_S ,

Field	Bits	Type	Description
ALy (y=02)	y	rh	Alarm y 1 _B IR_S,
ALy (y=03)	y	rh	Alarm y 1 _B SFI_F2S_S,
ALy (y=04)	y	rh	Alarm y 1 _B SCU_S,
ALy (y=05)	y	rh	Alarm y 1 _B SMU_S,
ALy (y=06)	y	rh	Alarm y 1 _B PMC_SCR_S,
ALy (y=07)	y	rh	Alarm y 1 _B MTU_S,
ALy (y=08)	y	rh	Alarm y 1 _B IOM_S,
ALy (y=09)	y	rh	Alarm y 1 _B Reserved,
ALy (y=10)	y	rh	Alarm y 1 _B ASCLIN01_S,
ALy (y=11)	y	rh	Alarm y 1 _B ASCLIN23_S,
ALy (y=12)	y	rh	Alarm y 1 _B ASCLIN45_S,
ALy (y=13)	y	rh	Alarm y 1 _B ASCLIN67_S,
ALy (y=14)	y	rh	Alarm y 1 _B QSPI0_S,
ALy (y=15)	y	rh	Alarm y 1 _B QSPI1_S,
ALy (y=16)	y	rh	Alarm y 1 _B QSPI2_S,
ALy (y=17)	y	rh	Alarm y 1 _B QSPI3_S,
ALy (y=18-19,21,24-27,31)	y	rh	Alarm y
ALy (y=20)	y	rh	Alarm y 1 _B FCE0_S,
ALy (y=22)	y	rh	Alarm y 1 _B STM0_S,
ALy (y=23)	y	rh	Alarm y 1 _B STM1_S,
ALy (y=28)	y	rh	Alarm y 1 _B PS15_S,

Field	Bits	Type	Description
ALy (y=29)	y	rh	Alarm y 1 _B PSI5S_S,
ALy (y=30)	y	rh	Alarm y 1 _B ERAY0_S,

SBCU_ALSTATx (x=1)

BCU EDC Alarm Status Register x

(0060_H+x*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	AL30	AL29	AL28	AL27	AL26	AL25	AL24	AL23	AL22	AL21	AL20	AL19	AL18	AL17	AL16
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	AL14	AL13	AL12	AL11	AL10	AL09	AL08	AL07	AL06	AL05	AL04	AL03	AL02	AL01	AL00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	Alarm y 1 _B GPT12_S, an EDC error was detected in an active phase of the GPT12 Slave Interface.
ALy (y=01)	y	rh	Alarm y 1 _B CCU6_S,
ALy (y=02)	y	rh	Alarm y 1 _B GTM_S,
ALy (y=03)	y	rh	Alarm y 1 _B MSC0_S,
ALy (y=04-06,15,17-18,22-30)	y	rh	Alarm y
ALy (y=07)	y	rh	Alarm y 1 _B SENT_S,
ALy (y=08)	y	rh	Alarm y 1 _B ETH_S,
ALy (y=09)	y	rh	Alarm y 1 _B EVADC_S,
ALy (y=10)	y	rh	Alarm y 1 _B EDSADC_S,
ALy (y=11)	y	rh	Alarm y 1 _B HSM_S,
ALy (y=12)	y	rh	Alarm y 1 _B HSSL0_S,
ALy (y=13)	y	rh	Alarm y 1 _B CAN0_S,

Field	Bits	Type	Description
ALy (y=14)	y	rh	Alarm y 1 _B CAN1_S,
ALy (y=16)	y	rh	Alarm y 1 _B I2C0_S,
ALy (y=19)	y	rh	Alarm y 1 _B CONVCTRL_S,
ALy (y=20)	y	rh	Alarm y 1 _B ASCLIN89_S,
ALy (y=21)	y	rh	Alarm y 1 _B ASCLIN1011_S,
ALy (y=31)	y	rh	Alarm y 1 _B CERBERUS_S,

SBCU_ALSTATx (x=2)

BCU EDC Alarm Status Register x

(0060_H+x*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	AL30	AL29	AL28	AL27	AL26	AL25	AL24	AL23	AL22	AL21	AL20	AL19	AL18	AL17	AL16
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	AL14	AL13	AL12	AL11	AL10	AL09	AL08	AL07	AL06	AL05	AL04	AL03	AL02	AL01	AL00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	Alarm y 1 _B P00_S, an EDC error was detected in an active phase of the Port 00 Slave Interface.
ALy (y=01,03,10,15-20,23-24,26-28,30)	y	rh	Alarm y
ALy (y=02)	y	rh	Alarm y 1 _B P02_S,
ALy (y=04)	y	rh	Alarm y 1 _B P10_S,
ALy (y=05)	y	rh	Alarm y 1 _B P11_S,
ALy (y=06)	y	rh	Alarm y 1 _B P12_S,
ALy (y=07)	y	rh	Alarm y 1 _B P13_S,

Field	Bits	Type	Description
ALy (y=08)	y	rh	Alarm y 1 _B P14_S,
ALy (y=09)	y	rh	Alarm y 1 _B P15_S,
ALy (y=11)	y	rh	Alarm y 1 _B P20_S,
ALy (y=12)	y	rh	Alarm y 1 _B P21_S,
ALy (y=13)	y	rh	Alarm y 1 _B P22_S,
ALy (y=14)	y	rh	Alarm y 1 _B P23_S,
ALy (y=21)	y	rh	Alarm y 1 _B P32_S,
ALy (y=22)	y	rh	Alarm y 1 _B P33_S,
ALy (y=25)	y	rh	Alarm y 1 _B P40_S,
ALy (y=29)	y	rh	Alarm y 1 _B HSCT0_S,
ALy (y=31)	y	rh	Alarm y 1 _B SBCU_M, an EDC error was detected in an active phase of the SBCU Master Interface.

SBCU_ALSTATx (x=3)

BCU EDC Alarm Status Register x (0060_H+x*4) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	AL30	AL29	AL28	AL27	AL26	AL25	AL24	AL23	AL22	AL21	AL20	AL19	AL18	AL17	AL16
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	AL14	AL13	AL12	AL11	AL10	AL09	AL08	AL07	AL06	AL05	AL04	AL03	AL02	AL01	AL00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	Alarm y 1 _B A_EN, multiple output enables active: A_EN_N (Master)
ALy (y=01)	y	rh	Alarm y 1 _B ABORT_EN, multiple output enables active: ABORT_EN_N (Master)
ALy (y=02)	y	rh	Alarm y 1 _B ACK_EN, multiple output enables active: ACK_EN_N (Default Master and Slave)

Field	Bits	Type	Description
ALy (y=03)	y	rh	Alarm y 1 _B D_EN , multiple output enables active: D_EN_N (Master and Slave)
ALy (y=04-15,17-18,20-21,24-27,30-31)	y	rh	Alarm y
ALy (y=16)	y	rh	Alarm y 1 _B DMA_M , an EDC error was detected in an active phase of the DMA / Cerberus Master Interface.
ALy (y=19)	y	rh	Alarm y 1 _B HSSLO_M ,
ALy (y=22)	y	rh	Alarm y 1 _B CPU0_M ,
ALy (y=23)	y	rh	Alarm y 1 _B CPU1_M ,
ALy (y=28)	y	rh	Alarm y 1 _B HSMRMI_M ,
ALy (y=29)	y	rh	Alarm y 1 _B HSMCMI_M ,

4.7.3 Connectivity

4.7.3.1 SBCU Connectivity

Table 13 List of SBCU Interface Signals

Interface Signals	I/O	Description
INT	out	Bus Control Unit SPB Service Request
INT	out	Bus Control Unit BBB Service Request

Table 14 Connections of SBCU

Interface Signals	connects	Description
SBCU:INT	to INT:sbcu.INT	Bus Control Unit SPB Service Request

4.7.4 Revision History

Table 15 Revision History

Reference	Change to Previous Version	Comment
V1.2.7		
	No functional change.	
V1.2.8		
-	No functional changes.	-

Table 15 Revision History (cont'd)

Reference	Change to Previous Version	Comment
V1.2.9		
-	No functional changes.	-

CPU Subsystem (CPU)

5 CPU Subsystem (CPU)

This chapter describes the CPU subsystem module of the TC36x.

5.1 TC36x Specific Configuration

No product specific configuration for CPU

5.2 TC36x Specific Register Set

Register Address Space Table

Table 16 Register Address Space - CPU

Module	Base Address	End Address	Note
(CPU0)	70000000 _H	7002FFFF _H	Data ScratchPad RAM interface
	70030000 _H	70033FFF _H	Data Cache RAM interface
	700C0000 _H	700C17FF _H	Data Cache Tag RAM interface
	70100000 _H	70107FFF _H	Program ScratchPad RAM interface
	70108000 _H	7010FFFF _H	Program Cache RAM interface
	701C0000 _H	701C2FFF _H	Program Cache TAG RAM interface
	90000000 _H	9000FFFF _H	DLMU RAM interface (cached)
	B0000000 _H	B000FFFF _H	DLMU RAM interface (non-cached)
CPU0	F8800000 _H	F881FFFF _H	SRI slave interface for SFR+CSFR
(CPU1)	60000000 _H	6002FFFF _H	Data ScratchPad RAM interface
	60030000 _H	60033FFF _H	Data Cache RAM interface
	600C0000 _H	600C17FF _H	Data Cache Tag RAM interface
	60100000 _H	60107FFF _H	Program ScratchPad RAM interface
	60108000 _H	6010FFFF _H	Program Cache RAM interface
	601C0000 _H	601C2FFF _H	Program Cache TAG RAM interface
	90010000 _H	9001FFFF _H	DLMU RAM interface (cached)
	B0010000 _H	B001FFFF _H	DLMU RAM interface (non-cached)
CPU1	F8820000 _H	F883FFFF _H	SRI slave interface for SFR+CSFR

Register Overview Table

CPU Subsystem (CPU)
Register Overview Tables of CPU**Table 17 Register Overview - CPU0 (ascending Offset Address)**

Short Name	Long Name	Offset Address	Page Number
CPU0_FLASHCON0	CPUx Flash Configuration Register 0	01100 _H	17
CPU0_FLASHCON1	CPUx Flash Configuration Register 1	01104 _H	See Family Spec
CPU0_FLASHCON2	CPUx Flash Configuration Register 2	01108 _H	See Family Spec
CPU0_FLASHCON3	CPUx Flash Configuration Register 3	0110C _H	See Family Spec
CPU0_FLASHCON4	CPUx Flash Configuration Register 4	01110 _H	See Family Spec
CPU0_KRST0	CPUx Reset Register 0	0D000 _H	See Family Spec
CPU0_KRST1	CPUx Reset Register 1	0D004 _H	See Family Spec
CPU0_KRSTCLR	CPUx Reset Clear Register	0D008 _H	See Family Spec
CPU0_SPR_SPROT_RGNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 _H +i*10 _H	See Family Spec
CPU0_SPR_SPROT_RGNUAI (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 _H +i*10 _H	See Family Spec
CPU0_SPR_SPROT_RGNACCENAI_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 _H +i*10 _H	See Family Spec
CPU0_SPR_SPROT_RGNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C _H +i*10 _H	See Family Spec
CPU0_SPR_SPROT_RGNACCENAI_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 _H +i*10 _H	See Family Spec
CPU0_SPR_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C _H +i*10 _H	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_SFR_SPROT_A CCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 _H	See Family Spec
CPU0_SFR_SPROT_A CCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 _H	See Family Spec
CPU0_LPB_SPROT_A CCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 _H	See Family Spec
CPU0_LPB_SPROT_A CCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 _H	See Family Spec
CPU0_DLMU_SPROT _RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 _H +i*10 _H	See Family Spec
CPU0_DLMU_SPROT _RGNUAI (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 _H +i*10 _H	See Family Spec
CPU0_DLMU_SPROT _RGNACCENAI_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 _H +i*10 _H	See Family Spec
CPU0_DLMU_SPROT _RGNACCENBI_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C _H +i*10 _H	See Family Spec
CPU0_DLMU_SPROT _RGNACCENAI_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 _H +i*10 _H	See Family Spec
CPU0_DLMU_SPROT _RGNACCENBI_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C _H +i*10 _H	See Family Spec
CPU0_OSEL	CPUx Overlay Range Select Register	0FB00 _H	See Family Spec
CPU0_RABRI (i=0-31)	CPUx Redirected Address Base Register i	0FB10 _H +i*12	See Family Spec
CPU0_OTARI (i=0-31)	CPUx Overlay Target Address Register i	0FB14 _H +i*12	See Family Spec
CPU0_OMASKI (i=0-31)	CPUx Overlay Mask Register i	0FB18 _H +i*12	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_SEGEN	CPUx SRI Error Generation Register	11030 _H	See Family Spec
CPU0_TASK_ASI	CPUx Task Address Space Identifier Register	18004 _H	See Family Spec
CPU0_PMA0	CPUx Data Access Cacheability Register	18100 _H	See Family Spec
CPU0_PMA1	CPUx Code Access Cacheability Register	18104 _H	See Family Spec
CPU0_PMA2	CPUx Peripheral Space Identifier register	18108 _H	See Family Spec
CPU0_DCON2	CPUx Data Control Register 2	19000 _H	See Family Spec
CPU0_SMACON	CPUx SIST Mode Access Control Register	1900C _H	See Family Spec
CPU0_DSTR	CPUx Data Synchronous Trap Register	19010 _H	See Family Spec
CPU0_DATR	CPUx Data Asynchronous Trap Register	19018 _H	See Family Spec
CPU0_DEADD	CPUx Data Error Address Register	1901C _H	See Family Spec
CPU0_DIEAR	CPUx Data Integrity Error Address Register	19020 _H	See Family Spec
CPU0_DIETR	CPUx Data Integrity Error Trap Register	19024 _H	See Family Spec
CPU0_DCON0	CPUx Data Memory Control Register	19040 _H	See Family Spec
CPU0_PSTR	CPUx Program Synchronous Trap Register	19200 _H	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_PCON1	CPUx Program Control 1	19204 _H	See Family Spec
CPU0_PCON2	CPUx Program Control 2	19208 _H	See Family Spec
CPU0_PCON0	CPUx Program Control 0	1920C _H	See Family Spec
CPU0_PIEAR	CPUx Program Integrity Error Address Register	19210 _H	See Family Spec
CPU0_PIETR	CPUx Program Integrity Error Trap Register	19214 _H	See Family Spec
CPU0_COMPAT	CPUx Compatibility Control Register	19400 _H	See Family Spec
CPU0_FPU_TRAP_CON	CPUx Trap Control Register	1A000 _H	See Family Spec
CPU0_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 _H	See Family Spec
CPU0_FPU_TRAP_OPC	CPUx Trapping Instruction Opcode Register	1A008 _H	See Family Spec
CPU0_FPU_TRAP_SRC1	CPUx Trapping Instruction Operand Register	1A010 _H	See Family Spec
CPU0_FPU_TRAP_SRC2	CPUx Trapping Instruction Operand Register	1A014 _H	See Family Spec
CPU0_FPU_TRAP_SRC3	CPUx Trapping Instruction Operand Register	1A018 _H	See Family Spec
CPU0_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 _H +y*8	See Family Spec
CPU0_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 _H +y*8	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 _H +y*8	See Family Spec
CPU0_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 _H +y*8	See Family Spec
CPU0_CPXE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 _H +y*4	See Family Spec
CPU0_DPRE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 _H +y*4	See Family Spec
CPU0_DPWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 _H +y*4	See Family Spec
CPU0_CPXE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 _H +(y-4)*4	See Family Spec
CPU0_DPRE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 _H +(y-4)*4	See Family Spec
CPU0_DPWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 _H +(y-4)*4	See Family Spec
CPU0_TPS_CON	CPUx Temporal Protection System Control Register	1E400 _H	See Family Spec
CPU0_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 _H +y*4	See Family Spec
CPU0_TPS_EXTIM_ENTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 _H	See Family Spec
CPU0_TPS_EXTIM_ENTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 _H	See Family Spec
CPU0_TPS_EXTIM_EXIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 _H	See Family Spec
CPU0_TPS_EXTIM_EXIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C _H	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_TPS_EXTIM_C LASS_EN	CPUx Exception Timer Class Enable Register	1E450 _H	See Family Spec
CPU0_TPS_EXTIM_S TAT	CPUx Exception Timer Status Register	1E454 _H	See Family Spec
CPU0_TPS_EXTIM_F CX	CPUx Exception Timer FCX Register	1E458 _H	See Family Spec
CPU0_TRiEVT (i=0-7)	CPUx Trigger Event i	1F000 _H +i*8	See Family Spec
CPU0_TRiADR (i=0-7)	CPUx Trigger Address i	1F004 _H +i*8	See Family Spec
CPU0_CCTRL	CPUx Counter Control	1FC00 _H	See Family Spec
CPU0_CCNT	CPUx CPU Clock Cycle Count	1FC04 _H	See Family Spec
CPU0_ICNT	CPUx Instruction Count	1FC08 _H	See Family Spec
CPU0_M1CNT	CPUx Multi-Count Register 1	1FC0C _H	See Family Spec
CPU0_M2CNT	CPUx Multi-Count Register 2	1FC10 _H	See Family Spec
CPU0_M3CNT	CPUx Multi-Count Register 3	1FC14 _H	See Family Spec
CPU0_DBGSR	CPUx Debug Status Register	1FD00 _H	See Family Spec
CPU0_EXEVT	CPUx External Event Register	1FD08 _H	See Family Spec
CPU0_CREVT	CPUx Core Register Access Event	1FD0C _H	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_SWEVT	CPUx Software Debug Event	1FD10 _H	See Family Spec
CPU0_TRIG_ACC	CPUx TriggerAddressx	1FD30 _H	See Family Spec
CPU0_DMS	CPUx Debug Monitor Start Address	1FD40 _H	See Family Spec
CPU0_DCX	CPUx Debug Context Save Area Pointer	1FD44 _H	See Family Spec
CPU0_DBGTCR	CPUx Debug Trap Control Register	1FD48 _H	See Family Spec
CPU0_PCXI	CPUx Previous Context Information Register	1FE00 _H	See Family Spec
CPU0_PSW	CPUx Program Status Word	1FE04 _H	See Family Spec
CPU0_PC	CPUx Program Counter	1FE08 _H	See Family Spec
CPU0_SYSCON	CPUx System Configuration Register	1FE14 _H	See Family Spec
CPU0_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 _H	See Family Spec
CPU0_CORE_ID	CPUx Core Identification Register	1FE1C _H	See Family Spec
CPU0_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 _H	See Family Spec
CPU0_BTV	CPUx Base Trap Vector Table Pointer	1FE24 _H	See Family Spec
CPU0_ISP	CPUx Interrupt Stack Pointer	1FE28 _H	See Family Spec

CPU Subsystem (CPU)

Table 17 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_ICR	CPUx Interrupt Control Register	1FE2C _H	See Family Spec
CPU0_FCX	CPUx Free CSA List Head Pointer	1FE38 _H	See Family Spec
CPU0_LCX	CPUx Free CSA List Limit Pointer	1FE3C _H	See Family Spec
CPU0_CUS_ID	CPUx Customer ID register	1FE50 _H	See Family Spec
CPU0_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 _H +y*4	See Family Spec
CPU0_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 _H +y*4	See Family Spec

Table 18 Register Overview - CPU1 (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
CPU1_FLASHCON0	CPUx Flash Configuration Register 0	01100 _H	17
CPU1_FLASHCON1	CPUx Flash Configuration Register 1	01104 _H	See Family Spec
CPU1_FLASHCON2	CPUx Flash Configuration Register 2	01108 _H	See Family Spec
CPU1_FLASHCON3	CPUx Flash Configuration Register 3	0110C _H	See Family Spec
CPU1_FLASHCON4	CPUx Flash Configuration Register 4	01110 _H	See Family Spec
CPU1_KRST0	CPUx Reset Register 0	0D000 _H	See Family Spec
CPU1_KRST1	CPUx Reset Register 1	0D004 _H	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_KRSTCLR	CPUx Reset Clear Register	0D008 _H	See Family Spec
CPU1_SPR_SPROT_RGNLAI (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	0E000 _H +i*10 _H	See Family Spec
CPU1_SPR_SPROT_RGNUAI (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	0E004 _H +i*10 _H	See Family Spec
CPU1_SPR_SPROT_RGNACCENAI_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	0E008 _H +i*10 _H	See Family Spec
CPU1_SPR_SPROT_RGNACCENBI_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	0E00C _H +i*10 _H	See Family Spec
CPU1_SPR_SPROT_RGNACCENAI_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	0E088 _H +i*10 _H	See Family Spec
CPU1_SPR_SPROT_RGNACCENBI_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	0E08C _H +i*10 _H	See Family Spec
CPU1_SFR_SPROT_ACCENA_W	CPUx Safety Protection Register Access Enable Register A	0E100 _H	See Family Spec
CPU1_SFR_SPROT_ACCENB_W	CPUx Safety Protection Region Access Enable Register B	0E104 _H	See Family Spec
CPU1_LPB_SPROT_ACCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	0E110 _H	See Family Spec
CPU1_LPB_SPROT_ACCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	0E114 _H	See Family Spec
CPU1_DLMU_SPROT_RGNLAI (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	0E200 _H +i*10 _H	See Family Spec
CPU1_DLMU_SPROT_RGNUAI (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	0E204 _H +i*10 _H	See Family Spec
CPU1_DLMU_SPROT_RGNACCENAI_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	0E208 _H +i*10 _H	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_DLMU_SPROT_RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	0E20C _H +i*10 _H	See Family Spec
CPU1_DLMU_SPROT_RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	0E288 _H +i*10 _H	See Family Spec
CPU1_DLMU_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	0E28C _H +i*10 _H	See Family Spec
CPU1_OSEL	CPUx Overlay Range Select Register	0FB00 _H	See Family Spec
CPU1_RABRi (i=0-31)	CPUx Redirected Address Base Register i	0FB10 _H +i*12	See Family Spec
CPU1_OTARi (i=0-31)	CPUx Overlay Target Address Register i	0FB14 _H +i*12	See Family Spec
CPU1_OMASKi (i=0-31)	CPUx Overlay Mask Register i	0FB18 _H +i*12	See Family Spec
CPU1_SEGEN	CPUx SRI Error Generation Register	11030 _H	See Family Spec
CPU1_TASK_ASI	CPUx Task Address Space Identifier Register	18004 _H	See Family Spec
CPU1_PMA0	CPUx Data Access Cacheability Register	18100 _H	See Family Spec
CPU1_PMA1	CPUx Code Access Cacheability Register	18104 _H	See Family Spec
CPU1_PMA2	CPUx Peripheral Space Identifier register	18108 _H	See Family Spec
CPU1_DCON2	CPUx Data Control Register 2	19000 _H	See Family Spec
CPU1_SMACON	CPUx SIST Mode Access Control Register	1900C _H	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_DSTR	CPUx Data Synchronous Trap Register	19010 _H	See Family Spec
CPU1_DATR	CPUx Data Asynchronous Trap Register	19018 _H	See Family Spec
CPU1_DEADD	CPUx Data Error Address Register	1901C _H	See Family Spec
CPU1_DIEAR	CPUx Data Integrity Error Address Register	19020 _H	See Family Spec
CPU1_DIETR	CPUx Data Integrity Error Trap Register	19024 _H	See Family Spec
CPU1_DCON0	CPUx Data Memory Control Register	19040 _H	See Family Spec
CPU1_PSTR	CPUx Program Synchronous Trap Register	19200 _H	See Family Spec
CPU1_PCON1	CPUx Program Control 1	19204 _H	See Family Spec
CPU1_PCON2	CPUx Program Control 2	19208 _H	See Family Spec
CPU1_PCON0	CPUx Program Control 0	1920C _H	See Family Spec
CPU1_PIEAR	CPUx Program Integrity Error Address Register	19210 _H	See Family Spec
CPU1_PIETR	CPUx Program Integrity Error Trap Register	19214 _H	See Family Spec
CPU1_COMPAT	CPUx Compatibility Control Register	19400 _H	See Family Spec
CPU1_FPU_TRAP_CO N	CPUx Trap Control Register	1A000 _H	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	1A004 _H	See Family Spec
CPU1_FPU_TRAP_OP C	CPUx Trapping Instruction Opcode Register	1A008 _H	See Family Spec
CPU1_FPU_TRAP_SR C1	CPUx Trapping Instruction Operand Register	1A010 _H	See Family Spec
CPU1_FPU_TRAP_SR C2	CPUx Trapping Instruction Operand Register	1A014 _H	See Family Spec
CPU1_FPU_TRAP_SR C3	CPUx Trapping Instruction Operand Register	1A018 _H	See Family Spec
CPU1_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	1C000 _H +y*8	See Family Spec
CPU1_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	1C004 _H +y*8	See Family Spec
CPU1_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	1D000 _H +y*8	See Family Spec
CPU1_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	1D004 _H +y*8	See Family Spec
CPU1_CPXE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	1E000 _H +y*4	See Family Spec
CPU1_DPPE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	1E010 _H +y*4	See Family Spec
CPU1_DPWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	1E020 _H +y*4	See Family Spec
CPU1_CPXE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	1E040 _H +(y-4)*4	See Family Spec
CPU1_DPPE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	1E050 _H +(y-4)*4	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_DPWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	1E060 _H +(y-4)*4	See Family Spec
CPU1_TPS_CON	CPUx Temporal Protection System Control Register	1E400 _H	See Family Spec
CPU1_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	1E404 _H +y*4	See Family Spec
CPU1_TPS_EXTIM_ENTRY_LVAL	CPUx Exception Entry Timer Load Value	1E440 _H	See Family Spec
CPU1_TPS_EXTIM_ENTRY_CVAL	CPUx Exception Entry Timer Current Value	1E444 _H	See Family Spec
CPU1_TPS_EXTIM_EXIT_LVAL	CPUx Exception Exit Timer Load Value	1E448 _H	See Family Spec
CPU1_TPS_EXTIM_EXIT_CVAL	CPUx Exception Exit Timer Current Value	1E44C _H	See Family Spec
CPU1_TPS_EXTIM_CLASS_EN	CPUx Exception Timer Class Enable Register	1E450 _H	See Family Spec
CPU1_TPS_EXTIM_STATUS	CPUx Exception Timer Status Register	1E454 _H	See Family Spec
CPU1_TPS_EXTIM_FCX	CPUx Exception Timer FCX Register	1E458 _H	See Family Spec
CPU1_TRIEVT (i=0-7)	CPUx Trigger Event i	1F000 _H +i*8	See Family Spec
CPU1_TRIADR (i=0-7)	CPUx Trigger Address i	1F004 _H +i*8	See Family Spec
CPU1_CCTRL	CPUx Counter Control	1FC00 _H	See Family Spec
CPU1_CCNT	CPUx CPU Clock Cycle Count	1FC04 _H	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_ICNT	CPUx Instruction Count	1FC08 _H	See Family Spec
CPU1_M1CNT	CPUx Multi-Count Register 1	1FC0C _H	See Family Spec
CPU1_M2CNT	CPUx Multi-Count Register 2	1FC10 _H	See Family Spec
CPU1_M3CNT	CPUx Multi-Count Register 3	1FC14 _H	See Family Spec
CPU1_DBGSR	CPUx Debug Status Register	1FD00 _H	See Family Spec
CPU1_EXEVT	CPUx External Event Register	1FD08 _H	See Family Spec
CPU1_CREVT	CPUx Core Register Access Event	1FD0C _H	See Family Spec
CPU1_SWEVT	CPUx Software Debug Event	1FD10 _H	See Family Spec
CPU1_TRIG_ACC	CPUx TriggerAddressx	1FD30 _H	See Family Spec
CPU1_DMS	CPUx Debug Monitor Start Address	1FD40 _H	See Family Spec
CPU1_DCX	CPUx Debug Context Save Area Pointer	1FD44 _H	See Family Spec
CPU1_DBGTCR	CPUx Debug Trap Control Register	1FD48 _H	See Family Spec
CPU1_PCXI	CPUx Previous Context Information Register	1FE00 _H	See Family Spec
CPU1_PSW	CPUx Program Status Word	1FE04 _H	See Family Spec

CPU Subsystem (CPU)

Table 18 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_PC	CPUx Program Counter	1FE08 _H	See Family Spec
CPU1_SYSCON	CPUx System Configuration Register	1FE14 _H	See Family Spec
CPU1_CPU_ID	CPUx Identification Register TC1.6.2P	1FE18 _H	See Family Spec
CPU1_CORE_ID	CPUx Core Identification Register	1FE1C _H	See Family Spec
CPU1_BIV	CPUx Base Interrupt Vector Table Pointer	1FE20 _H	See Family Spec
CPU1_BTV	CPUx Base Trap Vector Table Pointer	1FE24 _H	See Family Spec
CPU1_ISP	CPUx Interrupt Stack Pointer	1FE28 _H	See Family Spec
CPU1_ICR	CPUx Interrupt Control Register	1FE2C _H	See Family Spec
CPU1_FCX	CPUx Free CSA List Head Pointer	1FE38 _H	See Family Spec
CPU1_LCX	CPUx Free CSA List Limit Pointer	1FE3C _H	See Family Spec
CPU1_CUS_ID	CPUx Customer ID register	1FE50 _H	See Family Spec
CPU1_Dy (y=0-15)	CPUx Data General Purpose Register y	1FF00 _H +y*4	See Family Spec
CPU1_Ay (y=0-15)	CPUx Address General Purpose Register y	1FF80 _H +y*4	See Family Spec

CPU Subsystem (CPU)

5.3 TC36x Specific Registers

5.3.1 SRI slave interface for SFR+CSFR

CPUx Flash Configuration Register 0

Software may program a Flash Prefetch Buffer with a master tag identifier stored in Flash Configuration Register 0.

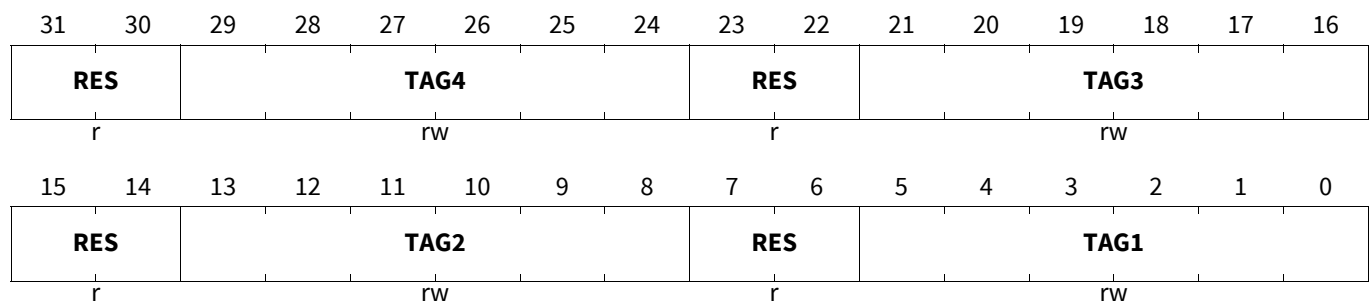
If a CPU instance does not have a local PFlash bank then the FLASHCON0 register associated with that instance will have no functionality.

CPU0_FLASHCON0

CPUx Flash Configuration Register 0 (01100_H) **Reset Value: Table 19**

CPU1_FLASHCON0

CPUx Flash Configuration Register 0 (01100_H) **Reset Value: Table 20**



Field	Bits	Type	Description
TAG1	5:0	rw	Flash Prefetch Buffer 1 Configuration FPB is assigned to on chip bus master with master tag id equal to TAG1.
RES	7:6, 15:14, 23:22, 31:30	r	Reserved Always read as 0; should be written with 0.
TAG2	13:8	rw	Flash Prefetch Buffer 2 Configuration FPB is assigned to on chip bus master with master tag id equal to TAG2.
TAG3	21:16	rw	Flash Prefetch Buffer 3 Configuration FPB is assigned to on chip bus master with master tag id equal to TAG3.
TAG4	29:24	rw	Flash Prefetch Buffer 4 Configuration FPB is assigned to on chip bus master with master tag id equal to TAG4.

Table 19 Reset Values of CPU0_FLASHCON0

Reset Type	Reset Value	Note
Application Reset	3F3F 3F3F _H	
CFS Value	2121 2020 _H	

CPU Subsystem (CPU)
Table 20 Reset Values of **CPU1_FLASHCON0**

Reset Type	Reset Value	Note
Application Reset	3F3F 3F3F _H	
CFS Value	2020 2121 _H	

5.4 Connectivity

No connections in TC36x

5.5 Revision History**Table 21** Revision History

Reference	Change to Previous Version	Comment
V1.1.16		
	No change	
V1.1.17		
	No change	
V1.1.18		
	No change	
V1.1.19		
	No change	
V1.1.20		
Page 2, 9	Change index variable from 'x' to intended 'i' for registers SPR_SPROT_RGNACCENAi_R and SPR_SPROT_RGNACCENBi_R to remove confusion with CPU instance variable.	
Page 2, 9	Change index variable from 'x' to intended 'i' for registers all DLMU_SPROT registers to remove confusion with CPU instance variable.	
V1.1.21		
	No change	

6 Non Volatile Memory (NVM) Subsystem

6.1 Overview

The Non Volatile Memory (NVM) Subsystem comprises of the Data Memory Unit (DMU), Program Flash Interface (PFI), and Non Volatile Memory module (comprising of the Flash Standard Interface (FSI), Program and Data Flash memories and Program Flash Read Write buffer (PFRWB)).

- Data Memory Unit (DMU): Controls command sequences executed on all program and data flash memories.
- Flash Standard Interface (FSI): Executes erase, program and verify operations on all flash memories.
- Program Flash (PFLASH): Divided into one or more banks each connected to a CPU. It is used by the application to store program code and data constants. Compute performance is optimized by using a point-to-point interface to minimize latency and maximize bandwidth. Each PFLASH is connected to a PFlash Read Write Buffer (PFRWB) that performs the ECC correction and detection and provides the read data to the system.
- Program Flash Interface (PFI): Each PFLASH bank has a unique point-to-point fast connection to a CPU provided by a PFI. The PFI interfaces between the CPU and the PFRWB and contains the Prefetch Buffers for storing speculative data.
- Data Flash (DFLASH): The Data Flash Module is used to emulate EEPROM and store data and divided into two banks. DFLASH read accesses are relatively slow compared to PFLASH accesses. The DFlash Read Write Buffer (DFRWB) in the FSI interfaces to the DFLASH to provide the read data. Data Flash Module also contains regions to store configuration data - User Configuration Blocks (UCBs), and Configuration Sector (CFS) which is not accessible by user.
- Boot ROM (BROM): Connected to the system via the DMU SRI port.
 - Tuning protection (commonly called the “Secure Watchdog”) to protect user software and data from maltuning data.

Attention: *The ‘Non Volatile Memory Subsystem’ chapter is the AURIX PMU chapter re-structured for closer alignment to AURIXTC3XX product architecture. It comprises of the DMU, PFI, NVM and UCB Chapters. Please note that the application accessible registers located in the FSI, and the PFLASH read status and control registers are described in the NVM chapter.*

Non Volatile Memory (NVM) Subsystem

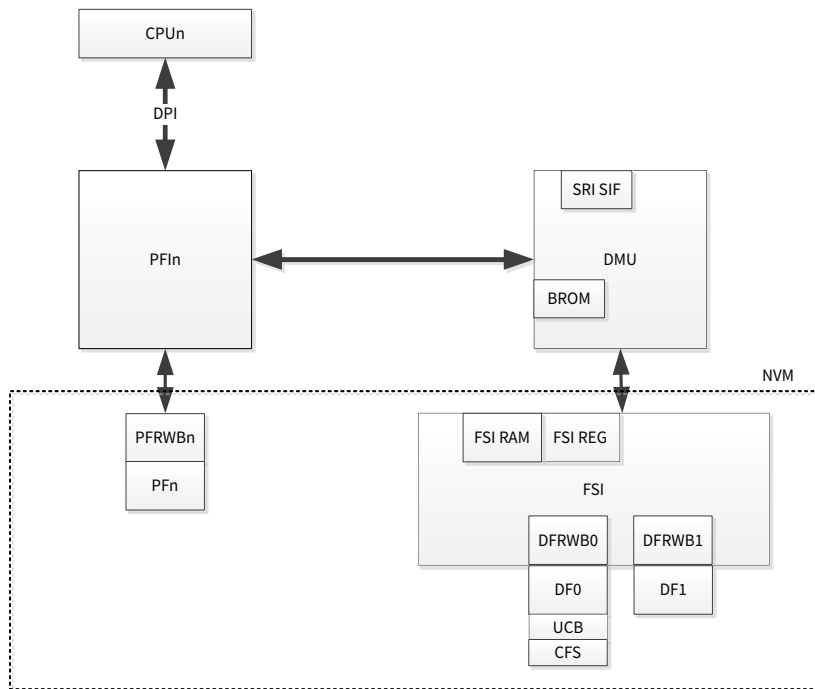


Figure 3 Non Volatile Memory (NVM) Subsystem

The purpose of the PFLASH NVM is:

- One or more PFLASH banks stores program code and data constants.
- Implementation of Erase Counters.

The purpose of the DFLASH NVM is:

- Emulation of Electrically Erasable Programmable Read Only Memory (EEPROM):
 - CPU-EEPROM used by the user application.
 - HSM-EEPROM used by the security application.
- Multiple User Configuration Blocks (UCB) used for:
 - Password based read protection combined with write protection.
 - Read-only UCB configured by IFX with unique chip identifier and trimming data.
- Configuration Sector (CFS) stores system set-up data not accessible by the user.

Data stored in the NVM is protected by ECC checksum.

- An ECC decoder at the output of the NVM corrects and detects faults in the NVM array.
- The NVM is fault tolerant and supports system operation in the presence of a number of NVM bit errors.
- For Program Flash the calculation of the ECC checksum is extended across the address to provide read protection against addressing faults.

If the Flash is not operating in the application then the NVM may be programmed and erased by command sequences executed by the FSI micro controller. All read accesses to Flash are memory mapped reads. Margin read levels may be used to check how completely a cell is programmed or erased.

The Non Volatile Memory interface micro architecture includes a security layer and a safety layer.

Security Layer (provided by DMU and PFI)

- Read protection is enabled/disabled with a Flash Module (Bank) granularity.

Non Volatile Memory (NVM) Subsystem

- Write protection is enabled/disabled with a Flash Module sector based granularity.

Safety Layer

- Master specific read access protection to each Flash Module (Bank).
- Master specific read and write access control to individual Special Function Registers (SFRs).
- Integrity of data stored in the NVM is ensured by an ECC checksum
- Integrity of PFlash read path is ensured by monitoring of read parameters in the FSI (MISR, redundant Flip Flops etc.), PFI partial lockstep mechanism, protection of PFlash wait cycles with ECC checksum, protection of data from PFI to CPU by ECC checksum and an additional safety mechanism to ensure that the local PFlash is not being programmed/erased when not expected by PFI.

Non Volatile Memory (NVM) Subsystem**6.2 Revision History****Table 22 Revision History**

Reference	Change to Previous Version	Comment
V2.0.3		
	Created to form a concise introduction chapter for the appendices	
V2.0.4		
	No Changes.	
V2.0.5		
	No Changes.	
V2.0.6		
	No Changes.	
V2.0.7		
	No Changes.	

6.3 Data Memory Unit (DMU)

This chapter supplements the family documentation with the device specific information for TC36x.

6.3.1 TC36x Specific Register Set

Register Address Space Table

Table 23 Register Address Space - PMU

Module	Base Address	End Address	Note
PMU	F8038000 _H	F803FFFF _H	sri slave interface

Table 24 Register Address Space - DMU

Module	Base Address	End Address	Note
(DMU)	8FFF0000 _H	8FFFFFFF _H	Boot ROM (BROM)
	AF000000 _H	AF01FFFF _H	Data Flash 0 EEPROM (DF0) and Host Command Sequence Interpreter
	AFC00000 _H	AFC1FFFF _H	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter
	AFFF0000 _H	AFFFFFFF _H	Boot ROM (BROM)
DMU	F8040000 _H	F807FFFF _H	SRI slave interface - Register Address Space
(DMU)	FFC00000 _H	FFC1FFFF _H	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter

Register Overview Table

Table 25 Register Overview - PMU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMU_ID	Module Identification Register	0508 _H	U,SV	BE	Application Reset	See Family Spec

Table 26 Register Overview - DMU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_ID	Module Identification Register	0000008 _H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_STATUS	Flash Status Register	0000010 _H	U,SV	BE	Application Reset	11

Table 26 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_CONTR OL	Flash Control Register	0000014 H	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_OPERA TION	Flash Operation Register	0000018 H	U,SV	BE	System Reset	See Family Spec
DMU_HF_PROTE CT	Flash Protection Status Register	000001C H	U,SV	BE	Application Reset	13
DMU_HF_CONFI RM0	Flash Confirm Status Register 0	0000020 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFI RM1	Flash Confirm Status Register 1	0000024 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFI RM2	Flash Confirm Status Register 2	0000028 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_EER	Enable Error Interrupt Control Register	0000030 H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_ERRSR	Error Status Register	0000034 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CLRE	Clear Error Register	0000038 H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_ECCR	DF0 ECC Read Register	0000040 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_ECCS	DF0 ECC Status Register	0000044 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_ECCC	DF0 ECC Control Register	0000048 H	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_ECCW	DF0 ECC Write Register	000004C H	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_CCONT ROL	Cranking Control Register	0000050 H	U,SV	P,SV	System Reset	See Family Spec

Table 26 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_PSTAT US	Power Status Register	0000060 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_PCONT ROL	Power Control Register	0000064 H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_PWAIT	PFLASH Wait Cycle Register	0000068 H	U,SV	P,SV,E	System Reset	See Family Spec
DMU_HF_DWAIT	DFLASH Wait Cycle Register	000006C H	U,SV	P,SV,E	System Reset	See Family Spec
DMU_HF_PROCO NUSR	DF0 User Mode Control	0000074 H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NPF	PFLASH Protection Configuration	0000080 H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NTP	Tuning Protection Configuration	0000084 H	U,SV	BE	See page 15	15
DMU_HF_PROCO NDF	DFLASH Protection Configuration	0000088 H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NRAM	RAM Configuration	000008C H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCO NDBG	Debug Interface Protection Configuration	0000090 H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_SUSPE ND	Suspend Control Register	00000F0 H	U,SV	P,U,SV	Application Reset	See Family Spec
DMU_HF_MARGI N	Margin Control Register	00000F4 H	U,SV	P,U,SV	Application Reset	See Family Spec
DMU_HF_ACCEN 1	Access Enable Register 1	00000F8 H	U,SV	SV,SE	Application Reset	See Family Spec
DMU_HF_ACCEN 0	Access Enable Register 0	00000FC H	U,SV	SV,SE	Application Reset	See Family Spec

Table 26 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HP_PROCO NPi0 (i=0-1)	PFLASH Bank i Protection Configuration 0	0010000 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NPi1 (i=0-1)	PFLASH Bank i Protection Configuration 1	0010004 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NPi2 (i=0-1)	PFLASH Bank i Protection Configuration 2	0010008 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NPi3 (i=0-1)	PFLASH Bank i Protection Configuration 3	001000C H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NPi4 (i=0-1)	PFLASH Bank i Protection Configuration 4	0010010 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NPi5 (i=0-1)	PFLASH Bank i Protection Configuration 5	0010014 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NOTPi0 (i=0-1)	PFLASH Bank i OTP Protection Configuration 0	0010040 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NOTPi1 (i=0-1)	PFLASH Bank i OTP Protection Configuration 1	0010044 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NOTPi2 (i=0-1)	PFLASH Bank i OTP Protection Configuration 2	0010048 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NOTPi3 (i=0-1)	PFLASH Bank i OTP Protection Configuration 3	001004C H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NOTPi4 (i=0-1)	PFLASH Bank i OTP Protection Configuration 4	0010050 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NOTPi5 (i=0-1)	PFLASH Bank i OTP Protection Configuration 5	0010054 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NWOPi0 (i=0-1)	PFLASH Bank i WOP Configuration 0	0010080 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NWOPi1 (i=0-1)	PFLASH Bank i WOP Configuration 1	0010084 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec

Table 26 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HP_PROCO NWOPi2 (i=0-1)	PFLASH Bank i WOP Configuration 2	0010088 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NWOPi3 (i=0-1)	PFLASH Bank i WOP Configuration 3	001008C H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NWOPi4 (i=0-1)	PFLASH Bank i WOP Configuration 4	0010090 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCO NWOPi5 (i=0-1)	PFLASH Bank i WOP Configuration 5	0010094 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI Oi0 (i=0-1)	PFLASH Bank i Erase Counter Priority configuration 0	00100A0 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI Oi1 (i=0-1)	PFLASH Bank i Erase Counter Priority Configuration 1	00100A4 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI Oi2 (i=0-1)	PFLASH Bank i Erase Counter Priority Configuration 2	00100A8 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI Oi3 (i=0-1)	PFLASH Bank i Erase Counter Priority Configuration 3	00100AC H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI Oi4 (i=0-1)	PFLASH Bank i Erase Counter Priority Configuration 4	00100B0 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRI Oi5 (i=0-1)	PFLASH Bank i Erase Counter Priority Configuration 5	00100B4 H+i*100 _H	U,SV	BE	See Family Spec	See Family Spec
DMU_SF_STATU S	HSM Flash Status Register	0020010 H	H	BE	Application Reset	See Family Spec
DMU_SF_CONTR OL	HSM Flash Configuration Register	0020014 H	H	H	Application Reset	See Family Spec
DMU_SF_OPERA TION	HSM Flash Operation Register	0020018 H	H	BE	System Reset	See Family Spec
DMU_SF_EER	HSM Enable Error Interrupt Control Register	0020030 H	H	H	Application Reset	See Family Spec

Table 26 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_SF_ERRSR	HSM Error Status Register	0020034 H	H	BE	Application Reset	See Family Spec
DMU_SF_CLRE	HSM Clear Error Register	0020038 H	H	H	Application Reset	See Family Spec
DMU_SF_ECCR	HSM DF1 ECC Read Register	0020040 H	H	BE	Application Reset	See Family Spec
DMU_SF_ECCS	HSM DF1 ECC Status Register	0020044 H	H	BE	Application Reset	See Family Spec
DMU_SF_ECCC	HSM DF1 ECC Control Register	0020048 H	H	H	Application Reset	See Family Spec
DMU_SF_ECCW	HSM DF1 ECC Write Register	002004C H	H	H	Application Reset	See Family Spec
DMU_SF_PROCONUSR	HSM DF1 User Mode Control	0020074 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SF_SUSPEND	HSM Suspend Control Register	00200E8 H	H	H	Application Reset	See Family Spec
DMU_SF_MARGIN	HSM DF1 Margin Control Register	00200EC H	H	H	Application Reset	See Family Spec
DMU_SP_PROCONHSMCFG	HSM Protection Configuration	0030000 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCBS	HSM Code Boot Sector	0030004 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCX0	HSM Code Exclusive Protection Configuration	0030008 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCX1	HSM Code Exclusive Protection Configuration	003000C H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCOTP0	HSM Code OTP Protection Configuration	0030010 H	U,SV	BE	See Family Spec	See Family Spec

Table 26 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_SP_PROCO NHSMCOTP1	HSM Code OTP Protection Configuration	0030014 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCO NHSM	HSM Interface Protection Configuration	0030040 H	U,SV	BE	See Family Spec	See Family Spec

6.3.2 TC36x Specific Registers

6.3.2.1 SRI slave interface - Register Address Space

Flash Status Register

The Flash Status Register reflects the status of the Flash Banks after reset.

Note: The *DxBUSY* and *PxBUSY* flags cannot be cleared with the “Clear Status” command or with the “Reset to Read” command. These flags are controlled by HW.

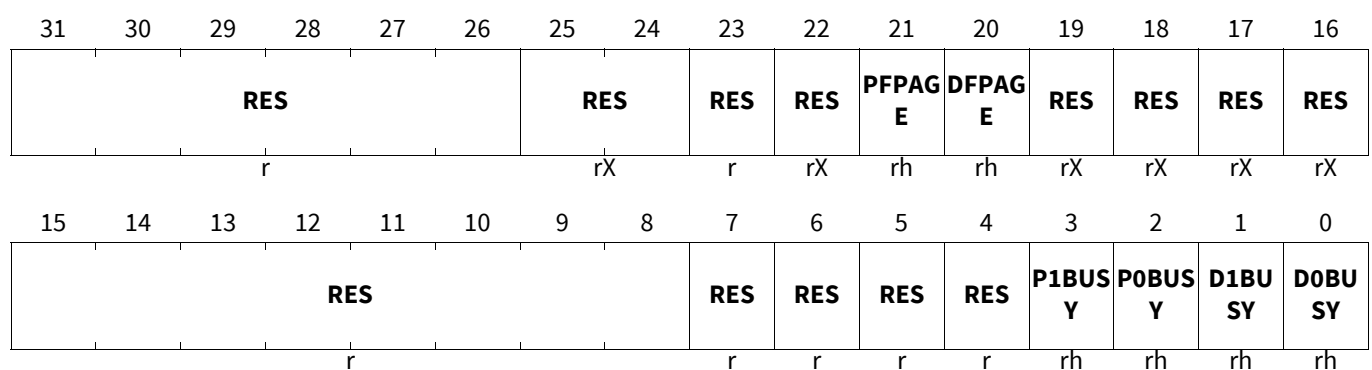
Note: After every reset, the busy bits are set while the Flash module is busy with startup (until the operation mode is entered). Also the protection installation bits are always set until end of startup.

DMU_HF_STATUS

Flash Status Register

(0000010_H)

Application Reset Value: 0000 00FF_H



Field	Bits	Type	Description
D0BUSY	0	rh	<p>Data Flash Bank 0 Busy HW-controlled status flag. Indication of busy state of DFLASH bank 0 because of active execution of an operation; DF0 busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the DF0 does not allow read access.</p> <p>0_B DF0 ready, not busy; DF0 in operation mode. 1_B DF0 busy; DF0 not in operation mode.</p>

Field	Bits	Type	Description
D1BUSY	1	rh	<p>Data Flash Bank 1 Busy HW-controlled status flag. Indication of busy state of DFLASH bank 1 because of active execution of an operation; DF1 busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the DF1 does not allow read access. Bit is not set for program/erase operations initiated by the HSM interface.</p> <p>0_B DF1 ready, not busy; DF1 in operation mode. 1_B DF1 busy; DF1 not in operation mode.</p>
PxBUSY (x=0-1)	x+2	rh	<p>Program Flash PxFxBUSY HW-controlled status flag. Indication of busy state of PFX because of active execution of an operation; PFX busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the PFX does not allow read access.</p> <p>0_B PFX ready, not busy; PFX in operation mode. 1_B PFX busy; PFX not in operation mode.</p>
RES (x=2-5)	x+2	r	<p>Reserved Always read as 0; should be written with 0.</p>
RES	15:8, 23, 31:26	r	<p>Reserved Always read as 0; should be written with 0.</p>
RES	16, 17, 18, 19, 22, 25:24	rX	<p>Reserved Undefined.</p>
DFPAGE	20	rh	<p>Data Flash in Page Mode HW-controlled status flag. Set with Enter Page Mode for DFLASH, cleared with Write Page command. This bit is not set by “Enter Page Mode” initiated by the HSM interface.</p> <p><i>Note: Read accesses are allowed while in page mode.</i></p> <p>0_B Data Flash not in page mode 1_B Data Flash in page mode</p>

Field	Bits	Type	Description
PFPAGE	21	rh	<p>Program Flash in Page Mode HW-controlled status flag. Set with Enter Page Mode for Flash, cleared with Write Page command This bit is not set by “Enter Page Mode” initiated by the HSM interface.</p> <p><i>Note:</i> <i>Read accesses are allowed while in page mode.</i></p> <p>0_B Flash not in page mode. 1_B Flash in page mode.</p>

Flash Protection Status Register

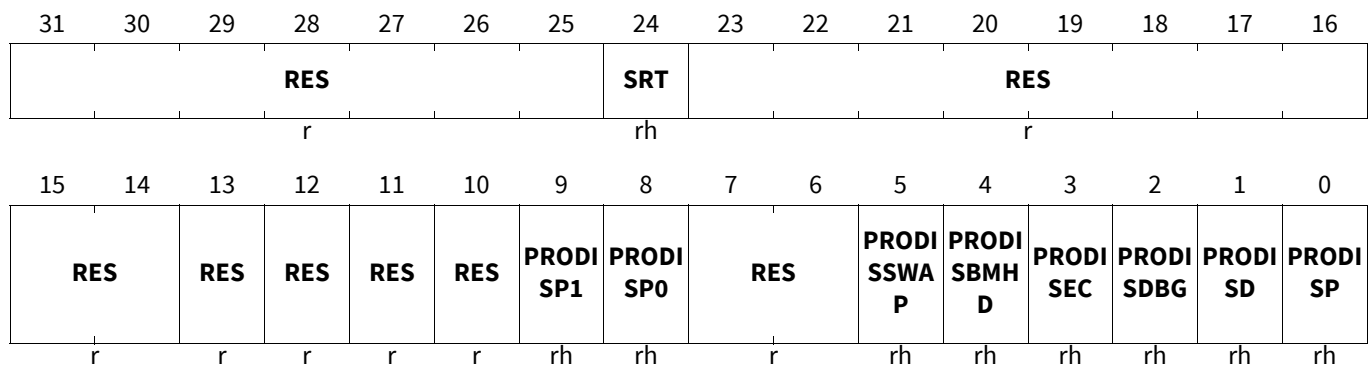
This register reports the state of the Flash protection and contains protection relevant control fields.

DMU_HF_PROTECT

Flash Protection Status Register

(000001C_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PRODISP	0	rh	<p>PFLASH Protection Disabled The protection configured by UCB_PFLASH_ORIG and UCB_PFLASH_COPY was successfully disabled by supplying the correct password to “Disable Protection”.</p> <p><i>Note:</i> <i>Cleared with command “Resume Protection”.</i></p>
PRODISD	1	rh	<p>DFLASH Protection Disabled The protection configured by UCB_DFLASH_ORIG and UCB_DFLASH_COPY was successfully disabled by supplying the correct password to “Disable Protection”.</p> <p><i>Note:</i> <i>Cleared with command “Resume Protection”.</i></p>
PRODISDBG	2	rh	<p>Debug Interface Password Protection Disabled The password configured by UCB_DBG_ORIG and UCB_DBG_COPY was correctly received with “Disable Protection”. When DMU_SP_PROCONHSMCFG.DESTDBG is “destructive” then only the SSW can disable this protection.</p> <p><i>Note:</i> <i>Cleared with command “Resume Protection”.</i></p>

Field	Bits	Type	Description
PRODISEC	3	rh	<p>Erase Counter Priority Protection Disabled The protection configured by UCB_ECPRIO_ORIG and UCB_ECPRIO_COPY was successfully disabled by supplying the correct password to “Disable Protection”.</p> <p><i>Note: Cleared with command "Resume Protection".</i></p>
PRODISBMHD	4	rh	<p>BMHD Protection Disabled The protection configured by UCB_BMHD0_ORIG and UCB_BMHD0_COPY was successfully disabled by supplying the correct password to “Disable Protection”.</p> <p><i>Note: Cleared with command "Resume Protection".</i></p>
PRODISSWAP	5	rh	<p>UCB_SWAP protection Disabled The protection configured by UCB_SWAP_ORIG and UCB_SWAP_COPY was successfully disabled by supplying the correct password to “Disable Protection”.</p> <p><i>Note: Cleared with command "Resume Protection".</i></p>
RES	7:6, 23:14, 31:25	r	<p>Reserved Always read as 0; should be written with 0.</p>
PRODISPx (x=0-1)	x+8	rh	<p>Program Flash Protection Disable PRODISPx The protection configured for PFx by UCB_PFLASH_ORIG and UCB_PFLASH_COPY was successfully disabled by supplying the correct password to “Disable Protection”.</p> <p><i>Note: Cleared with command "Resume Protection".</i></p>
RES (x=2-5)	x+8	r	<p>Reserved Always read as 0; should be written with 0.</p>
SRT	24	rh	<p>Secure Retest Password Protection Disabled</p> <p><i>Note: Cleared with command “Resume Protection”.</i></p> <p>0_B Secure Retest protection is not disabled. 1_B Secure Retest protection is disabled.</p>

Tuning Protection Configuration

DMU_HF_PROCONTP

Tuning Protection Configuration

(0000084_H)

Reset Value: [Table 27](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UCB								RES	RES	RES	RES	CPU1 DDIS	CPU0 DDIS	SWAPEN	
rh								r	r	r	r	rh	rh	rh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UCB						BML		UCB						TP	
rh						rh		rh						rh	

Field	Bits	Type	Description
TP	0	rh	<p>Tuning Protection</p> <p>This bit indicates whether tuning protection is installed or not.</p> <p>0_B Tuning protection is not configured.</p> <p>1_B Tuning protection is configured and installed, if correctly confirmed.</p>
UCB	7:1, 15:10, 31:24	rh	<p>Reserved for UCB</p> <p>Deliver the corresponding content of UCB.</p>
BML	9:8	rh	<p>Boot Mode Lock</p> <p>Used by the SSW to restrict the boot mode selection.</p> <p>00_B Boot flow with standard evaluation of boot headers.</p> <p>01_B Restricted boot flow, never evaluating HWCFG pins and without fallback to boot loader.</p> <p>...</p> <p>11_B Restricted boot flow, never evaluating HWCFG pins and without fallback to boot loader.</p>
SWAPEN	17:16	rh	<p>Enable SOTA mode</p> <p>This field enables the entry into "Software update Over the Air(SOTA) mode". In this mode, an alternate PFLASH address map can be selected. Please refer to the SOTA section of the Introduction chapter for more details.</p> <p>00_B Disabled, SOTA mode disabled.</p> <p>...</p> <p>10_B Disabled, SOTA mode disabled.</p> <p>11_B Enabled, SOTA mode enabled.</p>
CPUxDDIS (x=0-1)	x+18	rh	<p>Disable direct LPB access</p> <p>Disable direct LPB access by the CPU to the Local PFlash Bank (LPB).</p> <p>0_B Direct LPB access is enabled.</p> <p>1_B Direct LPB access is disabled.</p>
RES (x=2-5)	x+18	r	<p>Reserved</p> <p>Always read as 0; should be written with 0.</p>

Table 27 Reset Values of **DMU_HF_PROCONT**

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	
CFS Value	0000 0000 _H	

6.3.3 Connectivity

Table 28 Connections of DMU

Interface Signals	connects		Description
DMU:HOST_INT	to	INT:dmu.HOST_INT	PMU Host Service Request
DMU:FSI_INT	to	INT:dmu.FSI_INT	PMU FSI Service Request

6.3.4 Revision History

Table 29 Revision History

Reference	Change to Previous Version	Comment
V2.0.9		
	No document changes - version update to remain aligned with family document.	
V2.0.10		
	No document changes - version update to remain aligned with family document.	
V2.0.11		
Page 11	Updated register DMU_HF_STATUS .	
Page 16	Connectivity - Table updated.	
	No functional changes.	
V2.0.12		
-	No functional changes.	

6.4 Non Volatile Memory (NVM)

This chapter supplements the family documentation with the device specific information for TC36x.

6.4.1 TC36x Specific Register Set

Register Address Space Table

Table 30 Register Address Space - FSI

Module	Base Address	End Address	Note
FSI	F8030000 _H	F80300FF _H	sri slave interface

Table 31 Register Address Space - PFI

Module	Base Address	End Address	Note
(PFI0)	80000000 _H	801FFFFFF _H	Program Flash cached address space
	A0000000 _H	A01FFFFFF _H	Program Flash non-cached address space
	A8000000 _H	A8003FFF _H	Erase Counter address space
PFI0	A8080000 _H	A80FFFFFF _H	Register address space
(PFI1)	80300000 _H	804FFFFFF _H	Program Flash cached address space
	A0300000 _H	A04FFFFFF _H	Program Flash non-cached address space
	A8300000 _H	A8303FFF _H	Erase Counter address space
PFI1	A8380000 _H	A83FFFFFF _H	Register address space

Register Overview Table

Table 32 Register Overview - FSI (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FSI_COMM_1	Communication Register 1	0004 _H	U,SV	U,SV	System Reset	See Family Spec
FSI_COMM_2	Communication Register 2	0005 _H	U,SV	U,SV	System Reset	See Family Spec
FSI_HSMCOMM_1	HSM Communication Register 1	0006 _H	H	H	System Reset	See Family Spec
FSI_HSMCOMM_2	HSM Communication Register 2	0007 _H	H	H	System Reset	See Family Spec

Table 33 Register Overview - PFI (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
PFI0_ECCR	ECC Read Register	000000 _H	See Family Spec
PFI1_ECCR	ECC Read Register	000000 _H	See Family Spec
PFI0_ECCS	ECC Status Register	000020 _H	See Family Spec
PFI1_ECCS	ECC Status Register	000020 _H	See Family Spec
PFI0_SBABRECORDx (x=0-16)	SBAB Record x	002000 _H +x*20 H	See Family Spec
PFI1_SBABRECORDx (x=0-16)	SBAB Record x	002000 _H +x*20 H	See Family Spec
PFI0_DBABRECORDx (x=0-1)	DBAB Record x	004000 _H +x*20 H	See Family Spec
PFI1_DBABRECORDx (x=0-1)	DBAB Record x	004000 _H +x*20 H	See Family Spec
PFI0_MBABRECORDx (x=0)	MBAB Record 0	008000 _H	See Family Spec
PFI1_MBABRECORDx (x=0)	MBAB Record 0	008000 _H	See Family Spec
PFI0_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 _H +x*20 H	See Family Spec
PFI1_ZBABRECORDx (x=0-3)	ZBAB Record x	00C000 _H +x*20 H	See Family Spec

6.4.2 Connectivity

No connections in device.

6.4.3 Revision History

Table 34 Revision History

Reference	Change to Previous Version	Comment
V2.0.4		
	No document changes - version update to remain aligned with family document.	
V2.0.5		
Page 18	Register Address Space Table - Corrected segment A PFI address size for derivative. PFI instances not used in this device removed.	
V2.0.6		
	No functional changes.	

Local Memory Unit (LMU)

7 Local Memory Unit (LMU)

This device doesn't contain a LMU module.

Default Application Memory (LMU_DAM)

8 Default Application Memory (LMU_DAM)

This device doesn't contain LMU_DAM.

System Control Unit (SCU)

9 System Control Unit (SCU)

This chapter describes the System Control Unit (short SCU) Module of the TC36x.

9.1 TC36x Specific IP Configuration

Table 35 TC36x specific configuration of SCU

Parameter	SCU
Number of WDT linked to the number of CPU	2
Name of the ssw value	After SSW execution
CFS value for DTSCBGOCTRL register	40 _H
CFS value for DTSCCON register	200 _H

The following sections describe several differences that are device specific at the SCU level.

9.1.1 LBIST considerations for TC36x

The LBIST function can be controlled via four registers available at SCU level: LBISTCTRL0, LBISTCTRL1, LBISTCTRL2 and LBISTCTRL3 (for a complete description of these register, please address the family specification).

The LBISTCTRL3 register contains the MISR signature value that can be read back via software, after the LBIST execution (and the execution is valid).

9.1.1.1 TC36x AA

LBIST Configuration A

LBISTCTRL0.PATTERNS = 0x180;

LBISTCTRL2.LENGTH = 0x2F;

With LBISTCTRL1.BODY = 0:

- LBISTCTRL1 = 0x54000007
- LBISTCTRL3 = 0xCB195811

With LBISTCTRL1.BODY = 1:

- LBISTCTRL1 = 0x5C000007
- LBISTCTRL3 = 0xE619D483

System Control Unit (SCU)

9.2 TC36x Specific Register Set

The address space for the module registers is defined in [Register Address Space - SCU](#).

Table 36 Register Address Space - SCU

Module	Base Address	End Address	Note
SCU	F0036000 _H	F00363FF _H	SCU: Connections to FPI/BPI bus

Table 37 Register Overview - SCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (0010 _H Byte)	0000 _H	BE	BE		
SCU_ID	Identification Register	0008 _H	U,SV	BE	System Reset	See Family Spec
	Reserved (0010 _H Byte)	000C _H	BE	BE		
SCU_OSCCON	OSC Control Register	0010 _H	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_SYSPLLSTA T	System PLL Status Register	0014 _H	U,SV	BE	See Family Spec	See Family Spec
SCU_SYSPLLCON 0	System PLL Configuration 0 Register	0018 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_SYSPLLCON 1	System PLL Configuration 1 Register	001C _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_SYSPLLCON 2	System PLL Configuration 2 Register	0020 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_PERPLLSTA T	Peripheral PLL Status Register	0024 _H	U,SV	BE	System Reset	See Family Spec
SCU_PERPLLCO N0	Peripheral PLL Configuration 0 Register	0028 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_PERPLLCO N1	Peripheral PLL Configuration 1 Register	002C _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON0	CCU Clock Control Register 0	0030 _H	U,SV	SV,SE,P0	See Family Spec	See Family Spec

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_CCUCON1	CCU Clock Control Register 1	0034 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_FDR	Fractional Divider Register	0038 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_EXTCON	External Clock Control Register	003C _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON2	CCU Clock Control Register 2	0040 _H	U,SV	SV,SE,P0	System Reset	22
SCU_CCUCON3	CCU Clock Control Register 3	0044 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON4	CCU Clock Control Register 4	0048 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON5	CCU Clock Control Register 5	004C _H	U,SV	SV,SE,P0	System Reset	24
SCU_RSTSTAT	Reset Status Register	0050 _H	U,SV	BE	See page 16	16
	Reserved (0004 _H Byte)	0054 _H	BE	BE		
SCU_RSTCON	Reset Configuration Register	0058 _H	U,SV	SV,SE,P0	See page 18	18
SCU_ARSTDIS	Application Reset Disable Register	005C _H	U,SV	SV,E,P0	PowerOn Reset	20
SCU_SWRSTCON	Software Reset Configuration Register	0060 _H	U,SV	SV,E,P0	See Family Spec	See Family Spec
SCU_RSTCON2	Additional Reset Control Register	0064 _H	U,SV	SV,E,P0	See Family Spec	See Family Spec
SCU_RSTCON3	Reset Configuration Register 3	0068 _H	U,SV	SV,E,P0	See Family Spec	See Family Spec
	Reserved (0004 _H Byte)	006C _H	BE	BE		
SCU_ESRCFGx (x=0-1)	ESRx Input Configuration Register	0070 _H +x *4	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_ESROCFG	ESR Output Configuration Register	0078 _H	U,SV	SV,E,P0	System Reset	See Family Spec

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_SYSCON	System Control Register	007C _H	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_CCUCON6	CCU Clock Control Register 6	0080 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON7	CCU Clock Control Register 7	0084 _H	U,SV	SV,SE,P0	System Reset	See Family Spec
	Reserved (0004 _H Byte)	0098 _H	BE	BE		
SCU_PDR	ESR Pad Driver Mode Register	009C _H	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_IOCR	Input/Output Control Register	00A0 _H	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_OUT	ESR Output Register	00A4 _H	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_OMR	ESR Output Modification Register	00A8 _H	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_IN	ESR Input Register	00AC _H	U,SV	BE	System Reset	See Family Spec
	Reserved (0004 _H Byte)	00BC _H	BE	BE		
SCU_STSTAT	Start-up Status Register	00C0 _H	U,SV	BE	PowerOn Reset	See Family Spec
SCU_STCON	Start-up Configuration Register	00C4 _H	U,SV	ST,P0	Application Reset	See Family Spec
SCU_PMCSR0	Power Management Control and Status Register	00C8 _H	U,SV	SE,CE0,SV,P0	Application Reset	See Family Spec
SCU_PMCSR1	Power Management Control and Status Register	00CC _H	U,SV	SE,CE1,SV,P0	Application Reset	See Family Spec
SCU_PMCSR2	Power Management Control and Status Register	00D0 _H	U,SV	SE,CE2,SV,P0	Application Reset	See Family Spec

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_PMCSR3	Power Management Control and Status Register	00D4 _H	U,SV	SE,CE3,SV,P0	Application Reset	See Family Spec
SCU_PMCSR4	Power Management Control and Status Register	00D8 _H	U,SV	SE,CE4,SV,P0	Application Reset	See Family Spec
SCU_PMCSR5	Power Management Control and Status Register	00DC _H	U,SV	SE,CE5,SV,P0	Application Reset	See Family Spec
SCU_PMSTAT0	Power Management Status Register 0	00E4 _H	U,SV	BE	Application Reset	See Family Spec
SCU_PMSWCR1	Standby and Wake-up Control Register 1	00E8 _H	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
	Reserved (0020 _H Byte)	00F0 _H	BE	BE		
SCU_EMRSR	Emergency Stop Register	00FC _H	U,SV	SV,SE,P0	Application Reset	See Family Spec
SCU_EMSSW	Emergency Stop Software set and clear register	0100 _H	U,SV	U,SV,P0	Application Reset	See Family Spec
SCU_DTSCSTAT	Core Die Temperature Sensor Status Register	0104 _H	U,SV	BE	Application Reset	See Family Spec
SCU_DTSCCLIM	Core Die Temperature Sensor Limit Register	0108 _H	U,SV	U,SV,P	Application Reset	See Family Spec
	Reserved (0060 _H Byte)	0114 _H	BE	BE		
SCU_TRAPDIS1	Trap Disable Register 1	0120 _H	U,SV	SV,E,P0	Application Reset	21
SCU_TRAPSTAT	Trap Status Register	0124 _H	U,SV	BE	System Reset	See Family Spec
SCU_TRAPSET	Trap Set Register	0128 _H	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_TRAPCLR	Trap Clear Register	012C _H	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_TRAPDIS0	Trap Disable Register 0	0130 _H	U,SV	SV,E,P0	Application Reset	21

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_LCLCON0	LCL CPU0 and CPU2 Control Register	0134 _H	U,SV	SV,SE,ST,P0	See page 10	10
SCU_LCLCON1	LCL CPU1 and CPU3 Control Register	0138 _H	U,SV	SV,SE,ST,P0	See page 10	10
SCU_LCLTEST	LCL Test Register	013C _H	U,SV	U,SV,P0	System Reset	11
SCU_CHIPID	Chip Identification Register	0140 _H	U,SV	ST,P0	See Family Spec	See Family Spec
SCU_MANID	Manufacturer Identification Register	0144 _H	U,SV	BE	System Reset	See Family Spec
SCU_SWAPCTRL	Address Map Control Register	014C _H	U,SV	ST,P0	System Reset	See Family Spec
	Reserved (0060 _H Byte)	0158 _H	BE	BE		
	Reserved (0060 _H Byte)	015C _H	BE	BE		
	Reserved (0060 _H Byte)	0160 _H	BE	BE		
SCU_LBISTCTRL0	Logic BIST Control 0 Register	0164 _H	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL1	Logic BIST Control 1 Register	0168 _H	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL2	Logic BIST Control 2 Register	016C _H	U,SV	SV,SE,P0	See page 13	13
SCU_LBISTCTRL3	Logic BIST Control 3 Register	0170 _H	U,SV	BE	See Family Spec	See Family Spec
	Reserved (0020 _H Byte)	0178 _H	BE	BE		
SCU_STMEM1	Start-up Memory Register 1	0184 _H	U,SV	ST,P0	PowerOn Reset	See Family Spec
SCU_STMEM2	Start-up Memory Register 2	0188 _H	U,SV	ST,P0	System Reset	See Family Spec
SCU_PDISC	Pad Disable Control Register	018C _H	U,SV	SV,E,P0	System Reset	See Family Spec
	Reserved (0020 _H Byte)	0194 _H	BE	BE		

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_PMTRCSR0	Power Management Transition Control and Status Register 0	0198 _H	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR1	Power Management Transition Control and Status Register 1	019C _H	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR2	Power Management Transition Control and Status Register 2	01A0 _H	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR3	Power Management Transition Control and Status Register 3	01A4 _H	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_STMEM3	Start-up Memory Register 3	01C0 _H	U,SV	ST,P0	Application Reset	See Family Spec
SCU_STMEM4	Start-up Memory Register 4	01C4 _H	U,SV	ST,P0	Cold PowerOn Reset	See Family Spec
SCU_STMEM5	Start-up Memory Register 5	01C8 _H	U,SV	ST,P0	PowerOn Reset	See Family Spec
SCU_STMEM6	Start-up Memory Register 6	01CC _H	U,SV	ST,P0	System Reset	See Family Spec
SCU_OVCENABLER	Overlay Enable Register	01E0 _H	U,SV	SV,SE,P0	Application Reset	13
SCU_OVCCON	Overlay Control Register	01E4 _H	U,SV	SV,P0	Application Reset	14
SCU_EIFILT	External Input Filter Register	020C _H	U,SV	SE,SV,P0	Application Reset	See Family Spec
SCU_EICR _i (i=0-3)	External Input Channel Register i	0210 _H +i*4	U,SV	SE,SV,P0	Application Reset	See Family Spec
SCU_EIFR	External Input Flag Register	0220 _H	U,SV	BE	Application Reset	See Family Spec
SCU_FMR	Flag Modification Register	0224 _H	U,SV	U,SV,P0	Application Reset	See Family Spec

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_PDRR	Pattern Detection Result Register	0228 _H	U,SV	BE	Application Reset	See Family Spec
SCU_IGCRj (j=0-3)	Flag Gating Register j	022C _H +j*4	U,SV	SE,SV,P0	Application Reset	See Family Spec
	Reserved (0030 _H Byte)	023C _H	BE	BE		
SCU_WDTCPUyC ON0 (y=0) (y=1)	CPUy WDT Control Register 0	024C _H +y*12	U,SV	U,SV,32,CP Uy (y=CPU number)	Application Reset	See Family Spec
SCU_WDTCPUyC ON1 (y=0) (y=1)	CPUy WDT Control Register 1	0250 _H +y*12	U,SV	SV,CEy,P0	Application Reset	See Family Spec
SCU_WDTCPUyS R (y=0) (y=1)	CPUy WDT Status Register	0254 _H +y*12	U,SV	BE	Application Reset	See Family Spec
	Reserved (0030 _H Byte)	0264 _H	BE	BE		
SCU_EICON0	ENDINIT Global Control Register 0	029C _H	U,SV	U,SV,32,P0	Application Reset	See Family Spec
SCU_EICON1	ENDINIT Global Control Register 1	02A0 _H	U,SV	SV,E,P0	Application Reset	See Family Spec
SCU_EISR	ENDINIT Timeout Counter Status Register	02A4 _H	U,SV	BE	Application Reset	See Family Spec
SCU_WDTSCON0	Safety WDT Control Register 0	02A8 _H	U,SV	U,SV,32,P1	Application Reset	See Family Spec
SCU_WDTSCON1	Safety WDT Control Register 1	02AC _H	U,SV	SV,SE,P1	Application Reset	See Family Spec
SCU_WDTSSR	Safety WDT Status Register	02B0 _H	U,SV	BE	Application Reset	See Family Spec
SCU_SEICON0	Safety ENDINIT Control Register 0	02B4 _H	U,SV	U,SV,32,P1	Application Reset	See Family Spec

System Control Unit (SCU)

Table 37 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_SEICON1	Safety ENDINIT Control Register 1	02B8 _H	U,SV	SV,SE,P1	Application Reset	See Family Spec
SCU_SEISR	Safety ENDINIT Timeout Status Register	02BC _H	U,SV	BE	Application Reset	See Family Spec
	Reserved (0440 _H Byte)	02DC _H	BE	BE		
SCU_ACCEN11	Access Enable Register 11	03F0 _H	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN10	Access Enable Register 10	03F4 _H	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN01	Access Enable Register 01	03F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN00	Access Enable Register 00	03FC _H	U,SV	SV,SE	Application Reset	See Family Spec
	Reserved (0440 _H Byte)	0400 _H	BE	BE		

System Control Unit (SCU)

9.3 TC36x Specific Registers

9.3.1 SCU: Connections to FPI/BPI bus

LCL CPU0 and CPU2 Control Register

Provides control for CPU0 and CPU2 Lockstep Comparator Logic blocks.

SCU_LCLCON0

LCL CPU0 and CPU2 Control Register

(0134_H)

Reset Value: [Table 38](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LSEN0							0								LS0
rw							r								rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1							0								0
rw							r								r

Field	Bits	Type	Description
LS0	16	rh	Lockstep Mode Status This bit indicates whether CPU0 is currently running in lockstep monitor mode 0 _B Not in lockstep mode 1 _B Running in lockstep mode
LSEN0	31	rw	Lockstep Enable This bit may only be written by SSW during boot. Enable lockstep CPU monitoring for the associated processor core, CPU0. After cold reset, lockstep is enabled by default. The LSEN bit may be cleared during the boot to disable lockstep mode. SMU lockstep fault reporting should be disabled when lockstep is disabled. 0 _B Lockstep is disabled 1 _B Lockstep enabled (Default after Cold Power-On Reset)
0	0, 14:1, 30:17	r	Reserved in this product Reserved
1	15	rw	Reserved in this product Reserved

Table 38 Reset Values of SCU_LCLCON0

Reset Type	Reset Value	Note
Cold PowerOn Reset	8001 0000 _H	

LCL CPU1 and CPU3 Control Register

Provides control for CPU1 and CPU3 Lockstep Comparator Logic blocks.

System Control Unit (SCU)

SCU_LCLCON1

LCL CPU1 and CPU3 Control Register

(0138_H)

Reset Value: [Table 39](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LSEN1							0								LS1
rw							r								rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1							0								0
rw							r								r

Field	Bits	Type	Description
LS1	16	rh	<p>Lockstep Mode Status</p> <p>This bit indicates whether CPU1 is currently running in lockstep monitor mode</p> <p>0_B Not in lockstep mode</p> <p>1_B Running in lockstep mode</p>
LSEN1	31	rw	<p>Lockstep Enable</p> <p>This bit may only be written by SSW during boot. Enable lockstep CPU monitoring for the associated processor core, CPU1. If the product has no lockstep capability for CPU1, then this enables only the PFLASH access monitoring for CPU1. After cold reset, lockstep is enabled by default. The LSEN bit may be cleared during the boot to disable lockstep mode. SMU lockstep fault reporting should be disabled when lockstep is disabled.</p> <p>0_B Lockstep is disabled</p> <p>1_B Lockstep enabled (Default after Cold Power-On Reset)</p>
0	0, 14:1, 30:17	r	<p>Reserved in this product</p> <p>Reserved</p>
1	15	rw	<p>Reserved in this product</p> <p>Reserved</p>

Table 39 Reset Values of [SCU_LCLCON1](#)

Reset Type	Reset Value	Note
Cold PowerOn Reset	8001 0000 _H	

LCL Test Register

Provides the capability for software to inject a fault condition into the comparators of each Lockstep Comparator Logic block. The implementation should generate a single cycle fault each time the bit is written with ‘1’.

System Control Unit (SCU)

SCU_LCLTEST

LCL Test Register

(013C_H)

System Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					0					0	0	0	0	PLCLT 1	PLCLT 0
				r						r	r	r	r	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					0					0	0	0	0	LCLT1	LCLT0
				r						r	r	r	r	w	w

Field	Bits	Type	Description
LCLT0	0	w	LCL0 Lockstep Test Fault injection for LCL0. Reads as zero. 0 _B No action 1 _B Inject single fault in LCL0
LCLT1	1	w	LCL1 Lockstep Test Fault injection for LCL1. Reads as zero. 0 _B No action 1 _B Inject single fault in LCL1
PLCLT0	16	w	PFI0 Lockstep Test Fault injection for PFI0 lockstep. Reads as zero. 0 _B No action 1 _B Inject single fault in PFI0 lockstep
PLCLT1	17	w	PFI1 Lockstep Test Fault injection for PFI1 lockstep. Reads as zero. 0 _B No action 1 _B Inject single fault in PFI1 lockstep
0	2, 3, 4, 5, 15:6, 18, 19, 20, 21, 31:22	r	Reserved in this product will be read as 0 , should be written as 0

System Control Unit (SCU)

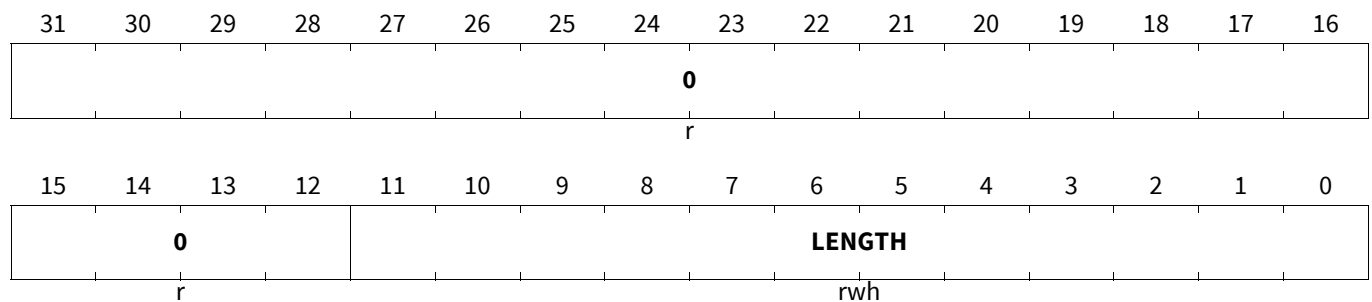
Logic BIST Control 2 Register

SCU_LBISTCTRL2

Logic BIST Control 2 Register

(016C_H)

Reset Value: [Table 40](#)



Field	Bits	Type	Description
LENGTH	11:0	rwh	LBIST Maximum Scan-Chain Length This field defines the number of shift-cycles for each LBIST scan-load. It will be automatically loaded with the product-specific value, stored in Flash config-sector during startup-software execution.
0	31:12	r	Reserved Read as 0; should be written with 0.

Table 40 Reset Values of [SCU_LBISTCTRL2](#)

Reset Type	Reset Value	Note
System Reset	0000 0000 _H	
CFS Value	0000 002F _H	

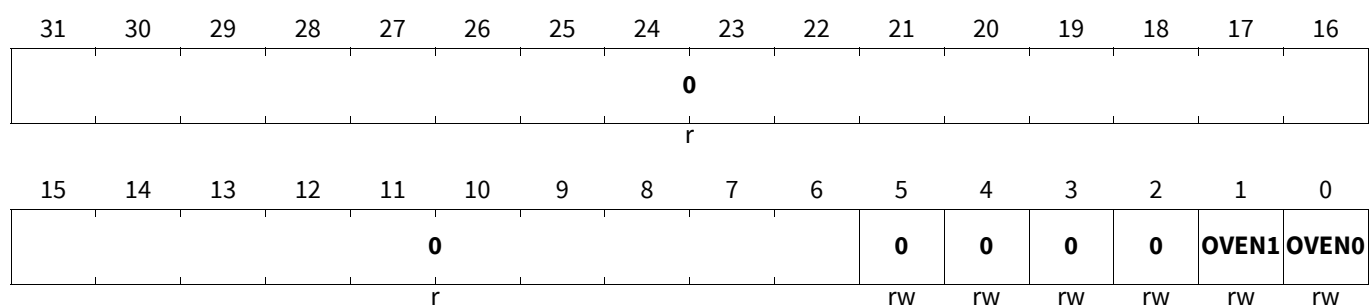
Overlay Enable Register

SCU_OVCENABLE

Overlay Enable Register

(01E0_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
OVEN0	0	rw	Overlay Enable 0 0 _B OVC is disabled on CPU0. All Overlay redirections are disabled regardless of the state of OVC0_RABRy.OVEN. 1 _B OVC is enabled on CPU0.

System Control Unit (SCU)

Field	Bits	Type	Description
OVEN1	1	rw	Overlay Enable 1 (If product has CPU1) 0 _B OVC is disabled on CPU1. All Overlay redirections are disabled regardless of the state of OVC1_RABRy.OVEN. 1 _B OVC is enabled on CPU1.
0	2, 3, 4, 5	rw	Reserved in this Product will be read as 0 , should be written as 0
0	31:6	r	Reserved Read/write 0.

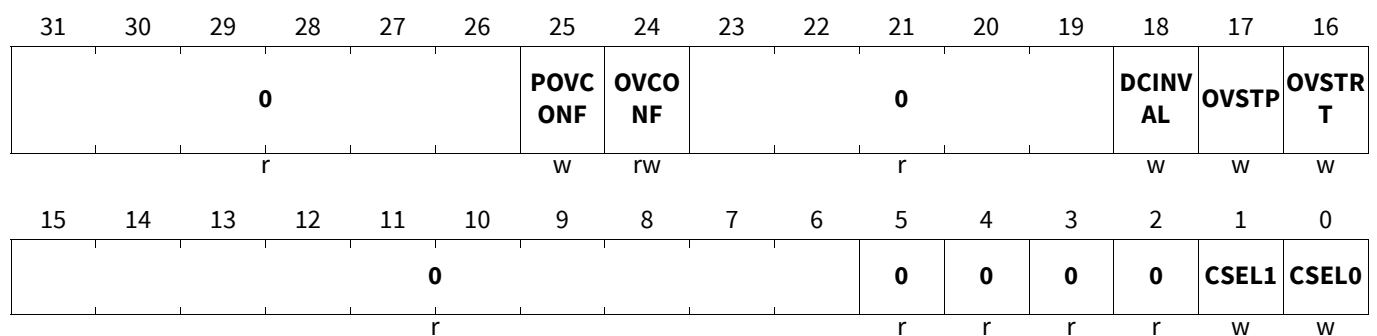
Overlay Control Register

SCU_OVCCON

Overlay Control Register

(01E4_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
CSEL0	0	w	CPU Select 0 Return 0 if read. 0 _B CPU0 not affected, 1 _B Action selected by OVSTRT, OVSTP, DCINVAL bits, set by the same register write access, is applied to CPU0.
CSEL1	1	w	CPU Select 1 (If product has CPU1) Return 0 if read. 0 _B CPU1 not affected, 1 _B Action selected by OVSTRT, OVSTP, DCINVAL bits, set by the same register write access, is applied to CPU1.
OVSTRT	16	w	Overlay Start CPUs which are not selected are not affected. No action is taken if OVSTP is also set. Return 0 if read. 0 _B No action 1 _B For each CPU selected with CSEL, all the blocks selected with OVCx_OSEL will be activated. In the selected CPUs all the blocks deselected with OVCx_OSEL will be deactivated.

System Control Unit (SCU)

Field	Bits	Type	Description
OVSTP	17	w	Overlay Stop CPUs which are not selected are not affected No action is taken if OVSTRT is also set. Return 0 if read. 0 _B No action 1 _B For CPUs selected with CSEL, all the overlay blocks are deactivated. OVCx_RABRy.OVEN bits are cleared.
DCINVAL	18	w	Data Cache Invalidate No function in devices without data cache in CPU. Data Cache is affected only in the CPUs selected with CSEL. Return 0 if read. 0 _B No action 1 _B Data Cache Lines in DMI are invalidated ¹⁾
OVCONF	24	rw	Overlay Configured Overlay configured status bit This bit may be used as handshake bit between a debug device (via JTAG interface and Cerberus) and CPU(s). 0 _B Overlay is not configured or it has been already started 1 _B Overlay block control registers are configured and ready for overlay start
POVCONF	25	w	Write Protection for OVCONF This bit enables OVCONF write during OVCCON write. Return 0 if read. 0 _B OVCONF remains unchanged. 1 _B OVCONF can be changed with write access to register OVCCON
0	2, 3, 4, 5, 15:6, 23:19, 31:26	r	Reserved in this Product Return 0 if read.

1) Dirty (modified) cache lines are not effected by this operation. If data cache contains modified data, it is not invalidated, and has to be written-back and invalidated by the user. Therefore, it is highly recommended to either: access overlaid data in read-only mode, or use only non-cached access.

System Control Unit (SCU)

Reset Status Register

SCU_RSTSTAT

Reset Status Register

(0050_H)Reset Value: [Table 41](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	LBTER M	LBPO RST	STBYR	HSMA	HSMS	SWD	EVR33	EVRC	R22	R21	CB3	CB1	CB0	0	PORS T
r	rh	rh	rh	rh	rh	rh	rh	rh	rX	rX	rh	rh	rh	r	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		0			0	0	0	0	STM1	STM0	SW	SMU	0	ESR1	ESR0
		r			r	r	r	r	rh	rh	rh	rh	r	rh	rh

Field	Bits	Type	Description
ESR0	0	rh	Reset Request Trigger Reset Status for ESR0 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
ESR1	1	rh	Reset Request Trigger Reset Status for ESR1 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
SMU	3	rh	Reset Request Trigger Reset Status for SMU (See SMU section for SMU trigger sources, including Watchdog Timers) 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
SW	4	rh	Reset Request Trigger Reset Status for SW 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
STM0	5	rh	Reset Request Trigger Reset Status for STM0 Compare Match 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
STM1	6	rh	Reset Request Trigger Reset Status for STM1 Compare Match (If Product has STM1) 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
PORST	16	rh	Reset Request Trigger Reset Status for PORST This bit is also set if the bits CB0, CB1, and CB3 are set in parallel. 0 _B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1 _B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
CB0	18	rh	Reset Request Trigger Reset Status for Cerberus System Reset 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger

System Control Unit (SCU)

Field	Bits	Type	Description
CB1	19	rh	Reset Request Trigger Reset Status for Cerberus Debug Reset 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
CB3	20	rh	Reset Request Trigger Reset Status for Cerberus Application Reset 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
R21	21	rX	Reserved - 0 Read as 0; should be written with 0.
R22	22	rX	Reserved - 0 Read as 0; should be written with 0.
EVRC	23	rh	Reset Request Trigger Reset Status for EVRC 0 _B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1 _B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
EVR33	24	rh	Reset Request Trigger Reset Status for EVR33 0 _B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1 _B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
SWD	25	rh	Reset Request Trigger Reset Status for Supply Watchdog (SWD) The Supply Watchdog trigger is described in Power Management Controller “Supply Monitoring” chapter 0 _B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1 _B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
HSMS	26	rh	Reset Request Trigger Reset Status for HSM System Reset (HSM S) 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
HSMA	27	rh	Reset Request Trigger Reset Status for HSM Application Reset (HSM A) 0 _B The last reset was not requested by this reset trigger 1 _B The last reset was requested by this reset trigger
STBYR	28	rh	Reset Request Trigger Reset Status for Standby Regulator Watchdog (STBYR) 0 _B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1 _B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)

System Control Unit (SCU)

Field	Bits	Type	Description
LBPORST	29	rh	<p>LBIST termination due to PORST This bitfield indicates if the LBIST was early terminated due to the occurrence of a Power On Reset. If the status of this bitfield is 0, the application must still check the LBTERM to check if the LBIST was terminated properly. This bitfield is cleared when the RSTCON2.CLRC is set.</p> <p>0_B LBIST was not terminated early due to a Power On Reset 1_B LBIST early termination due to the occurrence of Power On Reset</p>
LBTERM	30	rh	<p>LBIST was properly terminated This bitfield indicates if the LBIST was terminated properly. This bitfield is cleared when the RSTCON2.CLRC is set.</p> <p>0_B LBIST was not terminated properly 1_B LBIST was terminated properly</p>
0	2, 7, 8, 9, 10, 15:11, 17, 31	r	<p>Reserved Read as 0; should be written with 0.</p>

Table 41 Reset Values of **SCU_RSTSTAT**

Reset Type	Reset Value	Note
Cold PowerOn Reset	0XX1 0000 _H	RSTSTAT
Cold PowerOn Reset	1001 0000 _H	RSTSTAT (Triggered by LVD Reset)

Reset Configuration Register

SCU_RSTCON

Reset Configuration Register

(0058_H)

Reset Value: **Table 42**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				0						0		0		0	
				rw						rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	STM1	STM0	SW	SMU	0	ESR1	ESR0								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

System Control Unit (SCU)

Field	Bits	Type	Description
ESR0	1:0	rw	<p>ESR0 Reset Request Trigger Reset Configuration</p> <p>This bit field defines which reset is generated by a reset request trigger from ESR0 reset.</p> <p>00_B No reset is generated for a trigger of ESR0</p> <p>01_B A System Reset is generated for a trigger of ESR0 reset</p> <p>10_B An Application Reset is generated for a trigger of ESR0 reset</p> <p>11_B Reserved, do not use this combination</p>
ESR1	3:2	rw	<p>ESR1 Reset Request Trigger Reset Configuration</p> <p>This bit field defines which reset is generated by a reset request trigger from ESR1 reset.</p> <p>00_B No reset is generated for a trigger of ESR1</p> <p>01_B A System Reset is generated for a trigger of ESR1 reset</p> <p>10_B An Application Reset is generated for a trigger of ESR1 reset</p> <p>11_B Reserved, do not use this combination</p>
SMU	7:6	rw	<p>SMU Reset Request Trigger Reset Configuration</p> <p>This bit field defines which reset is generated by a reset request trigger from SMU reset.</p> <p>00_B No reset is generated for a trigger of SMU</p> <p>01_B A System Reset is generated for a trigger of SMU reset</p> <p>10_B An Application Reset is generated for a trigger of SMU reset</p> <p>11_B Reserved, do not use this combination</p>
SW	9:8	rw	<p>SW Reset Request Trigger Reset Configuration</p> <p>This bit field defines which reset is generated by a reset request trigger from software reset.</p> <p>00_B No reset is generated for a trigger of software reset</p> <p>01_B A System Reset is generated for a trigger of Software reset</p> <p>10_B An Application Reset is generated for a trigger of Software reset</p> <p>11_B Reserved, do not use this combination</p>
STM0	11:10	rw	<p>STM0 Reset Request Trigger Reset Configuration</p> <p>This bit field defines which reset is generated by a reset request trigger from STM0 compare match reset.</p> <p>00_B No reset is generated for an STM0 trigger</p> <p>01_B A System Reset is generated for a trigger of STM0 reset</p> <p>10_B An Application Reset is generated for a trigger of STM0 reset</p> <p>11_B Reserved, do not use this combination</p>
STM1	13:12	rw	<p>STM1 Reset Request Trigger Reset Configuration (If Product has STM1)</p> <p>This bit field defines which reset is generated by a reset request trigger from STM1 compare match reset.</p> <p>00_B No reset is generated for a trigger of STM1</p> <p>01_B A System Reset is generated for a trigger of STM1 reset</p> <p>10_B An Application Reset is generated for a trigger of STM1 reset</p> <p>11_B Reserved, do not use this combination</p>

System Control Unit (SCU)

Field	Bits	Type	Description
0	5:4, 15:14, 17:16, 19:18, 21:20, 31:22	rw	Reserved Should be written with 0.

Table 42 Reset Values of **SCU_RSTCON**

Reset Type	Reset Value	Note
PowerOn Reset	0000 0282 _H	RSTCON

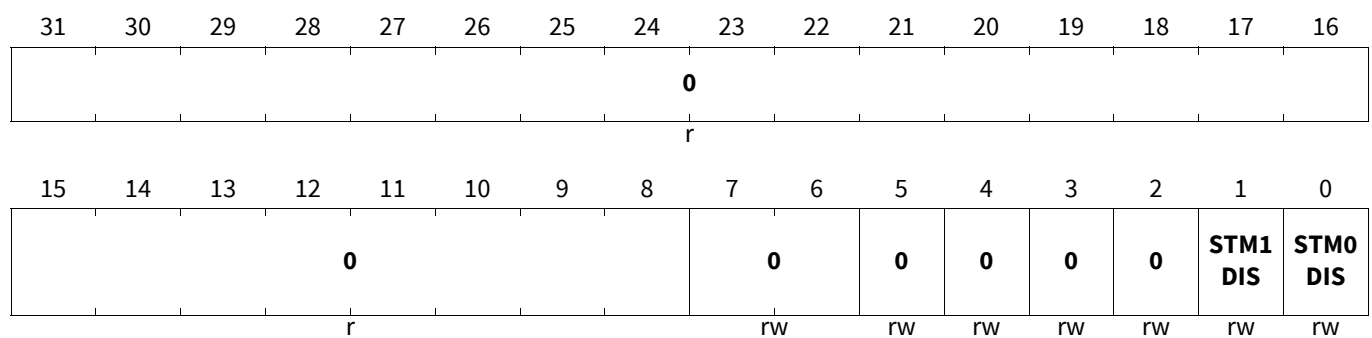
Application Reset Disable Register

SCU_ARSTDIS

Application Reset Disable Register

(005C_H)

PowerOn Reset Value: 0000 0000_H



Field	Bits	Type	Description
STM0DIS	0	rw	STM0 Disable Reset This bit field defines if an Application Reset leads to an reset for the STM0. 0 _B An Application Reset resets the STM0 1 _B An Application Reset has no effect for the STM0
STM1DIS	1	rw	STM1 Disable Reset This bit field defines if an Application Reset leads to an reset for the STM1. 0 _B An Application Reset resets the STM1 1 _B An Application Reset has no effect for the STM1
0	2, 3, 4, 5, 7:6	rw	Reserved Should be written with 0.
0	31:8	r	Reserved Read as 0; should be written with 0.

System Control Unit (SCU)

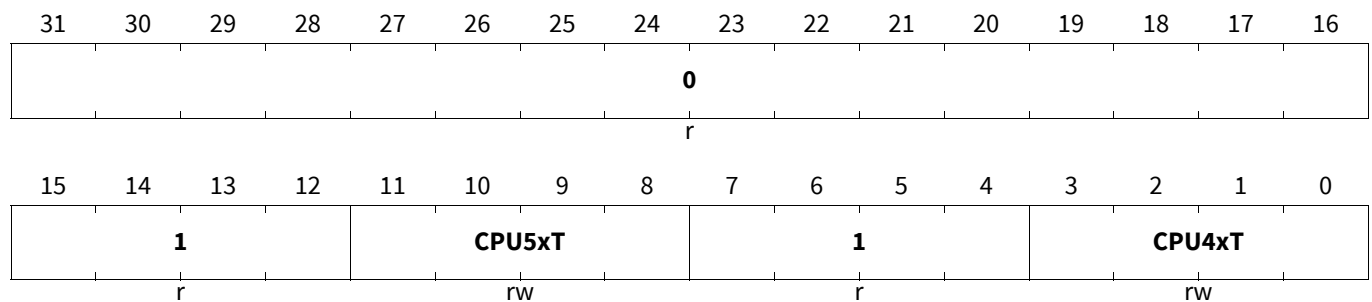
Trap Disable Register 1

SCU_TRAPDIS1

Trap Disable Register 1

(0120_H)

Application Reset Value: 0000 FFFF_H



Field	Bits	Type	Description
CPU4xT	3:0	rw	Reserved in this product
CPU5xT	11:8	rw	Reserved in this product
1	7:4, 15:12	r	Reserved Must only be written with one. Read as one.
0	31:16	r	Reserved Read as zero

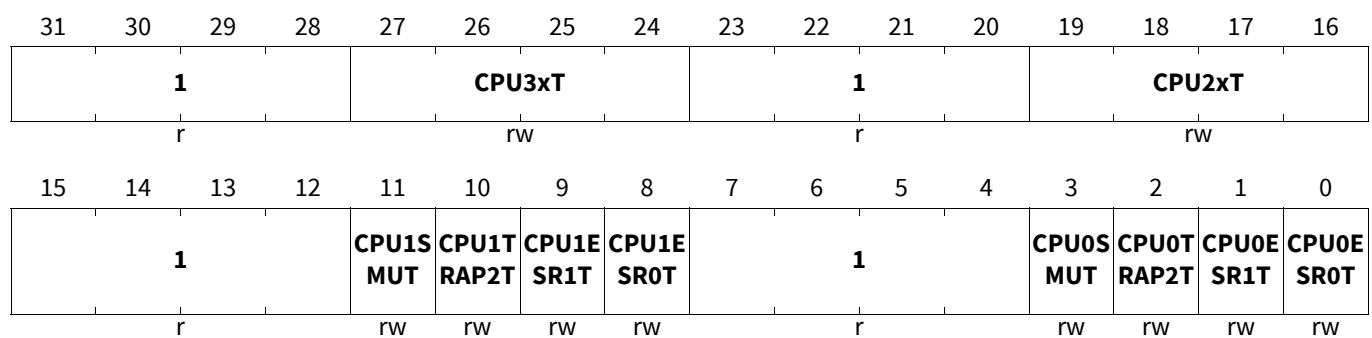
Trap Disable Register 0

SCU_TRAPDIS0

Trap Disable Register 0

(0130_H)

Application Reset Value: FFFF FFFF_H



Field	Bits	Type	Description
CPU0ESR0T	0	rw	Disable Trap Request ESR0T on CPU0 0 _B A CPU0 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU0ESR1T	1	rw	Disable Trap Request ESR1T on CPU0 0 _B A CPU0 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU0TRAP2T	2	rw	Disable Trap Request TRAP2T on CPU0 0 _B A CPU0 trap request can be generated for this source 1 _B No trap request can be generated for this source

System Control Unit (SCU)

Field	Bits	Type	Description
CPU0SMUT	3	rw	Disable Trap Request SMUT on CPU0 0 _B A CPU0 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU1ESR0T	8	rw	Disable Trap Request ESR0T on CPU1 (If product has CPU1) 0 _B A CPU1 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU1ESR1T	9	rw	Disable Trap Request ESR1T on CPU1 (If product has CPU1) 0 _B A CPU1 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU1TRAP2T	10	rw	Disable Trap Request TRAP2T on CPU1 (If product has CPU1) 0 _B A CPU1 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU1SMUT	11	rw	Disable Trap Request SMUT on CPU1 (If product has CPU1) 0 _B A CPU1 trap request can be generated for this source 1 _B No trap request can be generated for this source
CPU2xT	19:16	rw	Reserved in this product
CPU3xT	27:24	rw	Reserved in this product
1	7:4, 15:12, 23:20, 31:28	r	Reserved Must only be written with one. Read as one.

CCU Clock Control Register 2

SCU_CCUCON2

CCU Clock Control Register 2

(0040_H)

System Reset Value: 0700 0101_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCK		0			1	ERAYP ERON	1				0				
rh		rw			rw	rw	rw				rw				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		CLKSELASCL INS			ASCLINSDIV				0				ASCLINFDIV		
rw		rw			rw				rw				rw		

System Control Unit (SCU)

Field	Bits	Type	Description
ASCLINFDIV	3:0	rw	<p>ASCLIN Fast Divider Reload Value</p> <p>The resulting ASCLIN frequency is configured to $f_{ASCLINF} = f_{source2} / ASCLINFDIV$ for the allowed configurations. For ASCLINFDIV = 0000_B the clock is shut off. $f_{source2}$ could be configured either to f_{PLL2} (CLKSEL = 01_B) or f_{BACK} (CLKSEL = 00_B)</p> <p>0_H $f_{ASCLINF}$ is stopped</p> <p>1_H $f_{ASCLINF} = f_{source2}$</p> <p>2_H $f_{ASCLINF} = f_{source2}/2$</p> <p>3_H $f_{ASCLINF} = f_{source2}/3$</p> <p>4_H $f_{ASCLINF} = f_{source2}/4$</p> <p>5_H $f_{ASCLINF} = f_{source2}/5$</p> <p>6_H $f_{ASCLINF} = f_{source2}/6$</p> <p>7_H Reserved, do not use this combination</p> <p>8_H $f_{ASCLINF} = f_{source2}/8$</p> <p>9_H Reserved, do not use this combination</p> <p>A_H $f_{ASCLINF} = f_{source2}/10$</p> <p>B_H Reserved, do not use this combination</p> <p>C_H $f_{ASCLINF} = f_{source2}/12$</p> <p>D_H Reserved, do not use this combination</p> <p>E_H Reserved, do not use this combination</p> <p>F_H $f_{ASCLINF} = f_{source2}/15$</p>
ASCLINSDIV	11:8	rw	<p>ASCLIN Slow Divider Reload Value</p> <p>The resulting ASCLIN frequency is configured to $f_{ASCLINSI} = f_{source1} / ASCLINSDIV$ for the allowed configurations. For ASCLINSDIV = 0000_B the clock is shut off. $f_{source1}$ could be configured either to f_{PLL1} (CLKSEL = 01_B) or f_{BACK} (CLKSEL = 00_B)</p> <p>0_H $f_{ASCLINSI}$ is stopped</p> <p>1_H $f_{ASCLINSI} = f_{source1}$</p> <p>2_H $f_{ASCLINSI} = f_{source1}/2$</p> <p>3_H $f_{ASCLINSI} = f_{source1}/3$</p> <p>4_H $f_{ASCLINSI} = f_{source1}/4$</p> <p>5_H $f_{ASCLINSI} = f_{source1}/5$</p> <p>6_H $f_{ASCLINSI} = f_{source1}/6$</p> <p>7_H Reserved, do not use this combination</p> <p>8_H $f_{ASCLINSI} = f_{source1}/8$</p> <p>9_H Reserved, do not use this combination</p> <p>A_H $f_{ASCLINSI} = f_{source1}/10$</p> <p>B_H Reserved, do not use this combination</p> <p>C_H $f_{ASCLINSI} = f_{source1}/12$</p> <p>D_H Reserved, do not use this combination</p> <p>E_H Reserved, do not use this combination</p> <p>F_H $f_{ASCLINSI} = f_{source1}/15$</p>

System Control Unit (SCU)

Field	Bits	Type	Description
CLKSELASCLINS	13:12	rw	<p>Clock Selection for ASCLINS This bit field defines the clock source that is used for the clock generation of $f_{ASCLINS}$.</p> <p><i>Note:</i> For switching between two non-zero configurations the following sequence has to be applied: First step is to switch to 00_B. Second step is to switch to the new target configuration.</p> <p>00_B $f_{ASCLINS}$ clock is stopped 01_B $f_{ASCLINSI}$ is used as clock $f_{ASCLINS}$ 10_B f_{OSCO} is used as clock $f_{ASCLINS}$ 11_B Reserved, do not use this combination</p>
ERAYPERON	25	rw	<p>Power Safe SwitchOff for ERAY Clock This bit is used to control the ERAY peripheral clock f_{ERAY} for power saving purposes if the logic is not used by the application.</p> <p>0_B f_{ERAY} is stopped 1_B $f_{ERAY} = f_{source1} / 2$</p>
LCK	31	rh	<p>Lock Status This bit indicates if the register can be updated with a new value or if the register is locked and a write action from the bus side has no effect.</p> <p><i>Note:</i> The lock bit is set when at least one bit field is changed, and released when this change is executed.</p> <p>0_B The register is unlocked and can be updated 1_B The register is locked and can not be updated</p>
0	7:4, 23:14, 30:27	rw	<p>Reserved Should be written with 0.</p>
1	24, 26	rw	<p>Reserved Can be written either 0/1, not connected to HW.</p>

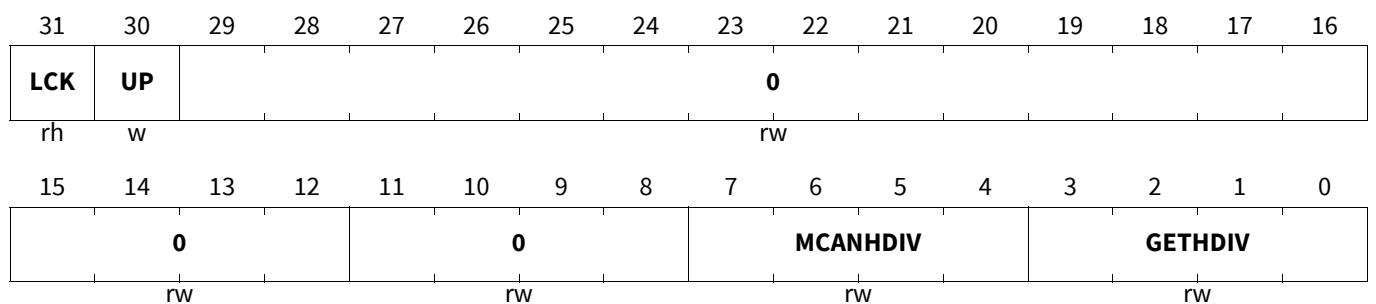
CCU Clock Control Register 5

SCU_CCUCON5

CCU Clock Control Register 5

(004C_H)

System Reset Value: 0000 0030_H



System Control Unit (SCU)

Field	Bits	Type	Description
GETHDIV	3:0	rw	<p>GETH Divider Reload Value</p> <p>The resulting GETH frequency is configured to $f_{GETH} = f_{source0} / GETHDIV$ for the allowed configurations. For $GETHDIV = 0000_B$ the clock is shut off. $f_{source0}$ could be configured either to f_{PLL0} ($CLKSEL = 01_B$) or f_{BACK} ($CLKSEL = 00_B$)</p> <p><i>Note: GETHDIV must be enabled (!=0) during an application reset to allow firmware related installation tasks.</i></p> <p>0_H f_{GETH} is stopped 1_H $f_{GETH} = f_{source0}$ 2_H $f_{GETH} = f_{source0}/2$ 3_H $f_{GETH} = f_{source0}/3$ 4_H $f_{GETH} = f_{source0}/4$ 5_H Reserved, do not use this combination 6_H Reserved, do not use this combination 7_H Reserved, do not use this combination 8_H Reserved, do not use this combination 9_H Reserved, do not use this combination A_H Reserved, do not use this combination B_H Reserved, do not use this combination C_H Reserved, do not use this combination ... E_H Reserved, do not use this combination F_H Reserved, do not use this combination</p>
MCANHDIV	7:4	rw	<p>MCANH Divider Reload Value</p> <p>The resulting MCANH frequency is configured to $f_{MCANH} = f_{SOURCE0} / MCANHDIV$ for the allowed configurations. For $MCANHDIV = 0000_B$ the clock is shut off.</p> <p>0_H f_{MCANH} is stopped 1_H $f_{MCANH} = f_{SOURCE0}$ 2_H $f_{MCANH} = f_{SOURCE0}/2$ 3_H $f_{MCANH} = f_{SOURCE0}/3$ 4_H $f_{MCANH} = f_{SOURCE0}/4$ 5_H $f_{MCANH} = f_{SOURCE0}/5$ 6_H $f_{MCANH} = f_{SOURCE0}/6$ 7_H Reserved, do not use this combination 8_H $f_{MCANH} = f_{SOURCE0}/8$ 9_H Reserved, do not use this combination A_H $f_{MCANH} = f_{SOURCE0}/10$ B_H Reserved, do not use this combination C_H $f_{MCANH} = f_{SOURCE0}/12$ D_H Reserved, do not use this combination E_H Reserved, do not use this combination F_H $f_{MCANH} = f_{SOURCE0}/15$</p>

System Control Unit (SCU)

Field	Bits	Type	Description
UP	30	w	Update Request Setting this bit will request an update for CCUCON0 and CCUCON5. Only one UP bit must be set either CCUCON0 or CCUCON5. This bit always reads as zero. 0 _B No action 1 _B A new complete parameter set is transferred to the CCU defined by register CCUCON0 and CCUCON5.
LCK	31	rh	Lock Status This bit indicates if the register can be updated with a new value or if the register is locked and a write action from the bus side has no effect. <i>Note: The lock bit is set when an update of CCUCON0/5 has been requested, and released when the update is complete.</i> 0 _B The register is unlocked and can be updated 1 _B The register is locked and can not be updated
0	11:8, 29:12	rw	Reserved Should be written with 0.

9.4 Connectivity

Table 43 Connections of SCU

Interface Signals	connects		Description
SCU:CBS_ENDINIT_DIS	from	CBS:ocds_oc(3)	Watchdog ENDINIT disable from Cerberus
SCU:CBS_WDT_SUSP	from	CBS:ocds_wdtsus	Watchdog suspend from Cerberus
SCU:EMGSTOP_PORT_A	from	SMU:FSPSCU	Emergency stop Port Pin A input request
SCU:EMGSTOP_PORT_B	from	P21.2:IN	Emergency stop Port Pin B input request
SCU:ESR0_PORT_IN	from	TC36x:ESR0	ESR0 Port Pin input - can be used to trigger a reset or an NMI
SCU:ESR1_PORT_IN	from	TC36x:ESR1	ESR1 Port Pin input - can be used to trigger a reset or an NMI
SCU:E_IOUT(0)	to	EVADC:G0REQTRH EVADC:G8REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(1)	to	EVADC:G1REQTRH EVADC:G9REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(2)	to	EVADC:G2REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(3)	to	EVADC:G3REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(3:2)	to	CAN0:ECTT(4:3)	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)

System Control Unit (SCU)

Table 43 Connections of SCU (cont'd)

Interface Signals	connects		Description
SCU:E_IOUT(4)	to	CAN0:TTCPT_TRIG(4)	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_PDOUT(0)	to	CCU60:CTRAPD	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		CCU60:T12HRH	
		EDSADC:ITR0G	
		EVADC:G0REQGTM	
		EVADC:G8REQGTM	
		GTM:TIM0_IN0(12)	
SCU:E_PDOUT(1)	to	CCU61:CTRAPD	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		CCU61:T12HRH	
		EDSADC:ITR1G	
		EVADC:G1REQGTM	
		EVADC:G9REQGTM	
		GTM:TIM0_IN1(12)	
SCU:E_PDOUT(2)	to	EDSADC:ITR2G	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EVADC:G2REQGTM	
		GTM:TIM0_IN2(12)	
SCU:E_PDOUT(3)	to	EVADC:G3REQGTM	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		GTM:TIM0_IN3(12)	
		EDSADC:ITR3G	
SCU:E_PDOUT(3:0)	to	ERAY0:STPWT(3:0)	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
SCU:E_PDOUT(4)	to	CCU60:CC62IND	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		GPT120:T3INC	
		GTM:TIM0_IN4(12)	
SCU:E_PDOUT(5)	to	CCU61:CC62IND	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		GTM:TIM0_IN5(12)	
SCU:E_PDOUT(6)	to	GPT120:CAPINB	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		GTM:TIM0_IN6(12)	
SCU:E_PDOUT(7)	to	GTM:TIM0_IN7(12)	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
SCU:E_REQ0(0)	from	P15.4:IN	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(1)	from	CCU60:COU60	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(2)	from	P10.7:IN	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(3)	from	MSC0:FCLP	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.

System Control Unit (SCU)

Table 43 Connections of SCU (cont'd)

Interface Signals	connects		Description
SCU:E_REQ1(0)	from	P14.3:IN	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(1)	from	CCU61:COU60	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(2)	from	P10.8:IN	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(3)	from	STM0:STMIR(0)	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(0)	from	P10.2:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(1)	from	P02.1:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(2)	from	P00.4:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(3)	from	ERAY0:MT	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(0)	from	P10.3:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(1)	from	P14.1:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(2)	from	P02.0:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(3)	from	STM1:STMIR(0)	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(0)	from	P33.7:IN	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(1)	from	GTM:SCU_TRIG(0)	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(2)	from	GPT120:T3OUT	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(3)	from	P15.5:IN	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(0)	from	P15.8:IN	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(1)	from	GTM:SCU_TRIG(1)	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(2)	from	GPT120:T6OUT	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(0)	from	P20.0:IN	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(1)	from	TC36x:ESR0	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.

System Control Unit (SCU)

Table 43 Connections of SCU (cont'd)

Interface Signals	connects		Description
SCU:E_REQ6(3)	from	P11.10:IN	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(0)	from	P20.9:IN	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(1)	from	TC36x:ESR1	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(2)	from	P15.1:IN	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:RST_REQ_STM(10)	from	HSM:SYSRST	Reset request from STMn (MSB is STM5 and LSB is STM0)
SCU:RST_REQ_STM(11)	from	HSM:APPRST	Reset request from STMn (MSB is STM5 and LSB is STM0)
SCU:SMU_EMGSTP_REQ	from	SMU:EMERGENCYSTOPREQ	Emergency stop request from SMU
SCU:SMU_TRAP_REQ	from	SMU:NMIREQ	TRAP request from the SMU
SCU:TRAP_CPU(0)	to	cpu_pfi_pfrwb_0:tc162p_nmi_trap	TRAP output to CPU _n (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(1)	to	cpu_pfi_pfrwb_1:tc162p_nmi_trap	TRAP output to CPU _n (MSB is CPU5 and LSB is CPU0)
SCU:ERU_INT(3:0)	to	INT:scu.ERU_INT(3:0)	SCU ERU Service Request x

9.5 Revision History

The following table contains the revision history of the SCU that is relevant for the TC36x device. For a complete revision history please address the family user manual.

This section only includes entries, respective to the Clock System, that are related to register updates. For a complete Clock System revision history please address the family user manual.

Table 44 Revision History

Reference	Change to Previous Version	Comment
V2.1.21		
	Revision History entries up to V2.1.20 removed.	
Page 26	Connectivity information updated.	
V2.1.22		
	Revision History entries up to V2.1.22 removed.	
Page 16	Cold PORST reset value changed from 1xx10000 to 0xx10000 in RSTSTAT register.	
Page 16	Additional cold_power_on_reset value “LVD Reset” added to RSTSTAT register.	
Page 1	LBIST Configuration MISR signature values updated.	
Page 10	LCLCON0 and LCLCON1: Cold PORST reset table values updated/corrected.	

System Control Unit (SCU)
Table 44 Revision History (cont'd)

Reference	Change to Previous Version	Comment
Page 26	Connection table fixed.	
V2.1.23		
	Revision History entries up to V2.1.21 removed.	
Page 26	Connectivity table updated due to update of Connexion DB.	
Page 1	LBISTCTRL register configuration corrected.	
Page 2, Page 10	LBISTCTRL0 removed from specific registers, see Family Spec instead.	
V2.1.24		
Page 10	Updated Cold PowerOn Reset Value of LCLCONx.	
Page 26	Updated connectivity table, no functional changes.	
V2.1.25		
-	No functional changes.	
V2.1.26		
-	No functional changes.	
V2.1.27		
	No functional changes.	

10 **Clocking System**

Device specific information about the clocking system is contained in the SCU chapter as both modules share a common bus interface.

Power Management System (PMS)**11 Power Management System (PMS)**

This chapter describes the Power Management System (PMS) Module of the TC36x.

11.1 TC36x Specific IP Configuration**Table 45 TC36x specific configuration of PMS**

Parameter	PMS
CFS value for the PMSWCR4 register	02000020 _H

Power Management System (PMS)

11.2 TC36x Specific Register Set

The PMS related SCU registers are specified in the SCU section of this appendix.

Table 46 Register Address Space - PMS

Module	Base Address	End Address	Note
(PMS)	F0240000 _H	F0241FFF _H	
PMS	F0248000 _H	F02481FF _H	FPI slave interface

Table 47 Register Overview - PMS (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_ID	Identification Register	0008 _H	U,SV	BE	Application Reset	See Family Spec
PMS_EVRSTAT	EVR Status Register	002C _H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRADCSTAT	EVR Primary ADC Status Register	0034 _H	U,SV	BE	LVD Reset	See Family Spec
PMS_EVRRSTCON	EVR Reset Control Register	003C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRRSTSTAT	EVR Reset Status Register	0044 _H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRTRIM	EVR Trim Control Register	004C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRTRIMSTAT	EVR Trim Status Register	0050 _H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONSTAT1	EVR Secondary ADC Status Register 1	0060 _H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONSTAT2	EVR Secondary ADC Status Register 2	0064 _H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONCTL	EVR Secondary Monitor Control Register	0068 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRMONFILTER	EVR Secondary Monitor Filter Register	0070 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec

Power Management System (PMS)

Table 47 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_PMSIEN	PMS Interrupt Enable Register	0074 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRUVMON	EVR Secondary Under-voltage Monitor Register	0078 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROVMON	EVR Secondary Over-voltage Monitor Register	007C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRUVMON 2	EVR Secondary Under-voltage Monitor Register 2	0080 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROVMON 2	EVR Secondary Over-voltage Monitor Register 2	0084 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_HSMUVMON	EVR Primary HSM Under-voltage Monitor Register	0088 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_HSMOVMON	EVR Primary HSM Over-voltage Monitor Register	008C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVR33CON	EVR33 Control Register	0090 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROSCCT RL	EVR Oscillator Control Register	00A0 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_PMSWCR0	Standby and Wake-up Control Register 0	00B4 _H	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR2	Standby and Wake-up Control Register 2	00B8 _H	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR3	Standby and Wake-up Control Register 3	00C0 _H	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR4	Standby and Wake-up Control Register 4	00C4 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_PMSWCR5	Standby and Wake-up Control Register 5	00C8 _H	U,SV	SV,SE,P	LVD Reset	See Family Spec

Power Management System (PMS)

Table 47 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_PMSWSTAT	Standby and Wake-up Status Register	00D4 _H	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWSTAT 2	Standby and Wake-up Status Register 2	00D8 _H	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWUTC NT	Standby WUT Counter Register	00DC _H	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWSTAT CLR	Standby and Wake-up Status Clear Register	00E8 _H	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_EVRSDSTAT 0	EVR SD Status Register 0	00FC _H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRSDCTRL 0	EVRC SD Control Register 0	0108 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 1	EVRC SD Control Register 1	010C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 2	EVRC SD Control Register 2	0110 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 3	EVRC SD Control Register 3	0114 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 4	EVRC SD Control Register 4	0118 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 5	EVRC SD Control Register 5	011C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 6	EVRC SD Control Register 6	0120 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 7	EVRC SD Control Register 7	0124 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 8	EVRC SD Control Register 8	0128 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec

Power Management System (PMS)

Table 47 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_EVRSDCTRL 9	EVRC SD Control Register 9	012C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 10	EVRC SD Control Register 10	0130 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL 11	EVRC SD Control Register 11	0134 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF0	EVRC SD Coefficient Register 0	0148 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF1	EVRC SD Coefficient Register 1	014C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF2	EVRC SD Coefficient Register 2	0150 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF3	EVRC SD Coefficient Register 3	0154 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF4	EVRC SD Coefficient Register 4	0158 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF5	EVRC SD Coefficient Register 5	015C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF6	EVRC SD Coefficient Register 6	0160 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF7	EVRC SD Coefficient Register 7	0164 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF8	EVRC SD Coefficient Register 8	0168 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOE FF9	EVRC SD Coefficient Register 9	016C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_AG2i_STDB Y (i=0-1)	Alarm Status Register	0188 _H +i* 4	U,SV	SV,SE,P	LVD Reset	See Family Spec

Power Management System (PMS)
Table 47 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_MONBISTS TAT	SMU_stdby BIST Status Register	0190 _H	U,SV	BE	See Family Spec	See Family Spec
PMS_MONBISTC TRL	SMU_stdby BIST Control Register	0198 _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_CMD_STDB Y	SMU_stdby Command Register	019C _H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_AG2iFSP_S TDBY (i=0-1)	SMU_stdby FSP Configuration Register	01A4 _H +i* 4	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_DTSSTAT	Die Temperature Sensor Status Register	01C0 _H	U,SV	BE	See Family Spec	See Family Spec
PMS_DTSLIM	Die Temperature Sensor Limit Register	01C8 _H	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSS	OCDS Trigger Set Select Register	01E0 _H	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSC0	OCDS Trigger Set Control 0 Register	01E4 _H	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSC1	OCDS Trigger Set Control 1 Register	01E8 _H	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_ACCEN1	Access Enable Register 1	01F8 _H	U,SV	SV,SE,32	Application Reset	See Family Spec
PMS_ACCEN0	Access Enable Register 0	01FC _H	U,SV	SV,SE,32	Application Reset	See Family Spec

11.3 TC36x Specific Registers

No deviations from the Family Spec

Power Management System (PMS)

11.4 Connectivity

Table 48 Connections of PMS

Interface Signals	connects		Description
PMS:DCDCSYNCO	to	P32.4:HWOUT(0) P32.2:ALT(6) P32.4:ALT(2)	DC-DC synchronization output
PMS:ESR0PORST	to	TC36x:ESR0	ESR0 control output during PORST activation
PMS:ESR0WKP	from	TC36x:ESR0	ESR0 pin input
PMS:ESR1WKP	from	TC36x:ESR1	ESR1 pin input
PMS:HWCFG1IN	from	TC36x:P14.5	HWCFG1 pin input
PMS:HWCFG2IN	from	TC36x:P14.2	HWCFG2 pin input
PMS:HWCFG4IN	from	TC36x:P10.5	HWCFG4 pin input
PMS:HWCFG5IN	from	TC36x:P10.6	HWCFG5 pin input
PMS:HWCFG6IN	from	TC36x:P14.4	HWCFG6 pin input
PMS:PINAWKP	from	TC36x:P14.1	PINA (P14.1) pin input
PMS:PINBWKP	from	TC36x:P33.12	PINB (P33.12) pin input
PMS:PORSTIN	from	TC36x:PORST	PORST pin input
PMS:PORSTOUT	to	TC36x:PORST	PORST pin output
PMS:TESTMODEIN	from	TC36x:P20.2	TESTMODE pin input
PMS:VDDMLVL	to	converter_0:converter_low_supp	VDDM monitor signal to Converter
PMS:VGATE1N	to	TC36x:CTRL1V3N TC36x:CTRL1V3N	DCDC N ch. MOSFET gate driver output
PMS:VGATE1P	to	TC36x:CTRL1V3P TC36x:CTRL1V3P	DCDC P ch. MOSFET gate driver output

11.5 Revision History

Table 49 Revision History

Reference	Change to Previous Version	Comment
V2.2.28		
	No changes.	
V2.2.29		
-	No functional changes.	
V2.2.30		
Page 2	Register “PMS_EVR33CON” now visible to the customer.	
V2.2.31		
-	No functional changes.	
V2.2.32		
-	No functional changes.	

Power Management System (PMS)**Table 49** Revision History (cont'd)

Reference	Change to Previous Version	Comment
V2.2.33		
-	No functional changes.	
V2.2.34		
-	No functional changes.	

12 Power Management System for Low-End (PMSLE)

This device doesn't contain a PMSLE module.

Memory Test Unit (MTU)**13 Memory Test Unit (MTU)**

For the generic description of the Memory Test Unit (MTU) and the SRAM Support Hardware (SSH), please refer to the platform chapter.

13.1 TC36x Specific IP Configuration

There is no device specific IP configuration. MTU+SSH is generic across all derivatives in the platforms. Only the SSH instances vary.

13.2 Handling of Large DSPR SRAMs

On this device, the CPU0 and CPU1 have large DSPR SRAMs. Therefore, there are two SSHs to support these SRAMs. These are named as CPUxDMEM and CPUxDMEM1 (x=0,1).

Logically, these 2 SSHs behave as separate SSHs, with their own MEMTEST_EN bits, Alarms to the SMU, error status flags etc. However special handling is required to enter test mode for these SSHs.

When running a Non-Destructive-test, only one of the DMEM SSHs shall be enabled at a time. This is because the ECC encoder and decoder are shared between the two SSHs.

However, as long as destructive tests or SSH register accesses are to be performed, then both SSHs can be enabled together.

Please note that when one of the DMEM SSH is enabled, the complete DSPR+DCACHE is unavailable for functional access. This is due to internal interleaving of the logical address space.

Although the DCACHE is also split equally between the two SRAMs, the entire cache has to be mapped at once to the system address map. Hence only a single bit is provided in the MTU_MEMMAP register for the entire DMEM.

The partial-erase (i.e. erasing the Cache area; refer the family spec) is triggered separately when each MEMTEST_EN bit is set.

The MEMMAP bit triggers the partial erase in both SSHs at the same time.

If both the SSHs are enabled / disabled at the same time, the software should check either the bits in the MTU_MEMSTAT register, or ensure that the EN bits for both the SSHs are set / cleared in the MEMTEST registers to ensure that the partial-erase has completed.

Memory Test Unit (MTU)

13.3 TC36x Specific Register Set

Register Address Space Table

Table 50 Register Address Space - MTU

Module	Base Address	End Address	Note
MTU	F0060000 _H	F006FFFF _H	FPI slave interface

Register Overview Table

Table 51 Register Overview - MTU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
MTU_CLC	Clock Control Register	0000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
MTU_ID	Identification Register	0008 _H	U,SV	BE	Application Reset	See Family Spec
MTU_MEMTESTi (i=0-2)	Memory MBIST Enable Register i	0010 _H +i* 4	U,SV	SV,SE,P	Application Reset	3
MTU_MEMMAP	Memory Mapping Enable Register	001C _H	U,SV	SV,SE,P	Application Reset	8
MTU_MEMSTATi (i=0-2)	Memory Status Register i	0038 _H +i* 4	U,SV	BE	Application Reset	10
MTU_MEMDONEi (i=0-2)	Memory Test Done Status Register i	0050 _H +i* 4	U,SV	BE	Application Reset	13
MTU_MEMFDAi (i=0-2)	Memory Test FDA Status Register i	0060 _H +i* 4	U,SV	BE	Application Reset	17
MTU_ACCEN1	Access Enable Register 1	00F8 _H	U,SV	BE	Application Reset	See Family Spec
MTU_ACCEN0	Access Enable Register 0	00FC _H	U,SV	SV,SE	Application Reset	See Family Spec
MTU_MCi_CONFI G0 (i=0-95)	Configuration Registers	1000 _H +i* 100 _H	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_CONFI G1 (i=0-95)	Configuration Register 1	1002 _H +i* 100 _H	U,SV,16	U,SV,P,16	Application Reset	See Family Spec

Memory Test Unit (MTU)

Table 51 Register Overview - MTU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
MTU_MCi_MCON TROL (i=0-95)	MBIST Control Register	1004 _H +i* 100 _H	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_MSTA TUS (i=0-95)	Status Register	1006 _H +i* 100 _H	U,SV,16	BE	Application Reset	See Family Spec
MTU_MCi_RANG E (i=0-95)	Range Register, single address mode	1008 _H +i* 100 _H	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_REVID (i=0-95)	Revision ID Register	100C _H +i* 100 _H	U,SV,16	BE	Application Reset	See Family Spec
MTU_MCi_ECCS (i=0-95)	ECC Safety Register	100E _H +i* 100 _H	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_ECCD (i=0-95)	Memory ECC Detection Register	1010 _H +i* 100 _H	U,SV,16	SV,P,16	See Family Spec	See Family Spec
MTU_MCi_ETRRx (i=0-95;x=0-4)	Error Tracking Register x	1012 _H +i* 100 _H +x* 2	U,SV,16	BE	PowerOn Reset	See Family Spec
MTU_MCi_RDBFL y (i=0-95;y=0-66)	Read Data and Bit Flip Register y	1060 _H +i* 100 _H +y* 2	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_ALMS RCS (i=0-95)	Alarm Sources Configuration Register	10EE _H +i* 100 _H	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_FAULT STS (i=0-95)	SSH Safety Faults Status Register	10F0 _H +i* 100 _H	U,SV,16	SV,SE,P,16	PowerOn Reset	See Family Spec
MTU_MCi_ERRIN FOx (i=0-95;x=0-4)	Error Information Register x	10F2 _H +i* 100 _H +x* 2	U,SV,16	BE	PowerOn Reset	See Family Spec

13.4 TC36x Specific Registers

13.4.1 MEMTEST Implementation

Memory MBIST Enable Register i

The memory test register MEMTEST holds CPU configurable select bits for the various SSH instances. See the product specific appendix for mapping of memory controller numbers.

Memory Test Unit (MTU)

MTU_MEMTESTi (i=0)

Memory MBIST Enable Register i

(0010_H+i*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	RES19	RES18	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	CPU1_DLMU_STBY_EN	CPU1_PTAG_EN	CPU1_PMEM_EN	CPU1_DTAG_EN	CPU1_DMEM_EN	CPU0_DLMU_STBY_EN	CPU0_PTAG_EN	CPU0_PMEM_EN	CPU0_DTAG_EN	CPU0_DMEM_EN
r	r	r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CPU0_DMEM_EN	0	rwh	CPU0 DMEM SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
RESx (x=10-31)	x	r	Reserved Reserved. Shall be written with zero.
CPU0_DTAG_EN	1	rwh	CPU0 DTAG SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU0_PMEM_EN	2	rwh	CPU0 PMEM SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU0_PTAG_EN	3	rwh	CPU0 PTAG SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU0_DLMU_STBY_EN	4	rwh	CPU0 STANDBY DLMU SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU1_DMEM_EN	5	rwh	CPU1 DMEM SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU1_DTAG_EN	6	rwh	CPU1 DTAG SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU1_PMEM_EN	7	rwh	CPU1 PMEM SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
CPU1_PTAG_EN	8	rwh	CPU1 PTAG SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled

Memory Test Unit (MTU)

Field	Bits	Type	Description
CPU1_DLMU_STBY_EN	9	rwh	CPU1 STANDBY DLMU SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled

MTU_MEMTESTi (i=1)

Memory MBIST Enable Register i (0010_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN_20_EN	MCAN_10_EN	RES29	GTM_DPLL2_EN	GTM_DPLL1_BC_EN	GTM_DPLL1_A_EN	GTM_MCS1F_AST_EN	RES24	GTM_MCS0F_AST_EN	RES22	GTM_FIFO_EN	RES20	RES19	RES18	RES17	RES16
rwh	rwh	r	rwh	rwh	rwh	rwh	r	rwh	r	rwh	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	SADMA_EN	R8	RES7	RES6	RES5	RES4	CPU1_DMEM1_EN	CPU0_DMEM1_EN	RES1	RES0
r	r	r	r	r	r	rwh	rwh	r	r	r	r	rwh	rwh	r	r

Field	Bits	Type	Description
RESx (x=0-1,4-7,10-20,22,24,29)	x	r	Reserved Reserved. Shall be written with zero.
CPU0_DMEM1_EN	2	rwh	CPU0 DMEM1 SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled ¹⁾ .
CPU1_DMEM1_EN	3	rwh	CPU1 DMEM1 SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled ²⁾ .
R8	8	rwh	Reserved - Res Reserved. Not used in this product. Shall be written with zero.
SADMA_EN	9	rwh	Safety DMA SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
GTM_FIFO_EN	21	rwh	GTM FIFO memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
GTM_MCS0FAST_EN	23	rwh	GTM MCS0 FAST memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
GTM_MCS1FAST_EN	25	rwh	GTM MCS1 FAST memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled

Memory Test Unit (MTU)

Field	Bits	Type	Description
GTM_DPLL1A_EN	26	rwh	GTM DPLL1A memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
GTM_DPLL1B_C_EN	27	rwh	GTM DPLL1BC memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
GTM_DPLL2_EN	28	rwh	GTM DPLL2 memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
MCAN10_EN	30	rwh	MCAN10 memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
MCAN20_EN	31	rwh	MCAN20 memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled

- 1) Please refer to separate section related to handling of the large DMEM on this device.
- 2) Please refer to separate section related to handling of the large DMEM on this device.

MTU_MEMTEST_i (i=2)

Memory MBIST Enable Register i

(0010_H+i*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	GIGET_H_TX_EN	GIGET_H_RX_EN	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	rwh	rwh	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	SCR_R_AMINT_EN	SCR_X_RAM_EN	R12	R11	R10	R9	R8	RES7	ERAY_MBF0_EN	RES5	ERAY_TBF_I_BF0_EN	RES3	ERAY_OBF0_EN	PSI5_EN	RES0
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	r	rwh	r	rwh	rwh	r

Field	Bits	Type	Description
RES_x (x=0,3,5,7,15-17,20-31)	x	r	Reserved Reserved. Shall be written with zero.
PSI5_EN	1	rwh	PSI5 memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
ERAY_OBF0_EN	2	rwh	ERAY OBF0 SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled

Memory Test Unit (MTU)

Field	Bits	Type	Description
ERAY_TBF_IBF0_EN	4	rwh	ERAY TBF IBF0 memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
ERAY_MBF0_EN	6	rwh	ERAY MBF0 memory SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
R8	8	rwh	Reserved - Res Reserved. Not used in this product. Shall be written with zero.
R9	9	rwh	Reserved - Res Reserved. Not used in this product. Shall be written with zero.
R10	10	rwh	Reserved - Res Reserved. Not used in this product. Shall be written with zero.
R11	11	rwh	Reserved - Res Reserved. Not used in this product. Shall be written with zero.
R12	12	rwh	Reserved - Res Reserved. Not used in this product. Shall be written with zero.
SCR_XRAM_EN	13	rwh	SCR XRAM SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
SCR_RAMINT_EN	14	rwh	SCR Internal RAM SSH instance Enable 0 _B SSH instance is disabled 1 _B SSH instance is enabled
GIGETH_RX_EN	18	rwh	Gigabit Ethernet RX SSH instance Enable 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GIGETH_TX_EN	19	rwh	Gigabit Ethernet TX SSH instance Enable 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1

Memory Test Unit (MTU)

13.4.2 MEMMAP Implementation

The Memory Mapping Enable register MEMMAP has configurable control bits to select memory-mapped test mode for each CPU memory.

Cache and Scratchpad memories are physically implemented as a single RAM, but this register function assumes two separate logical RAM partitions. In this register additional bits CPUxDCMAP and CPUxPCMAP are defined. These control the Cache partitions of the RAMs for Data Side and Program side respectively. Since cache content and tags of a cache must be simultaneously switched from memory mapped to cache functional mode, the control bits are mirrored and only one bit is writeable for each cache. The bits corresponding to the tag memories of the same cache will always take the same value as that written to the main Cache Memory control bit. This linkage is product specific.

Please note that the MEMMAP register is used only to map the Cache/Tag memories to system address space. These bits have no effect on testing these memories itself. For system address range into which the memories will be mapped, please refer to the memory map chapter.

Memory Mapping Enable Register

The Memory Mapping Enable register MEMMAP has configurable control bits to select memory-mapped test mode. See the Integration Section for mapping of memory controller numbers.

MTU_MEMMAP

Memory Mapping Enable Register

(001C_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R29		MEM2 8MAP	MEM2 7MAP	MEM2 6MAP	MEM2 5MAP	R24	MEM2 3MAP	MEM2 2MAP	MEM2 1MAP	MEM2 0MAP	R19	MEM1 8MAP	MEM1 7MAP	MEM1 6MAP
	r		r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM1 5MAP	R14	MEM1 3MAP	MEM1 2MAP	MEM1 1MAP	MEM1 0MAP	R9	CPU1_ PTMA P	CPU1_ PCMA P	CPU1_ DTMA P	CPU1_ DCMA P	R4	CPU0_ PTMA P	CPU0_ PCMA P	CPU0_ DTMA P	CPU0_ DCMA P
r	r	r	r	r	r	r	rh	rwh	rh	rwh	r	rh	rwh	rh	rwh

Field	Bits	Type	Description
CPU0_DCMAP	0	rwh	CPU0 DCache Mapping 0 _B Normal cache function 1 _B Memory-mapped
MEMxMAP (x=10-13,15-18,20-23,25-28)	x	r	MEMx Mapping Enable Reserved; Not used in this product. Shall be written with zero.
CPU0_DTMAP	1	rh	CPU0 DTAG Mapping Read only. Mirrors the state of CPU0_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0 _B Normal cache function 1 _B Memory-mapped

Memory Test Unit (MTU)

Field	Bits	Type	Description
CPU0_PCMAP	2	rwh	CPU0 PCACHE Mapping 0 _B Normal cache function 1 _B Memory-mapped
CPU0_PTMAP	3	rh	CPU0 PTAG Mapping Read only. Mirrors the state of CPU0_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0 _B Normal cache function 1 _B Memory-mapped
R4	4	r	Reserved - Res Reserved. Not used in this product.
CPU1_DCMAP	5	rwh	CPU1 DCache Mapping 0 _B Normal cache function 1 _B Memory-mapped
CPU1_DTMAP	6	rh	CPU1 DTAG Mapping Read only. Mirrors the state of CPU1_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0 _B Normal cache function 1 _B Memory-mapped
CPU1_PCMAP	7	rwh	CPU1 PCACHE Mapping 0 _B Normal cache function 1 _B Memory-mapped
CPU1_PTMAP	8	rh	CPU1 PTAG Mapping Read only. Mirrors the state of CPU1_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0 _B Normal cache function 1 _B Memory-mapped
R9	9	r	Reserved - Res Reserved. Not used in this product.
R14	14	r	Reserved - Res Reserved. Not used in this product.
R19	19	r	Reserved - Res Reserved. Not used in this product.
R24	24	r	Reserved - Res Reserved. Not used in this product.
R29	31:29	r	Reserved - Res Reserved. Not used in this product.

Memory Test Unit (MTU)

13.4.3 MEMSTAT Implementation

The Memory Status Registers MEMSTATx have an implemented bit for each security relevant RAM.

The Data- and Program- Cache and Scratchpad memories are physically implemented as a single RAM with a single MBIST. Hence CPUx_DMEN_AIU and CPUx_PMEM_AIU give the status of the partial initialization of the cache partitions for the Data and Program memories respectively.

Memory Status Register i

The memory status register MEMSTAT shows whether each SSH instance is currently executing an automatic initialization sequence.

MTU_MEMSTATi (i=0)

Memory Status Register i (0038_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R29		RES28	RES27	RES26	RES25	R24	RES23	RES22	RES21	RES20	R19	RES18	RES17	RES16
	r		r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	R14	RES13	RES12	RES11	RES10	R9	CPU1_PTAG_AIU	CPU1_PMEM_AIU	CPU1_DTAG_AIU	CPU1_DMEN_AIU	R4	CPU0_PTAG_AIU	CPU0_PMEM_AIU	CPU0_DTAG_AIU	CPU0_DMEN_AIU
r	r	r	r	r	r	r	rh	rh	rh	rh	r	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEN_AIU	0	rh	CPU0 DMEM Partial AutoInitialize of Cache Partition Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
RESx (x=10-13,15-18,20-23,25-28)	x	r	Reserved Reserved. Not used in this product.
CPU0_DTAG_AIU	1	rh	CPU0 DTAG MBIST AutoInitialize Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
CPU0_PMEM_AIU	2	rh	CPU0 PMEM Partial AutoInitialize of Cache Partition Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize

Memory Test Unit (MTU)

Field	Bits	Type	Description
CPU0_PTAG_AIU	3	rh	CPU0 PTAG MBIST AutoInitialize Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
R4	4	r	Reserved - Res Reserved. Not used in this product.
CPU1_DMEM_AIU	5	rh	CPU1 DMEM Partial AutoInitialize of Cache Partition Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
CPU1_DTAG_AIU	6	rh	CPU1 DTAG MBIST AutoInitialize Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
CPU1_PMEM_AIU	7	rh	CPU1 PMEM Partial AutoInitialize of Cache Partition Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
CPU1_PTAG_AIU	8	rh	CPU1 PTAG MBIST AutoInitialize Underway This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the initialization sequence has not yet completed. 0 _B MBIST not running autoinitialize 1 _B MBIST running autoinitialize
R9	9	r	Reserved - Res Reserved. Not used in this product.
R14	14	r	Reserved - Res Reserved. Not used in this product.
R19	19	r	Reserved - Res Reserved. Not used in this product.
R24	24	r	Reserved - Res Reserved. Not used in this product.
R29	31:29	r	Reserved - Res Reserved. Not used in this product.

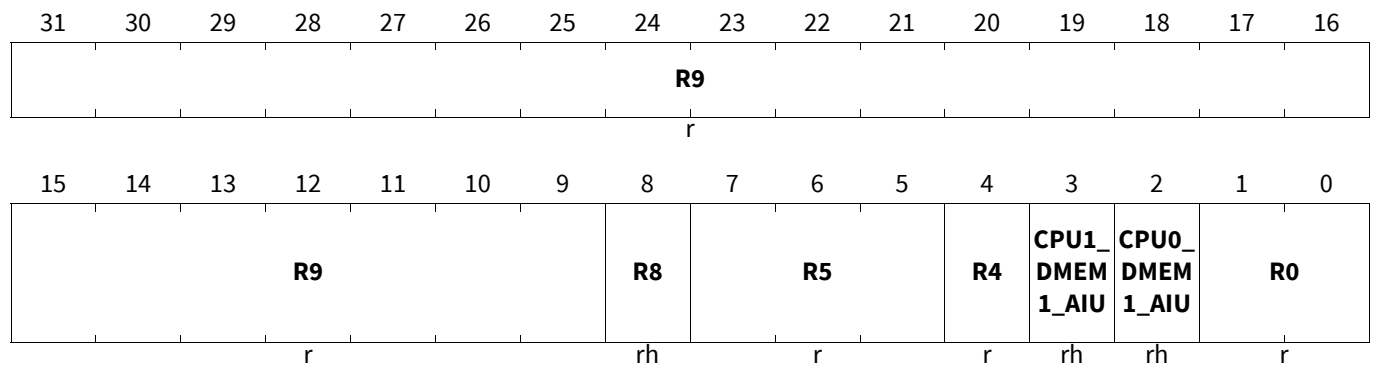
Memory Test Unit (MTU)

MTU_MEMSTATi (i=1)

Memory Status Register i

(0038_H+i*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
R0	1:0	r	Reserved - Res Reserved. Not used in this product.
CPU0_DMEM1_AIU	2	rh	CPU0 DMEM1 Partial AutoInitialize of Cache Partition Underway 0 _B SSH instance is disabled 1 _B SSH instance is enabled ¹⁾ .
CPU1_DMEM1_AIU	3	rh	CPU1 DMEM1 Partial AutoInitialize of Cache Partition Underway 0 _B SSH instance is disabled 1 _B SSH instance is enabled ²⁾ .
R4	4	r	Reserved - Res Reserved. Not used in this product.
R5	7:5	r	Reserved - Res Reserved. Not used in this product.
R8	8	rh	Reserved - Res Reserved. Not used in this product.
R9	31:9	r	Reserved - Res Reserved. Not used in this product.

1) Please refer to separate section related to handling of the large DMEM on this device.

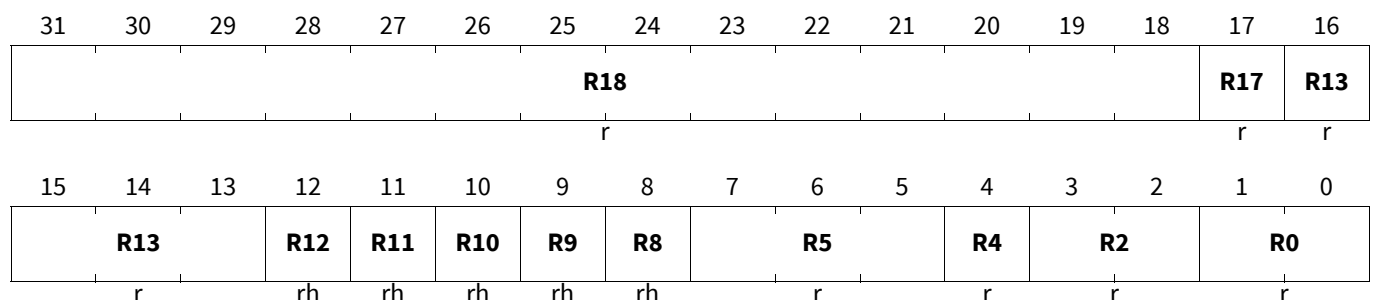
2) Please refer to separate section related to handling of the large DMEM on this device.

MTU_MEMSTATi (i=2)

Memory Status Register i

(0038_H+i*4)

Application Reset Value: 0000 0000_H



Memory Test Unit (MTU)

Field	Bits	Type	Description
R0	1:0	r	Reserved - Res Reserved. Not used in this product.
R2	3:2	r	Reserved - Res Reserved. Not used in this product.
R4	4	r	Reserved - Res Reserved. Not used in this product.
R5	7:5	r	Reserved - Res Reserved. Not used in this product.
R8	8	rh	Reserved - Res Reserved. Not used in this product.
R9	9	rh	Reserved - Res Reserved. Not used in this product.
R10	10	rh	Reserved - Res Reserved. Not used in this product.
R11	11	rh	Reserved - Res Reserved. Not used in this product.
R12	12	rh	Reserved - Res Reserved. Not used in this product.
R13	16:13	r	Reserved - Res Reserved. Not used in this product.
R17	17	r	Reserved - Res Reserved. Not used in this product.
R18	31:18	r	Reserved - Res Reserved. Not used in this product.

13.4.4 MEMDONE Implementation

Memory Test Done Status Register i

Each bit in one of the memory test done status registers MEMDONEx reflects the status of the MSTATUS.DONE bit in the corresponding SSH. See the implementation section for the implemented register bits.

MTU_MEMDONEi (i=0)

Memory Test Done Status Register i (0050_H+i*4) Application Reset Value: FFFF FFFF_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	RES19	RES18	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	CPU1_DLMU_STBY_DON	CPU1_PTAG_DONE	CPU1_PMEM_DON_E	CPU1_DTAG_DONE	CPU1_DMEM_DON_E	CPU0_DLMU_STBY_DON	CPU0_PTAG_DONE	CPU0_PMEM_DON_E	CPU0_DTAG_DONE	CPU0_DMEM_DON_E
r	r	r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Memory Test Unit (MTU)

Field	Bits	Type	Description
CPU0_DMEM_DONE	0	rh	CPU0 DMEM Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
RESz (z=10-31)	z	r	Reserved Reserved. Not used in this product.
CPU0_DTAG_DONE	1	rh	CPU0 DTAG Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU0_PMEM_DONE	2	rh	CPU0 PMEM Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU0_PTAG_DONE	3	rh	CPU0 PTAG Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU0_DLMU_STBY_DONE	4	rh	CPU0 STANDBY DLMU Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU1_DMEM_DONE	5	rh	CPU1 DMEM Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU1_DTAG_DONE	6	rh	CPU1 DTAG Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU1_PMEM_DONE	7	rh	CPU1 PMEM Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU1_PTAG_DONE	8	rh	CPU1 PTAG Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
CPU1_DLMU_STBY_DONE	9	rh	CPU1 STANDBY DLMU Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1

Memory Test Unit (MTU)

MTU_MEMDONE_i (i=1)

Memory Test Done Status Register i

(0050_H+i*4)

Application Reset Value: FFFF FFFF_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN_20_DONE	MCAN_10_DONE	RES29	GTM_DPLL2_DONE	GTM_DPLL1_BC_DONE	GTM_DPLL1_A_DONE	GTM_MCS1F_AST_DONE	RES24	GTM_MCS0F_AST_DONE	RES22	GTM_FIFO_DONE	RES20	RES19	RES18	RES17	RES16
rh	rh	r	rh	rh	rh	rh	r	rh	r	rh	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	SADM_A_DONE	R8	RES7	RES6	RES5	RES4	CPU1_DMEM1_DONE	CPU0_DMEM1_DONE	RES1	RES0
r	r	r	r	r	r	rh	rh	r	r	r	r	rh	rh	r	r

Field	Bits	Type	Description
RES _z (z=0-1,4-7,10-20,22,24,29)	z	r	Reserved Reserved. Not used in this product.
CPU0_DMEM1_DONE	2	rh	CPU0 DMEM1 Test Done Status 0 _B SSH instance is disabled 1 _B SSH instance is enabled ¹⁾ .
CPU1_DMEM1_DONE	3	rh	CPU1 DMEM1 Test Done Status 0 _B SSH instance is disabled 1 _B SSH instance is enabled ²⁾ .
R8	8	rh	Reserved - Res Reserved. Not used in this product.
SADMA_DONE	9	rh	Safety DMA Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GTM_FIFO_DONE	21	rh	GTM FIFO memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GTM_MCS0FAST_DONE	23	rh	GTM MCS0 FAST memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GTM_MCS1FAST_DONE	25	rh	GTM MCS1 FAST memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GTM_DPLL1A_DONE	26	rh	GTM DPLL1A memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GTM_DPLL1BC_DONE	27	rh	GTM DPLL1BC memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1

Memory Test Unit (MTU)

Field	Bits	Type	Description
GTM_DPLL2_DONE	28	rh	GTM DPLL2 memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
MCAN10_DON E	30	rh	MCAN10 memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
MCAN20_DON E	31	rh	MCAN20 memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1

- 1) Please refer to separate section related to handling of the large DMEM on this device.
- 2) Please refer to separate section related to handling of the large DMEM on this device.

MTU_MEMDONE_i (i=2)

Memory Test Done Status Register i

(0050_H+i*4)

Application Reset Value: FFFF FFFF_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	GIGET_H_TX_DONE	GIGET_H_RX_DONE	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	rh	rh	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	SCR_RAM_DONE	SCR_XRAM_DONE	R12	R11	R10	R9	R8	RES7	ERAY_MBF0_DONE	RES5	ERAY_TBF_IBF0_DONE	RES3	ERAY_OBF0_DONE	PSI5_DONE	RES0
r	rh	rh	rh	rh	rh	rh	rh	r	rh	r	rh	r	rh	rh	r

Field	Bits	Type	Description
RES_z (z=0,3,5,7,15-17,20-31)	z	r	Reserved Reserved. Not used in this product.
PSI5_DONE	1	rh	PSI5 memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
ERAY_OBF0_DONE	2	rh	ERAY OBF0 Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
ERAY_TBF_IBF0_DONE	4	rh	ERAY TBF IBF0 memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
ERAY_MBF0_DONE	6	rh	ERAY MBF0 memory Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
R8	8	rh	Reserved - Res Reserved. Not used in this product.

Memory Test Unit (MTU)

Field	Bits	Type	Description
R9	9	rh	Reserved - Res Reserved. Not used in this product.
R10	10	rh	Reserved - Res Reserved. Not used in this product.
R11	11	rh	Reserved - Res Reserved. Not used in this product.
R12	12	rh	Reserved - Res Reserved. Not used in this product.
SCR_XRAM_D ONE	13	rh	SCR XRAM Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
SCR_RAMINT_ DONE	14	rh	SCR Internal RAM Test Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GIGETH_RX_D ONE	18	rh	Gigabit Ethernet RX memoryTest Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GIGETH_TX_D ONE	19	rh	Gigabit Ethernet TX memoryTest Done Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1

13.4.5 MEMFDA Implementation

Memory Test FDA Status Register i

Each bit in one of the memory test done status registers MEMFDA_x reflects the status of the MSTATUS.FDA bit in the corresponding SSH. See the implementation section for the implemented register bits.

MTU_MEMFDA_i (i=0)

Memory Test FDA Status Register i (0060_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	RES19	RES18	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	CPU1_DLMU_STBY_FDA	CPU1_PTAG_FDA	CPU1_PMEM_FDA	CPU1_DTAG_FDA	CPU1_DMEM_FDA	CPU0_DLMU_STBY_FDA	CPU0_PTAG_FDA	CPU0_PMEM_FDA	CPU0_DTAG_FDA	CPU0_DMEM_FDA
r	r	r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEM_FDA	0	rh	CPU0 DMEM Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1

Memory Test Unit (MTU)

Field	Bits	Type	Description
RESz (z=10-31)	z	r	Reserved Reserved. Not used in this product.
CPU0_DTAG_FDA	1	rh	CPU0 DTAG Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU0_PMEM_FDA	2	rh	CPU0 PMEM Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU0_PTAG_FDA	3	rh	CPU0 PTAG Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU0_DLMU_STBY_FDA	4	rh	CPU0 STANDBY DLMU Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU1_DMEN_FDA	5	rh	CPU1 DMEM Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU1_DTAG_FDA	6	rh	CPU1 DTAG Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU1_PMEM_FDA	7	rh	CPU1 PMEM Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU1_PTAG_FDA	8	rh	CPU1 PTAG Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU1_DLMU_STBY_FDA	9	rh	CPU1 STANDBY DLMU Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1

MTU_MEMFDAi (i=1)

Memory Test FDA Status Register i (0060_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN_20_FD_A	MCAN_10_FD_A	RES29	GTM_DPLL2_FDA	GTM_DPLL1_BC_FD_A	GTM_DPLL1_A_FDA	GTM_MCS1F_AST_FDA	RES24	GTM_MCS0F_AST_FDA	RES22	GTM_IFO_FDA	RES20	RES19	RES18	RES17	RES16
rh	rh	r	rh	rh	rh	rh	r	rh	r	rh	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	SADM_A_FDA	R8	RES7	RES6	RES5	RES4	CPU1_DMEN_1_FDA	CPU0_DMEN_1_FDA	RES1	RES0
r	r	r	r	r	r	rh	rh	r	r	r	r	rh	rh	r	r

Memory Test Unit (MTU)

Field	Bits	Type	Description
RESz (z=0-1,4-7,10-20,22,24,29)	z	r	Reserved Reserved. Not used in this product.
CPU0_DMEM1_FDA	2	rh	CPU0 DMEM1 Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
CPU1_DMEM1_FDA	3	rh	CPU1 DMEM1 Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
R8	8	rh	Reserved - Res Reserved. Not used in this product.
SADMA_FDA	9	rh	Safety DMA Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GTM_FIFO_FDA	21	rh	GTM FIFO memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GTM_MCS0FA_ST_FDA	23	rh	GTM MCS0 FAST memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GTM_MCS1FA_ST_FDA	25	rh	GTM MCS1 FAST memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GTM_DPLL1A_FDA	26	rh	GTM DPLL1A memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GTM_DPLL1B_C_FDA	27	rh	GTM DPLL1BC memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GTM_DPLL2_FDA	28	rh	GTM DPLL2 memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
MCAN10_FDA	30	rh	MCAN10 memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
MCAN20_FDA	31	rh	MCAN20 memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1

Memory Test Unit (MTU)

MTU_MEMFDAi (i=2)

Memory Test FDA Status Register i

(0060_H+i*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	GIGET H_TX_ FDA	GIGET H_RX_ FDA	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	rh	rh	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	SCR_R AMINT_ FDA	SCR_X RAM_F DA	R12	R11	R10	R9	R8	RES7	ERAY_ MBF0_ FDA	RES5	ERAY_ TBF_I BF0_F DA	RES3	ERAY_ OBF0_ FDA	PSI5_ FDA	RES0
r	rh	rh	rh	rh	rh	rh	rh	r	rh	r	rh	r	rh	rh	r

Field	Bits	Type	Description
RESz (z=0,3,5,7,15-17,20-31)	z	r	Reserved Reserved. Not used in this product.
PSI5_FDA	1	rh	PSI5 memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
ERAY_OBF0_FDA	2	rh	ERAY OBF0 Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
ERAY_TBF_IBF0_FDA	4	rh	ERAY TBF IBF0 memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
ERAY_MBF0_FDA	6	rh	ERAY MBF0 memory Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
R8	8	rh	Reserved - Res Reserved. Not used in this product.
R9	9	rh	Reserved - Res Reserved. Not used in this product.
R10	10	rh	Reserved - Res Reserved. Not used in this product.
R11	11	rh	Reserved - Res Reserved. Not used in this product.
R12	12	rh	Reserved - Res Reserved. Not used in this product.
SCR_XRAM_FDA	13	rh	SCR XRAM Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1

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Field	Bits	Type	Description
SCR_RAMINT_FDA	14	rh	SCR Internal RAM Test FDA Status 0 _B SSH MSTATUS.FDA = 0 1 _B SSH MSTATUS.FDA = 1
GIGETH_RX_FDA	18	rh	Gigabit Ethernet RX memory Test FDA Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1
GIGETH_TX_FDA	19	rh	Gigabit Ethernet TX SSH memory Test FDA Status 0 _B SSH MSTATUS.DONE = 0 1 _B SSH MSTATUS.DONE = 1

Memory Test Unit (MTU)

13.5 SSH Instances

The system SRAMs do not all have the same configuration. [Table 52 “SSH instances” on Page 22](#) shows the instance-specific configurations of the SRAM Support Hardware.

The ECC values for all SRAMs are computed only out of the data information*.

The base address of an SSH instance MCx can be calculated from the MC_BASE (defined in the platform chapter) as: Base Address of SSH instance x (MCx) = MC_BASE + x*0x100

Table 52 SSH instances

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
0	CPU0_DMEN	5	SECDED	2	16
1	CPU0_DTAG	5	SECDED	2	4
2	CPU0_PMEM	5	SECDED	2	8
3	CPU0_PTAG	5	DED	2	4
4	CPU0_DLMU_STBY	5	SECDED	2	8
5	CPU1_DMEN	5	SECDED	2	16
6	CPU1_DTAG	5	SECDED	2	4
7	CPU1_PMEM	5	SECDED	2	8
8	CPU1_PTAG	5	DED	2	4
9	CPU1_DLMU_STBY	5	SECDED	2	8
10	Reserved				
11	Reserved				
12	Reserved				
13	Reserved				
14	Reserved				
15	Reserved				
16	Reserved				
17	Reserved				
18	Reserved				
19	Reserved				
20	Reserved				
21	Reserved				
22	Reserved				
23	Reserved				
24	Reserved				
25	Reserved				
26	Reserved				
27	Reserved				
28	Reserved				
29	Reserved				

Memory Test Unit (MTU)

Table 52 SSH instances (cont'd)

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
30	Reserved				
31	Reserved				
32	Reserved				
33	Reserved				
34	CPU0_DMEM1	5	SECDED	2	16
35	CPU1_DMEM1	5	SECDED	2	16
36-37	Reserved				
38	Reserved				
39	Reserved				
41	SADMA	5	SECDED	1	4
42	Reserved				
43	Reserved				
44	Reserved				
45	Reserved				
46	Reserved				
47	Reserved				
48	Reserved				
49	Reserved				
50	Reserved				
51	Reserved				
52	Reserved				
53	GTM_FIFO	5	SECDED	1	4
54	Reserved				
55	GTM_MCS0FAST	5	SECDED	1	4
56	Reserved				
57	GTM_MCS1FAST	5	SECDED	1	4
58	GTM_DPLL1A	5	SECDED	1	4
59	GTM_DPLL1BC	5	SECDED	1	4
60	GTM_DPLL2	5	SECDED	1	8
61	Reserved				
62	MCAN10	5	SECDED	1	16
63	MCAN20	5	SECDED	1	16
64	Reserved				
65	PSI5	5	SECDED	1	4
66	ERAY_OBF0	5	SECDED	1	4
67	Reserved				
68	ERAY_TBF_IBF0	5	SECDED	1	4

Memory Test Unit (MTU)
Table 52 SSH instances (cont'd)

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
69	Reserved				
70	ERAY_MBF0	5	SECDED	1	4
71	Reserved				
77	SCR_XRAM	5	SECDED	2	8
78	SCR_RAMINT	5	SECDED	1	4
79	Reserved				
80	Reserved				
81	Reserved				
82	GIGETH_RX_RAM	5	SECDED	1	4
83	GIGETH_TX_RAM	5	SECDED	1	4
84	Reserved				
85	Reserved				
86- 87	Reserved				
88	Reserved				
89	Reserved				
90	Reserved				
91	Reserved				
92	Reserved				
93	Reserved				
94	Reserved				
95	Reserved				

Memory Test Unit (MTU)

13.5.1 Ganging for SRAM test and initialization

Whenever an MBIST test or SRAM initialization is started via the MTU/SSH, there is a certain jump in the current consumption, due to the parallel accesses to the SRAM cells during the test or initialization. This current jump is different for the different SRAMs in the product, and depends on the size of the SRAM, the clock frequency e.t.c.

If too many SRAMs are tested or initialized in parallel, it may result in a significant current jump, which may put the device outside of the specified operating conditions. On the other hand, in order to reduce the overall test and/or initialization time, it may be imperative for the application to perform the test or initialization of many SRAMs in parallel.

In order to achieve this trade-off between current jump and test/initialization time - it is advised to partition the available SRAMs into different “Gangs”. This is referred to as Ganging. The SRAMs in each Gang are all initialized/tested in parallel - while the Gangs themselves are executed in sequence, one after the other. This ensures that the current jump never exceeds the allowed limits, while at the same time the overall test time is minimized.

Gangs 0-16 are defined for the platform. Depending on the device and the number of implemented SRAMs, the number of gangs needed may be less. The numbering of the gangs is not important and does not signify any order.

In the below ganging tables, a ganging configuration for this product is shown. This assumes a 4-march element (4N) non-destructive test (r,w*,r*,w) on a zero-data background (i.e. the SRAM is cleared with ECC-correct zero data). The same ganging may be used for SRAM initialization.

The provided ganging example is ensured to satisfy the specified limitations in current jumps of this device, while at the same time optimizing the overall test time. All implemented SRAMs are considered here. If certain SRAMs are not of interest to a particular application, then the gangs may be modified appropriately.

Table 53 GANG-0

MCx(x=)	Module / SRAM
04	CPU0_DLMU_STBY
05	CPU1_DMED
55	GTM_MCS0FAST
62	MCAN10
63	MCAN20
70	ERAY_MBF0
77	SCR_XRAM
78	SCR_RAMINT
82	GIGETH_RX

Table 54 GANG-1

MCx(x=)	Module / SRAM
00	CPU0_DMED
34	CPU0_DMED1
53	GTM_FIFO
60	GTM_DPLL2

Memory Test Unit (MTU)
Table 55 GANG-2

MCx(x=)	Module / SRAM
02	CPU0_PMEM
09	CPU1_DLMU_STBY
35	CPU1_DMEM1

Table 56 GANG-3

MCx(x=)	Module / SRAM
01	CPU0_DTAG
03	CPU0_PTAG
06	CPU1_DTAG
07	CPU1_PMEM
08	CPU1_PTAG
41	SADMA
57	GTM_MCS1FAST
58	GTM_DPLL1A
59	GTM_DPLL1BC
65	PSI5
66	ERAY_OBF0
68	ERAY_TBF_IBF0
83	GIGETH_TX

13.6 Connectivity**Table 57 Connections of MTU**

Interface Signals	connects		Description
MTU:CPU0DCMAP	to	cpu_pfi_pfrwb_0:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU1DCMAP	to	cpu_pfi_pfrwb_1:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU0PCMAP	to	cpu_pfi_pfrwb_0:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU1PCMAP	to	cpu_pfi_pfrwb_1:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:dmu_no_ram_init	from	DMU:MTU_NO_RAMIN	Disable RAM auto-initialization
MTU:scu_hsm_dbg	from	SCU:scu_hsm_dbg	HSM debug enable from SCU
MTU:sleep_n	from	SCU:scu_syst_sleep_n	Sleep request
MTU:DONE_INT	to	INT:mtu.DONE_INT	MTU Done Service Request
MTU:tcu_hsm_dbg_analysis_en	from	TCU:hsm_debug_mode	HSM debug request from TCU

Memory Test Unit (MTU)

13.7 Revision History

Table 58 Revision History

Reference	Change to Previous Version	Comment
V7.4.7		
Page 27	Revision History entries up to V7.4.6 removed.	
	No changes.	
Page 26	Connectivity information updated.	
V7.4.8		
Page 27	Revision History entries up to V7.4.7 removed.	
Page 8	MEMMAP Reserved (not implemented) bits changed to "read".	
Page 3, Page 13, Page 17	"SADMA" changed to "Safety DMA" in short description of MEMTEST1/9, MEMDONE1/9 and MEMFDA1/9 bit fields.	
V7.4.9		
Page 25	Unhide for external audience: MCAN10.	
Page 26	Unhide for external audience: CPU1_DLMU_STBY.	
Page 26	Typo fixed (CPU1_DMEM -> CPU1_DMEM1), unhide for external audience.	
Page 26	Unhide for external audience: CPU0_DTAG, CPU0_PTAG, CPU1_DTAG, CPU1_PTAG.	
Page 25	Typo fixed (CPU0_DMEM -> CPU0_DMEM1).	
V7.4.10		
-	No functional changes.	
V7.4.11		
-	No functional changes.	
V7.4.12		
-	No functional changes.	
V7.4.13		
Page 10	Wrongly mentioned bit field in MTU_MEMSTATi (i=2) fixed.	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

14 General Purpose I/O Ports and Peripheral I/O Lines (Ports)

This chapter supplements the family documentation with device specific information for TC36x.

14.1 TC36x Specific IP Configuration

The Ports configuration (which Port modules are implemented, their width and functionality) is represented by the device specific register set shown in this chapter.

14.2 TC36x Specific Register Set

Table 59 Register Address Space - Pn

Module	Base Address	End Address	Note
P00	F003A000 _H	F003A0FF _H	SPB bus slave interface
P02	F003A200 _H	F003A2FF _H	SPB bus slave interface
P10	F003AA00 _H	F003AAFF _H	SPB bus slave interface
P11	F003AB00 _H	F003ABFF _H	SPB bus slave interface
P12	F003AC00 _H	F003ACFF _H	SPB bus slave interface
P13	F003AD00 _H	F003ADFF _H	SPB bus slave interface
P14	F003AE00 _H	F003AEFF _H	SPB bus slave interface
P15	F003AF00 _H	F003AFF _H	SPB bus slave interface
P20	F003B400 _H	F003B4FF _H	SPB bus slave interface
P21	F003B500 _H	F003B5FF _H	SPB bus slave interface
P22	F003B600 _H	F003B6FF _H	SPB bus slave interface
P23	F003B700 _H	F003B7FF _H	SPB bus slave interface
P32	F003C000 _H	F003C0FF _H	SPB bus slave interface
P33	F003C100 _H	F003C1FF _H	SPB bus slave interface
P40	F003C800 _H	F003C8FF _H	SPB bus slave interface

Register Overview Tables of Pn

Table 60 Register Overview - P00 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_OUT	Port 00 Output Register	000 _H	U,SV	U,SV,P	Application Reset	25
P00_OMR	Port 00 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	29
P00_ID	Port 00 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P00_IOCRO	Port 00 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 60 Register Overview - P00 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_IOCRA4	Port 00 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
P00_IOCRA8	Port 00 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
P00_IOCRA12	Port 00 Input/Output Control Register 12	01C _H	U,SV	U,SV,P	See page 44	44
	Reserved (004 _H Byte)	020 _H	BE	BE		
P00_IN	Port 00 Input Register	024 _H	U,SV	BE	Application Reset	46
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P00_PDR0	Port 00 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P00_PDR1	Port 00 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 54	54
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P00_ESR	Port 00 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	56
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P00_PDISC	Port 00 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 62	62
P00_PCSR	Port 00 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	68
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P00_OMSR0	Port 00 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P00_OMSR4	Port 00 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P00_OMSR8	Port 00 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P00_OMSR12	Port 00 Output Modification Set Register 12	07C _H	U,SV	U,SV,P	Application Reset	80
P00_OMCR0	Port 00 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P00_OMCR4	Port 00 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P00_OMCR8	Port 00 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 60 Register Overview - P00 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_OMCR12	Port 00 Output Modification Clear Register 12	08C _H	U,SV	U,SV,P	Application Reset	87
P00_OMSR	Port 00 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	88
P00_OMCR	Port 00 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	92
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P00_ACCEN1	Port 00 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P00_ACCEN0	Port 00 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 61 Register Overview - P02 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P02_OUT	Port 02 Output Register	000 _H	U,SV	U,SV,P	Application Reset	26
P02_OMR	Port 02 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	30
P02_ID	Port 02 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P02_IOCRO	Port 02 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P02_IOCR4	Port 02 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
P02_IOCR8	Port 02 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
	Reserved (004 _H Byte)	020 _H	BE	BE		
P02_IN	Port 02 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P02_PDR0	Port 02 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P02_PDR1	Port 02 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 55	55

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 61 Register Overview - P02 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte) (x=0-1)	048 _H +x* 4	BE	BE		
P02_ESR	Port 02 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	58
	Reserved (004 _H Byte) (x=0-2)	054 _H +x* 4	BE	BE		
P02_PDISC	Port 02 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 64	64
P02_PCSR	Port 02 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	69
	Reserved (004 _H Byte) (x=0-1)	068 _H +x* 4	BE	BE		
P02_OMSR0	Port 02 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P02_OMSR4	Port 02 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P02_OMSR8	Port 02 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P02_OMCR0	Port 02 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P02_OMCR4	Port 02 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P02_OMCR8	Port 02 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P02_OMSR	Port 02 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	89
P02_OMCR	Port 02 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	93
	Reserved (004 _H Byte) (x=0-1)	098 _H +x* 4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x* 4	BE	BE		
P02_ACCEN1	Port 02 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P02_ACCEN0	Port 02 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 62 Register Overview - P10 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P10_OUT	Port 10 Output Register	000 _H	U,SV	U,SV,P	Application Reset	26
P10_OMR	Port 10 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	30
P10_ID	Port 10 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P10_IOCRO	Port 10 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P10_IOCRA	Port 10 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
P10_IOCRA8	Port 10 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
	Reserved (004 _H Byte)	020 _H	BE	BE		
P10_IN	Port 10 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P10_PDR0	Port 10 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P10_PDR1	Port 10 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 55	55
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P10_ESR	Port 10 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	58
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P10_PDISC	Port 10 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 64	64
P10_PCSR	Port 10 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	69
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P10_OMSR0	Port 10 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P10_OMSR4	Port 10 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P10_OMSR8	Port 10 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 62 Register Overview - P10 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P10_OMCR0	Port 10 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P10_OMCR4	Port 10 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P10_OMCR8	Port 10 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P10_OMSR	Port 10 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	89
P10_OMCR	Port 10 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	93
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P10_ACCEN1	Port 10 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P10_ACCEN0	Port 10 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 63 Register Overview - P11 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P11_OUT	Port 11 Output Register	000 _H	U,SV	U,SV,P	Application Reset	25
P11_OMR	Port 11 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	29
P11_ID	Port 11 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P11_IOCRO	Port 11 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P11_IOCRA4	Port 11 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
P11_IOCRA8	Port 11 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
P11_IOCRA12	Port 11 Input/Output Control Register 12	01C _H	U,SV	U,SV,P	See page 44	44
	Reserved (004 _H Byte)	020 _H	BE	BE		
P11_IN	Port 11 Input Register	024 _H	U,SV	BE	Application Reset	46

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 63 Register Overview - P11 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte) (x=0-5)	028 _H +x* 4	BE	BE		
P11_PDR0	Port 11 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P11_PDR1	Port 11 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 54	54
	Reserved (004 _H Byte) (x=0-1)	048 _H +x* 4	BE	BE		
P11_ESR	Port 11 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	56
	Reserved (004 _H Byte) (x=0-2)	054 _H +x* 4	BE	BE		
P11_PDISC	Port 11 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 62	62
P11_PCSR	Port 11 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	70
	Reserved (004 _H Byte) (x=0-1)	068 _H +x* 4	BE	BE		
P11_OMSR0	Port 11 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P11_OMSR4	Port 11 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P11_OMSR8	Port 11 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P11_OMSR12	Port 11 Output Modification Set Register 12	07C _H	U,SV	U,SV,P	Application Reset	80
P11_OMCR0	Port 11 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P11_OMCR4	Port 11 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P11_OMCR8	Port 11 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P11_OMCR12	Port 11 Output Modification Clear Register 12	08C _H	U,SV	U,SV,P	Application Reset	87
P11_OMSR	Port 11 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	88
P11_OMCR	Port 11 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	92
	Reserved (004 _H Byte) (x=0-1)	098 _H +x* 4	BE	BE		

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 63 Register Overview - P11 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x* 4	BE	BE		
P11_ACCEN1	Port 11 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P11_ACCEN0	Port 11 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 64 Register Overview - P12 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P12_OUT	Port 12 Output Register	000 _H	U,SV	U,SV,P	Application Reset	27
P12_OMR	Port 12 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	31
P12_ID	Port 12 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P12_IOCRO	Port 12 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
	Reserved (004 _H Byte)	020 _H	BE	BE		
P12_IN	Port 12 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x* 4	BE	BE		
P12_PDR0	Port 12 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 53	53
	Reserved (004 _H Byte) (x=0-1)	048 _H +x* 4	BE	BE		
P12_ESR	Port 12 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	59
	Reserved (004 _H Byte) (x=0-2)	054 _H +x* 4	BE	BE		
P12_PDISC	Port 12 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 65	65
P12_PCSR	Port 12 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	70
	Reserved (004 _H Byte) (x=0-1)	068 _H +x* 4	BE	BE		
P12_OMSR0	Port 12 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 64 Register Overview - P12 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P12_OMCR0	Port 12 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P12_OMSR	Port 12 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	90
P12_OMCR	Port 12 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	94
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P12_ACCEN1	Port 12 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P12_ACCEN0	Port 12 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 65 Register Overview - P13 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P13_OUT	Port 13 Output Register	000 _H	U,SV	U,SV,P	Application Reset	27
P13_OMR	Port 13 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	31
P13_ID	Port 13 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P13_IOCRO	Port 13 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
	Reserved (004 _H Byte)	020 _H	BE	BE		
P13_IN	Port 13 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P13_PDR0	Port 13 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 53	53
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P13_ESR	Port 13 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	59
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 65 Register Overview - P13 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P13_PDISC	Port 13 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 65	65
P13_PCSR	Port 13 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	70
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P13_OMSR0	Port 13 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P13_OMCR0	Port 13 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P13_OMSR	Port 13 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	90
P13_OMCR	Port 13 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	94
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
P13_LPCR _x	Port 13 LVDS Pad Control Register x	0A0 _H +x*4	U,SV	SV,E,P	See page 95	95
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P13_ACCEN1	Port 13 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P13_ACCEN0	Port 13 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 66 Register Overview - P14 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P14_OUT	Port 14 Output Register	000 _H	U,SV	U,SV,P	Application Reset	26
P14_OMR	Port 14 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	30
P14_ID	Port 14 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P14_IOCRO	Port 14 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P14_IOCRA	Port 14 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 66 Register Overview - P14 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P14_IOC8	Port 14 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
	Reserved (004 _H Byte)	020 _H	BE	BE		
P14_IN	Port 14 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P14_PDR0	Port 14 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P14_PDR1	Port 14 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 55	55
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P14_ESR	Port 14 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	58
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P14_PDISC	Port 14 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 64	64
P14_PCSR	Port 14 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	69
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P14_OMSR0	Port 14 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P14_OMSR4	Port 14 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P14_OMSR8	Port 14 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P14_OMCR0	Port 14 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P14_OMCR4	Port 14 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P14_OMCR8	Port 14 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P14_OMSR	Port 14 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	89
P14_OMCR	Port 14 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	93
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 66 Register Overview - P14 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P14_LPCR _x	Port 14 LVDS Pad Control Register _x	0A0 _H +x*4	U,SV	SV,E,P	See page 97	97
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P14_ACCEN1	Port 14 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P14_ACCEN0	Port 14 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 67 Register Overview - P15 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P15_OUT	Port 15 Output Register	000 _H	U,SV	U,SV,P	Application Reset	26
P15_OMR	Port 15 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	30
P15_ID	Port 15 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P15_IOCRO	Port 15 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P15_IOCRR4	Port 15 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
P15_IOCRR8	Port 15 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
	Reserved (004 _H Byte)	020 _H	BE	BE		
P15_IN	Port 15 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P15_PDR0	Port 15 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P15_PDR1	Port 15 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 55	55
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P15_ESR	Port 15 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	58
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 67 Register Overview - P15 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P15_PDISC	Port 15 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 64	64
P15_PCSR	Port 15 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	69
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P15_OMSR0	Port 15 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P15_OMSR4	Port 15 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P15_OMSR8	Port 15 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P15_OMCR0	Port 15 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P15_OMCR4	Port 15 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P15_OMCR8	Port 15 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P15_OMSR	Port 15 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	89
P15_OMCR	Port 15 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	93
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P15_ACCEN1	Port 15 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P15_ACCEN0	Port 15 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 68 Register Overview - P20 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P20_OUT	Port 20 Output Register	000 _H	U,SV	U,SV,P	Application Reset	25
P20_OMR	Port 20 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	29
P20_ID	Port 20 Identification Register	008 _H	U,SV	BE	Application Reset	33

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 68 Register Overview - P20 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte)	00C _H	BE	BE		
P20_IOCRO	Port 20 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P20_IOCRA4	Port 20 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
P20_IOCRA8	Port 20 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
P20_IOCRA12	Port 20 Input/Output Control Register 12	01C _H	U,SV	U,SV,P	See page 44	44
	Reserved (004 _H Byte)	020 _H	BE	BE		
P20_IN	Port 20 Input Register	024 _H	U,SV	BE	Application Reset	46
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P20_PDR0	Port 20 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
P20_PDR1	Port 20 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 54	54
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P20_ESR	Port 20 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	56
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P20_PDISC	Port 20 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 62	62
P20_PCSR	Port 20 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	71
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P20_OMSR0	Port 20 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P20_OMSR4	Port 20 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P20_OMSR8	Port 20 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P20_OMSR12	Port 20 Output Modification Set Register 12	07C _H	U,SV	U,SV,P	Application Reset	80
P20_OMCRO	Port 20 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 68 Register Overview - P20 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P20_OMCR4	Port 20 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P20_OMCR8	Port 20 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P20_OMCR12	Port 20 Output Modification Clear Register 12	08C _H	U,SV	U,SV,P	Application Reset	87
P20_OMSR	Port 20 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	88
P20_OMCR	Port 20 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	92
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P20_ACCEN1	Port 20 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P20_ACCEN0	Port 20 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

Table 69 Register Overview - P21 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P21_OUT	Port 21 Output Register	000 _H	U,SV	U,SV,P	Application Reset	28
P21_OMR	Port 21 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	32
P21_ID	Port 21 Identification Register	008 _H	U,SV	BE	Application Reset	33
	Reserved (004 _H Byte)	00C _H	BE	BE		
P21_IOCRO	Port 21 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 35	35
P21_IOCRA	Port 21 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
	Reserved (004 _H Byte)	020 _H	BE	BE		
P21_IN	Port 21 Input Register	024 _H	U,SV	BE	Application Reset	48
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P21_PDR0	Port 21 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 69 Register Overview - P21 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte) (x=0-1)	048 _H +x* 4	BE	BE		
P21_ESR	Port 21 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	60
	Reserved (004 _H Byte) (x=0-2)	054 _H +x* 4	BE	BE		
P21_PDISC	Port 21 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 67	67
P21_PCSR	Port 21 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	72
	Reserved (004 _H Byte) (x=0-1)	068 _H +x* 4	BE	BE		
P21_OMSR0	Port 21 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	74
P21_OMSR4	Port 21 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P21_OMCR0	Port 21 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	81
P21_OMCR4	Port 21 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P21_OMSR	Port 21 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	91
P21_OMCR	Port 21 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	95
	Reserved (004 _H Byte) (x=0-1)	098 _H +x* 4	BE	BE		
P21_LPCR _x	Port 21 LVDS Pad Control Register x	0A0 _H +x* 4	U,SV	SV,E,P	See page 99	99
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x* 4	BE	BE		
P21_ACCEN1	Port 21 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	102
P21_ACCEN0	Port 21 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	105

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 70 Register Overview - P22 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P22_OUT	Port 22 Output Register	000 _H	U,SV	U,SV,P	Application Reset	27
P22_OMR	Port 22 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	31
P22_ID	Port 22 Identification Register	008 _H	U,SV	BE	Application Reset	35
	Reserved (004 _H Byte)	00C _H	BE	BE		
P22_IOCRO	Port 22 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 38	38
	Reserved (004 _H Byte)	020 _H	BE	BE		
P22_IN	Port 22 Input Register	024 _H	U,SV	BE	Application Reset	47
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P22_PDR0	Port 22 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 53	53
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P22_ESR	Port 22 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	59
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P22_PDISC	Port 22 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 65	65
P22_PCSR	Port 22 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	70
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P22_OMSR0	Port 22 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	76
P22_OMCR0	Port 22 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	83
P22_OMSR	Port 22 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	90
P22_OMCR	Port 22 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	94
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 70 Register Overview - P22 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P22_ACCEN1	Port 22 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	104
P22_ACCEN0	Port 22 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	107

Table 71 Register Overview - P23 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P23_OUT	Port 23 Output Register	000 _H	U,SV	U,SV,P	Application Reset	28
P23_OMR	Port 23 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	32
P23_ID	Port 23 Identification Register	008 _H	U,SV	BE	Application Reset	35
	Reserved (004 _H Byte)	00C _H	BE	BE		
P23_IOCRO	Port 23 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 38	38
P23_IOCRA	Port 23 Input/Output Control Register 1	014 _H	U,SV	U,SV,P	See page 39	39
	Reserved (004 _H Byte)	020 _H	BE	BE		
P23_IN	Port 23 Input Register	024 _H	U,SV	BE	Application Reset	48
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P23_PDR0	Port 23 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P23_ESR	Port 23 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	60
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P23_PDISC	Port 23 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 67	67
P23_PCSR	Port 23 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	72
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P23_OMSR0	Port 23 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	76

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 71 Register Overview - P23 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P23_OMSR4	Port 23 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P23_OMCR0	Port 23 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	83
P23_OMCR4	Port 23 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P23_OMSR	Port 23 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	91
P23_OMCR	Port 23 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	95
	Reserved (004 _H Byte) (x=0-1)	098 _H +x*4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x*4	BE	BE		
P23_ACCEN1	Port 23 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	104
P23_ACCEN0	Port 23 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	107

Table 72 Register Overview - P32 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P32_OUT	Port 32 Output Register	000 _H	U,SV	U,SV,P	Application Reset	28
P32_OMR	Port 32 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	32
P32_ID	Port 32 Identification Register	008 _H	U,SV	BE	Application Reset	35
	Reserved (004 _H Byte)	00C _H	BE	BE		
P32_IOCRO	Port 32 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 38	38
P32_IOCRA	Port 32 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 39	39
	Reserved (004 _H Byte)	020 _H	BE	BE		
P32_IN	Port 32 Input Register	024 _H	U,SV	BE	Application Reset	48
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P32_PDR0	Port 32 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 49	49

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 72 Register Overview - P32 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte) (x=0-1)	048 _H +x* 4	BE	BE		
P32_ESR	Port 32 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	60
	Reserved (004 _H Byte) (x=0-2)	054 _H +x* 4	BE	BE		
P32_PDISC	Port 32 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 67	67
P32_PCSR	Port 32 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	72
	Reserved (004 _H Byte) (x=0-1)	068 _H +x* 4	BE	BE		
P32_OMSR0	Port 32 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	76
P32_OMSR4	Port 32 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	77
P32_OMCR0	Port 32 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	83
P32_OMCR4	Port 32 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	84
P32_OMSR	Port 32 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	91
P32_OMCR	Port 32 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	95
	Reserved (004 _H Byte) (x=0-1)	098 _H +x* 4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x* 4	BE	BE		
P32_ACCEN1	Port 32 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	104
P32_ACCEN0	Port 32 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	107

Table 73 Register Overview - P33 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P33_OUT	Port 33 Output Register	000 _H	U,SV	U,SV,P	Application Reset	25
P33_OMR	Port 33 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	29

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 73 Register Overview - P33 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P33_ID	Port 33 Identification Register	008 _H	U,SV	BE	Application Reset	35
	Reserved (004 _H Byte)	00C _H	BE	BE		
P33_IOCRO	Port 33 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 38	38
P33_IOCRA	Port 33 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 41	41
P33_IOCRA8	Port 33 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
P33_IOCRA12	Port 33 Input/Output Control Register 12	01C _H	U,SV	U,SV,P	See page 44	44
	Reserved (004 _H Byte)	020 _H	BE	BE		
P33_IN	Port 33 Input Register	024 _H	U,SV	BE	Application Reset	46
	Reserved (004 _H Byte) (x=0-5)	028 _H +x*4	BE	BE		
P33_PDR0	Port 33 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 52	52
P33_PDR1	Port 33 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 54	54
	Reserved (004 _H Byte) (x=0-1)	048 _H +x*4	BE	BE		
P33_ESR	Port 33 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	61
	Reserved (004 _H Byte) (x=0-2)	054 _H +x*4	BE	BE		
P33_PDISC	Port 33 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 62	62
P33_PCSR	Port 33 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	72
	Reserved (004 _H Byte) (x=0-1)	068 _H +x*4	BE	BE		
P33_OMSR0	Port 33 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	76
P33_OMSR4	Port 33 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	78
P33_OMSR8	Port 33 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P33_OMSR12	Port 33 Output Modification Set Register 12	07C _H	U,SV	U,SV,P	Application Reset	80

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 73 Register Overview - P33 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P33_OMCR0	Port 33 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	83
P33_OMCR4	Port 33 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	85
P33_OMCR8	Port 33 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P33_OMCR12	Port 33 Output Modification Clear Register 12	08C _H	U,SV	U,SV,P	Application Reset	87
P33_OMSR	Port 33 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	88
P33_OMCR	Port 33 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	92
	Reserved (004 _H Byte) (x=0-1)	098 _H +x* 4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x* 4	BE	BE		
P33_ACCEN1	Port 33 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	104
P33_ACCEN0	Port 33 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	107

Table 74 Register Overview - P40 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P40_OUT	Port 40 Output Register	000 _H	U,SV	U,SV,P	Application Reset	26
P40_OMR	Port 40 Output Modification Register	004 _H	U,SV	U,SV,P	Application Reset	30
P40_ID	Port 40 Identification Register	008 _H	U,SV	BE	Application Reset	35
	Reserved (004 _H Byte)	00C _H	BE	BE		
P40_IOCRO	Port 40 Input/Output Control Register 0	010 _H	U,SV	U,SV,P	See page 38	38
P40_IOCR4	Port 40 Input/Output Control Register 4	014 _H	U,SV	U,SV,P	See page 41	41
P40_IOCR8	Port 40 Input/Output Control Register 8	018 _H	U,SV	U,SV,P	See page 42	42
	Reserved (004 _H Byte)	020 _H	BE	BE		
P40_IN	Port 40 Input Register	024 _H	U,SV	BE	Application Reset	47

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 74 Register Overview - P40 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004 _H Byte) (x=0-5)	028 _H +x* 4	BE	BE		
P40_PDR0	Port 40 Pad Driver Mode Register 0	040 _H	U,SV	SV,E,P	See page 52	52
P40_PDR1	Port 40 Pad Driver Mode Register 1	044 _H	U,SV	SV,E,P	See page 55	55
	Reserved (004 _H Byte) (x=0-1)	048 _H +x* 4	BE	BE		
P40_ESR	Port 40 Emergency Stop Register	050 _H	U,SV	SV,E,P	Application Reset	62
	Reserved (004 _H Byte) (x=0-2)	054 _H +x* 4	BE	BE		
P40_PDISC	Port 40 Pin Function Decision Control Register	060 _H	U,SV	SV,E,P	See page 64	64
P40_PCSR	Port 40 Pin Controller Select Register	064 _H	U,SV	SV,SE	Application Reset	73
	Reserved (004 _H Byte) (x=0-1)	068 _H +x* 4	BE	BE		
P40_OMSR0	Port 40 Output Modification Set Register 0	070 _H	U,SV	U,SV,P	Application Reset	76
P40_OMSR4	Port 40 Output Modification Set Register 4	074 _H	U,SV	U,SV,P	Application Reset	78
P40_OMSR8	Port 40 Output Modification Set Register 8	078 _H	U,SV	U,SV,P	Application Reset	79
P40_OMCR0	Port 40 Output Modification Clear Register 0	080 _H	U,SV	U,SV,P	Application Reset	83
P40_OMCR4	Port 40 Output Modification Clear Register 4	084 _H	U,SV	U,SV,P	Application Reset	85
P40_OMCR8	Port 40 Output Modification Clear Register 8	088 _H	U,SV	U,SV,P	Application Reset	86
P40_OMSR	Port 40 Output Modification Set Register	090 _H	U,SV	U,SV,P	Application Reset	89
P40_OMCR	Port 40 Output Modification Clear Register	094 _H	U,SV	U,SV,P	Application Reset	93
	Reserved (004 _H Byte) (x=0-1)	098 _H +x* 4	BE	BE		
	Reserved (004 _H Byte) (x=0-13)	0C0 _H +x* 4	BE	BE		

General Purpose I/O Ports and Peripheral I/O Lines (Ports)**Table 74 Register Overview - P40 (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P40_ACCEN1	Port 40 Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	104
P40_ACCEN0	Port 40 Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	107

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

14.3 Pn Registers

14.3.1 SPB bus slave interface

Port 00 Output Register

The port output register determines the value of a GPIO pin when it is selected by Pn_IOC Rx as output. Writing a 0 to a Pn_OUT.Px (x = 0-15) bit position delivers a low level at the corresponding output pin. A high level is output when the corresponding bit is written with a 1. Note that the bits of Pn_OUT.Px can be individually set or cleared by writing appropriate values into the port output modification set register Pn_OMSR or port output modification clear register Pn_OMCR, respectively. The Pn_OUT.Px bits can also be set, cleared or toggled with register Pn_OMR within the same write operation.

P00_OUT

Port 00 Output Register (000_H) Application Reset Value: 0000 0000_H

P11_OUT

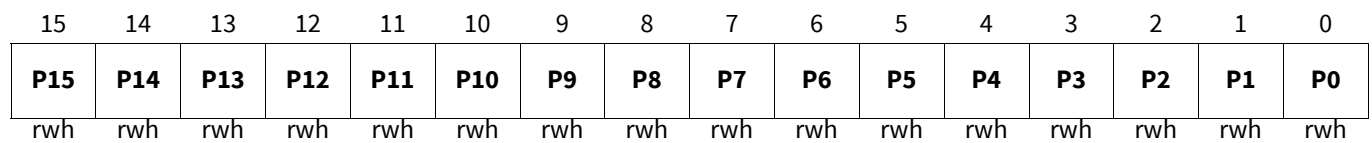
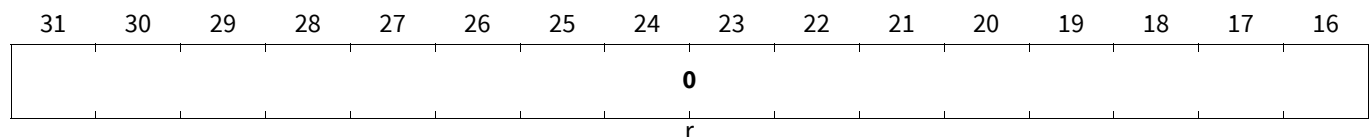
Port 11 Output Register (000_H) Application Reset Value: 0000 0000_H

P20_OUT

Port 20 Output Register (000_H) Application Reset Value: 0000 0000_H

P33_OUT

Port 33 Output Register (000_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
Px (x=0-15)	x	rwh	Output Bit x This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0 _B The output level of Pn.x is 0. 1 _B The output level of Pn.x is 1.
0	31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 75 Access Mode Restrictions sorted by descending priority

Applies to **P00_OUT**

Applies to **P11_OUT**

Applies to **P20_OUT**

Applies to **P33_OUT**

Mode Name	Access Mode	Description
Master enabled in ACCEN	rwh Px (x=0-15)	write access for enabled masters
Otherwise (default)	rh Px (x=0-15)	

P02_OUT

Port 02 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P10_OUT

Port 10 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P14_OUT

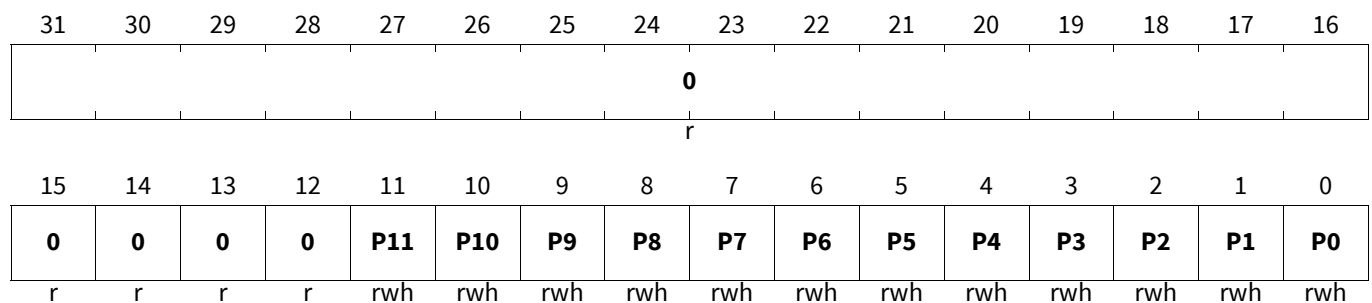
Port 14 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P15_OUT

Port 15 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P40_OUT

Port 40 Output Register (000_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
Px (x=0-11)	x	rwh	Output Bit x This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0 _B The output level of Pn.x is 0. 1 _B The output level of Pn.x is 1.
0	15, 14, 13, 12, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 76 Access Mode Restrictions sorted by descending priority

Applies to **P02_OUT**
 Applies to **P10_OUT**
 Applies to **P14_OUT**
 Applies to **P15_OUT**
 Applies to **P40_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-11)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-11)	

P12_OUT

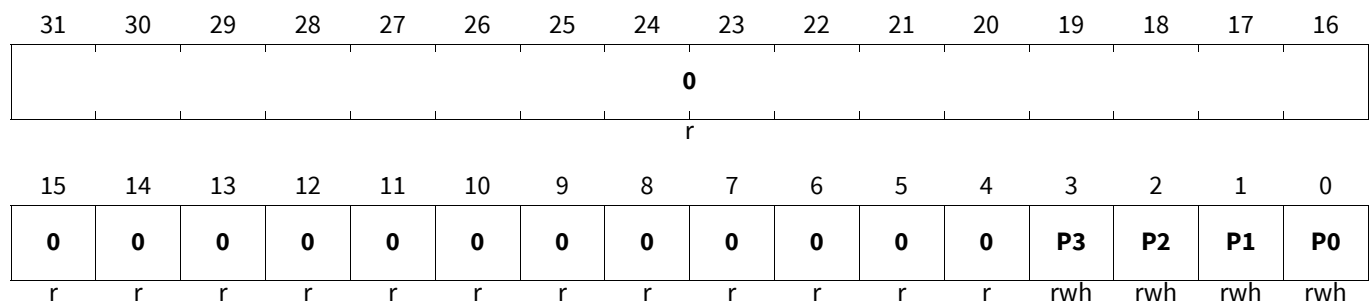
Port 12 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P13_OUT

Port 13 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P22_OUT

Port 22 Output Register (000_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
Px (x=0-3)	x	rwh	Output Bit x This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0 _B The output level of Pn.x is 0. 1 _B The output level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 77 Access Mode Restrictions sorted by descending priority

Applies to **P12_OUT**

Applies to **P13_OUT**

Applies to **P22_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-3)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-3)	

P21_OUT

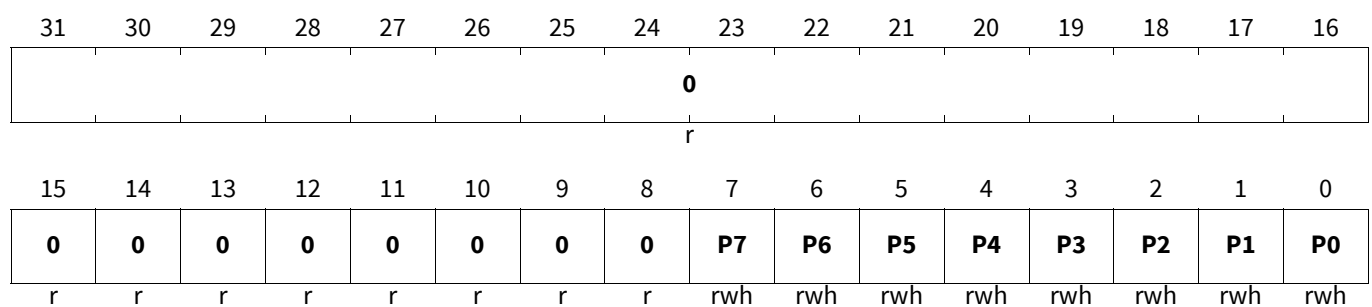
Port 21 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P23_OUT

Port 23 Output Register (000_H) **Application Reset Value: 0000 0000_H**

P32_OUT

Port 32 Output Register (000_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
Px (x=0-7)	x	rwh	Output Bit x This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0 _B The output level of Pn.x is 0. 1 _B The output level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 78 Access Mode Restrictions sorted by descending priority

Applies to **P21_OUT**

Applies to **P23_OUT**

Applies to **P32_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-7)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-7)	

Port 00 Output Modification Register

The port output modification register contains control bits that make it possible to individually set, clear or toggle the logic state of a single port line by manipulating the output register.

P00_OMR

Port 00 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P11_OMR

Port 11 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P20_OMR

Port 20 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P33_OMR

Port 33 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL9	PCL8	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-15)	x	w0	Set Bit x Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Sets or toggles Pn_OUT.Px.
PCLx (x=0-15)	x+16	w0	Clear Bit x Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Clears or toggles Pn_OUT.Px.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 79 Access Mode Restrictions sorted by descending priority

Applies to [P00_OMR](#)

Applies to [P11_OMR](#)

Applies to [P20_OMR](#)

Applies to [P33_OMR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15), PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15), PSx (x=0-15)	

Note: Register Pn_OMR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Table 80 Function of the Bits PCLx and PSx

PCLx	PSx	Function
0	0	Bit Pn_OUT.Px is not changed.
0	1	Bit Pn_OUT.Px is set.
1	0	Bit Pn_OUT.Px is reset.
1	1	Bit Pn_OUT.Px is toggled.

P02_OMR

Port 02 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P10_OMR

Port 10 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P14_OMR

Port 14 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P15_OMR

Port 15 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P40_OMR

Port 40 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	PCL11	PCL10	PCL9	PCL8	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-11)	x	w0	Set Bit x Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Sets or toggles Pn_OUT.Px.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=0-11)	x+16	w0	Clear Bit x Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Clears or toggles Pn_OUT.Px.
0	15, 14, 13, 12, 31, 30, 29, 28	r	Reserved Read as 0; should be written with 0.

Table 81 Access Mode Restrictions sorted by descending priority

Applies to [P02_OMR](#)
 Applies to [P10_OMR](#)
 Applies to [P14_OMR](#)
 Applies to [P15_OMR](#)
 Applies to [P40_OMR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-11), PSx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-11), PSx (x=0-11)	

P12_OMR
Port 12 Output Modification Register (004_H) **Application Reset Value: 0000 0000_H**
P13_OMR
Port 13 Output Modification Register (004_H) **Application Reset Value: 0000 0000_H**
P22_OMR
Port 22 Output Modification Register (004_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PS3	PS2	PS1	PS0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-3)	x	w0	Set Bit x Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Sets or toggles Pn_OUT.Px.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	Clear Bit x Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Clears or toggles Pn_OUT.Px.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20	r	Reserved Read as 0; should be written with 0.

Table 82 Access Mode Restrictions sorted by descending priority

Applies to [P12_OMR](#)
Applies to [P13_OMR](#)
Applies to [P22_OMR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3), PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3), PSx (x=0-3)	

P21_OMR

Port 21 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P23_OMR

Port 23 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

P32_OMR

Port 32 Output Modification Register (004_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-7)	x	w0	Set Bit x Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Sets or toggles Pn_OUT.Px.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=0-7)	x+16	w0	Clear Bit x Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in Table 80 . 0 _B No operation 1 _B Clears or toggles Pn_OUT.Px.
0	15, 14, 13, 12, 11, 10, 9, 8, 31, 30, 29, 28, 27, 26, 25, 24	r	Reserved Read as 0; should be written with 0.

Table 83 Access Mode Restrictions sorted by descending priority

Applies to [P21_OMR](#)

Applies to [P23_OMR](#)

Applies to [P32_OMR](#)

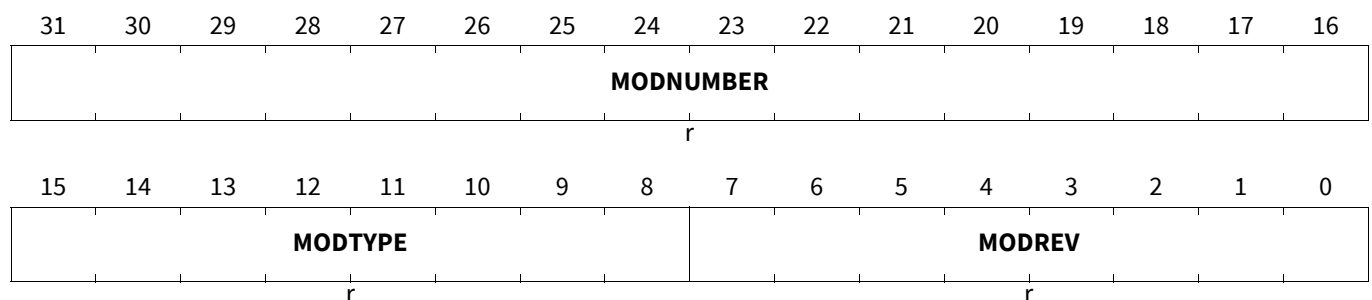
Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-7), PSx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-7), PSx (x=0-7)	

Port 00 Identification Register

The module Identification Register ID contains read-only information about the module version.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

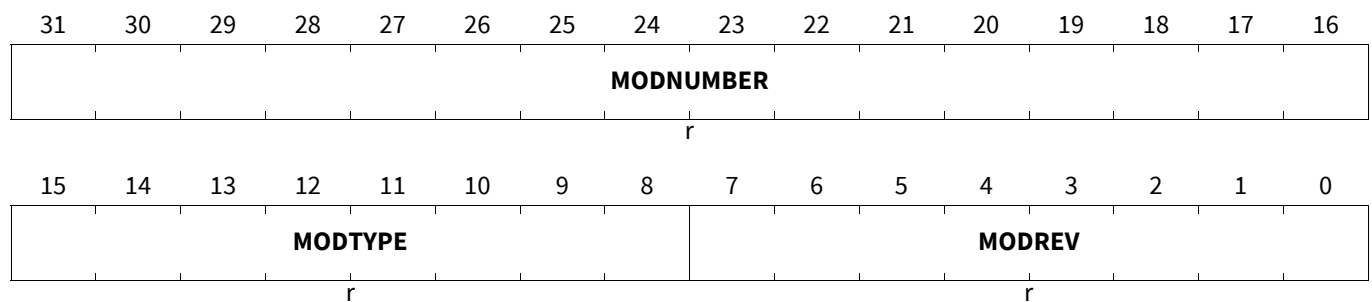
P00_ID		
Port 00 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P02_ID		
Port 02 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P10_ID		
Port 10 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P11_ID		
Port 11 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P12_ID		
Port 12 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P13_ID		
Port 13 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P14_ID		
Port 14 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P15_ID		
Port 15 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P20_ID		
Port 20 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P21_ID		
Port 21 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H



Field	Bits	Type	Description
MODREV	7:0	r	Module Revision Number This bit field indicates the revision number of the TC36x module (01 _H = first revision).
MODTYPE	15:8	r	Module Type This bit field is C0 _H . It defines a 32-bit module
MODNUMBER	31:16	r	Module Number This bit field defines the module identification number. The value for the Ports module is 00C8 _H

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P22_ID		
Port 22 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P23_ID		
Port 23 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P32_ID		
Port 32 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P33_ID		
Port 33 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H
P40_ID		
Port 40 Identification Register	(008_H)	Application Reset Value: 00C8 C0XX_H



Field	Bits	Type	Description
MODREV	7:0	r	Module Revision Number This bit field indicates the revision number of the TC36x module (01 _H = first revision).
MODTYPE	15:8	r	Module Type This bit field is C0 _H . It defines a 32-bit module
MODNUMBER	31:16	r	Module Number This bit field defines the module identification number. The value for the Ports module is 00C8 _H

Port 00 Input/Output Control Register 0

The port input/output control registers select the digital output and input driver functionality and characteristics of a GPIO port pin. Port direction (input or output), pull-up, pull-down, or no pull devices for inputs, and push-pull or open-drain functionality for outputs can be selected by the corresponding bit fields PC_x (x = 0-15). Each 32-bit wide port input/output control register controls four GPIO port lines:

- Register P_n_IOCR0 controls the P_n.[3:0] port lines
- Register P_n_IOCR4 controls the P_n.[7:4] port lines
- Register P_n_IOCR8 controls the P_n.[11:8] port lines
- Register P_n_IOCR12 controls the P_n.[15:12] port lines

The structure with one control bit field for each port pin located in different register bytes offers the possibility to configure the port pin functionality of a single pin with byte-oriented accesses without accessing the other PC_x bit fields.

The reset values of 1010 1010_H and 0000 0000_H for P_n_IOCR_x registers represents input pull-up and no input pull device (tri-state mode) being activated, respectively. The switching of the intended mode of the device is controlled by HWCFG6. When a cold reset is activated and HWCFG6=1, the port pins except P33.8, P40 and P41 are set to input pull-up mode, P33.8, P40 and P41 are in tri-state mode as long as PORST is activated. If HWCFG6=0, the pins have the default state of tri-state mode. The pad state can also be configured by software through

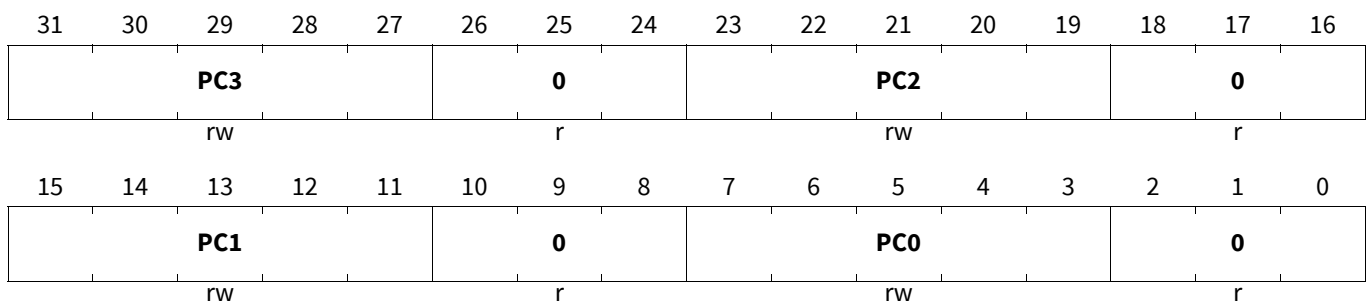
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

PMSWCR5.TRISTREQ bit. In the event of a warm reset or wake-up from standby mode, PMSWCR5.TRISTREQ is not affected by reset, hence Pn_IOCRx registers have the reset values configured as per the last state of the TRISTREQ bit.

Note: In LVDS (RX and TX) operation the IOCR register of both pins of the LVDS pair must be configured as output, i.e. 1xxx_B. This ensures that the pull devices are disconnected and don't interfere with LVDS operation.

Register Pn_IOCR0 controls the Pn.[3:0] port lines

P00_IOCR0															
Port 00 Input/Output Control Register 0															
P02_IOCR0															
Port 02 Input/Output Control Register 0															
P10_IOCR0															
Port 10 Input/Output Control Register 0															
P11_IOCR0															
Port 11 Input/Output Control Register 0															
P12_IOCR0															
Port 12 Input/Output Control Register 0															
P13_IOCR0															
Port 13 Input/Output Control Register 0															
P14_IOCR0															
Port 14 Input/Output Control Register 0															
P15_IOCR0															
Port 15 Input/Output Control Register 0															
P20_IOCR0															
Port 20 Input/Output Control Register 0															
P21_IOCR0															
Port 21 Input/Output Control Register 0															



Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	Port Control for Pin x This bit field defines the Port n line x functionality according to Table 86 .
0	26:24, 18:16, 10:8, 2:0	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 84 Access Mode Restrictions sorted by descending priority

Applies to **P00_IOCR0**

Applies to **P02_IOCR0**

Applies to **P10_IOCR0**

Applies to **P11_IOCR0**

Applies to **P12_IOCR0**

Applies to **P13_IOCR0**

Applies to **P14_IOCR0**

Applies to **P15_IOCR0**

Applies to **P20_IOCR0**

Applies to **P21_IOCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

Table 85 Reset Values

Applies to **P00_IOCR0**

Applies to **P02_IOCR0**

Applies to **P10_IOCR0**

Applies to **P11_IOCR0**

Applies to **P12_IOCR0**

Applies to **P13_IOCR0**

Applies to **P14_IOCR0**

Applies to **P15_IOCR0**

Applies to **P20_IOCR0**

Applies to **P21_IOCR0**

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 _H	HWCFG6 is 1 (input pull-up mode)

Port Control Coding

Table 86 describes the coding of the PCx bit fields that determine the port line functionality.

Table 86 PCx Coding

PCx[4:0]	I/O	Characteristics	Selected Pull-up / Pull-down / Selected Output Function
0XX00 _B	Input	–	No input pull device connected, tri-state mode
0XX01 _B			Input pull-down device connected
0XX10 _B			Input pull-up device connected ¹⁾
0XX11 _B			No input pull device connected, tri-state mode

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 86 PCx Coding (cont'd)

PCx[4:0]	I/O	Characteristics	Selected Pull-up / Pull-down / Selected Output Function
10000 _B	Output	Push-pull	General-purpose output
10001 _B			Alternate output function 1
10010 _B			Alternate output function 2
10011 _B			Alternate output function 3
10100 _B			Alternate output function 4
10101 _B			Alternate output function 5
10110 _B			Alternate output function 6
10111 _B			Alternate output function 7
11000 _B		Open-drain	General-purpose output
11001 _B			Alternate output function 1
11010 _B			Alternate output function 2
11011 _B			Alternate output function 3
11100 _B			Alternate output function 4
11101 _B			Alternate output function 5
11110 _B			Alternate output function 6
11111 _B			Alternate output function 7

1) This is the default pull device setting after reset for powertrain applications.

P22_IOCRO

Port 22 Input/Output Control Register 0 (010_H) **Reset Value: Table 88**

P23_IOCRO

Port 23 Input/Output Control Register 0 (010_H) **Reset Value: Table 88**

P32_IOCRO

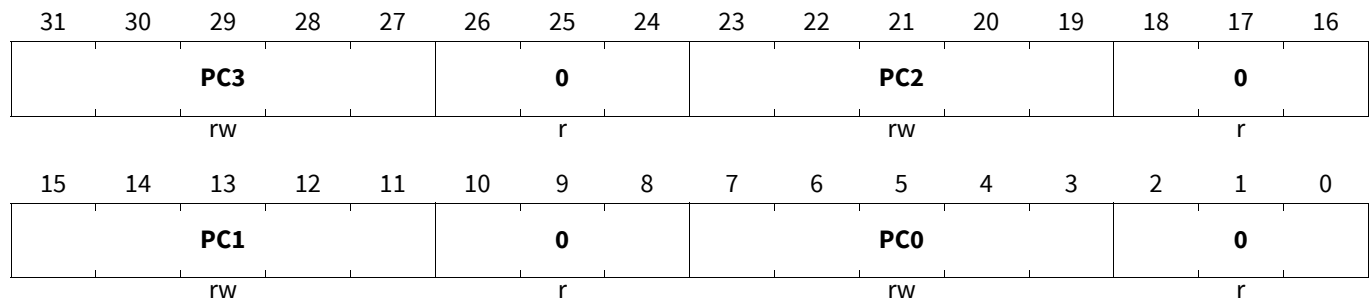
Port 32 Input/Output Control Register 0 (010_H) **Reset Value: Table 88**

P33_IOCRO

Port 33 Input/Output Control Register 0 (010_H) **Reset Value: Table 88**

P40_IOCRO

Port 40 Input/Output Control Register 0 (010_H) **Reset Value: Table 89**



Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	Port Control for Pin x This bit field defines the Port n line x functionality according to Table 86 .

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	26:24, 18:16, 10:8, 2:0	r	Reserved Read as 0; should be written with 0.

Table 87 Access Mode Restrictions sorted by descending priority

Applies to [P22_IOCRO](#)

Applies to [P23_IOCRO](#)

Applies to [P32_IOCRO](#)

Applies to [P33_IOCRO](#)

Applies to [P40_IOCRO](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

Table 88 Reset Values variant 1

Applies to [P22_IOCRO](#)

Applies to [P23_IOCRO](#)

Applies to [P32_IOCRO](#)

Applies to [P33_IOCRO](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 _H	HWCFG6 is 1 (input pull-up mode)

Table 89 Reset Values of [P40_IOCRO](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 _H	HWCFG6 is 1 (input pull-up mode)

Port 00 Input/Output Control Register 4

Register Pn_IOCRO4 controls the Pn.[7:4] port lines

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_IOC4 Port 00 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P02_IOC4 Port 02 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P10_IOC4 Port 10 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P11_IOC4 Port 11 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P14_IOC4 Port 14 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P15_IOC4 Port 15 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P20_IOC4 Port 20 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P21_IOC4 Port 21 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P23_IOC4 Port 23 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91
P32_IOC4 Port 32 Input/Output Control Register 4	(014 _H)	Reset Value: Table 91

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC7				0	PC6				0						
rw				r	rw				r						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC5				0	PC4				0						
rw				r	rw				r						

Field	Bits	Type	Description
PCx (x=4-7)	8*x-25:8*x-29	rw	Port Control for Port 00 Pin x This bit field defines the Port n line x functionality according to Table 86 .
0	26:24, 18:16, 10:8, 2:0	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 90 Access Mode Restrictions sorted by descending priority

Applies to [P00_IOCR4](#)
 Applies to [P02_IOCR4](#)
 Applies to [P10_IOCR4](#)
 Applies to [P11_IOCR4](#)
 Applies to [P14_IOCR4](#)
 Applies to [P15_IOCR4](#)
 Applies to [P20_IOCR4](#)
 Applies to [P21_IOCR4](#)
 Applies to [P23_IOCR4](#)
 Applies to [P32_IOCR4](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=4-7)	write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)	

Table 91 Reset Values

Applies to [P00_IOCR4](#)
 Applies to [P02_IOCR4](#)
 Applies to [P10_IOCR4](#)
 Applies to [P11_IOCR4](#)
 Applies to [P14_IOCR4](#)
 Applies to [P15_IOCR4](#)
 Applies to [P20_IOCR4](#)
 Applies to [P21_IOCR4](#)
 Applies to [P23_IOCR4](#)
 Applies to [P32_IOCR4](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 _H	HWCFG6 is 1 (input pull-up mode)

P33_IOCR4

Port 33 Input/Output Control Register 4 (014_H)

Reset Value: [Table 93](#)

P40_IOCR4

Port 40 Input/Output Control Register 4 (014_H)

Reset Value: [Table 94](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC7			0			PC6			0						
rw			r			rw			r						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC5			0			PC4			0						
rw			r			rw			r						

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCx (x=4-7)	8*x-25:8*x-29	rw	Port Control for Port 33 Pin x This bit field defines the Port n line x functionality according to Table 86 .
0	26:24, 18:16, 10:8, 2:0	r	Reserved Read as 0; should be written with 0.

Table 92 Access Mode Restrictions sorted by descending priority

Applies to [P33_IOCR4](#)

Applies to [P40_IOCR4](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=4-7)	write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)	

Table 93 Reset Values of [P33_IOCR4](#)

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 _H	HWCFG6 is 1 (input pull-up mode)

Table 94 Reset Values of [P40_IOCR4](#)

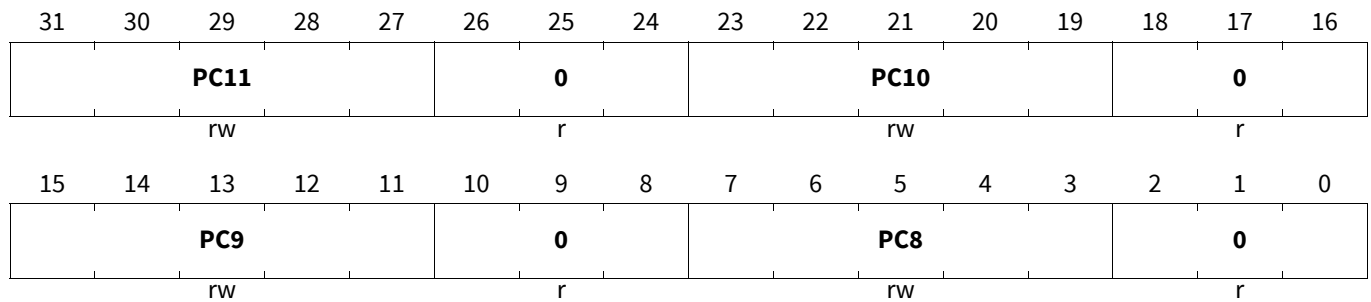
Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 _H	HWCFG6 is 1 (input pull-up mode)

Port 00 Input/Output Control Register 8

Register Pn_IOCR8 controls the Pn.[11:8] port lines

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_IOC8	Port 00 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P02_IOC8	Port 02 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P10_IOC8	Port 10 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P11_IOC8	Port 11 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P14_IOC8	Port 14 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P15_IOC8	Port 15 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P20_IOC8	Port 20 Input/Output Control Register 8	(018 _H)	Reset Value: Table 96
P33_IOC8	Port 33 Input/Output Control Register 8	(018 _H)	Reset Value: Table 97
P40_IOC8	Port 40 Input/Output Control Register 8	(018 _H)	Reset Value: Table 98



Field	Bits	Type	Description
PCx (x=8-11)	8*x-57:8*x-61	rw	Port Control for Port 00 Pin x This bit field defines the Port n line x functionality according to Table 86 .
0	26:24, 18:16, 10:8, 2:0	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 95 Access Mode Restrictions sorted by descending priority

Applies to **P00_IOCR8**

Applies to **P02_IOCR8**

Applies to **P10_IOCR8**

Applies to **P11_IOCR8**

Applies to **P14_IOCR8**

Applies to **P15_IOCR8**

Applies to **P20_IOCR8**

Applies to **P33_IOCR8**

Applies to **P40_IOCR8**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PCx (x=8-11)	

Table 96 Reset Values variant 1

Applies to **P00_IOCR8**

Applies to **P02_IOCR8**

Applies to **P10_IOCR8**

Applies to **P11_IOCR8**

Applies to **P14_IOCR8**

Applies to **P15_IOCR8**

Applies to **P20_IOCR8**

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 _H	HWCFG6 is 1 (input pull-up mode)

Table 97 Reset Values of P33_IOCR8

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1000 _H	HWCFG6 is 1 (input pull-up mode)

Table 98 Reset Values of P40_IOCR8

Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	0000 0000 _H	HWCFG6 is 1 (input pull-up mode)

Port 00 Input/Output Control Register 12

Register Pn_IOCR12 controls the Pn.[15:12] port lines

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_IOCR12		
Port 00 Input/Output Control Register 12	(01C _H)	Reset Value: Table 100
P11_IOCR12		
Port 11 Input/Output Control Register 12	(01C _H)	Reset Value: Table 100
P20_IOCR12		
Port 20 Input/Output Control Register 12	(01C _H)	Reset Value: Table 100
P33_IOCR12		
Port 33 Input/Output Control Register 12	(01C _H)	Reset Value: Table 100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC15				0				PC14				0			
rw				r				rw				r			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC13				0				PC12				0			
rw				r				rw				r			

Field	Bits	Type	Description
PCx (x=12-15)	8*x-89:8*x-93	rw	Port Control for Port 00 Pin x This bit field defines the Port n line x functionality according to Table 86 .
0	26:24, 18:16, 10:8, 2:0	r	Reserved Read as 0; should be written with 0.

Table 99 Access Mode Restrictions sorted by descending priority

Applies to [P00_IOCR12](#)
 Applies to [P11_IOCR12](#)
 Applies to [P20_IOCR12](#)
 Applies to [P33_IOCR12](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=12-15)	write access for enabled masters
Otherwise (default)	r	PCx (x=12-15)	

Table 100 Reset Values

Applies to [P00_IOCR12](#)
 Applies to [P11_IOCR12](#)
 Applies to [P20_IOCR12](#)
 Applies to [P33_IOCR12](#)

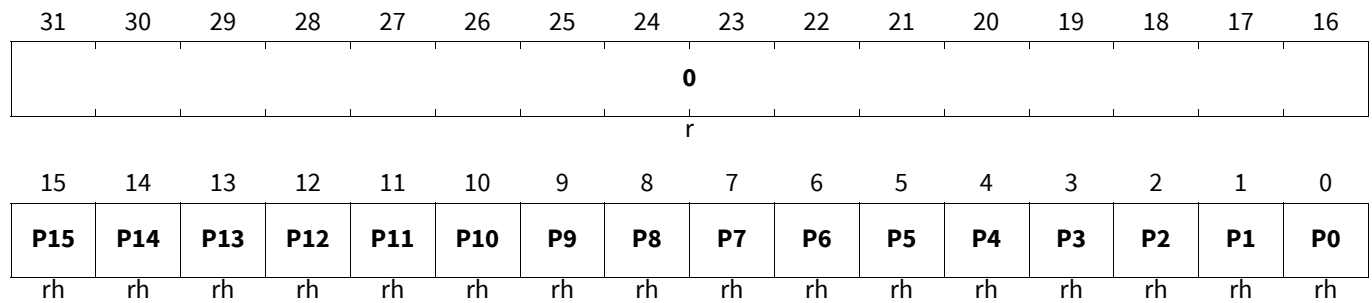
Reset Type	Reset Value	Note
Application Reset	0000 0000 _H	HWCFG6 is 0 (tri-state mode)
Application Reset	1010 1010 _H	HWCFG6 is 1 (input pull-up mode)

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Port 00 Input Register

The logic level of a GPIO pin can be read via the read-only port input register Pn_IN. Reading the Pn_IN register always returns the current logical value at the GPIO pin independently whether the pin is selected as input or output.

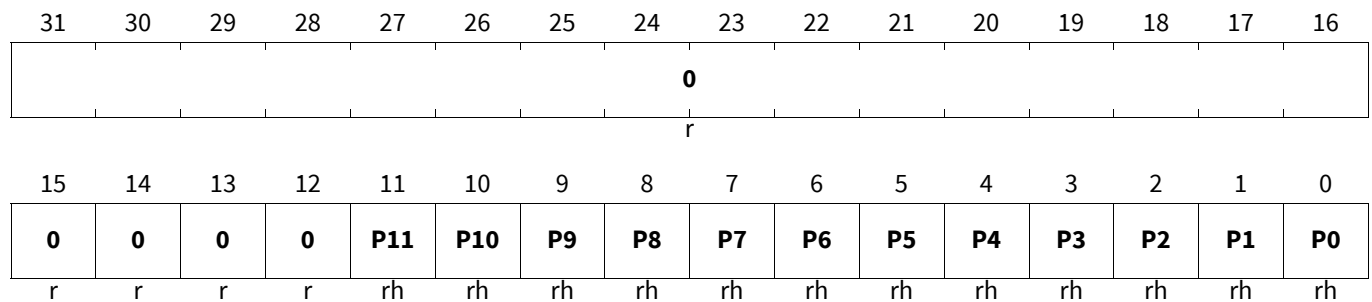
P00_IN		
Port 00 Input Register	(024_H)	Application Reset Value: 0000 XXXX_H
P11_IN		
Port 11 Input Register	(024_H)	Application Reset Value: 0000 XXXX_H
P20_IN		
Port 20 Input Register	(024_H)	Application Reset Value: 0000 XXXX_H
P33_IN		
Port 33 Input Register	(024_H)	Application Reset Value: 0000 XXXX_H



Field	Bits	Type	Description
Px (x=0-15)	x	rh	Input Bit x This bit indicates the level at the input pin Pn.x. 0 _B The input level of Pn.x is 0. 1 _B The input level of Pn.x is 1.
0	31:16	r	Reserved Read as 0.

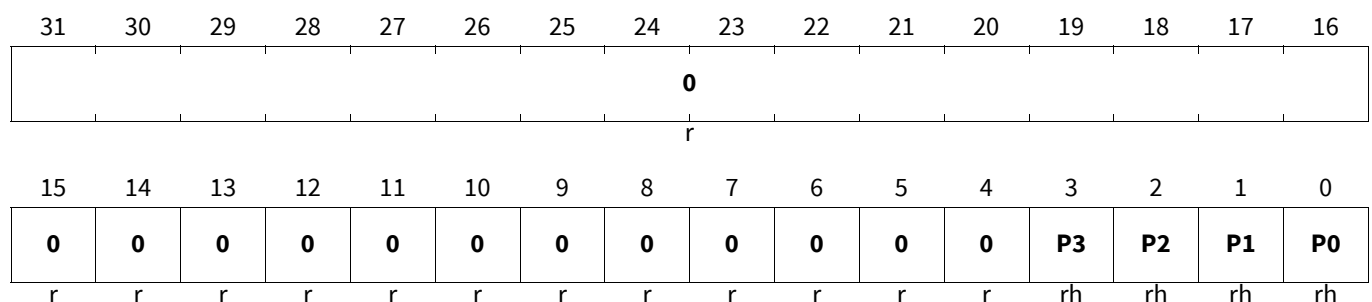
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P02_IN Port 02 Input Register	(024 _H)	Application Reset Value: 0000 0XXX_H
P10_IN Port 10 Input Register	(024 _H)	Application Reset Value: 0000 0XXX_H
P14_IN Port 14 Input Register	(024 _H)	Application Reset Value: 0000 0XXX_H
P15_IN Port 15 Input Register	(024 _H)	Application Reset Value: 0000 0XXX_H
P40_IN Port 40 Input Register	(024 _H)	Application Reset Value: 0000 0XXX_H



Field	Bits	Type	Description
Px (x=0-11)	x	rh	Input Bit x This bit indicates the level at the input pin Pn.x. 0 _B The input level of Pn.x is 0. 1 _B The input level of Pn.x is 1.
0	15, 14, 13, 12, 31:16	r	Reserved Read as 0; should be written with 0.

P12_IN Port 12 Input Register	(024 _H)	Application Reset Value: 0000 000X_H
P13_IN Port 13 Input Register	(024 _H)	Application Reset Value: 0000 000X_H
P22_IN Port 22 Input Register	(024 _H)	Application Reset Value: 0000 000X_H



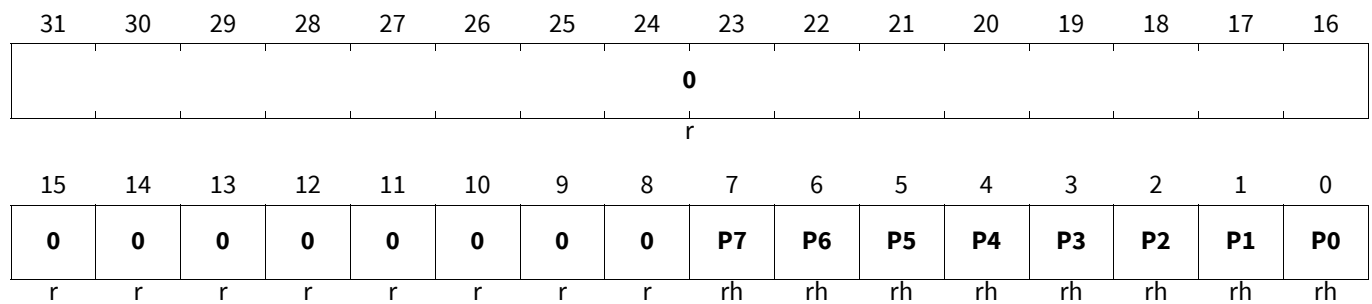
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Px (x=0-3)	x	rh	Input Bit x This bit indicates the level at the input pin Pn.x. 0 _B The input level of Pn.x is 0. 1 _B The input level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	Reserved Read as 0; should be written with 0.

P21_IN
Port 21 Input Register (024_H) Application Reset Value: 0000 00XX_H

P23_IN
Port 23 Input Register (024_H) Application Reset Value: 0000 00XX_H

P32_IN
Port 32 Input Register (024_H) Application Reset Value: 0000 00XX_H



Field	Bits	Type	Description
Px (x=0-7)	x	rh	Input Bit x This bit indicates the level at the input pin Pn.x. 0 _B The input level of Pn.x is 0. 1 _B The input level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Port 00 Pad Driver Mode Register 0

P00_PDR0		
Port 00 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P02_PDR0		
Port 02 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P10_PDR0		
Port 10 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P11_PDR0		
Port 11 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P14_PDR0		
Port 14 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P15_PDR0		
Port 15 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P20_PDR0		
Port 20 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P21_PDR0		
Port 21 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P23_PDR0		
Port 23 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102
P32_PDR0		
Port 32 Pad Driver Mode Register 0	(040 _H)	Reset Value: Table 102

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL7	PD7	PL6	PD6	PL5	PD5	PL4	PD4								
rw	rw	rw	rw	rw	rw	rw	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL3	PD3	PL2	PD2	PL1	PD1	PL0	PD0								
rw	rw	rw	rw	rw	rw	rw	rw								

Field	Bits	Type	Description
PDx (x=0-7)	4*x+1:4*x	rw	Pad Driver Mode for Pin x
PLx (x=0-7)	4*x+3:4*x+2	rw	Pad Level Selection for Pin x

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 101 Access Mode Restrictions sorted by descending priority

Applies to **P00_PDR0**

Applies to **P02_PDR0**

Applies to **P10_PDR0**

Applies to **P11_PDR0**

Applies to **P14_PDR0**

Applies to **P15_PDR0**

Applies to **P20_PDR0**

Applies to **P21_PDR0**

Applies to **P23_PDR0**

Applies to **P32_PDR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)	

Table 102 Reset Values

Applies to **P00_PDR0**

Applies to **P02_PDR0**

Applies to **P10_PDR0**

Applies to **P11_PDR0**

Applies to **P14_PDR0**

Applies to **P15_PDR0**

Applies to **P20_PDR0**

Applies to **P21_PDR0**

Applies to **P23_PDR0**

Applies to **P32_PDR0**

Reset Type	Reset Value	Note
After SSW execution	2222 2222 _H	Initial value in largest package
After SSW execution	---- ---- _H	Initial value package dependent

Output Characteristics

The pad structure of the GPIO lines offers the possibility to select the output driver strength and the slew rate. These two parameters are controlled by the PDx bit fields in the pad driver mode registers Pn_PDR0/1 for output modes. The available modes depend on the respective pad type.

Table 103 Pad Driver Mode Selection for RFast Pads

PDx.1	PDx.0	Speed Grade	Driver Setting
0	0	1	Strong driver, sharp edge (“ss”)
0	1	2	Strong driver, medium edge (“sm”)
1	0	3	Medium driver (“m”)
1	1	4	RGMII driver.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 104 Pad Driver Mode Selection for Fast Pads

PDx.1	PDx.0	Speed Grade	Driver Setting
0	0	1	Strong driver, sharp edge (“ss”)
0	1	2	Strong driver, medium edge (“sm”)
1	0	3	Medium driver (“m”)
1	1	4	TC39x A-Step: Medium driver (“m”) Else: Reserved when operating as output. When operating as input see below “Pad Level Selection for Input Function”.

Table 105 Pad Driver Mode Selection for Slow Pads

PDx.1	PDx.0	Speed Grade	Driver Setting
X	0	1	Medium driver, sharp edge (“sm”) ¹⁾
X	1	2	Medium driver (“m”)

1) This setting is marked “sm” as the electrical characteristics are identical to the strong driver medium edge setting. The Data Sheet contains also only common “sm” tables.

Note: The Data Sheet describes the DC characteristics of all pad classes.

TTL/Automotive Input Selection

The input function can operate with different VIH and VIL levels depending on the pad supply voltage, the pad type and the selection done by the PLx bits of the Pn_PDRx as of [Table 106](#). PLx.1 changes additionally the pull-up and pull-down resistors.

Table 106 Pad Level Selection for Input Function

PLx.1	PLx.0	Input Levels
0	X	Automotive level “AL”.
1	0	TTL level for 5V pad supply. Degraded TTL level used for CIF when pad supply is 3.3V
1	1	TTL level for 3.3V pad supply.
X	X	Only for pads with RGMII input buffer (marked “RGMII_Input” in the pinning table): <ul style="list-style-type: none"> when PDx.1=1 and PDx.0=1 the input level RGMII is selected. for other PDx values the input level is determined by PLx as for all other pads (first three rows of this table).

LVDS

The default CMOS mode can be switched to LVDS mode in LVDS pads through the LPCRx register.

Pad Driver Mode Registers

This is the general description of the PDR registers. Each port contains its own specific PDR registers, described additionally at each port, that can contain between one and eight PDx fields for PDR0 and PDR1 registers, respectively. Each PDx field controls 1 pin. For coding of PDx, see [Table 103](#), [Table 104](#) and [Table 105](#). Similarly, each PLx bit controls 1 pin. For coding of PLx, see [Table 106](#).

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

The boot software configures the reset value of Pn_PDR0 and Pn_PDR1 registers from 0000 0000_H to 2222 2222_H except for analog ports and if the package doesn't make any of the related pins available. The resulting value depends on the implemented port width. The documented value is valid for the largest package.

P33_PDR0

Port 33 Pad Driver Mode Register 0 (040_H)

Reset Value: Table 108

P40_PDR0

Port 40 Pad Driver Mode Register 0 (040_H)

Reset Value: Table 109

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL7	PD7	PL6	PD6	PL5	PD5	PL4	PD4								
rw	rw	rw	rw	rw	rw	rw	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL3	PD3	PL2	PD2	PL1	PD1	PL0	PD0								
rw	rw	rw	rw	rw	rw	rw	rw								

Field	Bits	Type	Description
PDx (x=0-7)	4*x+1:4*x	rw	Pad Driver Mode for Pin x
PLx (x=0-7)	4*x+3:4*x+2	rw	Pad Level Selection for Pin x

Table 107 Access Mode Restrictions sorted by descending priority

Applies to **P33_PDR0**

Applies to **P40_PDR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)	

Table 108 Reset Values of P33_PDR0

Reset Type	Reset Value	Note
After SSW execution	2222 2222 _H	Initial value in largest package
After SSW execution	---- ---- _H	Initial value package dependent

Table 109 Reset Values of P40_PDR0

Reset Type	Reset Value	Note
After SSW execution	0000 0000 _H	Initial value in largest package
After SSW execution	---- ---- _H	Initial value package dependent

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P12_PDR0

Port 12 Pad Driver Mode Register 0 (040_H)

Reset Value: [Table 111](#)

P13_PDR0

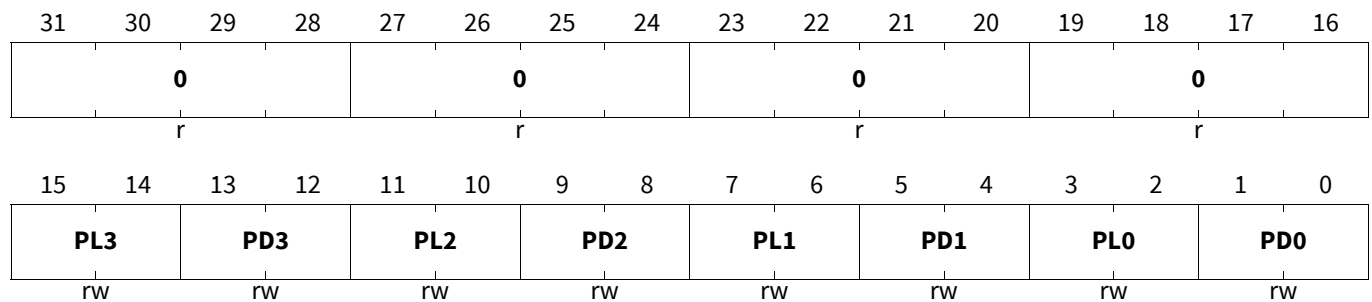
Port 13 Pad Driver Mode Register 0 (040_H)

Reset Value: [Table 111](#)

P22_PDR0

Port 22 Pad Driver Mode Register 0 (040_H)

Reset Value: [Table 111](#)



Field	Bits	Type	Description
PDx (x=0-3)	4*x+1:4*x	rw	Pad Driver Mode for Pin x
PLx (x=0-3)	4*x+3:4*x+2	rw	Pad Level Selection for Pin x
0	31:28, 27:24, 23:20, 19:16	r	Reserved Read as 0; should be written with 0.

Table 110 Access Mode Restrictions sorted by descending priority

Applies to [P12_PDR0](#)

Applies to [P13_PDR0](#)

Applies to [P22_PDR0](#)

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw PDx (x=0-3), PLx (x=0-3)	write access for enabled masters
Otherwise (default)	r PDx (x=0-3), PLx (x=0-3)	

Table 111 Reset Values

Applies to [P12_PDR0](#)

Applies to [P13_PDR0](#)

Applies to [P22_PDR0](#)

Reset Type	Reset Value	Note
After SSW execution	0000 2222 _H	Initial value in largest package
After SSW execution	0000 ---- _H	Initial value package dependent

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Port 00 Pad Driver Mode Register 1

P00_PDR1

Port 00 Pad Driver Mode Register 1 (044_H) Reset Value: Table 113

P11_PDR1

Port 11 Pad Driver Mode Register 1 (044_H) Reset Value: Table 113

P20_PDR1

Port 20 Pad Driver Mode Register 1 (044_H) Reset Value: Table 113

P33_PDR1

Port 33 Pad Driver Mode Register 1 (044_H) Reset Value: Table 113

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL15	PD15	PL14	PD14	PL13	PD13	PL12	PD12								
rw	rw	rw	rw	rw	rw	rw	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL11	PD11	PL10	PD10	PL9	PD9	PL8	PD8								
rw	rw	rw	rw	rw	rw	rw	rw								

Field	Bits	Type	Description
PDx (x=8-15)	4*x-31:4*x-32	rw	Pad Driver Mode for Pin x
PLx (x=8-15)	4*x-29:4*x-30	rw	Pad Level Selection for Pin x

Table 112 Access Mode Restrictions sorted by descending priority

Applies to P00_PDR1

Applies to P11_PDR1

Applies to P20_PDR1

Applies to P33_PDR1

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-15), PLx (x=8-15)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-15), PLx (x=8-15)	

Table 113 Reset Values

Applies to P00_PDR1

Applies to P11_PDR1

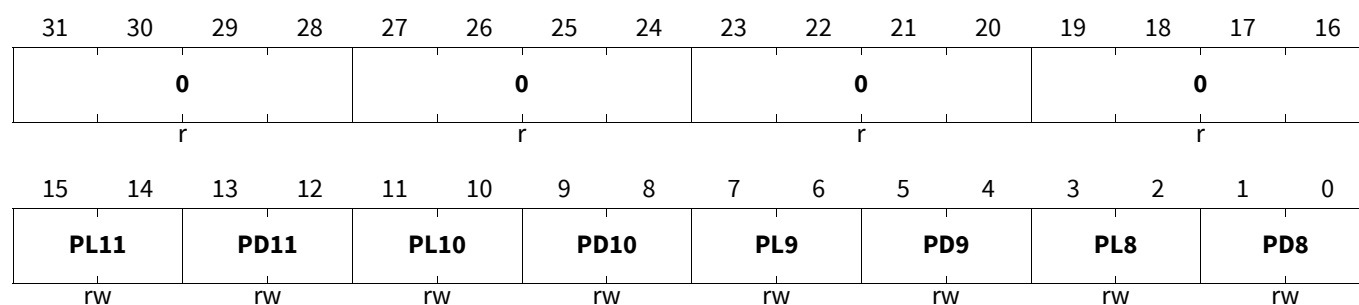
Applies to P20_PDR1

Applies to P33_PDR1

Reset Type	Reset Value	Note
After SSW execution	2222 2222 _H	Initial value in largest package
After SSW execution	---- ---- _H	Initial value package dependent

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P02_PDR1 Port 02 Pad Driver Mode Register 1	(044 _H)	Reset Value: Table 115
P10_PDR1 Port 10 Pad Driver Mode Register 1	(044 _H)	Reset Value: Table 115
P14_PDR1 Port 14 Pad Driver Mode Register 1	(044 _H)	Reset Value: Table 115
P15_PDR1 Port 15 Pad Driver Mode Register 1	(044 _H)	Reset Value: Table 115
P40_PDR1 Port 40 Pad Driver Mode Register 1	(044 _H)	Reset Value: Table 116



Field	Bits	Type	Description
PDx (x=8-11)	4*x-31:4*x-32	rw	Pad Driver Mode for Pin x
PLx (x=8-11)	4*x-29:4*x-30	rw	Pad Level Selection for Pin x
0	31:28, 27:24, 23:20, 19:16	r	Reserved Read as 0; should be written with 0.

Table 114 Access Mode Restrictions sorted by descending priority

Applies to [P02_PDR1](#)
 Applies to [P10_PDR1](#)
 Applies to [P14_PDR1](#)
 Applies to [P15_PDR1](#)
 Applies to [P40_PDR1](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-11), PLx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-11), PLx (x=8-11)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 115 Reset Values variant 1

Applies to **P02_PDR1**

Applies to **P10_PDR1**

Applies to **P14_PDR1**

Applies to **P15_PDR1**

Reset Type	Reset Value	Note
After SSW execution	0000 2222 _H	Initial value in largest package
After SSW execution	0000 ---- _H	Initial value package dependent

Table 116 Reset Values of P40_PDR1

Reset Type	Reset Value	Note
After SSW execution	0000 0000 _H	Initial value in largest package
After SSW execution	0000 ---- _H	Initial value package dependent

Port 00 Emergency Stop Register

P00_ESR

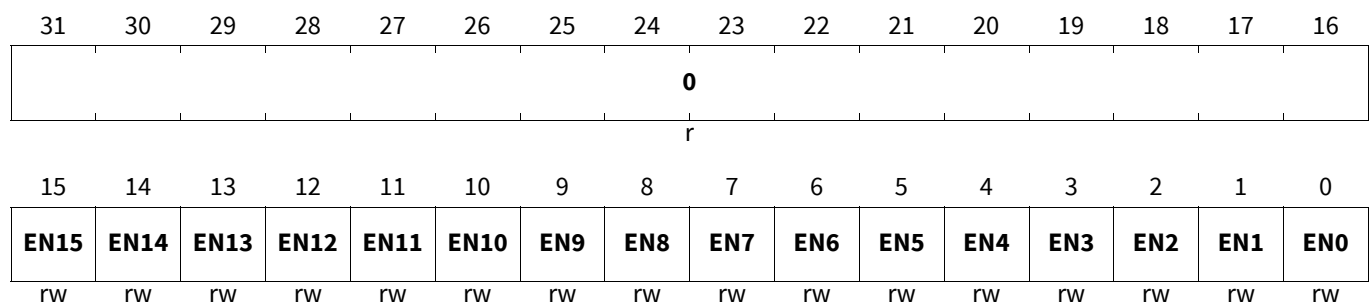
Port 00 Emergency Stop Register (050_H) **Application Reset Value: 0000 0000_H**

P11_ESR

Port 11 Emergency Stop Register (050_H) **Application Reset Value: 0000 0000_H**

P20_ESR

Port 20 Emergency Stop Register (050_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ENx (x=0-15)	x	rw	Emergency Stop Enable for Pin x This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 _B Emergency stop function for Pn.x is disabled. 1 _B Emergency stop function for Pn.x is enabled.
0	31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 117 Access Mode Restrictions sorted by descending priority

Applies to [P00_ESR](#)

Applies to [P11_ESR](#)

Applies to [P20_ESR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-15)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-15)	

Most GPIO lines have an emergency stop logic implemented (see Figure “General Structure of a Port Pin” in the Family chapter).

Each of these GPIO lines has its own emergency stop enable bit ENx that is located in the emergency stop register Pn_ESR of Port n. If the emergency stop signal becomes active, one of two states can be selected:

- Emergency stop function disabled (ENx = 0):
The output line remains connected (alternate function).
- Emergency stop function enabled (ENx = 1):
The mapped output function is disconnected and the safe state is entered by switching to input function with internal pull-up connected or tri-state, depending on the configured reset value of the corresponding Pn_IOCR register through PMSWCR5.TRISTREQ or setting of HWCFG[6].(the content of the corresponding PCx bit fields in register Pn_IOCR will not be considered).

Exceptions for Emergency Stop Implementation

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlaid with Testmode)
- Not available for P40.x and P41.x (analog input ANx overlaid with GPI)
- Not available for P32.0 and P32.1 when using EVRC regulator.
- Not available for P21.2 (used as EMGSTOPB pin).
- Not available for P33.8 (used as EMGSTOPA pin).
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

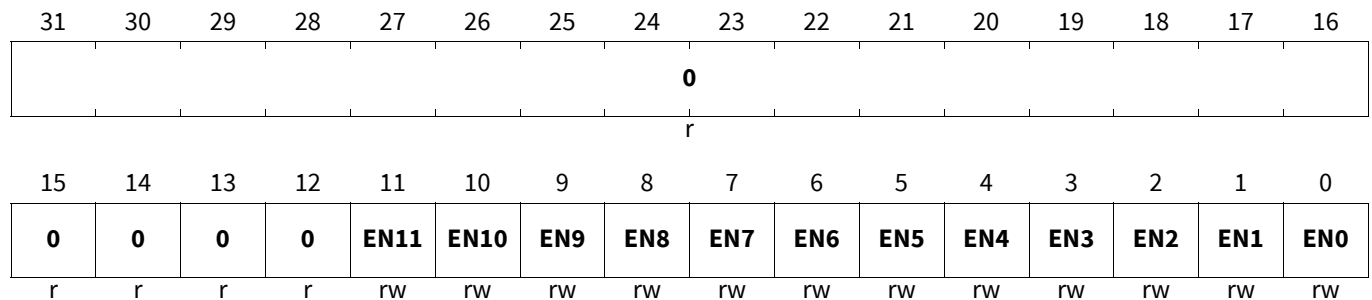
The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00_PCSR.
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL (DAP over CAN physical layer) mode. No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode.
- P33.0-7, P33.9-15 and P34.1: Emergency Stop can be overruled by the 8-Bit Standby Controller (SCR), if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR.

On pins with LVDS TX pads the Emergency Stop affects only the CMOS driver not the LVDS driver. Thus only when LPCR_x.TX_EN selects CMOS mode the output is switched off. When TX_EN selects LVDS mode the output is not switched off.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P02_ESR		
Port 02 Emergency Stop Register	(050_H)	Application Reset Value: 0000 0000_H
P10_ESR		
Port 10 Emergency Stop Register	(050_H)	Application Reset Value: 0000 0000_H
P14_ESR		
Port 14 Emergency Stop Register	(050_H)	Application Reset Value: 0000 0000_H
P15_ESR		
Port 15 Emergency Stop Register	(050_H)	Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
ENx (x=0-11)	x	rw	Emergency Stop Enable for Pin x This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 _B Emergency stop function for Pn.x is disabled. 1 _B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 31:16	r	Reserved Read as 0; should be written with 0.

Table 118 Access Mode Restrictions sorted by descending priority

Applies to [P02_ESR](#)
 Applies to [P10_ESR](#)
 Applies to [P14_ESR](#)
 Applies to [P15_ESR](#)

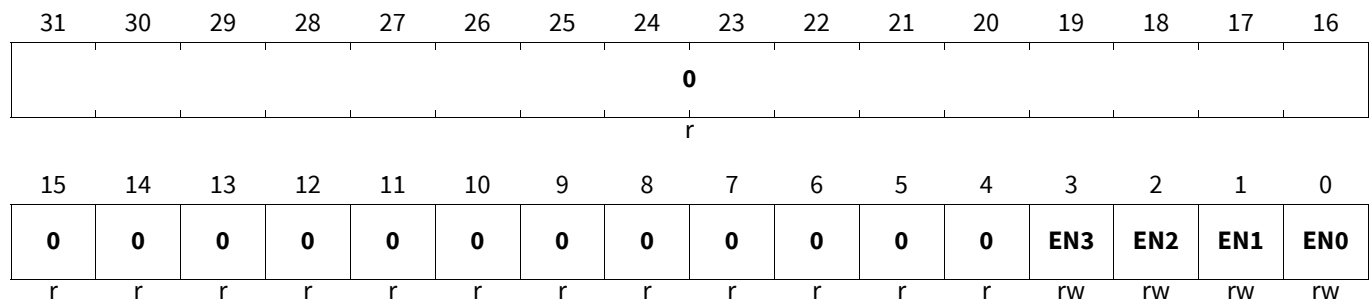
Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-11)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-11)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P12_ESR
Port 12 Emergency Stop Register (050_H) **Application Reset Value: 0000 0000_H**

P13_ESR
Port 13 Emergency Stop Register (050_H) **Application Reset Value: 0000 0000_H**

P22_ESR
Port 22 Emergency Stop Register (050_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ENx (x=0-3)	x	rw	Emergency Stop Enable for Pin x This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 _B Emergency stop function for Pn.x is disabled. 1 _B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	Reserved Read as 0; should be written with 0.

Table 119 Access Mode Restrictions sorted by descending priority

Applies to **P12_ESR**
 Applies to **P13_ESR**
 Applies to **P22_ESR**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-3)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-3)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P21_ESR

Port 21 Emergency Stop Register

(050_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	EN7	EN6	EN5	EN4	EN3	0	EN1	EN0
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	r	rw	rw

Field	Bits	Type	Description
ENx (x=0-1,3-7)	x	rw	<p>Emergency Stop Enable for Pin x</p> <p>This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function.</p> <p>0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.</p>
0	15, 14, 13, 12, 11, 10, 9, 8, 2, 31:16	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

Table 120 Access Mode Restrictions of P21_ESR sorted by descending priority

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw ENx (x=0-1,3-7)	write access for enabled masters
Otherwise (default)	r ENx (x=0-1,3-7)	

P23_ESR

Port 23 Emergency Stop Register

(050_H)

Application Reset Value: 0000 0000_H

P32_ESR

Port 32 Emergency Stop Register

(050_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
ENx (x=0-7)	x	rw	Emergency Stop Enable for Pin x This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 _B Emergency stop function for Pn.x is disabled. 1 _B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	Reserved Read as 0; should be written with 0.

Table 121 Access Mode Restrictions sorted by descending priority

Applies to [P23_ESR](#)

Applies to [P32_ESR](#)

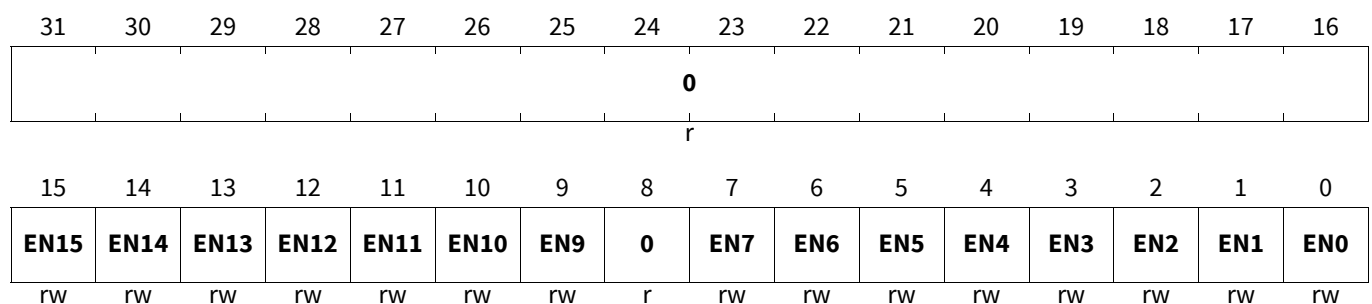
Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw ENx (x=0-7)	write access for enabled masters
Otherwise (default)	r ENx (x=0-7)	

P33_ESR

Port 33 Emergency Stop Register

(050_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
ENx (x=0-7,9-15)	x	rw	Emergency Stop Enable for Pin x This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0 _B Emergency stop function for Pn.x is disabled. 1 _B Emergency stop function for Pn.x is enabled.
0	8, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 122 Access Mode Restrictions of P33_ESR sorted by descending priority

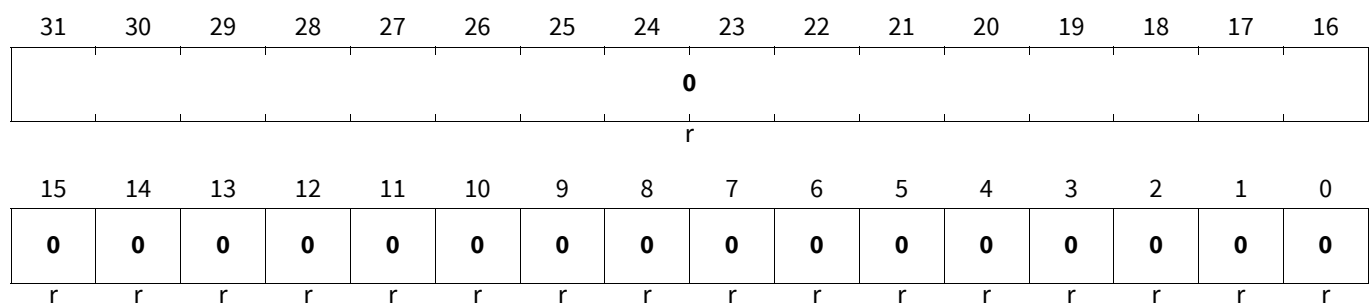
Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-7,9-15)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-7,9-15)	

P40_ESR

Port 40 Emergency Stop Register

(050_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 31:16	r	Reserved Read as 0; should be written with 0.

Table 123 Access Mode Restrictions of P40_ESR sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	-	See bit field definitions above	write access for enabled masters
Otherwise (default)	-	See bit field definitions above	

Port 00 Pin Function Decision Control Register

The pad structure of the GPIO lines offers the possibility to disable/enable port pad, select digital input or analog ADC input functionalities. Note that Class S pads have different characteristics than other digital input pads. For analog inputs, setting PDISx to 1 disables the Schmitt trigger input buffer, which would otherwise reduce analog input accuracy. For the ADC diagnostic features “PDD” and “MD” however the corresponding PDISx needs to be 0 to allow activation of their pull resistors. This feature can be controlled by individual bits in the Pn_PDISC register, independently from input/output and pull-up/pull-down control functionality as programmed in the Pn_IOCR register. One Pn_PDISC register is assigned to each port.

Note: After reset, all Px_PDISC registers have the reset value of 0000 0000_H. The startup software enables only the pads with digital input/output functionality which are available in that package. P40_PDISC and

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P41_PDISC are configured by the SSW for analog input function (kept disabled). The documented reset value shows the value in the largest package.

P00_PDISC

Port 00 Pin Function Decision Control Register (060_H)

Reset Value: Table 125

P11_PDISC

Port 11 Pin Function Decision Control Register (060_H)

Reset Value: Table 125

P20_PDISC

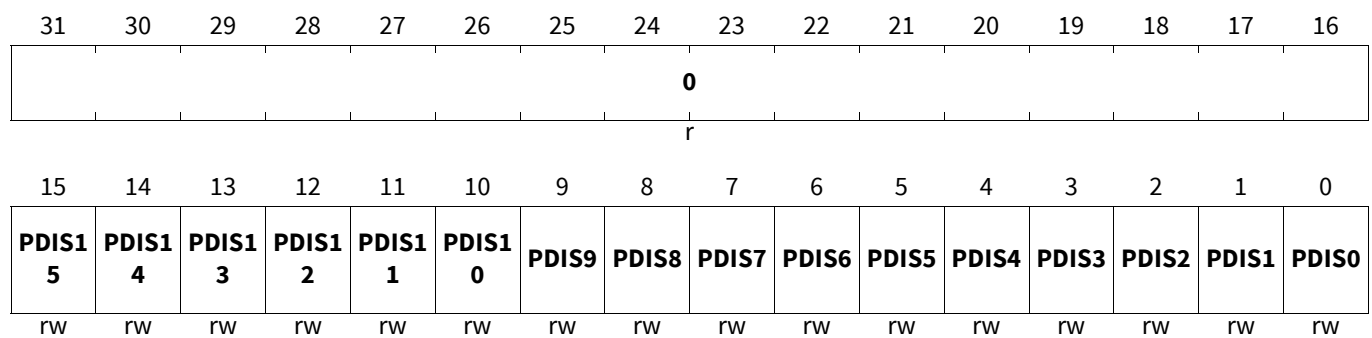
Port 20 Pin Function Decision Control Register (060_H)

Reset Value: Table 125

P33_PDISC

Port 33 Pin Function Decision Control Register (060_H)

Reset Value: Table 125



Field	Bits	Type	Description
PDISx (x=0-15)	x	rw	Pin Function Decision Control for Pin x This bit selects the function of the port pad. 0 _B Digital functionality of pad Pn.x is enabled. 1 _B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	31:16	r	Reserved Read as 0; should be written with 0.

Table 124 Access Mode Restrictions sorted by descending priority

Applies to **P00_PDISC**

Applies to **P11_PDISC**

Applies to **P20_PDISC**

Applies to **P33_PDISC**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-15)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-15)	

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Table 125 Reset Values

Applies to **P00_PDISC**

Applies to **P11_PDISC**

Applies to **P20_PDISC**

Applies to **P33_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 _H	Initial value in largest package
After SSW execution	0000 ---- _H	Initial value package dependent

P02_PDISC

Port 02 Pin Function Decision Control Register (060_H)

Reset Value: [Table 127](#)

P10_PDISC

Port 10 Pin Function Decision Control Register (060_H)

Reset Value: [Table 127](#)

P14_PDISC

Port 14 Pin Function Decision Control Register (060_H)

Reset Value: [Table 127](#)

P15_PDISC

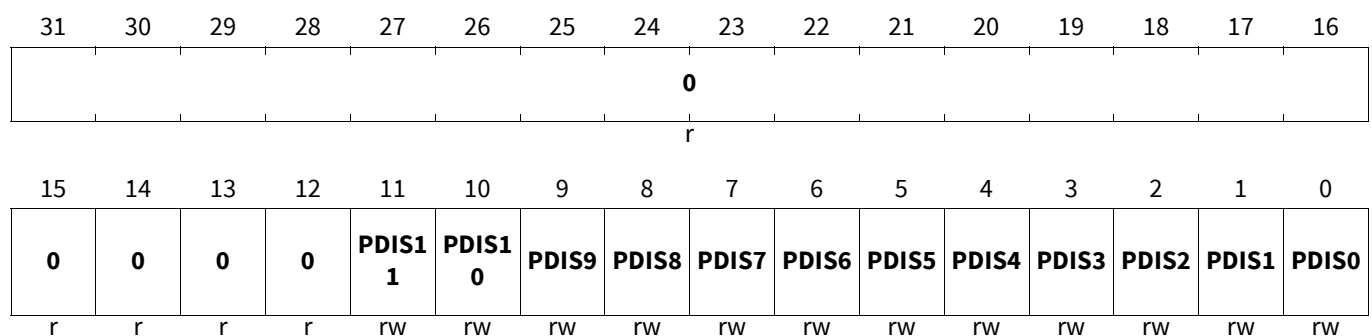
Port 15 Pin Function Decision Control Register (060_H)

Reset Value: [Table 127](#)

P40_PDISC

Port 40 Pin Function Decision Control Register (060_H)

Reset Value: [Table 128](#)



Field	Bits	Type	Description
PDISx (x=0-11)	x	rw	Pin Function Decision Control for Pin x This bit selects the function of the port pad. 0 _B Digital functionality of pad Pn.x is enabled. 1 _B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	15, 14, 13, 12, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 126 Access Mode Restrictions sorted by descending priority

Applies to [P02_PDISC](#)
 Applies to [P10_PDISC](#)
 Applies to [P14_PDISC](#)
 Applies to [P15_PDISC](#)
 Applies to [P40_PDISC](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-11)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-11)	

Table 127 Reset Values variant 1

Applies to [P02_PDISC](#)
 Applies to [P10_PDISC](#)
 Applies to [P14_PDISC](#)
 Applies to [P15_PDISC](#)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 _H	Initial value in largest package
After SSW execution	0000 0--- _H	Initial value package dependent

Table 128 Reset Values of P40_PDISC

Reset Type	Reset Value	Note
After SSW execution	0000 0FFF _H	Initial value in largest package
After SSW execution	0000 0--- _H	Initial value package dependent

P12_PDISC

Port 12 Pin Function Decision Control Register (060_H)

Reset Value: [Table 130](#)

P13_PDISC

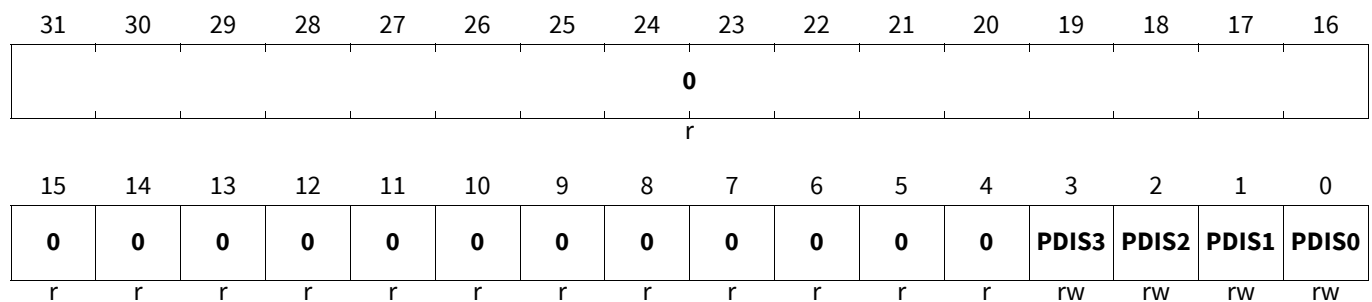
Port 13 Pin Function Decision Control Register (060_H)

Reset Value: [Table 130](#)

P22_PDISC

Port 22 Pin Function Decision Control Register (060_H)

Reset Value: [Table 130](#)



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PDISx (x=0-3)	x	rw	Pin Function Decision Control for Pin x This bit selects the function of the port pad. 0 _B Digital functionality of pad Pn.x is enabled. 1 _B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	Reserved Read as 0; should be written with 0.

Table 129 Access Mode Restrictions sorted by descending priority

Applies to [P12_PDISC](#)

Applies to [P13_PDISC](#)

Applies to [P22_PDISC](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-3)	

Table 130 Reset Values

Applies to [P12_PDISC](#)

Applies to [P13_PDISC](#)

Applies to [P22_PDISC](#)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 _H	Initial value in largest package
After SSW execution	0000 000 _{-H}	Initial value package dependent

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P21_PDISC

Port 21 Pin Function Decision Control Register (060_H)

Reset Value: [Table 132](#)

P23_PDISC

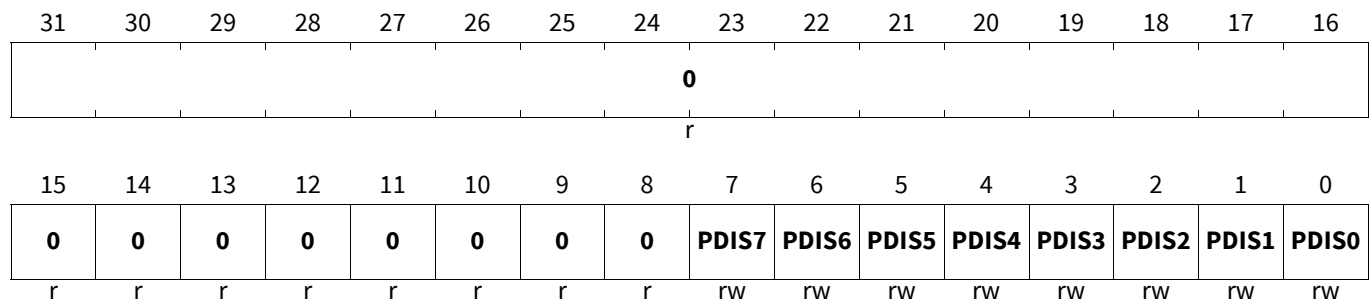
Port 23 Pin Function Decision Control Register (060_H)

Reset Value: [Table 132](#)

P32_PDISC

Port 32 Pin Function Decision Control Register (060_H)

Reset Value: [Table 132](#)



Field	Bits	Type	Description
PDISx (x=0-7)	x	rw	Pin Function Decision Control for Pin x This bit selects the function of the port pad. 0 _B Digital functionality of pad Pn.x is enabled. 1 _B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	Reserved Read as 0; should be written with 0.

Table 131 Access Mode Restrictions sorted by descending priority

Applies to [P21_PDISC](#)

Applies to [P23_PDISC](#)

Applies to [P32_PDISC](#)

Mode Name	Access Mode	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-7)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 132 Reset Values

Applies to **P21_PDISC**

Applies to **P23_PDISC**

Applies to **P32_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 0000 _H	Initial value in largest package
After SSW execution	0000 00-- _H	Initial value package dependent

Port 00 Pin Controller Select Register

This register has different functionality in each port:

- In Ports shared with the standby controller (SCR) it selects if the SCR or the Tricore system control data and control functions of these port lines.
- In Ports with analog inputs to the EVADC it enables control of pull by the EVADC for the Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature.
- In Ports with Ethernet output it selects between alternate output and fast RGMII/RMII/MII mode.
- In Ports with SMU FSP pin (P33.8) the PCSR.SEL bit enables the SMU to override pad configuration signals. Therefore this bit has the reset value 1_B and shall be kept 1_B by the application. The SMU override is documented in the SMU chapter (see SMU_PCTL.PCFG and Figure “SMU/PAD Control Interface to the PADS”).

P00_PCSR

Port 00 Pin Controller Select Register

(064_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	R13	R12	SEL11	SEL10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw															

Field	Bits	Type	Description
SELx (x=10-11)	x	rw	Output Select for Pin x This bit enables or disables EVADC control of the pulls for Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature. 0 _B Disable EVADC PDD/MD feature of pin x. 1 _B Enable EVADC PDD/MD feature of pin x.
Rx (x=0-9,12-15)	x	rw	Reserved Read as 0; should be written with 0.
0	30:16, 31	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 133 Access Mode Restrictions of P00_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-9,12-15)	write access only for masters with supervisor mode
	rw	SELx (x=10-11)	
Otherwise (default)	r	Rx (x=0-9,12-15), SELx (x=10-11)	

P02_PCSR

Port 02 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

P10_PCSR

Port 10 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

P14_PCSR

Port 14 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

P15_PCSR

Port 15 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-11)	x	rw	Reserved Read as 0; should be written with 0.
0	15, 14, 13, 12, 30:16, 31	r	Reserved Read as 0; should be written with 0.

Table 134 Access Mode Restrictions sorted by descending priority

Applies to **P02_PCSR**

Applies to **P10_PCSR**

Applies to **P14_PCSR**

Applies to **P15_PCSR**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-11)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-11)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P11_PCSR

Port 11 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	R13	R12	R11	R10	R9	R8	R7	SEL6	R5	SEL4	SEL3	SEL2	SEL1	SEL0
rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw rw															

Field	Bits	Type	Description
SELx (x=0-4,6)	x	rw	Output Select for Pin x This bit enables or disables alternate/fast Ethernet output. 0 _B Ethernet output via ports alternate output of pin x. 1 _B Ethernet output via fast RGMII/RMII/MII mode of pin x.
Rx (x=5,7-15)	x	rw	Reserved Read as 0; should be written with 0.
0	30:16, 31	r	Reserved Read as 0; should be written with 0.

Table 135 Access Mode Restrictions of P11_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=5,7-15)	write access only for masters with supervisor mode
	rw	SELx (x=0-4,6)	
Otherwise (default)	r	Rx (x=5,7-15), SELx (x=0-4,6)	

P12_PCSR

Port 12 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

P13_PCSR

Port 13 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

P22_PCSR

Port 22 Pin Controller Select Register (064_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
r r r r r r r r r r r r												rw	rw	rw	rw

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
Rx (x=0-3)	x	rw	Reserved Read as 0; should be written with 0.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 30:16, 31	r	Reserved Read as 0; should be written with 0.

Table 136 Access Mode Restrictions sorted by descending priority

Applies to [P12_PCSR](#)
 Applies to [P13_PCSR](#)
 Applies to [P22_PCSR](#)

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-3)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-3)	

P20_PCSR

Port 20 Pin Controller Select Register

(064_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-15)	x	rw	Reserved Read as 0; should be written with 0.
0	30:16, 31	r	Reserved Read as 0; should be written with 0.

Table 137 Access Mode Restrictions of P20_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-15)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-15)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P21_PCSR
Port 21 Pin Controller Select Register (064_H) **Application Reset Value: 0000 0000_H**

P23_PCSR
Port 23 Pin Controller Select Register (064_H) **Application Reset Value: 0000 0000_H**

P32_PCSR
Port 32 Pin Controller Select Register (064_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-7)	x	rw	Reserved Read as 0; should be written with 0.
0	15, 14, 13, 12, 11, 10, 9, 8, 30:16, 31	r	Reserved Read as 0; should be written with 0.

Table 138 Access Mode Restrictions sorted by descending priority

Applies to [P21_PCSR](#)
 Applies to [P23_PCSR](#)
 Applies to [P32_PCSR](#)

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	r Rx (x=0-7)	write access only for masters with supervisor mode
Otherwise (default)	r Rx (x=0-7)	

P33_PCSR
Port 33 Pin Controller Select Register (064_H) **Application Reset Value: 0000 0100_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCK								0							
rh								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	R14	SEL13	SEL12	SEL11	SEL10	SEL9	SEL8	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
SELx (x=0-7,9-13)	x	rw	Output Select for Pin x This bit enables or disables SCR control. 0 _B Tricore selected for data and control of pin x and not SCR. 1 _B SCR selected for data and control of pin x.
SELx (x=8)	x	rw	Output Select for Pin x This bit enables or disables SMU to override pad configuration. 0 _B Disable SMU override of pad configuration for FSP pin x. 1 _B Enable SMU to override pad configuration for FSP pin x.
Rx (x=14-15)	x	rw	Reserved Read as 0; should be written with 0.
LCK	31	rh	Lock Status This bit indicates if the register can be updated with a new value or if the register is locked due to an ongoing transfer to the SCR and a write action from the bus has no effect. In Ports without SCR overlay this bit is always 0 _B . 0 _B The register is unlocked and can be updated. 1 _B The register is locked (a write transfer to SCR is ongoing) and can not be updated.
0	30:16	r	Reserved Read as 0; should be written with 0.

Table 139 Access Mode Restrictions of P33_PCSR sorted by descending priority

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	r Rx (x=14-15)	write access only for masters with supervisor mode
	rh LCK	
	rw SELx (x=0-7,9-13), SELx (x=8)	
Otherwise (default)	r Rx (x=14-15), SELx (x=0-7,9-13), SELx (x=8)	
	rh LCK	

P40_PCSR

Port 40 Pin Controller Select Register

(064_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								0							
r								r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	R11	R10	R9	R8	R7	R6	SEL5	R4	SEL3	SEL2	SEL1	R0
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
SELx (x=1-3,5)	x	rw	Output Select for Pin x This bit enables or disables EVADC control of the pulls for Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature. 0 _B Disable EVADC PDD/MD feature of pin x. 1 _B Enable EVADC PDD/MD feature of pin x.
Rx (x=0,4,6-11)	x	rw	Reserved Read as 0; should be written with 0.
0	15, 14, 13, 12, 30:16, 31	r	Reserved Read as 0; should be written with 0.

Table 140 Access Mode Restrictions of P40_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0,4,6-11)	write access only for masters with supervisor mode
	rw	SELx (x=1-3,5)	
Otherwise (default)	r	Rx (x=0,4,6-11), SELx (x=1-3,5)	

Port 00 Output Modification Set Register 0

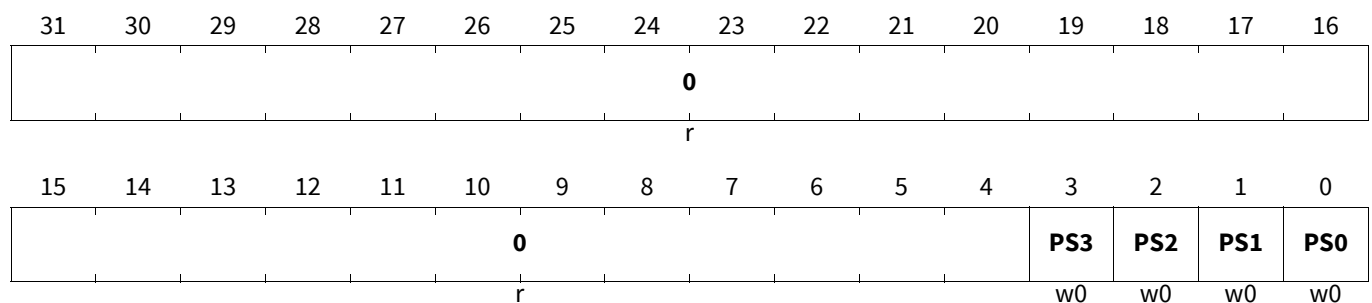
The port output modification set register x, (x = 0, 4, 8, 12) contains control bits to individually set the logic state of a single port line by manipulating the output register.

Note: Registers Pn_OMSRx (x = 0, 4, 8, 12) are virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Register Pn_OMSR0 sets the logic state of Pn.[3:0] port lines

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_OMSR0		
Port 00 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P02_OMSR0		
Port 02 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P10_OMSR0		
Port 10 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P11_OMSR0		
Port 11 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P12_OMSR0		
Port 12 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P13_OMSR0		
Port 13 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P14_OMSR0		
Port 14 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P15_OMSR0		
Port 15 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P20_OMSR0		
Port 20 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H
P21_OMSR0		
Port 21 Output Modification Set Register 0	(070 _H)	Application Reset Value: 0000 0000 _H



Field	Bits	Type	Description
PSx (x=0-3)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	31:4	r	Reserved Read as 0; should be written with 0.

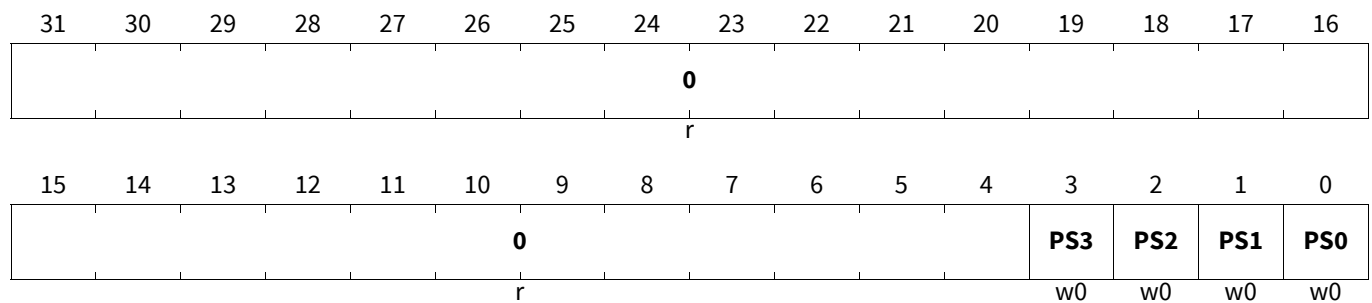
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 141 Access Mode Restrictions sorted by descending priority

- Applies to **P00_OMSRO**
- Applies to **P02_OMSRO**
- Applies to **P10_OMSRO**
- Applies to **P11_OMSRO**
- Applies to **P12_OMSRO**
- Applies to **P13_OMSRO**
- Applies to **P14_OMSRO**
- Applies to **P15_OMSRO**
- Applies to **P20_OMSRO**
- Applies to **P21_OMSRO**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

- P22_OMSRO**
Port 22 Output Modification Set Register 0 (070_H) Application Reset Value: 0000 0000_H
- P23_OMSRO**
Port 23 Output Modification Set Register 0 (070_H) Application Reset Value: 0000 0000_H
- P32_OMSRO**
Port 32 Output Modification Set Register 0 (070_H) Application Reset Value: 0000 0000_H
- P33_OMSRO**
Port 33 Output Modification Set Register 0 (070_H) Application Reset Value: 0000 0000_H
- P40_OMSRO**
Port 40 Output Modification Set Register 0 (070_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PSx (x=0-3)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	31:4	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 142 Access Mode Restrictions sorted by descending priority

Applies to **P22_OMSR0**

Applies to **P23_OMSR0**

Applies to **P32_OMSR0**

Applies to **P33_OMSR0**

Applies to **P40_OMSR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

Port 00 Output Modification Set Register 4

Register Pn_OMSR4 sets the logic state of Pn.[7:4] port lines

P00_OMSR4

Port 00 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P02_OMSR4

Port 02 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P10_OMSR4

Port 10 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P11_OMSR4

Port 11 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P14_OMSR4

Port 14 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P15_OMSR4

Port 15 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P20_OMSR4

Port 20 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P21_OMSR4

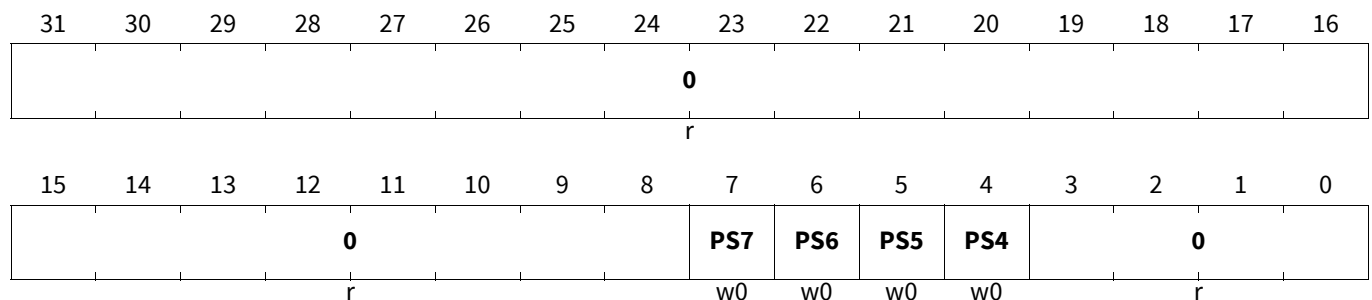
Port 21 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P23_OMSR4

Port 23 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H

P32_OMSR4

Port 32 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000_H



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PSx (x=4-7)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	3:0, 31:8	r	Reserved Read as 0; should be written with 0.

Table 143 Access Mode Restrictions sorted by descending priority

- Applies to [P00_OMSR4](#)
- Applies to [P02_OMSR4](#)
- Applies to [P10_OMSR4](#)
- Applies to [P11_OMSR4](#)
- Applies to [P14_OMSR4](#)
- Applies to [P15_OMSR4](#)
- Applies to [P20_OMSR4](#)
- Applies to [P21_OMSR4](#)
- Applies to [P23_OMSR4](#)
- Applies to [P32_OMSR4](#)

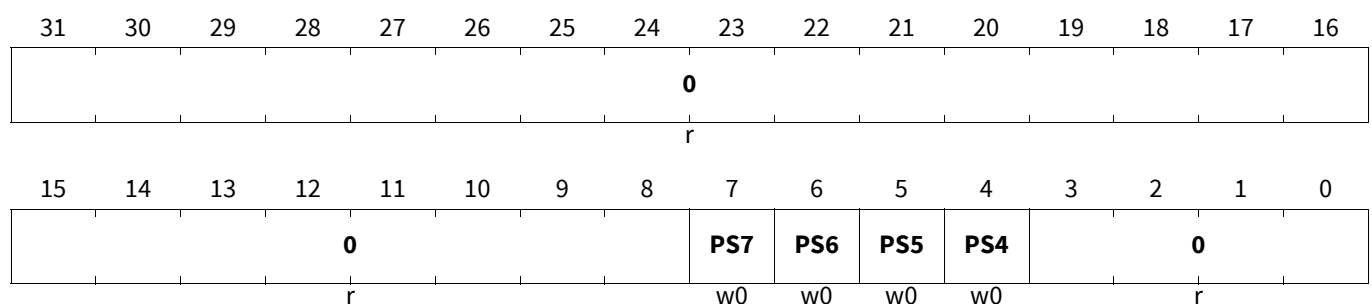
Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=4-7)	

P33_OMSR4

Port 33 Output Modification Set Register 4 (074_H) **Application Reset Value: 0000 0000_H**

P40_OMSR4

Port 40 Output Modification Set Register 4 (074_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
PSx (x=4-7)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	3:0, 31:8	r	Reserved Read as 0; should be written with 0.

Table 144 Access Mode Restrictions sorted by descending priority

Applies to **P33_OMSR4**

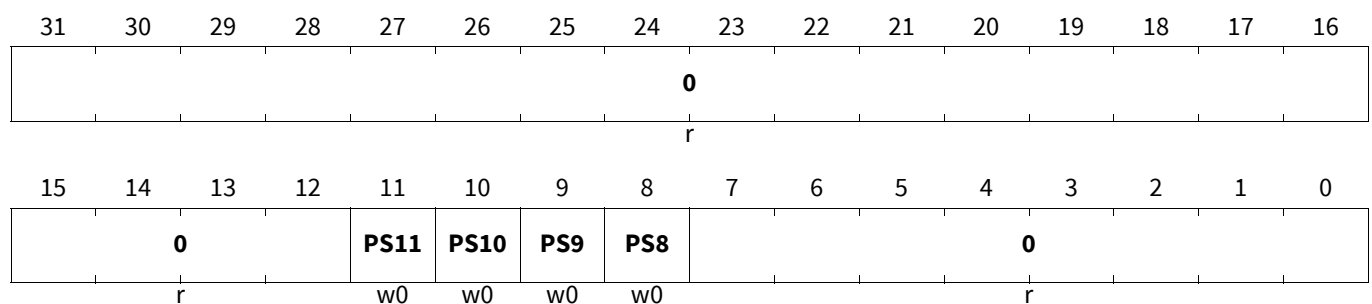
Applies to **P40_OMSR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=4-7)	

Port 00 Output Modification Set Register 8

Register Pn_OMSR8 sets the logic state of Pn.[11:8] port lines

P00_OMSR8		
Port 00 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P02_OMSR8		
Port 02 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P10_OMSR8		
Port 10 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P11_OMSR8		
Port 11 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P14_OMSR8		
Port 14 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P15_OMSR8		
Port 15 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P20_OMSR8		
Port 20 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P33_OMSR8		
Port 33 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H
P40_OMSR8		
Port 40 Output Modification Set Register 8	(078_H)	Application Reset Value: 0000 0000_H



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PSx (x=8-11)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	7:0, 31:12	r	Reserved Read as 0; should be written with 0.

Table 145 Access Mode Restrictions sorted by descending priority

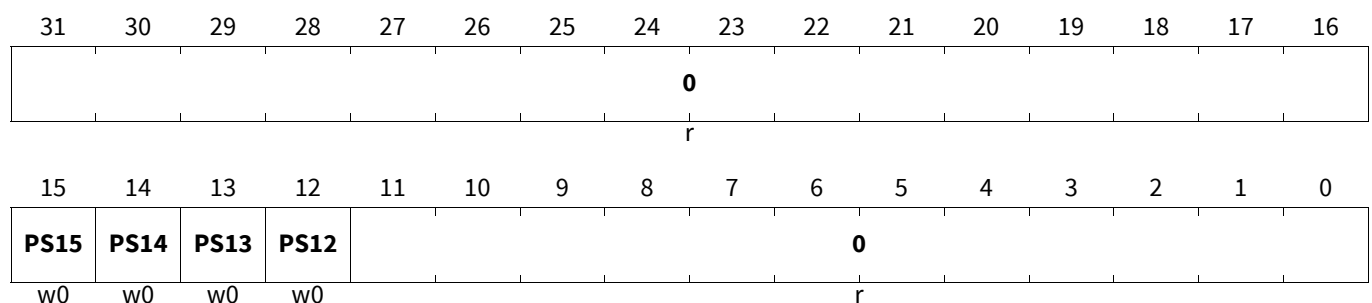
- Applies to [P00_OMSR8](#)
- Applies to [P02_OMSR8](#)
- Applies to [P10_OMSR8](#)
- Applies to [P11_OMSR8](#)
- Applies to [P14_OMSR8](#)
- Applies to [P15_OMSR8](#)
- Applies to [P20_OMSR8](#)
- Applies to [P33_OMSR8](#)
- Applies to [P40_OMSR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PSx (x=8-11)	

Port 00 Output Modification Set Register 12

Register Pn_OMSR12 sets the logic state of Pn.[15:12] port lines

- P00_OMSR12**
Port 00 Output Modification Set Register 12 (07C_H) Application Reset Value: 0000 0000_H
- P11_OMSR12**
Port 11 Output Modification Set Register 12 (07C_H) Application Reset Value: 0000 0000_H
- P20_OMSR12**
Port 20 Output Modification Set Register 12 (07C_H) Application Reset Value: 0000 0000_H
- P33_OMSR12**
Port 33 Output Modification Set Register 12 (07C_H) Application Reset Value: 0000 0000_H



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PSx (x=12-15)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	11:0, 31:16	r	Reserved Read as 0; should be written with 0.

Table 146 Access Mode Restrictions sorted by descending priority

Applies to [P00_OMSR12](#)

Applies to [P11_OMSR12](#)

Applies to [P20_OMSR12](#)

Applies to [P33_OMSR12](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=12-15)	write access for enabled masters
Otherwise (default)	r0	PSx (x=12-15)	

Port 00 Output Modification Clear Register 0

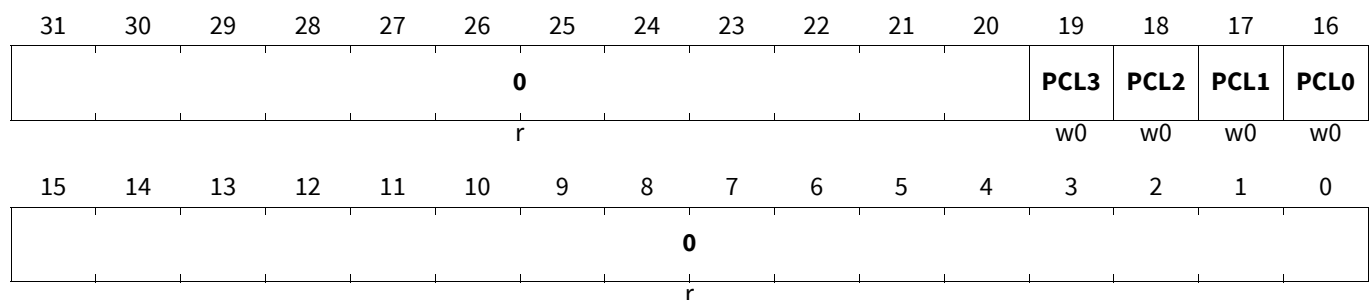
The port output modification clear register x, (x = 0, 4, 8, 12) contains control bits to individually clear the logic state of a single port line by manipulating the output register.

Note: Registers Pn_OMCRx (x = 0, 4, 8, 12) are virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Register Pn_OMCR0 clears the logic state of Pn.[3:0] port lines

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_OMCR0		
Port 00 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P02_OMCR0		
Port 02 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P10_OMCR0		
Port 10 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P11_OMCR0		
Port 11 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P12_OMCR0		
Port 12 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P13_OMCR0		
Port 13 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P14_OMCR0		
Port 14 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P15_OMCR0		
Port 15 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P20_OMCR0		
Port 20 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H
P21_OMCR0		
Port 21 Output Modification Clear Register 0	(080 _H)	Application Reset Value: 0000 0000 _H



Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px
0	15:0, 31:20	r	Reserved Read as 0; should be written with 0.

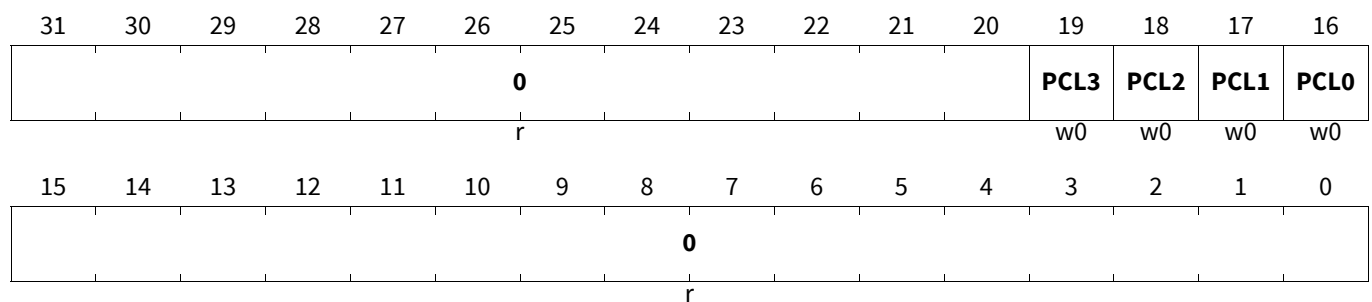
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 147 Access Mode Restrictions sorted by descending priority

- Applies to **P00_OMCR0**
- Applies to **P02_OMCR0**
- Applies to **P10_OMCR0**
- Applies to **P11_OMCR0**
- Applies to **P12_OMCR0**
- Applies to **P13_OMCR0**
- Applies to **P14_OMCR0**
- Applies to **P15_OMCR0**
- Applies to **P20_OMCR0**
- Applies to **P21_OMCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

- P22_OMCR0**
Port 22 Output Modification Clear Register 0 (080_H) **Application Reset Value: 0000 0000_H**
- P23_OMCR0**
Port 23 Output Modification Clear Register 0 (080_H) **Application Reset Value: 0000 0000_H**
- P32_OMCR0**
Port 32 Output Modification Clear Register 0 (080_H) **Application Reset Value: 0000 0000_H**
- P33_OMCR0**
Port 33 Output Modification Clear Register 0 (080_H) **Application Reset Value: 0000 0000_H**
- P40_OMCR0**
Port 40 Output Modification Clear Register 0 (080_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px
0	15:0, 31:20	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 148 Access Mode Restrictions sorted by descending priority

Applies to **P22_OMCR0**

Applies to **P23_OMCR0**

Applies to **P32_OMCR0**

Applies to **P33_OMCR0**

Applies to **P40_OMCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

Port 00 Output Modification Clear Register 4

Register Pn_OMCR4 clears the logic state of Pn.[7:4] port lines

P00_OMCR4

Port 00 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P02_OMCR4

Port 02 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P10_OMCR4

Port 10 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P11_OMCR4

Port 11 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P14_OMCR4

Port 14 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P15_OMCR4

Port 15 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P20_OMCR4

Port 20 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P21_OMCR4

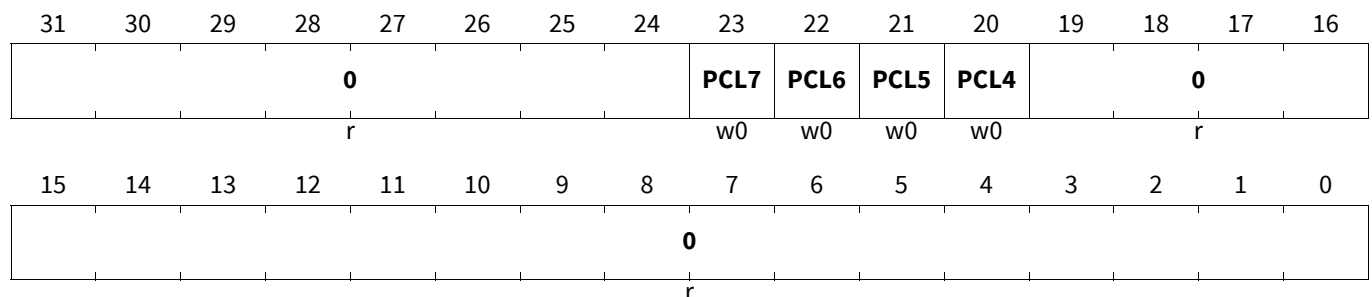
Port 21 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P23_OMCR4

Port 23 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H

P32_OMCR4

Port 32 Output Modification Clear Register 4 (084_H) Application Reset Value: 0000 0000_H



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px
0	19:0, 31:24	r	Reserved Read as 0; should be written with 0

Table 149 Access Mode Restrictions sorted by descending priority

- Applies to [P00_OMCR4](#)
- Applies to [P02_OMCR4](#)
- Applies to [P10_OMCR4](#)
- Applies to [P11_OMCR4](#)
- Applies to [P14_OMCR4](#)
- Applies to [P15_OMCR4](#)
- Applies to [P20_OMCR4](#)
- Applies to [P21_OMCR4](#)
- Applies to [P23_OMCR4](#)
- Applies to [P32_OMCR4](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=4-7)	

P33_OMCR4

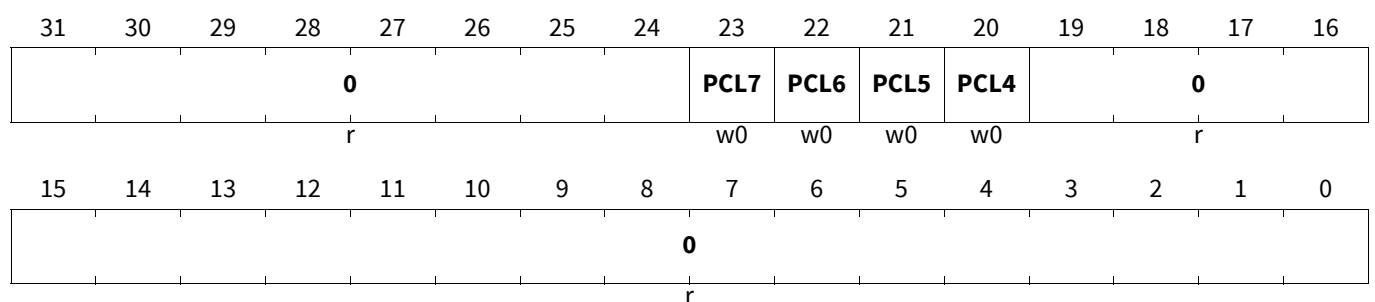
Port 33 Output Modification Clear Register 4 (084_H)

Application Reset Value: 0000 0000_H

P40_OMCR4

Port 40 Output Modification Clear Register 4 (084_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	19:0, 31:24	r	Reserved Read as 0; should be written with 0

Table 150 Access Mode Restrictions sorted by descending priority

Applies to **P33_OMCR4**

Applies to **P40_OMCR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=4-7)	

Port 00 Output Modification Clear Register 8

Register Pn_OMCR8 clears the logic state of Pn.[11:8] port lines

P00_OMCR8

Port 00 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P02_OMCR8

Port 02 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P10_OMCR8

Port 10 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P11_OMCR8

Port 11 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P14_OMCR8

Port 14 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P15_OMCR8

Port 15 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P20_OMCR8

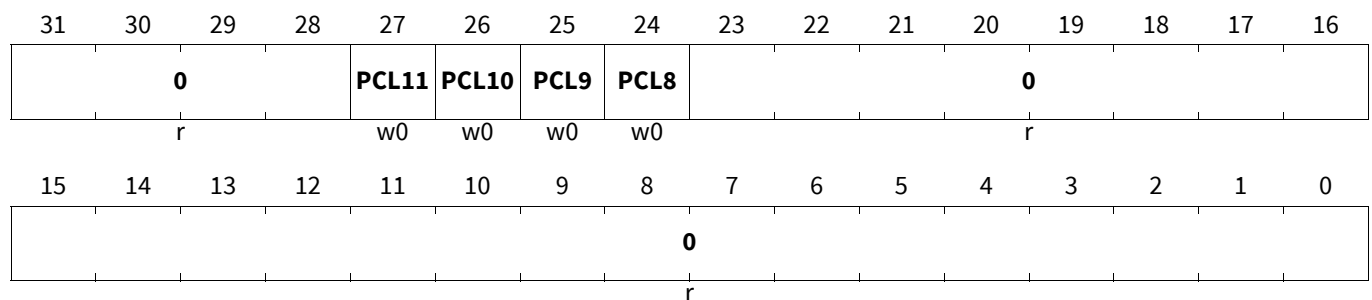
Port 20 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P33_OMCR8

Port 33 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H

P40_OMCR8

Port 40 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000_H



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=8-11)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px
0	23:0, 31:28	r	Reserved Read as 0; should be written with 0

Table 151 Access Mode Restrictions sorted by descending priority

- Applies to [P00_OMCR8](#)
- Applies to [P02_OMCR8](#)
- Applies to [P10_OMCR8](#)
- Applies to [P11_OMCR8](#)
- Applies to [P14_OMCR8](#)
- Applies to [P15_OMCR8](#)
- Applies to [P20_OMCR8](#)
- Applies to [P33_OMCR8](#)
- Applies to [P40_OMCR8](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=8-11)	

Port 00 Output Modification Clear Register 12

Register Pn_OMCR12 clears the logic state of Pn.[15:12] port lines

P00_OMCR12

Port 00 Output Modification Clear Register 12 (08C_H) **Application Reset Value: 0000 0000_H**

P11_OMCR12

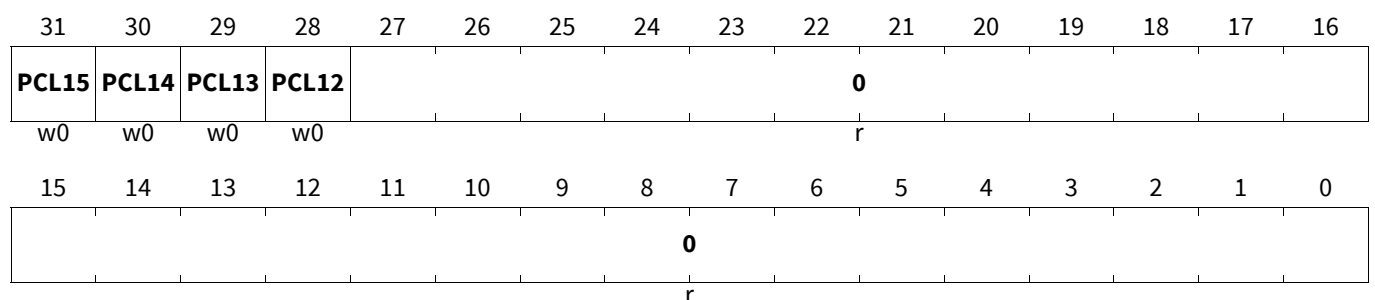
Port 11 Output Modification Clear Register 12 (08C_H) **Application Reset Value: 0000 0000_H**

P20_OMCR12

Port 20 Output Modification Clear Register 12 (08C_H) **Application Reset Value: 0000 0000_H**

P33_OMCR12

Port 33 Output Modification Clear Register 12 (08C_H) **Application Reset Value: 0000 0000_H**



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PCLx (x=12-15)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px
0	27:0	r	Reserved Read as 0; should be written with 0

Table 152 Access Mode Restrictions sorted by descending priority

Applies to [P00_OMCR12](#)
 Applies to [P11_OMCR12](#)
 Applies to [P20_OMCR12](#)
 Applies to [P33_OMCR12](#)

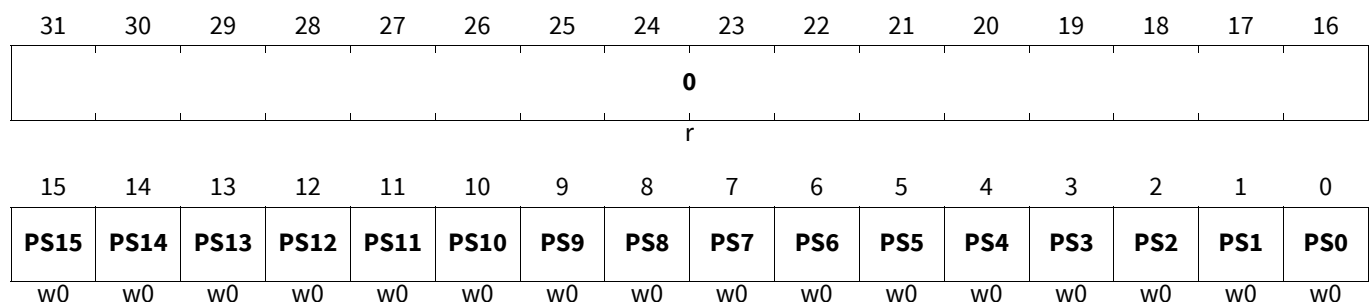
Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=12-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=12-15)	

Port 00 Output Modification Set Register

The port output modification set register contains control bits that make it possible to individually set the logic state of a single port line by manipulating the output register.

Note: Register Pn_OMSR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

P00_OMSR
Port 00 Output Modification Set Register (090_H) **Application Reset Value: 0000 0000_H**
P11_OMSR
Port 11 Output Modification Set Register (090_H) **Application Reset Value: 0000 0000_H**
P20_OMSR
Port 20 Output Modification Set Register (090_H) **Application Reset Value: 0000 0000_H**
P33_OMSR
Port 33 Output Modification Set Register (090_H) **Application Reset Value: 0000 0000_H**



General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
PSx (x=0-15)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	31:16	r	Reserved Read as 0; should be written with 0.

Table 153 Access Mode Restrictions sorted by descending priority

Applies to [P00_OMSR](#)
 Applies to [P11_OMSR](#)
 Applies to [P20_OMSR](#)
 Applies to [P33_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-15)	

P02_OMSR

Port 02 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P10_OMSR

Port 10 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P14_OMSR

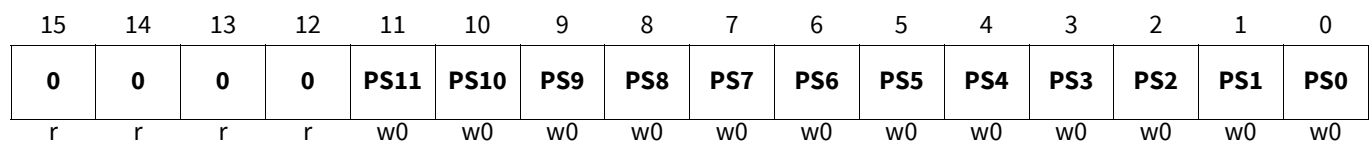
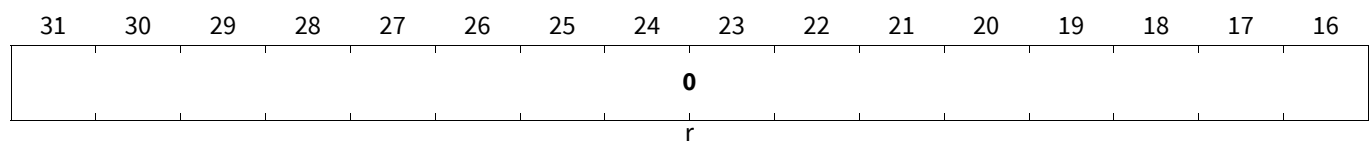
Port 14 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P15_OMSR

Port 15 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P40_OMSR

Port 40 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PSx (x=0-11)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
0	15, 14, 13, 12, 31:16	r	Reserved Read as 0; should be written with 0.

Table 154 Access Mode Restrictions sorted by descending priority

Applies to **P02_OMSR**
 Applies to **P10_OMSR**
 Applies to **P14_OMSR**
 Applies to **P15_OMSR**
 Applies to **P40_OMSR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-11)	

P12_OMSR

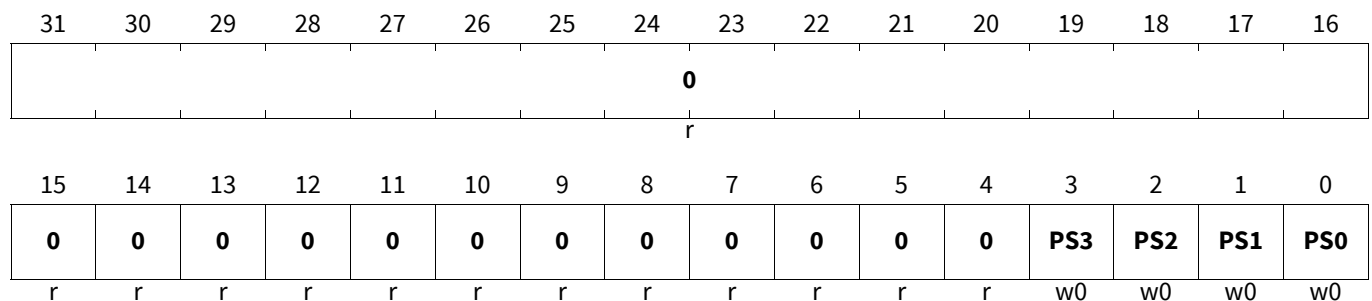
Port 12 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P13_OMSR

Port 13 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P22_OMSR

Port 22 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PSx (x=0-3)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	Reserved Read as 0; should be written with 0.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 155 Access Mode Restrictions sorted by descending priority

Applies to [P12_OMSR](#)

Applies to [P13_OMSR](#)

Applies to [P22_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

P21_OMSR

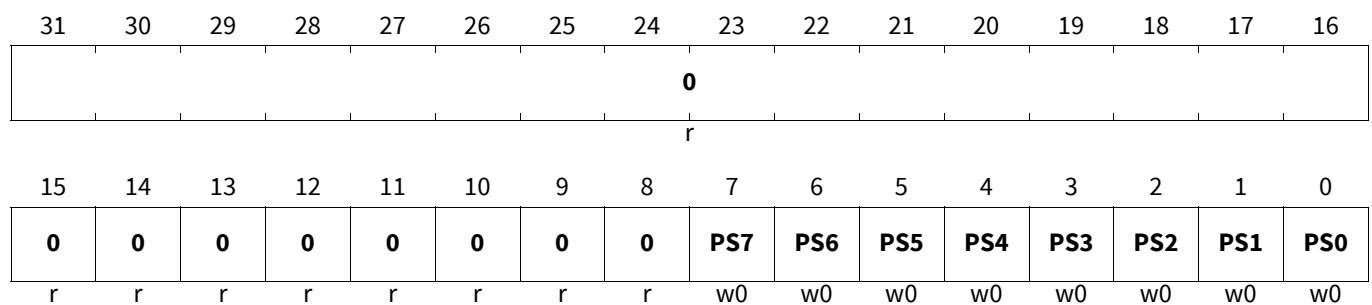
Port 21 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P23_OMSR

Port 23 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H

P32_OMSR

Port 32 Output Modification Set Register (090_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PSx (x=0-7)	x	w0	Set Bit x Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Sets Pn_OUT.Px
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	Reserved Read as 0; should be written with 0.

Table 156 Access Mode Restrictions sorted by descending priority

Applies to [P21_OMSR](#)

Applies to [P23_OMSR](#)

Applies to [P32_OMSR](#)

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-7)	

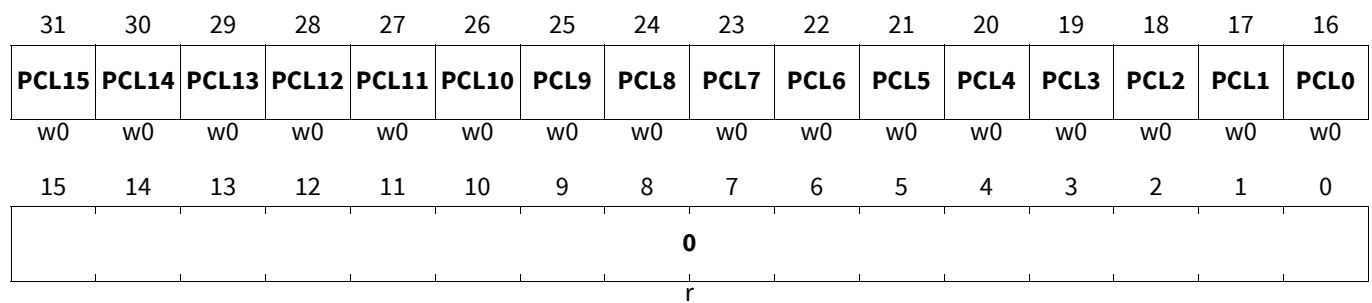
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Port 00 Output Modification Clear Register

The port output modification clear register contains control bits that make it possible to individually clear the logic state of a single port line by manipulating the output register.

Note: Register Pn_OMCR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

P00_OMCR		
Port 00 Output Modification Clear Register	(094_H)	Application Reset Value: 0000 0000_H
P11_OMCR		
Port 11 Output Modification Clear Register	(094_H)	Application Reset Value: 0000 0000_H
P20_OMCR		
Port 20 Output Modification Clear Register	(094_H)	Application Reset Value: 0000 0000_H
P33_OMCR		
Port 33 Output Modification Clear Register	(094_H)	Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
PCLx (x=0-15)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px.
0	15:0	r	Reserved Read as 0; should be written with 0

Table 157 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMCR**
 Applies to **P11_OMCR**
 Applies to **P20_OMCR**
 Applies to **P33_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P02_OMCR		
Port 02 Output Modification Clear Register	(094 _H)	Application Reset Value: 0000 0000 _H
P10_OMCR		
Port 10 Output Modification Clear Register	(094 _H)	Application Reset Value: 0000 0000 _H
P14_OMCR		
Port 14 Output Modification Clear Register	(094 _H)	Application Reset Value: 0000 0000 _H
P15_OMCR		
Port 15 Output Modification Clear Register	(094 _H)	Application Reset Value: 0000 0000 _H
P40_OMCR		
Port 40 Output Modification Clear Register	(094 _H)	Application Reset Value: 0000 0000 _H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	PCL11	PCL10	PCL9	PCL8	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-11)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28	r	Reserved Read as 0; should be written with 0

Table 158 Access Mode Restrictions sorted by descending priority

Applies to **P02_OMCR**
 Applies to **P10_OMCR**
 Applies to **P14_OMCR**
 Applies to **P15_OMCR**
 Applies to **P40_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-11)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P12_OMCR
Port 12 Output Modification Clear Register (094_H) **Application Reset Value: 0000 0000_H**

P13_OMCR
Port 13 Output Modification Clear Register (094_H) **Application Reset Value: 0000 0000_H**

P22_OMCR
Port 22 Output Modification Clear Register (094_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	PCL3	PCL2	PCL1	PCL0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20	r	Reserved Read as 0; should be written with 0

Table 159 Access Mode Restrictions sorted by descending priority

Applies to **P12_OMCR**

Applies to **P13_OMCR**

Applies to **P22_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P21_OMCR

Port 21 Output Modification Clear Register

(094_H)

Application Reset Value: 0000 0000_H

P23_OMCR

Port 23 Output Modification Clear Register

(094_H)

Application Reset Value: 0000 0000_H

P32_OMCR

Port 32 Output Modification Clear Register

(094_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
0	0	0	0	0	0	0	0	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
								0								
								r								

Field	Bits	Type	Description
PCLx (x=0-7)	x+16	w0	Clear Bit x Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0 _B No operation 1 _B Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28, 27, 26, 25, 24	r	Reserved Read as 0; should be written with 0

Table 160 Access Mode Restrictions sorted by descending priority

Applies to **P21_OMCR**

Applies to **P23_OMCR**

Applies to **P32_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-7)	

Port 13 LVDS Pad Control Register x

The LVDS Pad Control Register controls the RX or TX functions of the LVDS pads. For usage of RX pad, bit field [7:0] are applicable. If used for TX pad, bit field [15:7] apply.

The sleep functionality of the LVDS pads is not controllable via this register. This is exclusively controlled by the HSCT module when this is connected.

The register x controls in general the pad pair 2*x and 2*x+1 of the port n.

Exceptionally when available the pad pair P14.9 and P14.10 is controlled by P14_LPCR5.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Attention: The bit field P21_LPCR2.PS configures the pad supply for the LVDS bias distributor for all (not-RIF) LVDS pads and for the oscillator. Therefore even if no LVDS pad is used, this field has to be configured to the correct pad supply level.

P13_LPCR_x (x=0-1)

Port 13 LVDS Pad Control Register x (0A0_H+x*4) Reset Value: [Table 162](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_P WDPD	TX_PD	VOSEX T	VOSDY N	VDIFFADJ		TX_EN	TEN_C TRL	PS	0		0		0	0	0
rw	rw	rw	rw	rw		rw	rw	rw	r		r		r	r	r

Field	Bits	Type	Description
PS	7	rw	Pad Supply Selection Selects between 5V or 3.3V supply on V _{EXT} for the pad-pair. Used in RX and TX pads! 0 _B 3.3V supply 1 _B 5V supply
TEN_CTRL	8	rw	LVDS TX_EN controller The LVDS TX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 _B Port controlled 1 _B Reserved
TX_EN	9	rw	Enable Transmit LVDS Enable the transmit LVDS / disable CMOS path. If this bit is set to 0 - no transfer on LVDS data path can be initiated and the LVDS driver is disabled (powered down). 0 _B disable LVDS / enable CMOS mode 1 _B enable LVDS / disable CMOS mode
VDIFFADJ	11:10	rw	LVDS Output Amplitude Tuning With these two configuration bits the LVDS output current/amplitude can be adjusted. The voltage swing depending on VDIFFADJ setting is documented in the Data Sheet, see parameter V _{OD} .
VOSDYN	12	rw	Tune Bit of VOS Control Loop Static/Dynamic Tune bit to change V _{OS} control loop between static and dynamic mode. Don't change reset value.
VOSEXT	13	rw	Tune Bit of VOS Control Loop Internal/External Tune bit to change V _{OS} control loop. Don't change reset value.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
TX_PD	14	rw	LVDS Power Down Unused in this device. LVDS disabled by TX_EN means power down. 0 _B LVDS power on 1 _B LVDS power down (default)
TX_PWDPD	15	rw	Enable TX Power down pull down. This function disables or enables the LVDS pull down resistor. The application code must disable TX power down pull down resistor with a power up. With a LVDS Power Down configuration the pull down function must be enabled, if required. 0 _B disabled TX Power down pull down resistor. 1 _B enabled TX Power down pull down resistor.
0	0, 1, 2, 5:3, 6, 31:16	r	Reserved Read as 0; should be written with 0

Table 161 Access Mode Restrictions of P13_LPCR_x (x=0-1) sorted by descending priority

Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT
Otherwise (default)	r	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT

Table 162 Reset Values of P13_LPCR_x (x=0-1)

Reset Type	Reset Value	Note
After SSW execution	0000 5480 _H	Initial value of RX depends on trimming

P14_LPCR_x (x=5)

Port 14 LVDS Pad Control Register x (0A0_H+x*4) Reset Value: Table 164

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PS	LVDS M	LRXTERM	TERM	RX_EN	REN_C TRL		
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
REN_CTRL	0	rw	LVDS RX_EN controller The LVDS RX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 _B Port controlled 1 _B Reserved
RX_EN	1	rw	Enable Receive LVDS Enable the receive LVDS / disable CMOS path. If this bit is set to 0 – no transfer from the LVDS sender can be received and the receiver LVDS is in low power state. 0 _B disable LVDS / enable CMOS mode (reserved for pads without CMOS input stage) 1 _B enable LVDS / disable CMOS mode
TERM	2	rw	Select Receiver Termination Mode Selects a suitable internal load resistor between both pads. 0 _B external termination - on the PCB 1 _B 100 Ω Receiver internal termination
LRXTERM	5:3	rw	LVDS RX Poly-resistor configuration value Programming bits for the on die poly resistor termination. The value is configured during production test. Each chip configuration on this bit field is unique and configured during production testing. <i>Note: The configuration value shall not be changed by user after start-up for a guaranteed behavior.</i>
LVDSM	6	rw	LVDS-M Mode Selects reduced frequency mode “LVDS-M” of the receiver. This mode reduces the static current of the RX pad. The max data rate is reduced to 160 Mbps (80 MHz). 0 _B LVDS-H Mode 1 _B LVDS-M Mode
PS	7	rw	Pad Supply Selection Selects between 5V or 3.3V supply on V_{EXT} for the pad-pair. Used in RX and TX pads! 0 _B 3.3V supply 1 _B 5V supply
0	8, 9, 11:10, 12, 13, 14, 15, 31:16	r	Reserved Read as 0; should be written with 0

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 163 Access Mode Restrictions of P14_LPCR_x (x=5) sorted by descending priority

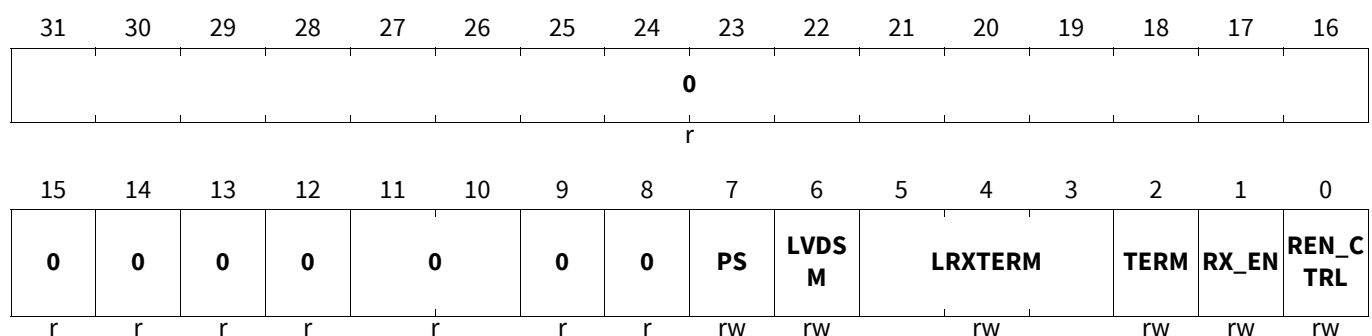
Mode Name	Access Mode	Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM
Otherwise (default)	r	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM

Table 164 Reset Values of P14_LPCR_x (x=5)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 0000 0000 0000 0000 11XX X000 _B	Initial value of RX depends on trimming

P21_LPCR_x (x=1)

Port 21 LVDS Pad Control Register x (0A0_H+x*4) Reset Value: Table 166



Field	Bits	Type	Description
REN_CTRL	0	rw	LVDS RX_EN controller The LVDS RX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 _B Port controlled 1 _B HSCT controlled
RX_EN	1	rw	Enable Receive LVDS Enable the receive LVDS / disable CMOS path. If this bit is set to 0 – no transfer from the LVDS sender can be received and the receiver LVDS is in low power state. 0 _B disable LVDS / enable CMOS mode (reserved for pads without CMOS input stage) 1 _B enable LVDS / disable CMOS mode
TERM	2	rw	Select Receiver Termination Mode Selects a suitable internal load resistor between both pads. 0 _B external termination - on the PCB 1 _B 100 Ω Receiver internal termination

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
LRXTERM	5:3	rw	LVDS RX Poly-resistor configuration value Programming bits for the on die poly resistor termination. The value is configured during production test. Each chip configuration on this bit field is unique and configured during production testing. <i>Note: The configuration value shall not be changed by user after start-up for a guaranteed behavior.</i>
LVDSM	6	rw	LVDS-M Mode Selects reduced frequency mode “LVDS-M” of the receiver. This mode reduces the static current of the RX pad. The max data rate is reduced to 160 Mbps (80 MHz). 0 _B LVDS-H Mode 1 _B LVDS-M Mode
PS	7	rw	Pad Supply Selection Selects between 5V or 3.3V supply on V _{EXT} for the pad-pair. Used in RX and TX pads! 0 _B 3.3V supply 1 _B 5V supply
0	8, 9, 11:10, 12, 13, 14, 15, 31:16	r	Reserved Read as 0; should be written with 0

Table 165 Access Mode Restrictions of P21_LPCR_x (x=1) sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM	write access for enabled masters
Otherwise (default)	r	LRXTERM, LVDSM, PS, REN_CTRL, RX_EN, TERM	

Table 166 Reset Values of P21_LPCR_x (x=1)

Reset Type	Reset Value	Note
After SSW execution	0000 0000 0000 0000 0000 0000 11XX X000 _B	Initial value of RX depends on trimming

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P21_LPCR_x (x=2)

Port 21 LVDS Pad Control Register x

(0A0_H+x*4)

Reset Value: [Table 168](#)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_P WDPD	TX_PD	VOSEX T	VOSDY N	VDIFFADJ		TX_EN	TEN_C TRL	PS	0	0		0	0	0	
rw	rw	rw	rw	rw		rw	rw	rw	r	r		r	r	r	

Field	Bits	Type	Description
PS	7	rw	Pad Supply Selection Selects between 5V or 3.3V supply on V _{EXT} for the pad-pair. Used in RX and TX pads! 0 _B 3.3V supply 1 _B 5V supply
TEN_CTRL	8	rw	LVDS TX_EN controller The LVDS TX_EN control function can be selected from the Port (default) or HSCT module (where this is connected). 0 _B Port controlled 1 _B HSCT controlled
TX_EN	9	rw	Enable Transmit LVDS Enable the transmit LVDS / disable CMOS path. If this bit is set to 0 - no transfer on LVDS data path can be initiated and the LVDS driver is disabled (powered down). 0 _B disable LVDS / enable CMOS mode 1 _B enable LVDS / disable CMOS mode
VDIFFADJ	11:10	rw	LVDS Output Amplitude Tuning With these two configuration bits the LVDS output current/amplitude can be adjusted. The voltage swing depending on VDIFFADJ setting is documented in the Data Sheet, see parameter V _{OD} .
VOSDYN	12	rw	Tune Bit of VOS Control Loop Static/Dynamic Tune bit to change V _{OS} control loop between static and dynamic mode. Don't change reset value.
VOSEXT	13	rw	Tune Bit of VOS Control Loop Internal/External Tune bit to change V _{OS} control loop. Don't change reset value.
TX_PD	14	rw	LVDS Power Down Unused in this device. LVDS disabled by TX_EN means power down. 0 _B LVDS power on 1 _B LVDS power down (default)

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Field	Bits	Type	Description
TX_PWDPD	15	rw	<p>Enable TX Power down pull down.</p> <p>This function disables or enables the LVDS pull down resistor. The application code must disable TX power down pull down resistor with a power up. With a LVDS Power Down configuration the pull down function must be enabled, if required.</p> <p>0_B disabled TX Power down pull down resistor. 1_B enabled TX Power down pull down resistor.</p>
0	0, 1, 2, 5:3, 6, 31:16	r	<p>Reserved</p> <p>Read as 0; should be written with 0</p>

Table 167 Access Mode Restrictions of P21_LPCR_x (x=2) sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT	write access for enabled masters
Otherwise (default)	r	PS, TEN_CTRL, TX_EN, TX_PD, TX_PWDPD, VDIFFADJ, VOSDYN, VOSEXT	

Table 168 Reset Values of P21_LPCR_x (x=2)

Reset Type	Reset Value	Note
After SSW execution	0000 5480 _H	Initial value of RX depends on trimming

Port 00 Access Enable Register 1

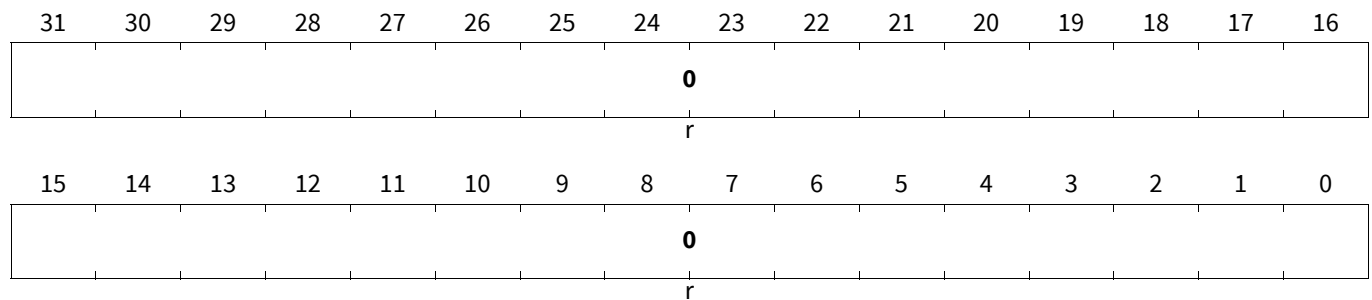
Each port has its own dedicated ACCEN0 and ACCEN1 registers.

The Access Enable Register 1 controls write¹⁾ access for transactions with the on chip bus master TAG ID 100000B to 111111B (see On Chip Bus chapter for the products TAG ID <-> master peripheral mapping). The BPI_FPI is prepared for a 6-bit TAG ID. ACCEN1 is not implemented with register bits as the related TAG IDs are not used in this product.

Mapping of TAG IDs to ACCEN1.EN_x: EN0 -> TAG ID 100000B, EN1 -> TAG ID 100001B, ... ,EN31 -> TAG ID 111111B.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_ACCEN1		
Port 00 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P02_ACCEN1		
Port 02 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P10_ACCEN1		
Port 10 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P11_ACCEN1		
Port 11 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P12_ACCEN1		
Port 12 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P13_ACCEN1		
Port 13 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P14_ACCEN1		
Port 14 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P15_ACCEN1		
Port 15 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P20_ACCEN1		
Port 20 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H
P21_ACCEN1		
Port 21 Access Enable Register 1	(0F8 _H)	Application Reset Value: 0000 0000 _H



Field	Bits	Type	Description
0	31:0	r	Reserved Read as 0; should be written with 0

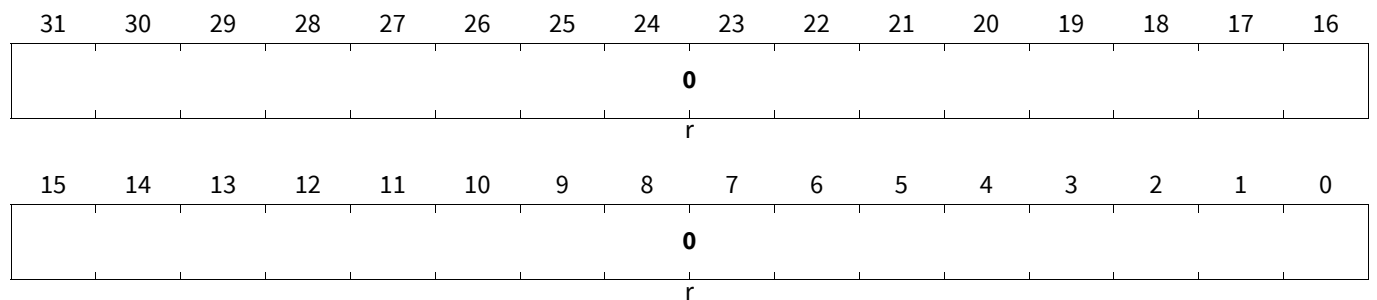
General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 169 Access Mode Restrictions sorted by descending priority

- Applies to **P00_ACCEN1**
- Applies to **P02_ACCEN1**
- Applies to **P10_ACCEN1**
- Applies to **P11_ACCEN1**
- Applies to **P12_ACCEN1**
- Applies to **P13_ACCEN1**
- Applies to **P14_ACCEN1**
- Applies to **P15_ACCEN1**
- Applies to **P20_ACCEN1**
- Applies to **P21_ACCEN1**

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above

- P22_ACCEN1**
Port 22 Access Enable Register 1 (0F8_H) **Application Reset Value: 0000 0000_H**
- P23_ACCEN1**
Port 23 Access Enable Register 1 (0F8_H) **Application Reset Value: 0000 0000_H**
- P32_ACCEN1**
Port 32 Access Enable Register 1 (0F8_H) **Application Reset Value: 0000 0000_H**
- P33_ACCEN1**
Port 33 Access Enable Register 1 (0F8_H) **Application Reset Value: 0000 0000_H**
- P40_ACCEN1**
Port 40 Access Enable Register 1 (0F8_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
0	31:0	r	Reserved Read as 0; should be written with 0

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 170 Access Mode Restrictions sorted by descending priority

 Applies to **P22_ACCEN1**

 Applies to **P23_ACCEN1**

 Applies to **P32_ACCEN1**

 Applies to **P33_ACCEN1**

 Applies to **P40_ACCEN1**

Mode Name	Access Mode	Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above

Port 00 Access Enable Register 0

Each port has its own dedicated ACCEN0 and ACCEN1 registers.

The Access Enable Register 0 controls write¹⁾ access for transactions with the on chip bus master TAG ID 000000B to 011111B (see On Chip Bus chapter for the products TAG ID <-> master peripheral mapping). The BPI_FPI is prepared for a 6-bit TAG ID. The registers ACCEN0 and ACCEN1 are providing one enable bit for each possible 6-bit TAG ID encoding.

Mapping of TAG IDs to ACCEN0.ENx: EN0 -> TAG ID 000000B, EN1 -> TAG ID 000001B , ... ,EN31 -> TAG ID 011111B.

1) The BPI_FPI Access Enable functionality controls only write transactions to the kernel registers. Read transactions are not influenced. SW has to take care for destructive/modifying read functionality in kernel registers.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

P00_ACCEN0		
Port 00 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P02_ACCEN0		
Port 02 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P10_ACCEN0		
Port 10 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P11_ACCEN0		
Port 11 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P12_ACCEN0		
Port 12 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P13_ACCEN0		
Port 13 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P14_ACCEN0		
Port 14 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P15_ACCEN0		
Port 15 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P20_ACCEN0		
Port 20 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H
P21_ACCEN0		
Port 21 Access Enable Register 0	(0FC _H)	Application Reset Value: FFFF FFFF _H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN31	EN30	EN29	EN28	EN27	EN26	EN25	EN24	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	Access Enable for Master TAG ID x This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n 0 _B Write access will not be executed 1 _B Write access will be executed

General Purpose I/O Ports and Peripheral I/O Lines (Ports)

Table 171 Access Mode Restrictions sorted by descending priority

- Applies to **P00_ACCENO**
- Applies to **P02_ACCENO**
- Applies to **P10_ACCENO**
- Applies to **P11_ACCENO**
- Applies to **P12_ACCENO**
- Applies to **P13_ACCENO**
- Applies to **P14_ACCENO**
- Applies to **P15_ACCENO**
- Applies to **P20_ACCENO**
- Applies to **P21_ACCENO**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rw	ENx (x=0-31)	write access only for masters with supervisor mode
Otherwise (default)	r	ENx (x=0-31)	

- P22_ACCENO**
Port 22 Access Enable Register 0 (0FC_H) Application Reset Value: FFFF FFFF_H
- P23_ACCENO**
Port 23 Access Enable Register 0 (0FC_H) Application Reset Value: FFFF FFFF_H
- P32_ACCENO**
Port 32 Access Enable Register 0 (0FC_H) Application Reset Value: FFFF FFFF_H
- P33_ACCENO**
Port 33 Access Enable Register 0 (0FC_H) Application Reset Value: FFFF FFFF_H
- P40_ACCENO**
Port 40 Access Enable Register 0 (0FC_H) Application Reset Value: FFFF FFFF_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN31	EN30	EN29	EN28	EN27	EN26	EN25	EN24	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	Access Enable for Master TAG ID x This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n 0 _B Write access will not be executed 1 _B Write access will be executed

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
Table 172 Access Mode Restrictions sorted by descending priority

 Applies to **P22_ACCENO**

 Applies to **P23_ACCENO**

 Applies to **P32_ACCENO**

 Applies to **P33_ACCENO**

 Applies to **P40_ACCENO**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rw	ENx (x=0-31)	write access only for masters with supervisor mode
Otherwise (default)	r	ENx (x=0-31)	

14.4 Connectivity

The connectivity of the Ports is documented in the Pinning documentation of each device.

General Purpose I/O Ports and Peripheral I/O Lines (Ports)
14.5 Revision History**Table 173 Revision History**

Reference	Changes to Previous Version	Comment
V1.8.20		
Page 35	Removed confusing phrase “, only input selection apply.” from register IOCRx from bitfield description of PC.	
–	Only cosmetic change: register documentation generator merges more reserved bit fields (e.g. “0” or “1” bit fields).	
V1.8.21		
–	No content of this Appx changed. TC3Ax Appx added to delivery package and change in Feature List of family chapter.	

Safety Management Unit (SMU)

15 Safety Management Unit (SMU)

This chapter describes the Safety Management Unit (short SMU) module of the TC36x.

15.1 TC36x Specific IP Configuration

See features in family spec.

Safety Management Unit (SMU)

15.2 TC36x Specific Register Set

SMU_core Specific Register Set

Register Address Space Table

Table 174 Register Address Space - SMU

Module	Base Address	End Address	Note
SMU	F0036800 _H	F0036FFF _H	FPI slave interface

Register Overview Table

Table 175 Register Overview - SMU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_CLC	Clock Control Register	000 _H	U,SV	SV,P	Application Reset	See Family Spec
SMU_ID	Module Identification Register	008 _H	U,SV	BE	Application Reset	See Family Spec
SMU_CMD	Command Register	020 _H	U,SV	SV,P,32	Application Reset	See Family Spec
SMU_STS	Status Register	024 _H	U,SV	SV,P,32	Application Reset	See Family Spec
SMU_FSP	Fault Signaling Protocol	028 _H	U,SV	SV,P,SE,32	PowerOn Reset	See Family Spec
SMU_AGC	Alarm Global Configuration	02C _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTC	Recovery Timer Configuration	030 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_KEYS	Key Register	034 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_DBG	Debug Register	038 _H	U,SV	BE	PowerOn Reset	See Family Spec

Safety Management Unit (SMU)

Table 175 Register Overview - SMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_PCTL	Port Control	03C _H	U,SV	SV,P,SE,32	PowerOn Reset	See Family Spec
SMU_AFCNT	Alarm and Fault Counter	040 _H	U,SV	BE	PowerOn Reset	See Family Spec
SMU_RTAC00	Recovery Timer 0 Alarm Configuration 0	060 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC01	Recovery Timer 0 Alarm Configuration 1	064 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC10	Recovery Timer 1 Alarm Configuration 0	068 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC11	Recovery Timer 1 Alarm Configuration 1	06C _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_AEX	Alarm Executed Status Register	070 _H	U,SV	BE	Application Reset	See Family Spec
SMU_AEXCLR	Alarm Executed Status Clear Register	074 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_AGiCFj (i=0-1;j=0-2) (i=2-5;j=0-2) (i=6;j=0-2) (i=7;j=0-2) (i=8;j=0-2) (i=9;j=0-2) (i=10;j=0-2) (i=11;j=0-2)	Alarm Configuration Register	100 _H +i*1 2+j*4	U,SV	SV,P,SE,32	Application Reset	5
SMU_AGiFSP (i=0-11)	SMU_core FSP Configuration Register	190 _H +i*4	U,SV	SV,P,SE,32	Application Reset	10
SMU_AGi (i=0-11)	Alarm Status Register	1C0 _H +i*4	U,SV	SV,P,SE,32	Application Reset	14
SMU_ADi (i=0-11)	Alarm Debug Register	200 _H +i*4	U,SV	BE	PowerOn Reset	18
SMU_RMCTL	Register Monitor Control	300 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec

Safety Management Unit (SMU)
Table 175 Register Overview - SMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_RMEF	Register Monitor Error Flags	304 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RMSTS	Register Monitor Self Test Status	308 _H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_OCS	OCDS Control and Status	7E8 _H	U,SV	SV,P,OEN	Debug Reset	See Family Spec
SMU_ACCEN1	SMU_core Access Enable Register 1	7F8 _H	U,SV	BE	Application Reset	See Family Spec
SMU_ACCEN0	SMU_core Access Enable Register 0	7FC _H	U,SV	SV,SE	Application Reset	See Family Spec

SMU_stdby Specific Register Set

For SMU_stdby specific register set refer to the Power Management System chapter.

15.3 TC36x Specific Registers

Safety Management Unit (SMU)

15.3.1 TC36x Specific Registers

15.3.1.1 FPI slave interface

Alarm Configuration Register

SMU_AGiCFj (i=0-1;j=0-2)

Alarm Configuration Register (100_H+i*12+j*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	CF24	CF23	CF22	0	0	0	0	0	0
r	r	r	r	r	r	r	rw	rw	rw	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	0	CF2	CF1	CF0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-2,4-14,22-24)	z	rw	<p>Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group.</p> <p>0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1</p>
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	<p>Reserved Read as 0; should be written with 0.</p>

SMU_AGiCFj (i=2-5;j=0-2)

Alarm Configuration Register (100_H+i*12+j*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Safety Management Unit (SMU)

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	Reserved Read as 0; should be written with 0.

SMU_AGiCFj (i=6;j=0-2)

Alarm Configuration Register

$$(100_H + i * 12 + j * 4)$$

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	CF25	CF24	CF23	0	CF21	CF20	CF19	CF18	CF17	CF16
r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	CF14	CF13	CF12	CF11	CF10	0	CF8	CF7	CF6	CF5	CF4	0	CF2	CF1	CF0
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-2, 4-8, 10-21, 23-25)	z	rw	Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 _B Configuration flag x (x=0-2) is set to 0 1 _B Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 22, 9, 3	r	Reserved Read as 0; should be written with 0.

SMU_AGiCFj (i=7;j=0-2)

Alarm Configuration Register

$$(100_H + i * 12 + j * 4)$$

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24	CF23	CF22	0	CF20	0	0	CF17	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	r	r	rw	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	CF2	CF1	CF0
r	r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw

Safety Management Unit (SMU)

Field	Bits	Type	Description
CFz (z=0-2,17,20,22-31)	z	rw	Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 _B Configuration flag x (x=0-2) is set to 0 1 _B Configuration flag x (x=0-2) is set to 1
0	21, 19, 18, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3	r	Reserved Read as 0; should be written with 0.

SMU_AGiCFj (i=8;j=0,2)

Alarm Configuration Register

(100_H+i*12+j*4)

Application Reset Value: 0001 FC00_H

SMU_AGiCFj (i=8;j=1)

Alarm Configuration Register

(100_H+i*12+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	CF30	CF29	CF28	CF27	CF26	CF25	0	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-11,16-23,25-31)	z	rw	Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 _B Configuration flag x (x=0-2) is set to 0 1 _B Configuration flag x (x=0-2) is set to 1
0	24, 15, 14, 13, 12	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGiCFj (i=9;j=0-2)

Alarm Configuration Register (100_H+i*12+j*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	CF17	CF16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	0	0	0	0	0	0	0	0	0	CF5	0	CF3	0	CF1	CF0
rw	r	r	r	r	r	r	r	r	r	rw	r	rw	r	rw	rw

Field	Bits	Type	Description
CFz (z=0-1,3,5,15-17)	z	rw	<p>Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group.</p> <p>0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1</p>
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	<p>Reserved Read as 0; should be written with 0.</p>

SMU_AGiCFj (i=10;j=0)

Alarm Configuration Register (100_H+i*12+j*4) Application Reset Value: 0000 0000_H

SMU_AGiCFj (i=10;j=1-2)

Alarm Configuration Register (100_H+i*12+j*4) Application Reset Value: 0003 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	CF22	CF21	CF20	0	CF18	CF17	CF16
r	r	r	r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Safety Management Unit (SMU)

Field	Bits	Type	Description
CFz (z=0-18,20-22)	z	rw	Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 _B Configuration flag x (x=0-2) is set to 0 1 _B Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	Reserved Read as 0; should be written with 0.

SMU_AGiCFj (i=11;j=0-2)

Alarm Configuration Register (100 _H +i*12+j*4)										Application Reset Value: 0000 0000 _H					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	CF13	CF12	0	CF10	CF9	0	0	0	CF5	CF4	CF3	CF2	0	0
r	r	rw	rw	r	rw	rw	r	r	r	rw	rw	rw	rw	r	r

Field	Bits	Type	Description
CFz (z=2-5,9-10,12-13)	z	rw	Configuration flag x (x=0-2) for alarm z belonging to alarm group i. The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0 _B Configuration flag x (x=0-2) is set to 0 1 _B Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 8, 7, 6, 1, 0	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_core FSP Configuration Register

SMU_AGiFSP (i=0-1)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	FE24	FE23	FE22	0	0	0	0	0	0
r	r	r	r	r	r	r	rw	rw	rw	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FE14	FE13	FE12	FE11	FE10	FE9	FE8	FE7	FE6	FE5	FE4	0	FE2	FE1	FE0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-2,4-14,22-24)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	Reserved Read as 0; should be written with 0.

SMU_AGiFSP (i=2-5)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGiFSP (i=6)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	FE25	FE24	FE23	0	FE21	FE20	FE19	FE18	FE17	FE16
r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	FE14	FE13	FE12	FE11	FE10	0	FE8	FE7	FE6	FE5	FE4	0	FE2	FE1	FE0
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-2,4-8,10-21,23-25)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 22, 9, 3	r	Reserved Read as 0; should be written with 0.

SMU_AGiFSP (i=7)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FE31	FE30	FE29	FE28	FE27	FE26	FE25	FE24	FE23	FE22	0	FE20	0	0	FE17	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	r	r	rw	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	FE2	FE1	FE0
r	r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-2,17,20,22-31)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	21, 19, 18, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGiFSP (i=8)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FE31	FE30	FE29	FE28	FE27	FE26	FE25	0	FE23	FE22	FE21	FE20	FE19	FE18	FE17	FE16
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	FE11	FE10	FE9	FE8	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-11,16-23,25-31)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	24, 15, 14, 13, 12	r	Reserved Read as 0; should be written with 0.

SMU_AGiFSP (i=9)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	FE17	FE16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	0	0	0	0	0	0	0	0	0	FE5	0	FE3	0	FE1	FE0
rw	r	r	r	r	r	r	r	r	r	rw	r	rw	r	rw	rw

Field	Bits	Type	Description
FEz (z=0-1,3,5,15-17)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGiFSP (i=10)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0003 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	FE22	FE21	FE20	0	FE18	FE17	FE16
r	r	r	r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-18,20-22)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	Reserved Read as 0; should be written with 0.

SMU_AGiFSP (i=11)

SMU_core FSP Configuration Register (190_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	FE13	FE12	0	FE10	FE9	0	0	0	FE5	FE4	FE3	FE2	0	0
r	r	rw	rw	r	rw	rw	r	r	r	rw	rw	rw	rw	r	r

Field	Bits	Type	Description
FEz (z=2-5,9-10,12-13)	z	rw	Fault signaling configuration flag for alarm z belonging to alarm group i. 0 _B FSP disabled for this alarm event 1 _B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 8, 7, 6, 1, 0	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

Alarm Status Register

Refer to Alarm Status Registers for the conditions to set and reset the status flag by software.

SMU_AGi (i=0-1)

Alarm Status Register (1C0_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	SF24	SF23	SF22	0	0	0	0	0	0
r	r	r	r	r	r	r	rwh	rwh	rwh	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SF14	SF13	SF12	SF11	SF10	SF9	SF8	SF7	SF6	SF5	SF4	0	SF2	SF1	SF0
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-2,4-14,22-24)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	Reserved Read as 0; should be written with 0.

SMU_AGi (i=2-5)

Alarm Status Register (1C0_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGi (i=6)

Alarm Status Register

(1C0_H+i*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	SF25	SF24	SF23	0	SF21	SF20	SF19	SF18	SF17	SF16
r	r	r	r	r	r	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	SF14	SF13	SF12	SF11	SF10	0	SF8	SF7	SF6	SF5	SF4	0	SF2	SF1	SF0
rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-2,4-8,10-21,23-25)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 22, 9, 3	r	Reserved Read as 0; should be written with 0.

SMU_AGi (i=7)

Alarm Status Register

(1C0_H+i*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SF31	SF30	SF29	SF28	SF27	SF26	SF25	SF24	SF23	SF22	0	SF20	0	0	SF17	0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	r	r	rwh	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	SF2	SF1	SF0
r	r	r	r	r	r	r	r	r	r	r	r	r	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-2,17,20,22-31)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	21, 19, 18, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGi (i=8)

Alarm Status Register (1C0_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SF31	SF30	SF29	SF28	SF27	SF26	SF25	0	SF23	SF22	SF21	SF20	SF19	SF18	SF17	SF16
rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	SF11	SF10	SF9	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-11,16-23,25-31)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	24, 15, 14, 13, 12	r	Reserved Read as 0; should be written with 0.

SMU_AGi (i=9)

Alarm Status Register (1C0_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SF17	SF16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	0	0	0	0	0	0	0	0	0	SF5	0	SF3	0	SF1	SF0
rwh	r	r	r	r	r	r	r	r	r	rwh	r	rwh	r	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-1,3,5,15-17)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_AGi (i=10)

Alarm Status Register (1C0_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	SF22	SF21	SF20	0	SF18	SF17	SF16
r	r	r	r	r	r	r	r	r	rwh	rwh	rwh	r	rwh	rwh	rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	SF14	SF13	SF12	SF11	SF10	SF9	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-18,20-22)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	Reserved Read as 0; should be written with 0.

SMU_AGi (i=11)

Alarm Status Register (1C0_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SF13	SF12	0	SF10	SF9	0	0	0	SF5	SF4	SF3	SF2	0	0
r	r	rwh	rwh	r	rwh	rwh	r	r	r	rwh	rwh	rwh	rwh	r	r

Field	Bits	Type	Description
SFz (z=2-5,9-10,12-13)	z	rwh	Status flag for alarm z belonging to alarm group i. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 8, 7, 6, 1, 0	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

Alarm Debug Register

Note: Writing to this register has no effect

SMU_ADi (i=0-1)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	DF24	DF23	DF22	0	0	0	0	0	0
r	r	r	r	r	r	r	rh	rh	rh	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DF14	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	0	DF2	DF1	DF0
r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-2,4-14,22-24)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	Reserved Read as 0; should be written with 0.

SMU_ADi (i=2-5)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Safety Management Unit (SMU)

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	Reserved Read as 0; should be written with 0.

SMU_ADi (i=6)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	DF25	DF24	DF23	0	DF21	DF20	DF19	DF18	DF17	DF16
r	r	r	r	r	r	rh	rh	rh	r	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	DF14	DF13	DF12	DF11	DF10	0	DF8	DF7	DF6	DF5	DF4	0	DF2	DF1	DF0
rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh	rh	r	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-2,4-8,10-21,23-25)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 22, 9, 3	r	Reserved Read as 0; should be written with 0.

SMU_ADi (i=7)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF31	DF30	DF29	DF28	DF27	DF26	DF25	DF24	DF23	DF22	0	DF20	0	0	DF17	0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	r	rh	r	r	rh	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	DF2	DF1	DF0
r	r	r	r	r	r	r	r	r	r	r	r	r	rh	rh	rh

Safety Management Unit (SMU)

Field	Bits	Type	Description
DFz (z=0-2,17,20,22-31)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	21, 19, 18, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3	r	Reserved Read as 0; should be written with 0.

SMU_ADi (i=8)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF31	DF30	DF29	DF28	DF27	DF26	DF25	0	DF23	DF22	DF21	DF20	DF19	DF18	DF17	DF16
rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-11,16-23,25-31)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	24, 15, 14, 13, 12	r	Reserved Read as 0; should be written with 0.

SMU_ADi (i=9)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	DF17	DF16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	0	0	0	0	0	0	0	0	0	DF5	0	DF3	0	DF1	DF0
rh	r	r	r	r	r	r	r	r	r	rh	r	rh	r	rh	rh

Safety Management Unit (SMU)

Field	Bits	Type	Description
DFz (z=0-1,3,5,15-17)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	Reserved Read as 0; should be written with 0.

SMU_ADi (i=10)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	DF22	DF21	DF20	0	DF18	DF17	DF16
r	r	r	r	r	r	r	r	r	rh	rh	rh	r	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	DF14	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-18,20-22)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	Reserved Read as 0; should be written with 0.

Safety Management Unit (SMU)

SMU_ADi (i=11)

Alarm Debug Register

(200_H+i*4)

PowerOn Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DF13	DF12	0	DF10	DF9	0	0	0	DF5	DF4	DF3	DF2	0	0
r	r	rh	rh	r	rh	rh	r	r	r	rh	rh	rh	rh	r	r

Field	Bits	Type	Description
DFz (z=2-5,9-10,12-13)	z	rh	Diagnosis flag for alarm z belonging to alarm group i. The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0 _B Status flag z does not report a fault condition 1 _B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 8, 7, 6, 1, 0	r	Reserved Read as 0; should be written with 0.

15.4 TC36x Specific Alarm Mapping

This section defines the mapping between the alarm signals at the input of the SMU in the TC36x and the alarm. For that purpose alarm groups are defined. There is a one-to-one relationship between an alarm group index ALM<n>[index] signal and the alarm configuration and status registers (AG<n>[index]). A group is made of up to 32 alarms; for convenience some entries may be reserved.

15.4.1 TC36x Specific Pre-Alarms

There are situations where it is not necessary to implement configuration and status registers for every internal alarm event; a typical case is a module with multiple SRAMs. For that, alarm inputs, called pre-alarms, are combined together with a logical OR internally in SMU. The result is then connected to the alarm group.

Safety Management Unit (SMU)

MTU Pre-Alarm Mapping

Table 176 MTU Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
CPU0.DMEM - Correctable error CPU0.DLMU - Correctable error CPU0.DMEM1 - Correctable error	OR	ALM0[9]
CPU0.DMEM - Uncorrectable Critical error CPU0.DLMU - Uncorrectable Critical error CPU0.DMEM1 - Uncorrectable Critical error	OR	ALM0[10]
CPU0.DMEM - Miscellaneous error CPU0.DLMU - Miscellaneous error CPU0.DMEM1 - Miscellaneous error	OR	ALM0[11]
CPU1.DMEM - Correctable error CPU1.DLMU - Correctable error CPU1.DMEM1 - Correctable error	OR	ALM1[9]
CPU1.DMEM - Uncorrectable Critical error CPU1.DLMU - Uncorrectable Critical error CPU1.DMEM1 - Uncorrectable Critical error	OR	ALM1[10]
CPU1.DMEM - Miscellaneous error CPU1.DLMU - Miscellaneous error CPU1.DMEM1 - Miscellaneous error	OR	ALM1[11]
DAM0 - Correctable error FSI_RAM - Correctable error	OR	ALM7[0]
DAM0 - Uncorrectable critical error FSI_RAM - Uncorrectable critical error	OR	ALM7[1]
DAM0 - Miscellaneous error FSI_RAM - Miscellaneous error	OR	ALM7[2]
DMA - Correctable error PSI5 - Correctable error SCR.XRAM - Correctable error SCR.RAMINT - Correctable error GIGETHERNET.RX0 - Correctable error GIGETHERNET.TX0 - Correctable error	OR	ALM6[19]
DMA - Uncorrectable Critical error PSI5 - Uncorrectable Critical error SCR.XRAM - Uncorrectable critical error SCR.RAMINT - Uncorrectable Critical error GIGETHERNET.RX0 - Uncorrectable Critical error GIGETHERNET.TX0 - Uncorrectable Critical error	OR	ALM6[20]
DMA - Miscellaneous error PSI5 - Miscellaneous error SCR.XRAM - Miscellaneous error SCR.RAMINT - Miscellaneous error GIGETHERNET.RX0 - Miscellaneous error GIGETHERNET.TX0 - Miscellaneous error	OR	ALM6[21]

Safety Management Unit (SMU)
Table 176 MTU Pre-Alarm Mapping (cont'd)

Alarm Source	Logic	Alarm Index
GTM.FIFO - Correctable error GTM.MCS0F - Correctable error GTM.MCS1F - Correctable error GTM.DPLL1A - Correctable error GTM.DPLL1BC - Correctable error GTM.DPLL2 - Correctable error	OR	ALM6[10]
GTM.FIFO - Uncorrectable Critical error GTM.MCS0F - Uncorrectable Critical error GTM.MCS1F - Uncorrectable Critical error GTM.DPLL1A - Uncorrectable Critical error GTM.DPLL1BC - Uncorrectable Critical error GTM.DPLL2 - Uncorrectable Critical error	OR	ALM6[11]
GTM.FIFO - Miscellaneous error GTM.MCS0F - Miscellaneous error GTM.MCS1F - Miscellaneous error GTM.DPLL1A - Miscellaneous error GTM.DPLL1BC - Miscellaneous error GTM.DPLL2 - Miscellaneous error	OR	ALM6[12]
CAN.MCAN0 - Correctable error CAN.MCAN1 - Correctable error	OR	ALM6[16]
CAN.MCAN0 - Uncorrectable critical error CAN.MCAN1 - Uncorrectable critical error	OR	ALM6[17]
CAN.MCAN0 - Miscellaneous error CAN.MCAN1 - Miscellaneous error	OR	ALM6[18]
ERAY.OBF0 - Correctable error ERAY.TBF_IBF0 - Correctable error ERAY.MBF0 - Correctable error	OR	ALM6[13]
ERAY.OBF0 - Uncorrectable Critical error ERAY.TBF_IBF0 - Uncorrectable Critical error ERAY.MBF0 - Uncorrectable Critical error	OR	ALM6[14]
ERAY.OBF0 - Miscellaneous error ERAY.TBF_IBF0 - Miscellaneous error ERAY.MBF0 - Miscellaneous error	OR	ALM6[15]

Safety Management Unit (SMU)

Safety Flip-flop Pre-Alarm Mapping

Table 177 Safety Flip-flop Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
MTU - Safety flip-flop uncorrectable error IOM - Safety flip-flop uncorrectable error IR - Safety flip-flop uncorrectable error SCU - Safety flip-flop uncorrectable error PMS - Safety flip-flop uncorrectable error DMA - Safety flip-flop uncorrectable error SYS_PLL.PER_PLL - Safety flip-flop uncorrectable error CERBERUS - Safety flip-flop uncorrectable error CCU - Safety flip-flop uncorrectable error SMU_core - Safety flip-flop uncorrectable error	OR	ALM10[21]

Module Access Enable Pre-Alarm Mapping

Table 178 Module Access Enable Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
IR - Access Enable error HSM - Access Enable error	OR	ALM10[22]

PMS Pre-Alarm Mapping

Table 179 PMS Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
PMS - Uncorrectable error SMU.SMU_stdby - Safety flip-flop Uncorrectable error	OR	ALM21[7]
HSM.VDD - Under Voltage HSM.VDDP3 - Under Voltage HSM.VEXT - Under Voltage	OR	ALM9[17]
HSM.VDD - Over Voltage HSM.VDDP3 - Over Voltage HSM.VEXT - Over Voltage	OR	ALM9[16]
PMS.VDD - Over voltage PMS.VDDPD - Over voltage PMS.VDDP3 - Over voltage PMS.VDDM - Over voltage PMS.VEXT - Over voltage PMS.VEVR SB - Over voltage	OR	ALM9[3]

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Table 179 PMS Pre-Alarm Mapping (cont'd)

Alarm Source	Logic	Alarm Index
PMS.VDD - Under voltage PMS.VDDPD - Under voltage PMS.VDDP3 - Under voltage PMS.VDDM - Under voltage PMS.VEXT - Under voltage PMS.VEVR SB - Under voltage	OR	ALM9[5]
PMS.EVRC - Short to Low PMS.EVRC - Short to High PMS.EVR33 - Short to Low PMS.EVR33 - Short to High	OR	ALM9[15]

15.4.2 TC36x Specific Alarms

The following tables fully specify the mapping between the alarms provided by the safety mechanisms implemented by the microcontroller and the alarm groups.

In the following tables the column “Safety Mechanism & Error Indication” indicates to which safety mechanism the alarm is related. If multiple safety mechanisms are indicated, the alarm corresponds to the detection of an error by one of the listed safety mechanisms.

For some safety mechanisms different terms are used in the microcontroller documents; the following list provides a guideline between the term used in the alarm tables and the other definitions, in bold the definition used in the alarm tables.

- Register Access Protection or alternatively called Safety Register Protection
 - Purpose: Monitors the master identifier of a given bus-master during a write access to a configuration register. The master identifier is a hard-coded information that is provided during any bus access. If the master identifier is not enabled by the Register Access Protection configuration registers (ACCEN0) the write is aborted. Most of the modules do not provide a dedicated alarm for this event and instead will generate a bus error. Therefore the Register Access Protection is only documented where a dedicated alarm is available.
 - Note: for peripherals that implement memory-mapped SRAMs, the write accesses to the memories are monitored as well.
- Bus-level Memory Protection Unit (MPU) or alternatively called Safety Memory Protection
 - Purpose: Monitors the master identifier and the address of a given bus-master during a write access to a local SRAM. The master identifier is a hard-coded information that is provided during any bus access. If the master identifier is enabled by the Bus-level MPU configuration registers and the address is within the valid address range the write is accepted, otherwise the write is aborted and a Bus-level MPU alarm is issued.
 - The SRAMs monitored are the {PSPR, DSPR, DLMU} SRAMs of each CPU and the LMU SRAMs when available in the product.

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Alarm Mapping related to ALM0 group

Table 180 Alarm Mapping related to ALM0 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[0]	cpu_pfi_pfrwb_0	Safety Mechanism: Lockstep CPU Alarm: CPU0 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM0[1]	cpu_pfi_pfrwb_0	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU0 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse
ALM0[2]	cpu_pfi_pfrwb_0	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU0 PFLASH0 Read Path Error Alarm Type: Pulse
ALM0[3]	Reserved	Reserved
ALM0[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM0[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM0[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM0[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM0[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM0[9]	Page 23	Safety Mechanism: SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM0[10]	Page 23	Safety Mechanism: SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM0[11]	Page 23	Safety Mechanism(s): SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level

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Table 180 Alarm Mapping related to ALM0 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Single bit error correction Alarm Type: Level
ALM0[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM0[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM0[21:15]	Reserved	Reserved
ALM0[22]	cpu_pfi_pfrwb_0	Safety Mechanism: SRI End-to-End EDC Alarm: CPU0 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM0[23]	cpu_pfi_pfrwb_0	Safety Mechanism: SRI End-to-End EDC Alarm: CPU0 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM0[24]	cpu_pfi_pfrwb_0	Safety Mechanism: Exception Monitor Alarm: CPU0 exception (interrupt/trap) Alarm Type: Pulse
ALM0[31:25]	Reserved	Reserved

Alarm Mapping related to ALM1 group

Table 181 Alarm Mapping related to ALM1 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[0]	cpu_pfi_pfrwb_1	Safety Mechanism: Lockstep CPU Alarm: CPU1 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL1 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM1[1]	cpu_pfi_pfrwb_1	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU1 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse

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Table 181 Alarm Mapping related to ALM1 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[2]	cpu_pfi_pfrwb_1	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU1 PFLASH1 Read Path Error Alarm Type: Pulse Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT1 bitfield in SCU_LCLTEST Register.
ALM1[3]	Reserved	Reserved
ALM1[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM1[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM1[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM1[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM1[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM1[9]	Page 23	Safety Mechanism: SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM1[10]	Page 23	Safety Mechanism: SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM1[11]	Page 23	Safety Mechanism(s): SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM1[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Single bit error correction Alarm Type: Level
ALM1[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM1[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM1[21:15]	Reserved	Reserved

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Table 181 Alarm Mapping related to ALM1 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[22]	cpu_pfi_pfrwb_1	Safety Mechanism: SRI End-to-End EDC Alarm: CPU1 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM1[23]	cpu_pfi_pfrwb_1	Safety Mechanism: SRI End-to-End EDC Alarm: CPU1 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM1[24]	cpu_pfi_pfrwb_1	Safety Mechanism: Exception Monitor Alarm: CPU1 exception (interrupt/trap) Alarm Type: Pulse
ALM1[31:25]	Reserved	Reserved

Alarm Mapping related to ALM2 group

Table 182 Alarm Mapping related to ALM2 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM2[0]	Reserved	Reserved
ALM2[1]	Reserved	Reserved
ALM2[2]	Reserved	Reserved
ALM2[3]	Reserved	Reserved
ALM2[14:4]	Reserved	Reserved
ALM2[21:15]	Reserved	Reserved
ALM2[24:22]	Reserved	Reserved
ALM2[31:25]	Reserved	Reserved

Alarm Mapping related to ALM3 group

Table 183 Alarm Mapping related to ALM3 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM3[0]	Reserved	Reserved
ALM3[1]	Reserved	Reserved
ALM3[2]	Reserved	Reserved
ALM3[3]	Reserved	Reserved
ALM3[14:4]	Reserved	Reserved
ALM3[21:15]	Reserved	Reserved
ALM3[24:22]	Reserved	Reserved
ALM3[31:25]	Reserved	Reserved

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Alarm Mapping related to ALM4 group

Table 184 Alarm Mapping related to ALM4 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM4[2:0]	Reserved	Reserved
ALM4[3]	Reserved	Reserved
ALM4[14:4]	Reserved	Reserved
ALM4[21:15]	Reserved	Reserved
ALM4[24:22]	Reserved	Reserved
ALM4[31:25]	Reserved	Reserved

Alarm Mapping related to ALM5 group

Table 185 Alarm Mapping related to ALM5 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM5[2:0]	Reserved	Reserved
ALM5[3]	Reserved	Reserved
ALM5[14:4]	Reserved	Reserved
ALM5[21:15]	Reserved	Reserved
ALM5[24:22]	Reserved	Reserved
ALM5[31:25]	Reserved	Reserved

Alarm Mapping related to ALM6 group

Table 186 Alarm Mapping related to ALM6 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[0]	MTU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[1]	IOM	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[2]	INT	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[3]	Reserved	Reserved
ALM6[4]	SCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[5]	PMS	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level

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Table 186 Alarm Mapping related to ALM6 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[6]	DMA	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[7]	SMU_CORE	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[8]	CCU	Safety Mechanism: Safety Flip-flop Alarm: SYS_PLL.PER_PLL - Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[9]	Reserved	Reserved
ALM6[10]	Page 24	Safety Mechanism: SRAM Monitor Alarm: GTM Single bit error correction Alarm Type: Level
ALM6[11]	Page 24	Safety Mechanism: SRAM Monitor Alarm: GTM Uncorrectable critical error detection Alarm Type: Level
ALM6[12]	Page 24	Safety Mechanism: SRAM Monitor Alarm: GTM Miscellaneous error detection Alarm Type: Level
ALM6[13]	Page 24	Safety Mechanism: SRAM Monitor Alarm: ERAY Single bit error correction Alarm Type: Level
ALM6[14]	Page 24	Safety Mechanism: SRAM Monitor Alarm: ERAY Uncorrectable critical error detection Alarm Type: Level
ALM6[15]	Page 24	Safety Mechanism: SRAM Monitor Alarm: ERAY Miscellaneous error detection Alarm Type: Level
ALM6[16]	Page 24	Safety Mechanism: SRAM Monitor Alarm: CAN Single bit error correction Alarm Type: Level
ALM6[17]	Page 24	Safety Mechanism: SRAM Monitor Alarm: CAN Uncorrectable critical error detection Alarm Type: Level
ALM6[18]	Page 24	Safety Mechanism: SRAM Monitor Alarm: CAN Miscellaneous error detection Alarm Type: Level
ALM6[19]	Page 23	Safety Mechanism: SRAM Monitor Alarm: MISC Single bit error correction Alarm Type: Level
ALM6[20]	Page 23	Safety Mechanism: SRAM Monitor Alarm: MISC Uncorrectable critical error detection Alarm Type: Level

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Table 186 Alarm Mapping related to ALM6 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[21]	Page 23	Safety Mechanism: SRAM Monitor Alarm: MISC Miscellaneous error detection Alarm Type: Level
ALM6[22]	Reserved	Reserved
ALM6[23]	CBS	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[24]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop correctable error detected Alarm Type: Level
ALM6[25]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[31:26]	Reserved	Reserved

Alarm Mapping related to ALM7 group

Table 187 Alarm Mapping related to ALM7 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM7[0]	Page 23	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Single bit error correction Alarm Type: Level
ALM7[1]	Page 23	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Uncorrectable critical error detection Alarm Type: Level
ALM7[2]	Page 23	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Miscellaneous error detection Alarm Type: Level
ALM7[8:3]	Reserved	Reserved
ALM7[11:9]	Reserved	Reserved
ALM7[16:12]	Reserved	Reserved
ALM7[17]	SRI	Safety Mechanism: Built-in SRI Error Detection Alarm: XBAR0 Bus Error Event Alarm Type: Pulse
ALM7[18]	Reserved	Reserved
ALM7[19]	Reserved	Reserved
ALM7[20]	SBCU	Safety Mechanism: Built-in SPB Error Detection Alarm: SPB Bus Error Event Alarm Type: Pulse
ALM7[21]	Reserved	Reserved
ALM7[22]	FSI	Safety Mechanism: PFlash ECC Alarm: PFlash Single Bit Error Alarm Type: Level

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Table 187 Alarm Mapping related to ALM7 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM7[23]	FSI	Safety Mechanism: PFlash ECC Alarm: PFlash Double Bit Error Alarm Type: Level
ALM7[24]	FSI	Safety Mechanism: PFlash ECC Alarm: Single Bit Correction Tracking Buffer Full Alarm Type: Level
ALM7[25]	FSI	Safety Mechanism: PFlash ECC Alarm: Double Bit Correction Tracking Buffer Full Alarm Type: Level
ALM7[26]	FSI	Safety Mechanism: PFlash ECC Alarm: Multiple Bit Error Detection Tracking Buffer Full Alarm Type: Level
ALM7[27]	FSI	Safety Mechanism: PFlash ECC Alarm: Zero Bit Error Tracking Buffer Full Alarm Type: Level
ALM7[28]	FSI	Safety Mechanism: PFlash ECC Monitor Alarm: PFlash ECC Error Alarm Type: Level
ALM7[29]	FSI	Safety Mechanism: PFlash EDC Monitor Alarm: PFlash EDC Error Alarm Type: Level
ALM7[30]	FSI	Safety Mechanism: PFlash Configuration Monitor Alarm: CPU FLASHCON Configuration Error Alarm Type: Level
ALM7[31]	FSI	Safety Mechanism: PFlash Configuration Monitor Alarm: Flash Stored Configuration Error Alarm Type: Level

Alarm Mapping related to ALM8 group**Table 188 Alarm Mapping related to ALM8 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM8[0]	SCU	Safety Mechanism: Clock Monitor Alarm: OSC clock frequency out of range Alarm Type: Pulse
ALM8[1]	CCU	Safety Mechanism: Clock Monitor Alarm: Back-up clock out-of-range alarm Alarm Type: Level
ALM8[2]	CCU	Safety Mechanism: Clock Alive Monitor Alarm: Back-up clock alive alarm Alarm Type: Level
ALM8[3]	SCU	Safety Mechanism: PLL loss of lock detection Alarm: System PLL DCO loss of lock event Alarm Type: Pulse

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Table 188 Alarm Mapping related to ALM8 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM8[4]	SCU	Safety Mechanism: PLL loss of lock detection Alarm: Peripheral PLL DCO loss of lock event Alarm Type: Pulse
ALM8[5]	SCU	Safety Mechanism: LBIST Safe Reset State Alarm: LBIST Alarm Alarm Type: Level
ALM8[6]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 0 Alarm Type: Pulse
ALM8[7]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 1 Alarm Type: Pulse
ALM8[8]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 2 Alarm Type: Pulse
ALM8[9]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 3 Alarm Type: Pulse
ALM8[10]	SCU	Safety Mechanism: Watchdog Alarm: CPU0 Watchdog Time-out Alarm Type: Pulse
ALM8[11]	SCU	Safety Mechanism: Watchdog Alarm: CPU1 Watchdog Time-out Alarm Type: Pulse
ALM8[12]	Reserved	Reserved
ALM8[13]	Reserved	Reserved
ALM8[15:14]	Reserved	Reserved
ALM8[16]	SCU	Safety Mechanism: Watchdog Alarm: Safety Watchdog Time-out Alarm Type: Pulse
ALM8[17]	SCU	Safety Mechanism: All Watchdogs Alarm: Watchdog Time-out. This alarm is a logical OR over all watchdog time-out alarms Alarm Type: Pulse
ALM8[18]	SCU	Safety Mechanism: Lockstep Dual Rail Monitor Alarm: Dual Rail Error Alarm Type: Pulse
ALM8[19]	SCU	Safety Mechanism: Emergency Stop Alarm: External Emergency Stop Signal Event Alarm Type: Pulse

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Table 188 Alarm Mapping related to ALM8 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM8[20]	SCU	Safety Mechanism: Pad Monitor Alarm: Pad Heating Alarm Alarm Type: Pulse Note: This alarm is triggered by the pad-heating enable signal of all core supply-pads. It will also be triggered by the enable signal for initialisation of security sensitive RAMs and TCU test enable signals
ALM8[21]	SCU	Safety Mechanism: LBIST Test Mode Alarm: LBIST Test Mode Alarm Alarm Type: Level Note: This alarm is also set if TCU related signals are activated in the SCU causing it to fail
ALM8[22]	INT	Safety Mechanism: Interrupt Monitor Alarm: EDC Configuration and Data Path Error Alarm Type: Pulse
ALM8[23]	DMA	Safety Mechanism: DMA SRI ECC Alarm: DMA SRI ECC Error Alarm Type: Pulse
ALM8[24]	Reserved	Reserved
ALM8[25]	IOM	Safety Mechanism: External Alarm Alarm: Pin Mismatch Indication Alarm Type: Level
ALM8[26]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 4 Alarm Type: Pulse
ALM8[27]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 5 Alarm Type: Pulse
ALM8[28]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 6 Alarm Type: Pulse
ALM8[29]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 7 Alarm Type: Pulse
ALM8[30]	SCU	Safety Mechanism: Core Domain Die Temperature Sensor Alarm: Under Temperature Alarm Alarm Type: Level
ALM8[31]	SCU	Safety Mechanism: Core Domain Die Temperature Sensor Alarm: Over Temperature Alarm Alarm Type: Level

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Alarm Mapping related to ALM9 group

Table 189 Alarm Mapping related to ALM9 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM9[0]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature Overflow Alarm Type: Level
ALM9[1]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature Underflow Alarm Type: Level
ALM9[2]	Reserved	Reserved
ALM9[3]	Page 25	Safety Mechanism: Voltage Monitor Alarm: Over-voltage Alarm Alarm Type: Level
ALM9[4]	Reserved	Reserved
ALM9[5]	Page 26	Safety Mechanism: Voltage Monitor Alarm: Under-voltage Alarm Alarm Type: Level
ALM9[14:6]	Reserved	Reserved
ALM9[15]	Page 26	Safety Mechanism: Voltage Monitor Alarm: Short to Low/High Alarm Alarm Type: Level
ALM9[16]	Page 25	Safety Mechanism: Voltage Monitor Alarm: Over-voltage Alarm Alarm Type: Level
ALM9[17]	Page 25	Safety Mechanism: Voltage Monitor Alarm: Under-voltage Alarm Alarm Type: Level
ALM9[19:18]	Reserved	Reserved
ALM9[21:20]	Reserved	Reserved
ALM9[22]	Reserved	Reserved
ALM9[23]	Reserved	Reserved
ALM9[26:24]	Reserved	Reserved
ALM9[27]	Reserved	Reserved
ALM9[28]	Reserved	Reserved
ALM9[29]	Reserved	Reserved
ALM9[30]	Reserved	Reserved
ALM9[31]	Reserved	Reserved

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Alarm Mapping related to ALM10 group

Table 190 Alarm Mapping related to ALM10 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM10[0]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 0 Alarm Type: Pulse
ALM10[1]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 1 Alarm Type: Pulse
ALM10[2]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 2 Alarm Type: Pulse
ALM10[3]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 3 Alarm Type: Pulse
ALM10[4]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 4 Alarm Type: Pulse
ALM10[5]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 5 Alarm Type: Pulse
ALM10[6]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 6 Alarm Type: Pulse
ALM10[7]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 7 Alarm Type: Pulse
ALM10[8]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 8 Alarm Type: Pulse
ALM10[9]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 9 Alarm Type: Pulse
ALM10[10]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 10 Alarm Type: Pulse
ALM10[11]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 11 Alarm Type: Pulse
ALM10[12]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 12 Alarm Type: Pulse
ALM10[13]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 13 Alarm Type: Pulse

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Table 190 Alarm Mapping related to ALM10 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM10[14]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 14 Alarm Type: Pulse
ALM10[15]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 15 Alarm Type: Pulse
ALM10[16]	SMU_CORE	Safety Mechanism: Recovery Timer 0 Alarm: Timer Time-out Alarm Type: Pulse
ALM10[17]	SMU_CORE	Safety Mechanism: Recovery Timer 1 Alarm: Timer Time-out Alarm Type: Pulse
ALM10[18]	FSP	Safety Mechanism: ErrorPin Alarm: ErrorPin Fault State Activation Alarm Type: Pulse
ALM10[19]	Reserved	Reserved
ALM10[20]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop correctable error detected Alarm Type: Level
ALM10[21]	Page 25	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM10[22]	Page 25	Safety Mechanism: Access Enable Protection Alarm: Access Enable error Alarm Type: Pulse
ALM10[31:23]	Reserved	Reserved

Alarm Mapping related to ALM11 group

Table 191 Alarm Mapping related to ALM11 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM11[1:0]	Reserved	Reserved
ALM11[2]	SRI	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[3]	SRI	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[4]	DMU	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse

Safety Management Unit (SMU)

Table 191 Alarm Mapping related to ALM11 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM11[5]	DMU	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[7:6]	Reserved	Reserved
ALM11[8]	Reserved	Reserved
ALM11[9]	SFIBRIDGE1	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Read Phase Error Alarm Type: Pulse
ALM11[10]	HSSL0	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: HSSL0 EDC Read Phase Error Alarm Type: Pulse
ALM11[11]	Reserved	Reserved
ALM11[12]	converter_0	Safety Mechanism: Converter Alarm: Phase Synchronizer Error Alarm Type: Level
ALM11[13]	SRI	Safety Mechanism: SRI SOTA Monitor Alarm: SOTA Swap Error Alarm Type: Pulse
ALM11[31:14]	Reserved	Reserved

Alarm Mapping related to ALM20 group

Table 192 Alarm Mapping related to ALM20 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM20[3:0]	Reserved	Reserved
ALM20[4]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDD Over-voltage Alarm Alarm Type: Level
ALM20[5]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDPD Over-voltage Alarm Alarm Type: Level
ALM20[6]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Over-voltage Alarm Alarm Type: Level
ALM20[7]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDM Over-voltage Alarm Alarm Type: Level
ALM20[8]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEXT Over-voltage Alarm Alarm Type: Level
ALM20[9]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEVR SB Over-voltage Alarm Alarm Type: Level

Safety Management Unit (SMU)
Table 192 Alarm Mapping related to ALM20 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM20[10]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDD Under-voltage Alarm Alarm Type: Level
ALM20[11]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDPD Under-voltage Alarm Alarm Type: Level
ALM20[12]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Under-voltage Alarm Alarm Type: Level
ALM20[13]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDM Under-voltage Alarm Alarm Type: Level
ALM20[14]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEXT Under-voltage Alarm Alarm Type: Level
ALM20[15]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEVRSB Under-voltage Alarm Alarm Type: Level
ALM20[31:16]	Reserved	Reserved

Alarm Mapping related to ALM21 group**Table 193 Alarm Mapping related to ALM21 group**

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM21[0]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDD Under-voltage Alarm Alarm Type: Level
ALM21[1]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Under-voltage Alarm Alarm Type: Level
ALM21[2]	hsm	Safety Mechanism: Voltage Monitor Alarm: VEXT Under-voltage Alarm Alarm Type: Level
ALM21[3]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDD Over-voltage Alarm Alarm Type: Level
ALM21[4]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDDP3 over-voltage Alarm Alarm Type: Level
ALM21[5]	hsm	Safety Mechanism: Voltage Monitor Alarm: VEXT over-voltage Alarm Alarm Type: Level
ALM21[6]	Reserved	Reserved

Safety Management Unit (SMU)

Table 193 Alarm Mapping related to ALM21 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM21[7]	Page 25	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM21[8]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature underflow Alarm Type: Level
ALM21[9]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature overflow Alarm Type: Level
ALM21[10]	PMS	Safety Mechanism: Register Access Protection Alarm: Access Protection violation Alarm Type: Pulse
ALM21[11]	PMS	Safety Mechanism: Voltage Monitor Alarm: EVRC Short to Low Alarm Alarm Type: Level
ALM21[12]	PMS	Safety Mechanism: Voltage Monitor Alarm: EVRC Short to High Alarm Alarm Type: Level
ALM21[13]	PMS	Safety Mechanism: Voltage Monitor Alarm: EV33 Short to Low Alarm Alarm Type: Level
ALM21[14]	PMS	Safety Mechanism: Voltage Monitor Alarm: EV33 Short to High Alarm Alarm Type: Level
ALM21[15]	CCU	Safety Mechanism: Clock Alive Monitor Alarm: PLLx/fSPB Alive Alarm (provided on fBACK clock with x = 0..2) Alarm Type: Level Note: This alarm is also set if TCU related signals are activated in the CCU causing the clocks to fail
ALM21[16]	SMU_CORE	Safety Mechanism: SMU_core Alive Monitor Alarm: SMU_core Alive Alarm Alarm Type: Pulse
ALM21[31:17]	Reserved	Reserved

15.5 Connectivity

Table 194 Connections of SMU

Interface Signals	connects		Description
SMU:FSP(0)	to	P33.8:HWOUT(0)	FSP[1..0] Output Signals - Generated by SMU_core
SMU:FSP(1)	to	P33.10:HWOUT(0)	FSP[1..0] Output Signals - Generated by SMU_core

Safety Management Unit (SMU)

Table 194 Connections of SMU (cont'd)

Interface Signals	connects		Description
SMU:FSP_STS(0)	from	P33.8:IN	FSP Status Input - Shows the actual state of the FSP ErroPin
SMU:FSP_STS(1)	from	P33.10:IN	FSP Status Input - Shows the actual state of the FSP ErroPin
SMU:RUNSTATE	to	SCU:smu_wdt_run	SMU_core RUN state indication
SMU:INT(2:0)	to	INT:smu.INT(2:0)	SMU Service Request

15.6 Revision History

Table 195 Revision History

Reference	Change to Previous Version	Comment
V4.0.17		
Page 25	Updated PMS Pre-Alarm Mapping table	
V4.0.18		
Page 41	Updated description of ALM21[0] and ALM21[3]	
Page 41	Added description for ALM21[6]	
Page 34	Updated description for ALM8[20]	
Page 39	Updated description for ALM11[8]	
Page 17	Added bit [10] to SMU_AG11***	
Page 1	Missing blank fixed	
V4.0.19		
Page 23 , Page 33	Added FSI_RAM Alarms ALM7[0:2] which were not documented in the previous version	
Page 27	Added Alarm Types in Alarm Mapping Tables	
Page 43	Revision History updated	
V4.0.20		
Page 37	Updated grouping in ALM9 group, no functional change.	
V4.0.21		
-	No functional changes.	
V4.0.22		
Page 28	Updated description of ALM1[0] and ALM1[2]	
Page 33 , Page 39 , Page 6 , Page 9	Remove ALM7[12:16] and ALM11[0:1] as they don't exist in the device	
V4.0.23		
Page 31	Updated description of ALM6[8]	
Page 23	Added CPU0.DMEM1 Alarms ALM0[9:11] and CPU1.DMEM1 Alarms ALM1[9:11] which were not documented in the previous version	

Interrupt Router (IR)

16 Interrupt Router (IR)

This chapter supplements the family documentation with device specific information for TC36x.

The Interrupt Router allocates two address ranges

- Interrupt Router System and OTGM register address range: 2 * 256 byte address range covering the Interrupt Router system registers, ICU control registers and OTGM registers ([Chapter 16.2](#))
- SRC register address range: 8 KByte address range covering the Service Request Control registers ([Chapter 16.4](#))

16.1 TC36x Specific Interrupt Router Configuration

Table 196 TC36x specific configuration of INT

Parameter	INT
Number of Interrupt Service Providers	3
Number of SRB groups	2

Table 197 TC36x specific configuration of SRC

Parameter	SRC
Number of Service Request Nodes	1024

Interrupt Router (IR)

16.2 TC36x Specific Control Registers

This chapter describes the TC36x specific Interrupt Router system, OTGM and ICU registers

List of used Access Protection Register abbreviations

- P0 -> ACCEN_SRBx, write protection of the related SRBx register. Number of Service Request Broadcast registers (SRB) and the related ACCEN_SRB registers is equal to the number of implemented TriCore CPUs.
- P1 -> ACCEN_CONFIG, write protection of all SRCx[15:0] and ICUx Error Capture registers (ECRx)
- P2 -> ACCEN_SRC_TOSx, write protects bits [31:16] of all SRCs that are mapped to TOSx (SCR.TOS=x). For each implemented Interrupt Control Unit, one ACCEN_SRC_TOSx register is implemented.

Note: A violation of the access protection will not be executed (e.g. a write to a 'Px'/ACCEN protected register by an SPB access with a disabled Master TAG-ID). In this case an access protection error is signaled to the SMU. Beside this signaling to the SMU, no other error, interrupt or trap is generated.

Interrupt Router Module Registers

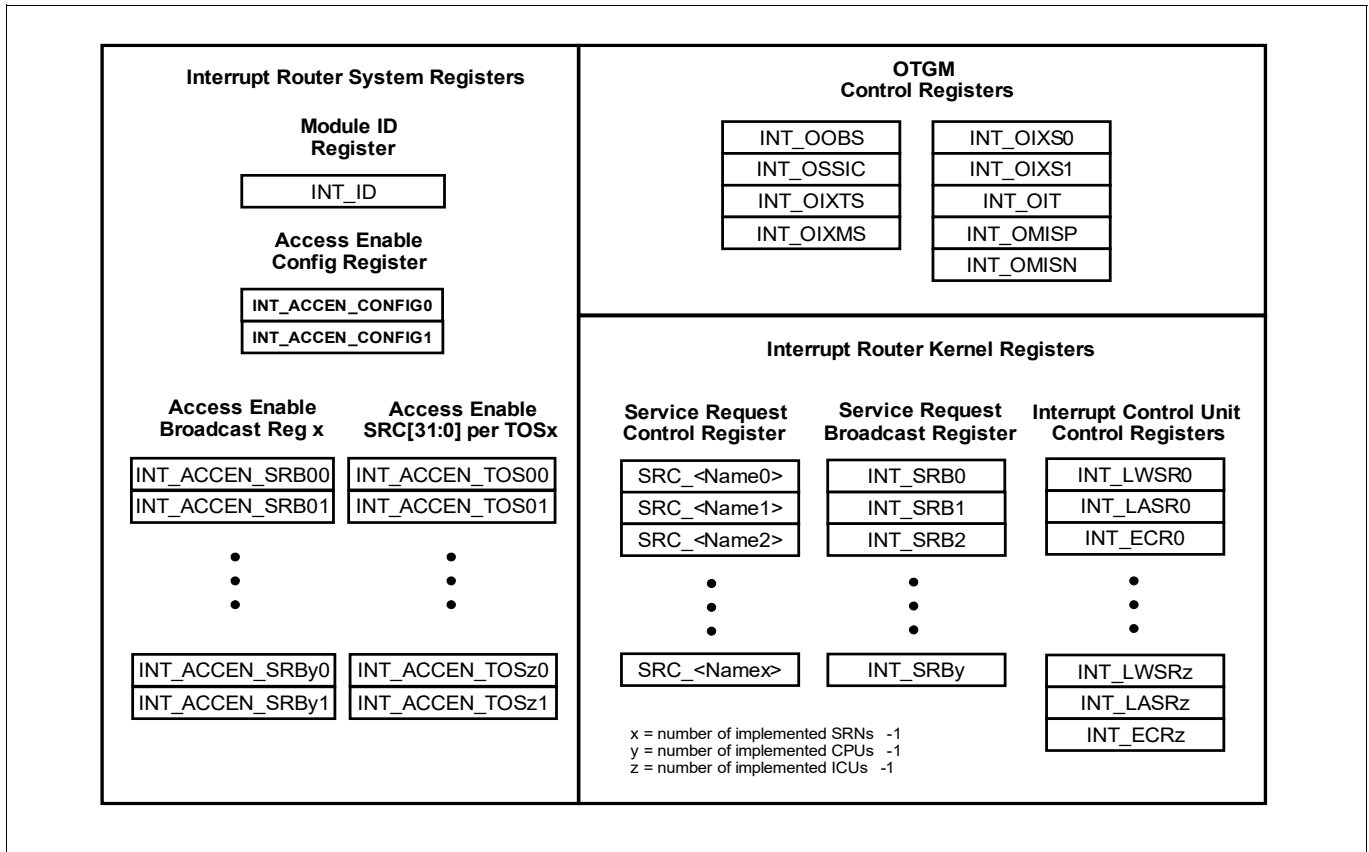


Figure 4 Interrupt Router module registers (SRC registers are described in [Chapter 16.4](#))

Table 198 Register Address Space - INT

Module	Base Address	End Address	Note
INT	F0037000 _H	F0037FFF _H	IR Status and Control Registers

Interrupt Router (IR)

Table 199 Register Overview - INT (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
INT_ID	Module Identification Register	0008 _H	U,SV	nBE	Application Reset	See Family Spec
INT_SRBx (x=0-1)	Service Request Broadcast Register x	0010 _H +x *4	U,SV	SV,P0	Application Reset	See Family Spec
INT_OOBS	OTGM OTGB0/1 Status	0080 _H	U,SV	nBE	Application Reset	See Family Spec
INT_OSSIC	OTGM SSI Control	0084 _H	U,SV	SV	Application Reset	See Family Spec
INT_OIXTS	OTGM IRQ MUX Trigger Set Select	0088 _H	U,SV	SV	Application Reset	See Family Spec
INT_OIXMS	OTGM IRQ MUX Missed IRQ Select	008C _H	U,SV	SV	Application Reset	See Family Spec
INT_OIXS0	OTGM IRQ MUX Select 0	0090 _H	U,SV	SV	Application Reset	See Family Spec
INT_OIXS1	OTGM IRQ MUX Select 1	0094 _H	U,SV	SV	Application Reset	See Family Spec
INT_OIT	OTGM IRQ Trace	00A0 _H	U,SV	SV	Application Reset	5
INT_OMISP	OTGM MCDS I/F Sensitivity Posedge	00A4 _H	U,SV	SV	Application Reset	See Family Spec
INT_OMISN	OTGM MCDS I/F Sensitivity Negedge	00A8 _H	U,SV	SV	Application Reset	See Family Spec
INT_ACCEN_CON FIG0	Access Enable covering all INT_ECRx and all SRCy[15:0], Register 0	00F0 _H	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_CON FIG1	Access Enable covering all INT_ECRx and all SRCy[15:0], Register 1	00F4 _H	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRB x0 (x=0-1)	Access Enable covering SRBx, Register 0	0100 _H +x *8	U,SV	SV,SE	Application Reset	See Family Spec

Interrupt Router (IR)

Table 199 Register Overview - INT (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
INT_ACCEN_SRB x1 (x=0-1)	Access Enable covering SRBx, Register 1	0104 _H +x *8	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRC _TOSx0 (x=0-2)	Access Enable covering all SRCx[31:16] mapped to ICUx, Register 0	0180 _H +x *8	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRC _TOSx1 (x=0-2)	Access Enable covering all SRCx[31:16] mapped to ICUx, Register 1	0184 _H +x *8	U,SV	SV,SE	Application Reset	See Family Spec
INT_LWSRx (x=0-2)	Latest Winning Service Request Register x, related to ICUx	0200 _H +x *10 _H	U,SV	nBE	Application Reset	See Family Spec
INT_LASRx (x=0-2)	Last Acknowledged Service Request Register x, related to ICUx	0204 _H +x *10 _H	U,SV	nBE	Application Reset	See Family Spec
INT_ECRx (x=0-2)	Error Capture Register x, related to ICUx	0208 _H +x *10 _H	U,SV	SV,P1	Application Reset	See Family Spec

Interrupt Router (IR)

16.3 TC36x Specific Registers

16.3.1 IR Status and Control Registers

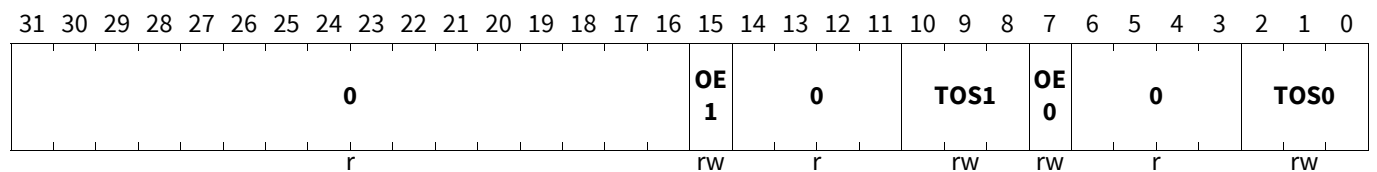
OTGM IRQ Trace

INT_OIT

OTGM IRQ Trace

(00A0_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
TOS0	2:0	rw	Type of Service for Observation on OTGB0 Trigger Set TS16_SP Family concept encoding, compatible with SRC.TOS 000 _B CPU0 service is observed 001 _B DMA service is observed 010 _B CPU1 service is observed others , Reserved (no action)
OE0	7	rw	Output Enable for OTGB0 0 _B Disabled 1 _B Enabled
TOS1	10:8	rw	Type of Service for Observation on OTGB1 Trigger Set TS16_SP Family concept encoding, compatible with SRC.TOS 000 _B CPU0 service is observed 001 _B DMA service is observed 010 _B CPU1 service is observed others , Reserved (no action)
OE1	15	rw	Output Enable for OTGB1 0 _B Disabled 1 _B Enabled
0	6:3, 14:11, 31:16	r	Reserved Read as 0; must be written with 0.

Interrupt Router (IR)

16.4 TC36x Specific Service Request Control (SRC) registers

This chapter describes the TC36x Service Request Control (SRC) registers.

Table 201 shows all registers associated with the Interrupt Router module in the device. This chapter describes the Service Request Control registers including:

- Mapping of Aurix module interrupt triggers to SRC
- SRC offsets
- The index number of an SRC can be calculated with the SRC Offset: $\text{Index}(\text{SRC}) = \langle \text{SRC Address Offset} \rangle / 4$

List of used Access Protection Register abbreviations

- P0 -> ACCEN_SRBx, write protection of the related SRBx register. Number of Service Request Broadcast registers (SRB) and the related ACCEN_SRB registers is equal to the number of implemented TriCore CPUs.
- P1 -> ACCEN_CONFIG, write protection of all SRCx[15:0] and ICUx Error Capture registers (ECRx)
- P2 -> ACCEN_SRC_TOSx, write protects bits [31:16] of all SRCs that are mapped to TOSx (SCR.TOS=x). For each implemented Interrupt Control Unit, one ACCEN_SRC_TOSx register is implemented.

Note: A violation of the access protection will not be executed (e.g. a write to a 'Px'/ACCEN protected register from a disabled master). In this case an access protection error is signaled to the SMU. Beside this signaling to the SMU, no other error, interrupt or trap is generated.

Table 200 Register Address Space - SRC

Module	Base Address	End Address	Note
SRC	F0038000 _H	F0039FFF _H	IR Service Request Control Registers (SRC)

Table 201 Register Overview - SRC (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_CPUxSB (x=0-1)	CPUx Software Breakpoint Service Request	00000 _H + x*4	U,SV	SV,P1,P2	Debug Reset	11
SRC_BCUSPB	SBCU Service Request (SPB Bus Control Unit)	00020 _H	U,SV	SV,P1,P2	Debug Reset	11
SRC_XBAR0	SRI Domain 0 Service Request	00030 _H	U,SV	SV,P1,P2	Debug Reset	11
SRC_CERBERUSy (y=0-1)	Cerberus Service Request y	00040 _H + y*4	U,SV	SV,P1,P2	Debug Reset	11
SRC_ASCLINxTX (x=0-11)	ASCLINx Transmit Service Request	00050 _H + x*12	U,SV	SV,P1,P2	Application Reset	11
SRC_ASCLINxRX (x=0-11)	ASCLINx Receive Service Request	00054 _H + x*12	U,SV	SV,P1,P2	Application Reset	11
SRC_ASCLINxER R (x=0-11)	ASCLINx Error Service Request	00058 _H + x*12	U,SV	SV,P1,P2	Application Reset	11
SRC_MTUDONE	MTU Done Service Request	000EC _H	U,SV	SV,P1,P2	Application Reset	11

Interrupt Router (IR)

Table 201 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_QSPIxTX (x=0-3)	QSPIx Transmit Service Request	000F0 _H + x*14 _H	U,SV	SV,P1,P2	Application Reset	11
SRC_QSPIxRX (x=0-3)	QSPIx Receive Service Request	000F4 _H + x*14 _H	U,SV	SV,P1,P2	Application Reset	11
SRC_QSPIxERR (x=0-3)	QSPIx Error Service Request	000F8 _H + x*14 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_QSPIxPT (x=0-3)	QSPIx Phase Transition Service Request	000FC _H + x*14 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_QSPIxU (x=0-3)	QSPIx User Defined Service Request	00100 _H + x*14 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_HSCTx (x=0)	HSCT0 Service Request	00180 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_HSSLxCOky (x=0;y=0-3)	HSSL0 Channel y OK Service Request	00190 _H + y*10 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_HSSLxRDly (x=0;y=0-3)	HSSL0 Channel y Read Data Service Request	00194 _H + y*10 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_HSSLxERRy (x=0;y=0-3)	HSSL0 Channel y Error Service Request	00198 _H + y*10 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_HSSLxTRGy (x=0;y=0-3)	HSSL0 Channel y Trigger Interrupt Service Request	0019C _H + y*10 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_HSSLxEXI (x=0)	HSSLx Exception Service Request	001D0 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_I2CxDTR (x=0)	I2Cx Data Transfer Request	00220 _H	U,SV	SV,P1,P2	Application Reset	14
SRC_I2CxERR (x=0)	I2Cx Error Service Request	00224 _H	U,SV	SV,P1,P2	Application Reset	16
SRC_I2CxP (x=0)	I2Cx Protocol Service Request	00228 _H	U,SV	SV,P1,P2	Application Reset	16
SRC_SENTx (x=0-9)	SENT TRIGx Service Request	00240 _H + x*4	U,SV	SV,P1,P2	Application Reset	16
SRC_MSCxSRy (x=0;y=0-4)	MSCx Service Request y	00270 _H + y*4	U,SV	SV,P1,P2	Application Reset	16
SRC_CCUXxSRy (x=0-1;y=0-3)	CCUXx Service Request y	002C0 _H + x*10 _H +y* 4	U,SV	SV,P1,P2	Application Reset	16
SRC_GPT120CIR Q	GPT120 CAPREL Service Request	002E0 _H	U,SV	SV,P1,P2	Application Reset	16
SRC_GPT120T2	GPT120 Timer 2 Service Request	002E4 _H	U,SV	SV,P1,P2	Application Reset	16
SRC_GPT120T3	GPT120 Timer 3 Service Request	002E8 _H	U,SV	SV,P1,P2	Application Reset	16

Interrupt Router (IR)

Table 201 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_GPT120T4	GPT120 Timer 4 Service Request	002EC _H	U,SV	SV,P1,P2	Application Reset	16
SRC_GPT120T5	GPT120 Timer 5 Service Request	002F0 _H	U,SV	SV,P1,P2	Application Reset	16
SRC_GPT120T6	GPT120 Timer 6 Service Request	002F4 _H	U,SV	SV,P1,P2	Application Reset	19
SRC_STMxSRy (x=0-1;y=0-1)	System Timer x Service Request y	00300 _H + x*8+y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_FCE0	FCE0 Error Service Request	00330 _H	U,SV	SV,P1,P2	Application Reset	19
SRC_DMAERRY (y=0-3)	DMA Error Service Request y	00340 _H + y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_DMACHy (y=0-63)	DMA Channel y Service Request	00370 _H + y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_GETHy (y=0-9)	GETH Service Request y	00580 _H + y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_CANxINTy (x=0-1;y=0-15)	CANx Service Request y	005B0 _H + x*40 _H +y* 4	U,SV	SV,P1,P2	Application Reset	19
SRC_VADCGxSRy (x=0-3;y=0-3)	EVADC Group x Service Request y	00670 _H + x*10 _H +y* 4	U,SV	SV,P1,P2	Application Reset	19
SRC_VADCG8SRy (y=0-3)	EVADC Group 8 Service Request y	006F0 _H + y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_VADCG9SRy (y=0-3)	EVADC Group 9 Service Request y	00700 _H + y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_VADCFcxSR 0 (x=0-1)	EVADC Fast Compare x Service Request SR0	00730 _H + x*4	U,SV	SV,P1,P2	Application Reset	21
SRC_VADCCGxSR y (x=0-1;y=0-3)	EVADC Common Group x Service Request y	00750 _H + x*10 _H +y* 4	U,SV	SV,P1,P2	Application Reset	21
SRC_DSADCSRM x (x=0-3)	DSADC SRMx Service Request	00770 _H + x*8	U,SV	SV,P1,P2	Application Reset	21
SRC_DSADCSRAx (x=0-3)	DSADC SRAx Service Request	00774 _H + x*8	U,SV	SV,P1,P2	Application Reset	21
SRC_ERAYxINT0 (x=0)	E-RAY x Service Request 0	00800 _H	U,SV	SV,P1,P2	Application Reset	21
SRC_ERAYxINT1 (x=0)	E-RAY x Service Request 1	00804 _H	U,SV	SV,P1,P2	Application Reset	21

Interrupt Router (IR)

Table 201 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_ERAYxTINT0 (x=0)	E-RAY x Timer Interrupt 0 Service Request	00808 _H	U,SV	SV,P1,P2	Application Reset	21
SRC_ERAYxTINT1 (x=0)	E-RAY x Timer Interrupt 1 Service Request	0080C _H	U,SV	SV,P1,P2	Application Reset	21
SRC_ERAYxNDAT 0 (x=0)	E-RAY x New Data 0 Service Request	00810 _H	U,SV	SV,P1,P2	Application Reset	21
SRC_ERAYxNDAT 1 (x=0)	E-RAY x New Data 1 Service Request	00814 _H	U,SV	SV,P1,P2	Application Reset	21
SRC_ERAYxMBSC 0 (x=0)	E-RAY x Message Buffer Status Changed 0 Service Request	00818 _H	U,SV	SV,P1,P2	Application Reset	24
SRC_ERAYxMBSC 1 (x=0)	E-RAY x Message Buffer Status Changed 1 Service Request	0081C _H	U,SV	SV,P1,P2	Application Reset	24
SRC_ERAYxOBUS Y (x=0)	E-RAY x Output Buffer Busy	00820 _H	U,SV	SV,P1,P2	Application Reset	24
SRC_ERAYxIBUSY (x=0)	E-RAY x Input Buffer Busy	00824 _H	U,SV	SV,P1,P2	Application Reset	24
SRC_DMUHOST	DMU Host Service Request	00860 _H	U,SV	SV,P1,P2	Application Reset	24
SRC_DMUFSI	DMU FSI Service Request	00864 _H	U,SV	SV,P1,P2	Application Reset	24
SRC_HSM _y (y=0-1)	HSM Service Request y	00870 _H + y*4	U,SV	SV,P1,P2	Application Reset	24
SRC_SCUERU _x (x=0-3)	SCU ERU Service Request x	00880 _H + x*4	U,SV	SV,P1,P2	Application Reset	24
SRC_PMSDTS	PMS DTS Service Request	008AC _H	U,SV	SV,P1,P2	Application Reset	24
SRC_PMS _x (x=0-3)	Power Management System Service Request x	008B0 _H + x*4	U,SV	SV,P1,P2	Application Reset	24
SRC_SCR	Stand By Controller Service Request	008C0 _H	U,SV	SV,P1,P2	Application Reset	26
SRC_SMU _y (y=0-2)	SMU Service Request y	008D0 _H + y*4	U,SV	SV,P1,P2	Application Reset	26
SRC_PSI5 _y (y=0-7)	PSI5 Service Request y	008E0 _H + y*4	U,SV	SV,P1,P2	Application Reset	26
SRC_PSI5S _y (y=0-7)	PSI5-S Service Request y	00950 _H + y*4	U,SV	SV,P1,P2	Application Reset	26

Interrupt Router (IR)

Table 201 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_GPSRxy (x=0-1;y=0-7)	General Purpose Group x Service Request y	00990 _H + x*20 _H +y* 4	U,SV	SV,P1,P2	Application Reset	26
SRC_GTMAEIRQ	AEI Shared Service Request	00A70 _H	U,SV	SV,P1,P2	Application Reset	26
SRC_GTMARUIRQ w (w=0-2)	ARU Shared Service Request w	00A74 _H + w*4	U,SV	SV,P1,P2	Application Reset	26
SRC_GTMBRCIRQ	BRC Shared Service Request	00A80 _H	U,SV	SV,P1,P2	Application Reset	26
SRC_GTMCMPIR Q	CMP Shared Service Request	00A84 _H	U,SV	SV,P1,P2	Application Reset	26
SRC_GTMSPEWIR Q (w=0-1)	SPEw Shared Service Request	00A88 _H + w*4	U,SV	SV,P1,P2	Application Reset	26
SRC_GTMPSMwx (w=0;x=0-7)	PSMw Shared Service Request x	00AA0 _H + x*4	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMDPLLw (w=0-26)	DPLL Service Request w	00B00 _H + w*4	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMERR	Error Service Request	00B70 _H	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMTIMwx (w=0-2;x=0-7)	TIMw Shared Service Request x	00B90 _H + w*20 _H +x *4	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMMCSwx (w=0-2;x=0-7)	MCSw Shared Service Request x	00CB0 _H + w*20 _H +x *4	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMTOMwx (w=0-1;x=0-7)	TOMw Shared Service Request x	00E10 _H + w*20 _H +x *4	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMATOMw x (w=0-3;x=0-3)	ATOMw Shared Service Request x	00EF0 _H + w*10 _H +x *4	U,SV	SV,P1,P2	Application Reset	29
SRC_GTMMCSW w (w=0-9)	GTM Multi Channel Sequencer Service Request w	00FD0 _H + w*4	U,SV	SV,P1,P2	Application Reset	29

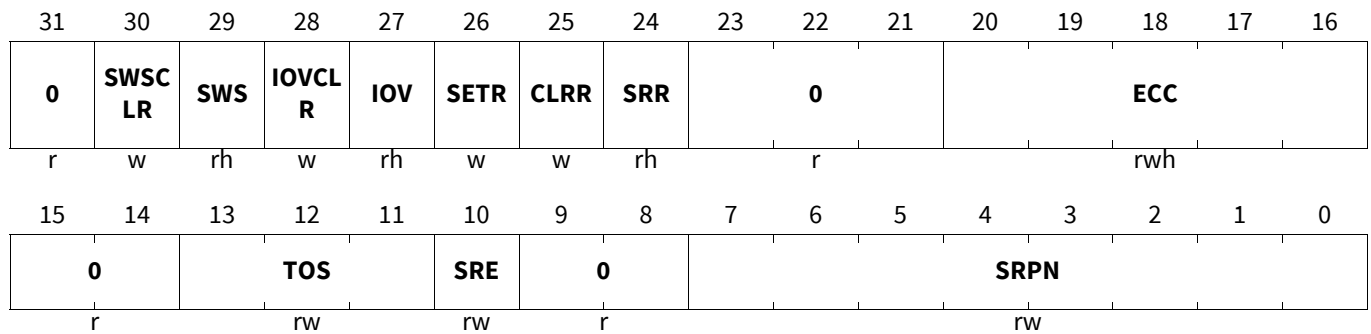
Interrupt Router (IR)

16.5 TC36x Specific Registers

16.5.1 IR Service Request Control Registers (SRC)

CPUx Software Breakpoint Service Request

SRC_CPUxSB (x=0-1)		
CPUx Software Breakpoint Service Request (0000 _H + x*4)		Debug Reset Value: 0000 0000 _H
SRC_BCUSPB		
SBCU Service Request [SPB Bus Control Unit] (00020 _H)		Debug Reset Value: 0000 0000 _H
SRC_XBAR0		
SRI Domain 0 Service Request (00030 _H)		Debug Reset Value: 0000 0000 _H
SRC_CERBERUSy (y=0-1)		
Cerberus Service Request y (00040 _H +y*4)		Debug Reset Value: 0000 0000 _H
SRC_ASCLINxTX (x=0-11)		
ASCLINx Transmit Service Request (00050 _H +x*12)		Application Reset Value: 0000 0000 _H
SRC_ASCLINxRX (x=0-11)		
ASCLINx Receive Service Request (00054 _H +x*12)		Application Reset Value: 0000 0000 _H
SRC_ASCLINxERR (x=0-11)		
ASCLINx Error Service Request (00058 _H +x*12)		Application Reset Value: 0000 0000 _H
SRC_MTUDONE		
MTU Done Service Request (000EC _H)		Application Reset Value: 0000 0000 _H
SRC_QSPIxTX (x=0-3)		
QSPIx Transmit Service Request (000F0 _H +x*14 _H)		Application Reset Value: 0000 0000 _H
SRC_QSPIxRX (x=0-3)		
QSPIx Receive Service Request (000F4 _H +x*14 _H)		Application Reset Value: 0000 0000 _H



Interrupt Router (IR)

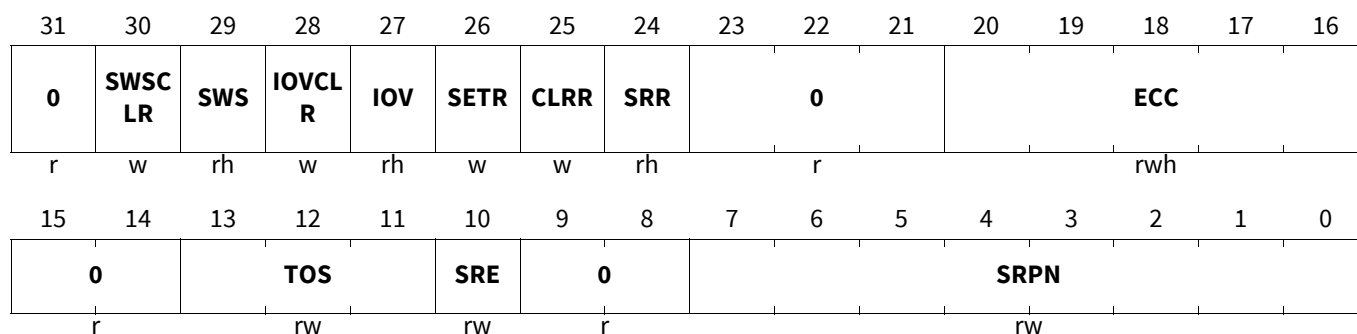
Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>
TOS	13:11	rw	<p>Type of Service Control</p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <p>000_B CPU0 service is initiated</p> <p>001_B DMA service is initiated</p> <p>010_B CPU1 service is initiated</p> <p>Others, Reserved (no action)</p>
ECC	20:16	rwh	<p>Error Correction Code</p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> Write or Read-Modify-Write to SRC[31:0] Write to SRC[15:0] (16-bit write) Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	<p>Service Request Flag</p> <p>The SRR bit shows the status of the Service Request.</p> <p>0_B No service request is pending</p> <p>1_B A service request is pending</p>
CLRR	25	w	<p>Request Clear Bit</p> <p>The CLRR bit is required to reset SRR.</p> <p>0_B No action</p> <p>1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>
SETR	26	w	<p>Request Set Bit</p> <p>The SETR bit is required to set SRR.</p> <p>0_B No action</p> <p>1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>

Interrupt Router (IR)

Field	Bits	Type	Description
IOV	27	rh	<p>Interrupt Trigger Overflow Bit</p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request.</p> <p>0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.</p>
IOVCLR	28	w	<p>Interrupt Trigger Overflow Clear Bit</p> <p>IOVCLR is required to reset IOV.</p> <p>0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.</p>
SWS	29	rh	<p>SW Sticky Bit</p> <p>The Software Sticky Bit is set when the SRR bit has been set via the SETR bit.</p> <p>This bit can be cleared by writing with 1 to SWSCLR. Writing to SWS has no effect.</p> <p>0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR</p>
SWSCLR	30	w	<p>SW Sticky Clear Bit</p> <p>SWSCLR is required to reset SWS.</p> <p>0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.</p>
0	9:8, 15:14, 23:21, 31	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

Interrupt Router (IR)

SRC_QSPIxERR (x=0-3)		
QSPIx Error Service Request	(000F8 _H +x*14 _H)	Application Reset Value: 0000 0000 _H
SRC_QSPIxPT (x=0-3)		
QSPIx Phase Transition Service Request	(000FC _H +x*14 _H)	Application Reset Value: 0000 0000 _H
SRC_QSPIxU (x=0-3)		
QSPIx User Defined Service Request	(00100 _H +x*14 _H)	Application Reset Value: 0000 0000 _H
SRC_HSCT0		
HSCT0 Service Request	(00180 _H)	Application Reset Value: 0000 0000 _H
SRC_HSSL0COKy (y=0-3)		
HSSL0 Channel y OK Service Request	(00190 _H +y*10 _H)	Application Reset Value: 0000 0000 _H
SRC_HSSL0RDy (y=0-3)		
HSSL0 Channel y Read Data Service Request	(00194 _H +y*10 _H)	Application Reset Value: 0000 0000 _H
SRC_HSSL0ERRy (y=0-3)		
HSSL0 Channel y Error Service Request	(00198 _H +y*10 _H)	Application Reset Value: 0000 0000 _H
SRC_HSSL0TRGy (y=0-3)		
HSSL0 Channel y Trigger Interrupt Service Request	(0019C _H +y*10 _H)	Application Reset Value: 0000 0000 _H
SRC_HSSL0EXI		
HSSL0 Exception Service Request	(001D0 _H)	Application Reset Value: 0000 0000 _H
SRC_I2C0DTR		
I2C0 Data Transfer Request	(00220 _H)	Application Reset Value: 0000 0000 _H



Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>

Interrupt Router (IR)

Field	Bits	Type	Description
TOS	13:11	rw	Type of Service Control The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000 _B CPU0 service is initiated 001 _B DMA service is initiated 010 _B CPU1 service is initiated Others , Reserved (no action)
ECC	20:16	rwh	Error Correction Code The ECC bit field will be updated by the SRN under the following conditions: <ul style="list-style-type: none"> • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	Service Request Flag The SRR bit shows the status of the Service Request. 0 _B No service request is pending 1 _B A service request is pending
CLRR	25	w	Request Clear Bit The CLRR bit is required to reset SRR . 0 _B No action 1 _B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	Request Set Bit The SETR bit is required to set SRR . 0 _B No action 1 _B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
IOV	27	rh	Interrupt Trigger Overflow Bit The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request. 0 _B No Interrupt Trigger Overflow detected 1 _B Interrupt Overflow Detected.
IOVCLR	28	w	Interrupt Trigger Overflow Clear Bit IOVCLR is required to reset IOV . 0 _B No action 1 _B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	SW Sticky Bit The Software Sticky Bit is set when the SRR bit has been set via the SETR bit. This bit can be cleared by writing with 1 to SWSCLR . Writing to SWS has no effect. 0 _B No interrupt was initiated via SETR 1 _B Interrupt was initiated via SETR

Interrupt Router (IR)

Field	Bits	Type	Description
SWSCLR	30	w	SW Sticky Clear Bit SWSCLR is required to reset SWS . 0 _B No action 1 _B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	Reserved Read as 0; should be written with 0.

SRC_I2C0ERR

I2C0 Error Service Request (00224_H) **Application Reset Value: 0000 0000_H**

SRC_I2C0P

I2C0 Protocol Service Request (00228_H) **Application Reset Value: 0000 0000_H**

SRC_SENTx (x=0-9)

SENT TRIGx Service Request (00240_H+x*4) **Application Reset Value: 0000 0000_H**

SRC_MSC0SRy (y=0-4)

MSC0 Service Request y (00270_H+y*4) **Application Reset Value: 0000 0000_H**

SRC_CCU6xSRy (x=0-1;y=0-3)

CCUx Service Request y (002C0_H+x*10_H+y*4) **Application Reset Value: 0000 0000_H**

SRC_GPT120CIRQ

GPT120 CAPREL Service Request (002E0_H) **Application Reset Value: 0000 0000_H**

SRC_GPT120T2

GPT120 Timer 2 Service Request (002E4_H) **Application Reset Value: 0000 0000_H**

SRC_GPT120T3

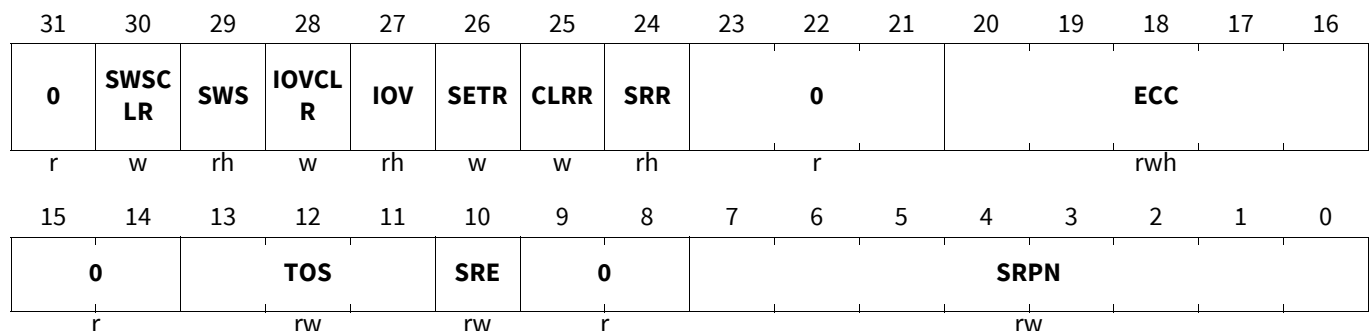
GPT120 Timer 3 Service Request (002E8_H) **Application Reset Value: 0000 0000_H**

SRC_GPT120T4

GPT120 Timer 4 Service Request (002EC_H) **Application Reset Value: 0000 0000_H**

SRC_GPT120T5

GPT120 Timer 5 Service Request (002F0_H) **Application Reset Value: 0000 0000_H**



Interrupt Router (IR)

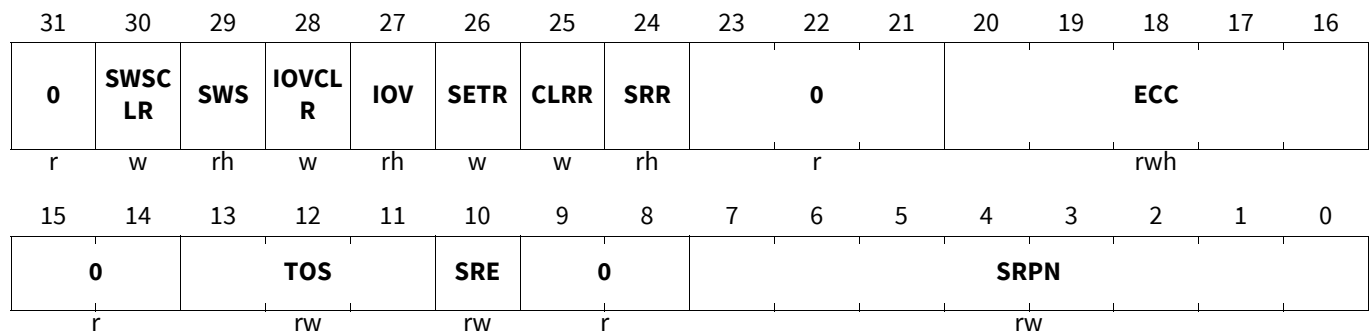
Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>
TOS	13:11	rw	<p>Type of Service Control</p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <p>000_B CPU0 service is initiated</p> <p>001_B DMA service is initiated</p> <p>010_B CPU1 service is initiated</p> <p>Others, Reserved (no action)</p>
ECC	20:16	rwh	<p>Error Correction Code</p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> Write or Read-Modify-Write to SRC[31:0] Write to SRC[15:0] (16-bit write) Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	<p>Service Request Flag</p> <p>The SRR bit shows the status of the Service Request.</p> <p>0_B No service request is pending</p> <p>1_B A service request is pending</p>
CLRR	25	w	<p>Request Clear Bit</p> <p>The CLRR bit is required to reset SRR.</p> <p>0_B No action</p> <p>1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>
SETR	26	w	<p>Request Set Bit</p> <p>The SETR bit is required to set SRR.</p> <p>0_B No action</p> <p>1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>

Interrupt Router (IR)

Field	Bits	Type	Description
IOV	27	rh	<p>Interrupt Trigger Overflow Bit</p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request.</p> <p>0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.</p>
IOVCLR	28	w	<p>Interrupt Trigger Overflow Clear Bit</p> <p>IOVCLR is required to reset IOV.</p> <p>0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.</p>
SWS	29	rh	<p>SW Sticky Bit</p> <p>The Software Sticky Bit is set when the SRR bit has been set via the SETR bit.</p> <p>This bit can be cleared by writing with 1 to SWSCLR. Writing to SWS has no effect.</p> <p>0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR</p>
SWSCLR	30	w	<p>SW Sticky Clear Bit</p> <p>SWSCLR is required to reset SWS.</p> <p>0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.</p>
0	9:8, 15:14, 23:21, 31	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

Interrupt Router (IR)

SRC_GPT120T6 GPT120 Timer 6 Service Request	(002F4 _H)	Application Reset Value: 0000 0000_H
SRC_STMxSRy (x=0-1;y=0-1) System Timer x Service Request y	(00300 _H +x*8+y*4)	Application Reset Value: 0000 0000_H
SRC_FCE0 FCE0 Error Service Request	(00330 _H)	Application Reset Value: 0000 0000_H
SRC_DMAERRy (y=0-3) DMA Error Service Request y	(00340 _H +y*4)	Application Reset Value: 0000 0000_H
SRC_DMACHy (y=0-63) DMA Channel y Service Request	(00370 _H +y*4)	Application Reset Value: 0000 0000_H
SRC_GETHy (y=0-9) GETH Service Request y	(00580 _H +y*4)	Application Reset Value: 0000 0000_H
SRC_CANxINTy (x=0-1;y=0-15) CANx Service Request y	(005B0 _H +x*40 _H +y*4)	Application Reset Value: 0000 0000_H
SRC_VADCGxSRy (x=0-3;y=0-3) EVADC Group x Service Request y	(00670 _H +x*10 _H +y*4)	Application Reset Value: 0000 0000_H
SRC_VADCG8SRy (y=0-3) EVADC Group 8 Service Request y	(006F0 _H +y*4)	Application Reset Value: 0000 0000_H
SRC_VADCG9SRy (y=0-3) EVADC Group 9 Service Request y	(00700 _H +y*4)	Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>

Interrupt Router (IR)

Field	Bits	Type	Description
TOS	13:11	rw	Type of Service Control The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000 _B CPU0 service is initiated 001 _B DMA service is initiated 010 _B CPU1 service is initiated Others , Reserved (no action)
ECC	20:16	rwh	Error Correction Code The ECC bit field will be updated by the SRN under the following conditions: <ul style="list-style-type: none"> • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	Service Request Flag The SRR bit shows the status of the Service Request. 0 _B No service request is pending 1 _B A service request is pending
CLRR	25	w	Request Clear Bit The CLRR bit is required to reset SRR . 0 _B No action 1 _B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	Request Set Bit The SETR bit is required to set SRR . 0 _B No action 1 _B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
IOV	27	rh	Interrupt Trigger Overflow Bit The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request. 0 _B No Interrupt Trigger Overflow detected 1 _B Interrupt Overflow Detected.
IOVCLR	28	w	Interrupt Trigger Overflow Clear Bit IOVCLR is required to reset IOV . 0 _B No action 1 _B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	SW Sticky Bit The Software Sticky Bit is set when the SRR bit has been set via the SETR bit. This bit can be cleared by writing with 1 to SWSCLR . Writing to SWS has no effect. 0 _B No interrupt was initiated via SETR 1 _B Interrupt was initiated via SETR

Interrupt Router (IR)

Field	Bits	Type	Description
SWSCLR	30	w	SW Sticky Clear Bit SWSCLR is required to reset SWS . 0 _B No action 1 _B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	Reserved Read as 0; should be written with 0.

SRC_VADCFCxSR0 (x=0-1)

EVADC Fast Compare x Service Request SR0 (00730_H+x*4) **Application Reset Value: 0000 0000_H**

SRC_VADCCGxSRy (x=0-1;y=0-3)

EVADC Common Group x Service Request y(00750_H+x*10_H+y*4) **Application Reset Value: 0000 0000_H**

SRC_DSADCSRMx (x=0-3)

DSADC SRMx Service Request (00770_H+x*8) **Application Reset Value: 0000 0000_H**

SRC_DSADCSRAX (x=0-3)

DSADC SRAX Service Request (00774_H+x*8) **Application Reset Value: 0000 0000_H**

SRC_ERAYOINT0

E-RAY 0 Service Request 0 (00800_H) **Application Reset Value: 0000 0000_H**

SRC_ERAYOINT1

E-RAY 0 Service Request 1 (00804_H) **Application Reset Value: 0000 0000_H**

SRC_ERAYOTINT0

E-RAY 0 Timer Interrupt 0 Service Request (00808_H) **Application Reset Value: 0000 0000_H**

SRC_ERAYOTINT1

E-RAY 0 Timer Interrupt 1 Service Request (0080C_H) **Application Reset Value: 0000 0000_H**

SRC_ERAYONDAT0

E-RAY 0 New Data 0 Service Request (00810_H) **Application Reset Value: 0000 0000_H**

SRC_ERAYONDAT1

E-RAY 0 New Data 1 Service Request (00814_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCL R	IOV	SETR	CLRR	SRR	0							ECC
r	w	rh	w	rh	w	w	rh	r							rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS			SRE	0									SRPN
r		rw			rw	r									rw

Interrupt Router (IR)

Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>
TOS	13:11	rw	<p>Type of Service Control</p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <p>000_B CPU0 service is initiated</p> <p>001_B DMA service is initiated</p> <p>010_B CPU1 service is initiated</p> <p>Others, Reserved (no action)</p>
ECC	20:16	rwh	<p>Error Correction Code</p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> Write or Read-Modify-Write to SRC[31:0] Write to SRC[15:0] (16-bit write) Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	<p>Service Request Flag</p> <p>The SRR bit shows the status of the Service Request.</p> <p>0_B No service request is pending</p> <p>1_B A service request is pending</p>
CLRR	25	w	<p>Request Clear Bit</p> <p>The CLRR bit is required to reset SRR.</p> <p>0_B No action</p> <p>1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>
SETR	26	w	<p>Request Set Bit</p> <p>The SETR bit is required to set SRR.</p> <p>0_B No action</p> <p>1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>

Interrupt Router (IR)

Field	Bits	Type	Description
IOV	27	rh	<p>Interrupt Trigger Overflow Bit</p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request.</p> <p>0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.</p>
IOVCLR	28	w	<p>Interrupt Trigger Overflow Clear Bit</p> <p>IOVCLR is required to reset IOV.</p> <p>0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.</p>
SWS	29	rh	<p>SW Sticky Bit</p> <p>The Software Sticky Bit is set when the SRR bit has been set via the SETR bit.</p> <p>This bit can be cleared by writing with 1 to SWSCLR. Writing to SWS has no effect.</p> <p>0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR</p>
SWSCLR	30	w	<p>SW Sticky Clear Bit</p> <p>SWSCLR is required to reset SWS.</p> <p>0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.</p>
0	9:8, 15:14, 23:21, 31	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

Interrupt Router (IR)

SRC_ERAY0MBSC0		
E-RAY 0 Message Buffer Status Changed 0 Service Request(00818 _H)		Application Reset Value: 0000 0000 _H
SRC_ERAY0MBSC1		
E-RAY 0 Message Buffer Status Changed 1 Service Request(0081C _H)		Application Reset Value: 0000 0000 _H
SRC_ERAY0OBUSY		
E-RAY 0 Output Buffer Busy	(00820 _H)	Application Reset Value: 0000 0000 _H
SRC_ERAY0IBUSY		
E-RAY 0 Input Buffer Busy	(00824 _H)	Application Reset Value: 0000 0000 _H
SRC_DMUHOST		
DMU Host Service Request	(00860 _H)	Application Reset Value: 0000 0000 _H
SRC_DMUFSI		
DMU FSI Service Request	(00864 _H)	Application Reset Value: 0000 0000 _H
SRC_HSM_y (y=0-1)		
HSM Service Request _y	(00870 _H + _y *4)	Application Reset Value: 0000 0000 _H
SRC_SCUERU_x (x=0-3)		
SCU ERU Service Request _x	(00880 _H + _x *4)	Application Reset Value: 0000 0000 _H
SRC_PMSDTS		
PMS DTS Service Request	(008AC _H)	Application Reset Value: 0000 0000 _H
SRC_PMS_x (x=0-3)		
Power Management System Service Request _x (008B0 _H + _x *4)		Application Reset Value: 0000 0000 _H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCLR	IOV	SETR	CLRR	SRR	0	0	0	0	0	0	0	0
r	w	rh	w	rh	w	w	rh	r	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	TOS	0	0	SRE	0	0	0	0	0	0	0	0	0	0
r	0	rw	0	0	rw	0	0	0	0	0	0	0	0	0	0

Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>

Interrupt Router (IR)

Field	Bits	Type	Description
TOS	13:11	rw	Type of Service Control The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000 _B CPU0 service is initiated 001 _B DMA service is initiated 010 _B CPU1 service is initiated Others , Reserved (no action)
ECC	20:16	rwh	Error Correction Code The ECC bit field will be updated by the SRN under the following conditions: <ul style="list-style-type: none"> • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	Service Request Flag The SRR bit shows the status of the Service Request. 0 _B No service request is pending 1 _B A service request is pending
CLRR	25	w	Request Clear Bit The CLRR bit is required to reset SRR . 0 _B No action 1 _B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	Request Set Bit The SETR bit is required to set SRR . 0 _B No action 1 _B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
IOV	27	rh	Interrupt Trigger Overflow Bit The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request. 0 _B No Interrupt Trigger Overflow detected 1 _B Interrupt Overflow Detected.
IOVCLR	28	w	Interrupt Trigger Overflow Clear Bit IOVCLR is required to reset IOV . 0 _B No action 1 _B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	SW Sticky Bit The Software Sticky Bit is set when the SRR bit has been set via the SETR bit. This bit can be cleared by writing with 1 to SWSCLR . Writing to SWS has no effect. 0 _B No interrupt was initiated via SETR 1 _B Interrupt was initiated via SETR

Interrupt Router (IR)

Field	Bits	Type	Description
SWSCLR	30	w	SW Sticky Clear Bit SWSCLR is required to reset SWS . 0 _B No action 1 _B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	Reserved Read as 0; should be written with 0.

SRC_SCR

Stand By Controller Service Request	(008C0 _H)	Application Reset Value: 0000 0000 _H
SRC_SMUy (y=0-2)		
SMU Service Request y	(008D0 _H +y*4)	Application Reset Value: 0000 0000 _H
SRC_PSI5y (y=0-7)		
PSI5 Service Request y	(008E0 _H +y*4)	Application Reset Value: 0000 0000 _H
SRC_PSI5Sy (y=0-7)		
PSI5-S Service Request y	(00950 _H +y*4)	Application Reset Value: 0000 0000 _H
SRC_GPSRxy (x=0-1;y=0-7)		
General Purpose Group x Service Request y(00990 _H +x*20 _H +y*4)		Application Reset Value: 0000 0000 _H
SRC_GTMAEIIRQ		
AEI Shared Service Request	(00A70 _H)	Application Reset Value: 0000 0000 _H
SRC_GTMARUIRQw (w=0-2)		
ARU Shared Service Request w	(00A74 _H +w*4)	Application Reset Value: 0000 0000 _H
SRC_GTMBRCIRQ		
BRC Shared Service Request	(00A80 _H)	Application Reset Value: 0000 0000 _H
SRC_GTMCMPIRQ		
CMP Shared Service Request	(00A84 _H)	Application Reset Value: 0000 0000 _H
SRC_GTMSPEwIRQ (w=0-1)		
SPEw Shared Service Request	(00A88 _H +w*4)	Application Reset Value: 0000 0000 _H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSC LR	SWS	IOVCL R	IOV	SETR	CLRR	SRR		0						ECC
r	w	rh	w	rh	w	w	rh		r						rwh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS			SRE		0								SRPN
r		rw			rw		r								rw

Interrupt Router (IR)

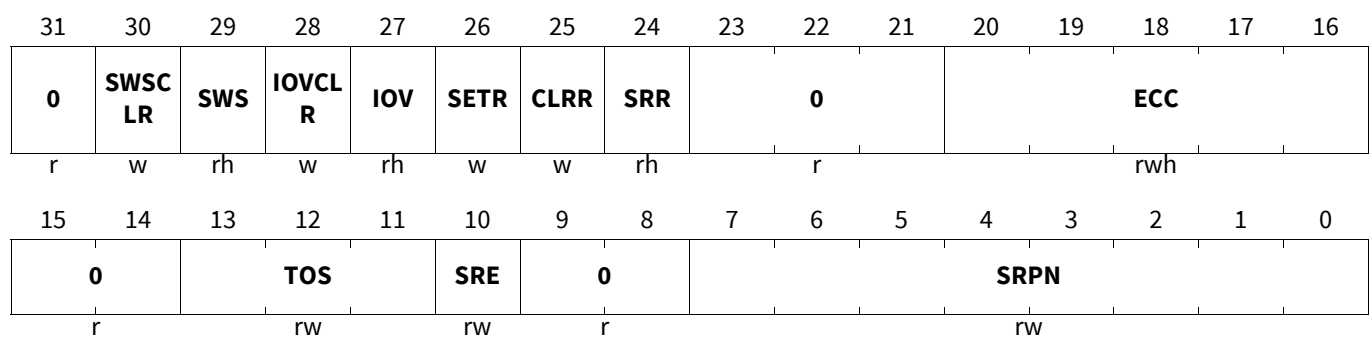
Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>
TOS	13:11	rw	<p>Type of Service Control</p> <p>The TOS bit field configuration maps a Service Request to an Interrupt Service Provider:</p> <p>000_B CPU0 service is initiated</p> <p>001_B DMA service is initiated</p> <p>010_B CPU1 service is initiated</p> <p>Others, Reserved (no action)</p>
ECC	20:16	rwh	<p>Error Correction Code</p> <p>The ECC bit field will be updated by the SRN under the following conditions:</p> <ul style="list-style-type: none"> Write or Read-Modify-Write to SRC[31:0] Write to SRC[15:0] (16-bit write) Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	<p>Service Request Flag</p> <p>The SRR bit shows the status of the Service Request.</p> <p>0_B No service request is pending</p> <p>1_B A service request is pending</p>
CLRR	25	w	<p>Request Clear Bit</p> <p>The CLRR bit is required to reset SRR.</p> <p>0_B No action</p> <p>1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.</p>
SETR	26	w	<p>Request Set Bit</p> <p>The SETR bit is required to set SRR.</p> <p>0_B No action</p> <p>1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.</p>

Interrupt Router (IR)

Field	Bits	Type	Description
IOV	27	rh	<p>Interrupt Trigger Overflow Bit</p> <p>The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request.</p> <p>0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.</p>
IOVCLR	28	w	<p>Interrupt Trigger Overflow Clear Bit</p> <p>IOVCLR is required to reset IOV.</p> <p>0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.</p>
SWS	29	rh	<p>SW Sticky Bit</p> <p>The Software Sticky Bit is set when the SRR bit has been set via the SETR bit.</p> <p>This bit can be cleared by writing with 1 to SWSCLR. Writing to SWS has no effect.</p> <p>0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR</p>
SWSCLR	30	w	<p>SW Sticky Clear Bit</p> <p>SWSCLR is required to reset SWS.</p> <p>0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.</p>
0	9:8, 15:14, 23:21, 31	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

Interrupt Router (IR)

SRC_GTMPSM0x (x=0-7)		
PSM0 Shared Service Request x	(00AA0_H+x*4)	Application Reset Value: 0000 0000_H
SRC_GTMDPLLw (w=0-26)		
DPLL Service Request w	(00B00_H+w*4)	Application Reset Value: 0000 0000_H
SRC_GTMERR		
Error Service Request	(00B70_H)	Application Reset Value: 0000 0000_H
SRC_GTMTIMwx (w=0-2;x=0-7)		
TIMw Shared Service Request x	(00B90_H+w*20_H+x*4)	Application Reset Value: 0000 0000_H
SRC_GTMMCSwx (w=0-2;x=0-7)		
MCSw Shared Service Request x	(00CB0_H+w*20_H+x*4)	Application Reset Value: 0000 0000_H
SRC_GTMTOMwx (w=0-1;x=0-7)		
TOMw Shared Service Request x	(00E10_H+w*20_H+x*4)	Application Reset Value: 0000 0000_H
SRC_GTMATOMwx (w=0-3;x=0-3)		
ATOMw Shared Service Request x	(00EF0_H+w*10_H+x*4)	Application Reset Value: 0000 0000_H
SRC_GTMMCSWw (w=0-9)		
GTM Multi Channel Sequencer Service Request w	(00FD0_H+w*4)	Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SRPN	7:0	rw	<p>Service Request Priority Number</p> <p>The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration):</p> <p>00_H -> Service request is on lowest priority</p> <p>...</p> <p>FF_H -> Service request is on highest priority</p> <p>Notes</p> <ol style="list-style-type: none"> For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0. For DMA, SRPN must not be greater than the highest implemented DMA channel number.
SRE	10	rw	<p>Service Request Enable</p> <p>0_B Service request is disabled</p> <p>1_B Service request is enabled</p>

Interrupt Router (IR)

Field	Bits	Type	Description
TOS	13:11	rw	Type of Service Control The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000 _B CPU0 service is initiated 001 _B DMA service is initiated 010 _B CPU1 service is initiated Others , Reserved (no action)
ECC	20:16	rwh	Error Correction Code The ECC bit field will be updated by the SRN under the following conditions: <ul style="list-style-type: none"> • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	Service Request Flag The SRR bit shows the status of the Service Request. 0 _B No service request is pending 1 _B A service request is pending
CLRR	25	w	Request Clear Bit The CLRR bit is required to reset SRR . 0 _B No action 1 _B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	Request Set Bit The SETR bit is required to set SRR . 0 _B No action 1 _B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
IOV	27	rh	Interrupt Trigger Overflow Bit The IOV bit is set by HW if a new service request was triggered via interrupt trigger or SETR bit while the SRN has still an pending service request. 0 _B No Interrupt Trigger Overflow detected 1 _B Interrupt Overflow Detected.
IOVCLR	28	w	Interrupt Trigger Overflow Clear Bit IOVCLR is required to reset IOV . 0 _B No action 1 _B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	SW Sticky Bit The Software Sticky Bit is set when the SRR bit has been set via the SETR bit. This bit can be cleared by writing with 1 to SWSCLR . Writing to SWS has no effect. 0 _B No interrupt was initiated via SETR 1 _B Interrupt was initiated via SETR

Interrupt Router (IR)

Field	Bits	Type	Description
SWSCLR	30	w	SW Sticky Clear Bit SWSCLR is required to reset SWS . 0 _B No action 1 _B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	Reserved Read as 0; should be written with 0.

16.6 Revision History**Table 202 Revision History**

Reference	Change to Previous Version	Comment
V1.2.6		
-	No functional changes	
V1.2.7		
Page 11	Changed SRC_VADCG8SR - SRC_VADCG9SR index name to 'y'.	
V1.2.8		
	Removed connection table.	
V1.2.9		
	No changes.	
V1.2.10		
-	No functional changes.	
V1.2.11		
Page 6	Updated bullet list item.	

Flexible CRC Engine (FCE)**17 Flexible CRC Engine (FCE)**

For the general description of the module and the registers, please refer to the family spec.

17.1 TC36x Specific IP Configuration

There are no device specific IP configurations.

Flexible CRC Engine (FCE)

17.2 TC36x Specific Register Set

Table 203 Register Address Space - FCE

Module	Base Address	End Address	Note
FCE	F0000000 _H	F00001FF _H	FPI slave interface

Table 204 Register Overview - FCE (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FCE_CLC	Clock Control Register	000 _H	U,SV	E,SV,P	Application Reset	See Family Spec
FCE_ID	Module Identification Register	008 _H	U,SV	BE	Application Reset	See Family Spec
FCE_CHSTS	Channels Status Register	020 _H	U,SV	BE	Application Reset	See Family Spec
FCE_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_KRST1	Kernel Reset Register 1	0F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_KRST0	Kernel Reset Register 0	0F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_ACCEN1	Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
FCE_ACCEN0	Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	See Family Spec
FCE_IRi (i=0-7)	Input Register i	100 _H +i*2 0 _H	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_RESi (i=0-7)	CRC Result Register i	104 _H +i*2 0 _H	U,SV	BE	Application Reset	See Family Spec
FCE_CFGi (i=0-7)	CRC Configuration Register i	108 _H +i*2 0 _H	U,SV	P,E,SV	Application Reset	See Family Spec
FCE_STSi (i=0-7)	CRC Status Register i	10C _H +i*2 0 _H	U,SV	P,U,SV	Application Reset	See Family Spec

Flexible CRC Engine (FCE)

Table 204 Register Overview - FCE (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FCE_LENGTHi (i=0-7)	CRC Length Register i	110 _H +i*2 0 _H	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CHECKi (i=0-7)	CRC Check Register i	114 _H +i*2 0 _H	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CRCi (i=0-7)	CRC Register i	118 _H +i*2 0 _H	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CTRi (i=0-7)	CRC Test Register i	11C _H +i*2 0 _H	U,SV	P,U,SV	Application Reset	See Family Spec

17.3 TC36x Specific Registers

No deviations from the Family Spec

17.4 Connectivity

Table 205 Connections of FCE

Interface Signals	connects		Description
FCE:SRC_FCE	to	INT:fce0.SRC_FCE	FCE Service Request

17.5 Revision History

Table 206 Revision History

Reference	Change to Previous Version	Comment
V4.2.9		
-	No functional changes.	

Direct Memory Access (DMA)

18 Direct Memory Access (DMA)

This is the TC36x specific information related to the DMA module of the AURIXTC3XX product family.

18.1 TC36x Specific IP Configuration

The TC36x DMA contains 64 DMA channels.

18.2 TC36x Specific Register Set

Table 207 Register Address Space - DMA

Module	Base Address	End Address	Note
DMA	F0010000 _H	F0013FFF _H	FPI slave interface

Table 208 Register Overview - DMA (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_CLC	DMA Clock Control Register	0000 _H	U,SV	SV,E,P00,P01	Application Reset	See Family Spec
DMA_ID	DMA Identification Register	0008 _H	U,SV	BE	Application Reset	See Family Spec
DMA_ACCENr0 (r=0-3)	RP r Access Enable Register 0	0040 _H +r*8	U,SV	SV,SE	Application Reset	See Family Spec
DMA_ACCENr1 (r=0-3)	RP r Access Enable Register 1	0044 _H +r*8	U,SV	nBE	Application Reset	See Family Spec
DMA_EERm (m=0-1)	ME m Enable Error Register	0120 _H +m*1000 _H	U,SV	SV	Application Reset	See Family Spec
DMA_ERRSRm (m=0-1)	ME m Error Status Register	0124 _H +m*1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_CLREm (m=0-1)	ME m Clear Error Register	0128 _H +m*1000 _H	U,SV	SV	Application Reset	See Family Spec
DMA_MEmSR (m=0-1)	ME m Status Register	0130 _H +m*1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm0R (m=0-1)	ME m Read Register 0	0140 _H +m*1000 _H	U,SV	BE	Application Reset	See Family Spec

Direct Memory Access (DMA)

Table 208 Register Overview - DMA (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_MEm1R (m=0-1)	ME m Read Register 1	0144 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm2R (m=0-1)	ME m Read Register 2	0148 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm3R (m=0-1)	ME m Read Register 3	014C _H + m*1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm4R (m=0-1)	ME m Read Register 4	0150 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm5R (m=0-1)	ME m Read Register 5	0154 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm6R (m=0-1)	ME m Read Register 6	0158 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm7R (m=0-1)	ME m Read Register 7	015C _H + m*1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmRDCR C (m=0-1)	ME m Channel Read Data CRC Register	0180 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSDCR C (m=0-1)	ME m Channel Source and Destination Address CRC Register	0184 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSADR (m=0-1)	ME m Channel Source Address Register	0188 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmDADR (m=0-1)	ME m Channel Destination Address Register	018C _H + m*1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmADICR (m=0-1)	ME m Channel Address and Interrupt Control Register	0190 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmCHCR (m=0-1)	ME m Channel Control Register	0194 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSHADR (m=0-1)	ME m Channel Shadow Address Register	0198 _H +m *1000 _H	U,SV	BE	Application Reset	See Family Spec

Direct Memory Access (DMA)

Table 208 Register Overview - DMA (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_MEmCHSR (m=0-1)	ME m Channel Status Register	019C _H + m*1000 _H	U,SV	BE	Application Reset	See Family Spec
DMA_OTSS	DMA OCDS Trigger Set Select	1200 _H	U,SV	SV	See Family Spec	See Family Spec
DMA_PRR0	DMA Pattern Read Register 0	1208 _H	U,SV	SV	Application Reset	See Family Spec
DMA_PRR1	DMA Pattern Read Register 1	120C _H	U,SV	SV	Application Reset	See Family Spec
DMA_TIME	DMA Time Register	1210 _H	U,SV	BE	Application Reset	See Family Spec
DMA_MODER (r=0-3)	RP r Mode Register	1300 _H +r* 4	U,SV	SV,SE,P00, P01	Application Reset	See Family Spec
DMA_ERRINTRr (r=0-3)	RP r Error Interrupt Set Register	1320 _H +r* 4	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_HRRc (c=000-63)	DMA Channel c Resource Partition Register	1800 _H +c *4	U,SV	SV,SE,P00, P01	Application Reset	See Family Spec
DMA_SUSENRc (c=000-63)	DMA Channel c Suspend Enable Register	1A00 _H +c *4	U,SV	SV,E,Pr	See Family Spec	See Family Spec
DMA_SUSACRc (c=000-63)	DMA Channel c Suspend Acknowledge Register	1C00 _H +c *4	U,SV	BE	See Family Spec	See Family Spec
DMA_TSRc (c=000-63)	DMA Channel c Transaction State Register	1E00 _H +c *4	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_RDCRCRc (c=000-63)	DMARAM Channel c Read Data CRC Register	2000 _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SDCRCRc (c=000-63)	DMARAM Channel c Source and Destination Address CRC Register	2004 _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SADRc (c=000-63)	DMARAM Channel c Source Address Register	2008 _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec

Direct Memory Access (DMA)

Table 208 Register Overview - DMA (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_DADRC (c=000-63)	DMARAM Channel c Destination Address Register	200C _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_ADICRC (c=000-63)	DMARAM Channel c Address and Interrupt Control Register	2010 _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_CHCFGRc (c=000-63)	DMARAM Channel c Configuration Register	2014 _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SHADRC (c=000-63)	DMARAM Channel c Shadow Address Register	2018 _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_CHCSRc (c=000-63)	DMARAM Channel c Control and Status Register	201C _H +c *20 _H	U,SV	SV,Pr	Application Reset	See Family Spec

18.3 TC36x Specific Registers

No deviations from the Family Spec

18.4 Connectivity

Table 209 Connections of DMA

Interface Signals	connects		Description
DMA:fpio_sleep_n	from	SCU:scu_syst_sleep_n	Sleep Control
DMA:ERR_INT(3:0)	to	INT:dma.ERR_INT(3:0)	DMA Error Service Request
DMA:CH_INT(127:0)	to	INT:dma.CH_INT(127:0)	DMA Channel Service Request

18.5 Revision History

Table 210 Revision History

Reference	Change to Previous Version	Comment
V0.1.15		
	Connectivity table updated.	
V0.1.16		
-	No functional changes.	
V0.1.17		
-	No functional changes.	
V0.1.18		
-	No functional changes.	

19 Signal Processing Unit (SPU)

This device doesn't contain a SPU module.

20 SPU Lockstep Comparator (SPULCKSTP)

This device doesn't contain a SPULCKSTP module.

Extension Memory (EMEM)

21 Extension Memory (EMEM)

This device doesn't contain an EMEM module.

22 Radar Interface (RIF)

This device doesn't contain a RIF module.

23 High Speed Pulse Density Modulation Module (HSPDM)

This device doesn't contain a HSPDM module.

24 Camera and ADC Interface (CIF)

This device doesn't contain a CIF module.

System Timer (STM)

25 System Timer (STM)

This chapter describes the device specific details in TC36x.

25.1 TC36x Specific IP Configuration

See features in family spec

25.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined below

Table 211 Register Address Space - STM

Module	Base Address	End Address	Note
STM0	F0001000 _H	F00010FF _H	FPI slave interface
STM1	F0001100 _H	F00011FF _H	FPI slave interface

Register Overview Table

There are no product specific register for this module.

25.3 TC36x Specific Registers

There are no product specific register for this module.

25.4 Connectivity

The tables below list all the connections of STM instances.

Table 212 Connections of STM0

Interface Signals	connects		Description
STM0:SR0_INT	to	INT:stm0.SR0_INT	System Timer Service Request 0
		CAN0:STM0.SR0_INT	
		CAN1:STM0.SR0_INT	
STM0:SR1_INT	to	INT:stm0.SR1_INT	System Timer Service Request 1
		CAN0:STM0.SR1_INT	
		CAN1:STM0.SR1_INT	

Table 213 Connections of STM1

Interface Signals	connects		Description
STM1:SR0_INT	to	INT:stm1.SR0_INT	System Timer Service Request 0
		CAN0:STM1.SR0_INT	
		CAN1:STM1.SR0_INT	

System Timer (STM)
Table 213 Connections of STM1 (cont'd)

Interface Signals	connects		Description
STM1:SR1_INT	to	INT:stm1.SR1_INT	System Timer Service Request 1
		CAN0:STM1.SR1_INT	
		CAN1:STM1.SR1_INT	

25.5 Revision History**Table 214 Revision History**

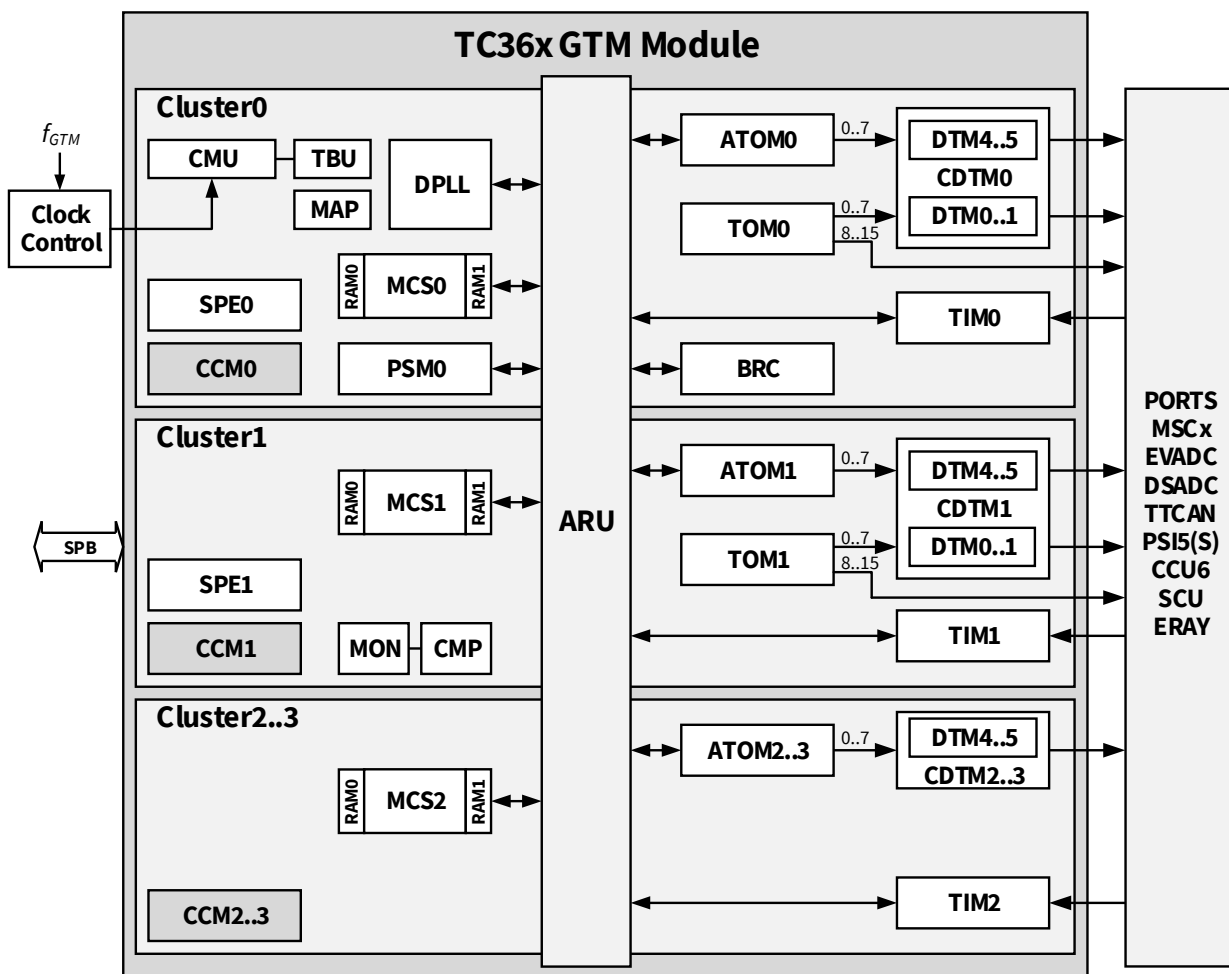
Reference	Change to Previous Version	Comment
V9.2.3		
Page 1	Connection tables updated.	
V9.2.4		
-	No changes.	

Generic Timer Module (GTM)

26 Generic Timer Module (GTM)

The following chapter describes the specific TC36x GTM configuration. For the GTM IP functionalities, please refer to the Family specification.

26.1 TC36x Specific IP Configuration



GTM_Block-Diagram_TC36x.vsd

Figure 5 GTM IP Block Diagram (TC36x)

Generic Timer Module (GTM)
Table 215 GTM Configuration by AURIX TC36x Product

GTM Modules	TC36x
TIM	3x8 ch. (TIM0-2)
TOM	2x16 ch. (TOM0-1)
ATOM	4x8 ch. (ATOM0-3)
DTM/CDTM	2x4 ch., 2x2 ch./4xCDTM
MCS	3x8 ch. (MCS0-2)
SPE	2 (SPE0-1)
PSM	1 (PSM0)
DPLL	1
TBU	4 (TBU0-3)
BRC	1
MON	1
CMP	1
GTM Clusters (max speed)	4 (CCM0-3) CCM0-3: 200 MHz max
ARU Latency (round robin)	81x10ns => 810ns @100MHz, (ARU_CADDR_END =80)

Table 216 CDTM Connections by AURIX TC36x Product

TC36x GTM (A)TOM Modules	CDTM
TOM0_CH0..CH3	CDTM0_DTM0
TOM0_CH4..CH7	CDTM0_DTM1
TOM1_CH0..CH3	CDTM1_DTM0
TOM1_CH4..CH7	CDTM1_DTM1
ATOM0_CH0..CH3	CDTM0_DTM4
ATOM0_CH4..CH7	CDTM0_DTM5
ATOM1_CH0..CH3	CDTM1_DTM4
ATOM1_CH4..CH7	CDTM1_DTM5
ATOM2_CH0..CH3	CDTM2_DTM4
ATOM2_CH4..CH7	CDTM2_DTM5
ATOM3_CH0..CH3	CDTM3_DTM4
ATOM3_CH4..CH7	CDTM3_DTM5
Total DTM Channels	12

Generic Timer Module (GTM)

Table 217 TC36x specific configuration of GTM

Parameter	GTM
Number of MCS modules	3
Number of DPLL modules	1
Number of PSM modules	1
Number of TIM modules	3
Number of ATOM DTM modules	4
Number of TOM DTM modules	2
Number of DSADC channels	4
Number of primary EVADC groups	4
Number of secondary EVADC groups	2
Number of MOSEL controlled trigger outputs	4
Number of TOUT signals	130
Number of SCU trigger outputs	4
Number of CAN modules	2
Number of MCS SET signals	4
Number of Fast Compare Channels of EVADC	2
Number of MSC modules	1
Number of DSADCINSEL registers	3
Number of PSI5/PSI5S modules	1
Number of EDSADC modules	1
Channel 3 of TBU is not available.	0
Number of CCM modules	4
Indicate cluster with high clock frequency	1,1,1,1
Number of ARU modules	1
Number of ATOM modules	4
Number of BRC modules	1
Number of TOM modules	2
Number of SPE modules	2
Number of CMP modules	1
Number of MON modules	1
Number of Address range protectors per CCM	10
Number of CDTM modules	4
List of DTM instances available within CDTM instance	(0, 1, 4, 5), (0, 1, 4, 5), (4, 5), (4, 5)
Number of MAP modules	1
Number of MCS channel in MCS module instance	8,8,8
Number of MCFG modules	1
List element 1 of MCS	8
List element 2 of MCS	8

Generic Timer Module (GTM)**Table 217 TC36x specific configuration of GTM (cont'd)**

Parameter	GTM
List element 3 of MCS	8
Number of Interrupt Groups for registers ICM_IRQG_CLS_k_MEI	1
CCM0_CFG Reset Value	131199
CCM1_CFG Reset Value	131215
CCM2_CFG Reset Value	131085
CCM3_CFG Reset Value	131076
Fast Clock in Cluster 0	1
Fast Clock in Cluster 1	1
Fast Clock in Cluster 2	1
Fast Clock in Cluster 3	1

Generic Timer Module (GTM)
26.2 TC36x Registers Register Set**Table 218 Register Address Space - GTM**

Module	Base Address	End Address	Note
GTM	F0100000 _H	F01FFFFFF _H	FPI slave interface

Register Overview Tables of GTM**Table 219 Register Overview - GTM (ascending Offset Address)**

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_REV	GTM Version Control Register	000000 _H	U,SV,32		Application Reset	35
GTM_RST	GTM Global Reset Register	000004 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CTRL	GTM Global Control Register	000008 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_AEI_ADDR_XPT	GTM AEI Timeout Exception Address Register	00000C _H	U,SV,32		Application Reset	See Family Spec
GTM_IRQ_NOTIFY	GTM Interrupt Notification Register	000010 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_IRQ_EN	GTM Interrupt Enable Register	000014 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_IRQ_FORCINT	GTM Software Interrupt Generation Register	000018 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_IRQ_MODE	GTM Top Level Interrupts Mode Selection Register	00001C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_EIRQ_EN	GTM Error Interrupt Enable Register	000020 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_HW_CONF	GTM Hardware Configuration Register	000024 _H	U,SV,32		Application Reset	See Family Spec
GTM_CFG	GTM Configuration Register	000028 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_AEI_STA_XPT	GTM AEI Non Zero Status Register	00002C _H	U,SV,32		Application Reset	See Family Spec
GTM_BRIDGE_MODE	GTM AEI Bridge Mode Register	000030 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRIDGE_PT_R1	GTM AEI Bridge Pointer 1 Register	000034 _H	U,SV,32		Application Reset	See Family Spec
GTM_BRIDGE_PT_R2	GTM AEI Bridge Pointer 2 Register	000038 _H	U,SV,32		Application Reset	See Family Spec
GTM_MCS_AEM_DIS	GTM MCS Master Port Disable Register	00003C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_AUX_IN_SRC (i=0-2)	GTM TIM i Module AUX_IN Source Selection Register	000040 _H +i*4	U,SV,32	U,SV,32,P	Application Reset	46
GTM_EXT_CAP_EN_i (i=0-2)	GTM External Capture Trigger Enable i	00005C _H +i*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_OUT (i=0-1)	GTM TOM i Output Level	000080 _H +i*4	U,SV,32		Application Reset	See Family Spec
GTM_ATOM0_OUT	GTM ATOM 0 Output Level	000098 _H	U,SV,32		Application Reset	See Family Spec
GTM_ATOM2_OUT	GTM ATOM 2 Output Level	00009C _H	U,SV,32		Application Reset	See Family Spec
GTM_CLS_CLK_CFG	GTM Cluster Clock Configuration	0000B0 _H	U,SV,32	U,SV,32,P	Application Reset	35
GTM_TBU_CHEN	TBU Global Channel Enable	000100 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH0_CTRL	TBU Channel 0 Control Register	000104 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH0_BASE	TBU Channel 0 Base Register	000108 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TBU_CH1_CTRL	TBU Channel 1 Control Register	00010C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH1_BASE	TBU Channel 1 Base Register	000110 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH2_CTRL	TBU Channel 2 Control Register	000114 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH2_BASE	TBU Channel 2 Base Register	000118 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_CTRL	TBU Channel 3 Control Register	00011C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_BASE	TBU Channel 3 Base Register	000120 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_BASE_MARK	TBU Channel 3 Modulo Value Register	000124 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TBU_CH3_BASE_CAPTURE	TBU Channel 3 Base Captured Register	000128 _H	U,SV,32		Application Reset	See Family Spec
GTM_MON_STAT_US	Monitor Status Register	000180 _H	U,SV,32	U,SV,32,P	Application Reset	36
GTM_MON_ACTIVITY_0	Monitor Activity Register 0	000184 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MON_ACTIVITY_MCSz (z=0-2)	Monitor Activity Register for MCS z	00018C _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_EN	CMP Comparator Enable Register	000200 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_NOTIFY	CMP Event Notification Register	000204 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_EN	CMP Interrupt Enable Register	000208 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_CMP_IRQ_F ORCINT	CMP Interrupt Force Register	00020C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_IRQ_ MODE	CMP Interrupt Mode Configuration Register	000210 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMP_EIRQ_ EN	CMP error interrupt enable register	000214 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_ACCE SS	ARU Access Register	000280 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DATA _H	ARU Access Register Upper Data Word	000284 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DATA _L	ARU Access Register Lower Data Word	000288 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DBG_ ACCESS0	ARU Debug Access Channel 0	00028C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DBG_ DATA0_H	ARU Debug Access 0 Transfer Register Upper Data Word	000290 _H	U,SV,32		Application Reset	See Family Spec
GTM_ARU_DBG_ DATA0_L	ARU Debug Access 0 Transfer Register Lower Data Word	000294 _H	U,SV,32		Application Reset	See Family Spec
GTM_ARU_DBG_ ACCESS1	ARU Debug Access Channel 1	000298 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_DBG_ DATA1_H	ARU Debug Access 1 Transfer Register Upper Data Word	00029C _H	U,SV,32		Application Reset	See Family Spec
GTM_ARU_DBG_ DATA1_L	ARU Debug Access 1 Transfer Register Lower Data Word	0002A0 _H	U,SV,32		Application Reset	See Family Spec
GTM_ARU_IRQ_N OTIFY	ARU Interrupt Notification Register	0002A4 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_IRQ_E N	ARU Interrupt Enable Register	0002A8 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ARU_IRQ_F ORCINT	ARU Force Interrupt Register	0002ACH	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_IRQ_ MODE	ARU Interrupt Mode Register	0002B0 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_CADD R_END	ARU caddr Counter End Value Register	0002B4 _H	U,SV,32	U,SV,32,P	Application Reset	37
GTM_ARU_CTRL	ARU Enable Dynamic Routing Register	0002BC _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN _CTRL (z=0-1)	ARU z Dynamic Routing Control Register	0002C0 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN _ROUTE_LOW (z=0-1)	ARU z Lower Bits of DYN_ROUTE Register	0002C8 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN _ROUTE_HIGH (z=0-1)	ARU z Higher Bits of DYN_ROUTE Register	0002D0 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN _ROUTE_SR_LO W (z=0-1)	ARU z Shadow Register for ARU_z_DYN_ROUTE_LOW	0002D8 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN _ROUTE_SR_HIG H (z=0-1)	ARU z Shadow Register for ARU_z_DYN_ROUTE_HIGH	0002E0 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_z_DYN _RDADDR (z=0-1)	ARU z Read ID for Dynamic Routing	0002E8 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ARU_CADD R	ARU caddr Counter Value	0002FC _H	U,SV,32		Application Reset	See Family Spec
GTM_CMU_CLK_ EN	CMU Clock Enable Register	000300 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_GCLK _NUM	CMU Global Clock Control Numerator	000304 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_GCLK _DEN	CMU Global Clock Control Denominator	000308 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_CMU_CLK_z_CTRL (z=0-7)	CMU Control for Clock Source z	00030C _H +z*4	U,SV,32	U,SV,32,P	Application Reset	45
GTM_CMU_ECLK_z_NUM (z=0-2)	CMU External Clock z Control Numerator	00032C _H +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_ECLK_z_DEN (z=0-2)	CMU External Clock z Control Denominator	000330 _H +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_FXCLK_CTRL	CMU Control FXCLK Sub-Unit Input Clock	000344 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_GLB_CTRL	CMU Synchronizing ARU and Clock Source	000348 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CMU_CLK_CTRL	CMU Control for Clock Source Selection	00034C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_SRC_z_ADDR (z=0-11)	BRC Read Address for Input Channel z	000400 _H +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_SRC_z_DEST (z=0-11)	BRC Destination Channels for Input Channel z	000404 _H +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_NOTIFY	BRC Interrupt Notification Register	000460 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_ENABLE	BRC Interrupt Enable Register	000464 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_FORCEINT	BRC Force Interrupt Register	000468 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_IRQ_MODE	BRC Interrupt Mode Configuration Register	00046C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_RST	BRC Software Reset Register	000470 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_BRC_EIRQ_ENABLE	BRC Error Interrupt Enable Register	000474 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ICM_IRQG_0	ICM Interrupt Group Register Covering Infrastructural and Safety Components ARU, BRC, AEI, PSM0, PSM1, MAP, CMP, SPE	000600 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_1	ICM Interrupt Group Register Covering DPLL	000604 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_2	ICM Interrupt Group Register Covering TIM0, TIM1, TIM2, TIM3	000608 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_4	ICM Interrupt Group Register Covering MCS0 to MCS3 Sub-Modules	000610 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_6	ICM Interrupt Group Register Covering GTM Output Sub-Modules TOM0 to TOM1	000618 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_9	ICM Interrupt Group Register Covering GTM Output Sub-Modules ATOM0, ATOM1, ATOM2 and ATOM3	000624 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_MEI	ICM Interrupt Group Register for Module Error Interrupt Information	000630 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI0	ICM Interrupt Group Register 0 for Channel Error Interrupt Information	000634 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI1	ICM Interrupt Group Register 1 for Channel Error Interrupt Information	000638 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CEI3	ICM Interrupt Group Register 3 for Channel Error Interrupt Information	000640 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_MCSi_CEI (i=0-2)	ICM Interrupt Group MCS i for Channel Error Interrupt information	000664 _H +i*4	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_PSM_k_CEI (k=0)	ICM Interrupt Group PSM 0 for Channel Error Interrupt information of FIFO0, FIFO1, FIFO2	0006A4 _H	U,SV,32		Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ICM_IRQG_SPE_CEI	ICM Interrupt Group SPE for Module Error Interrupt Information	0006B4 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_CLS_k_MEI (k=0)	ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm	000710 _H	U,SV,32		Application Reset	48
GTM_ICM_IRQG_MCSi_CI (i=0-2)	ICM Interrupt Group MCS i for Channel Interrupt Information	000720 _H +i*4	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_PSM_k_CI (k=0)	ICM Interrupt Group PSM 0 for Channel Interrupt Information of FIFO0, FIFO1, FIFO2	000760 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_SPE_CI	ICM Interrupt Group SPE for Module Interrupt Information	000770 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_ATOM_k_CI (k=0)	ICM Interrupt Group ATOM k for Channel Interrupt Information of ATOMm	000790 _H	U,SV,32		Application Reset	See Family Spec
GTM_ICM_IRQG_TOM_k_CI (k=0)	ICM Interrupt Group TOM k for Channel Interrupt Information of TOMm	0007A0 _H	U,SV,32		Application Reset	See Family Spec
GTM_SPEi_CTRL_STAT (i=0-1)	SPEi Control Status Register	000800 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_PAT (i=0-1)	SPEi Input Pattern Definition Register	000804 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_OUT_PATz (i=0-1;z=0-7)	SPEi Output Definition Register z	000808 _H +i*80 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_OUT_CTRL (i=0-1)	SPEi Output Control Register	000828 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_IRQ_NOTIFY (i=0-1)	SPEi Interrupt Notification Register	00082C _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_IRQ_EN (i=0-1)	SPEi Interrupt Enable Register	000830 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_SPEi_IRQ_F ORCINT (i=0-1)	SPEi Interrupt Generation by Software	000834 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_IRQ_ MODE (i=0-1)	SPEi Interrupt Mode Configuration Register	000838 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_EIRQ_ EN (i=0-1)	SPEi Error Interrupt Enable Register	00083C _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_REV_ CNT (i=0-1)	SPEi Input Revolution Counter	000840 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_REV_ CMP (i=0-1)	SPEi Revolution Counter Compare Value	000844 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_CTRL _STAT2 (i=0-1)	SPEi Control Status Register 2	000848 _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_SPEi_CMD (i=0-1)	SPEi Command register	00084C _H +i*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MAP_CTRL	MAP Control Register	000F00 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCFG_CTR L	MCFG Memory Layout Configuration Register	000F40 _H	U,SV,32	U,SV,32,P	Application Reset	38
GTM_TIMi_CHx_ GPR0 (i=0-2;x=0-7)	TIMi Channel x General Purpose 0 Register	001000 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_ GPR1 (i=0-2;x=0-7)	TIMi Channel x General Purpose 1 Register	001004 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_ CNT (i=0-2;x=0-7)	TIMi Channel x SMU Counter Register	001008 _H +i*800 _H + x*80 _H	U,SV,32		Application Reset	See Family Spec
GTM_TIMi_CHx_ ECNT (i=0-2;x=0-7)	TIMi Channel x SMU Edge Counter Register	00100C _H +i*800 _H + x*80 _H	U,SV,32		Application Reset	See Family Spec
GTM_TIMi_CHx_ CNTS (i=0-2;x=0-7)	TIMi Channel x SMU Shadow Counter Register	001010 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TIMi_CHx_TDUC (i=0-2;x=0-7)	TIMi Channel x TDU Counter Register	001014 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_TDUV (i=0-2;x=0-7)	TIMi Channel x TDU Control Register	001018 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_FLT_RE (i=0-2;x=0-7)	TIMi Channel x Filter Parameter 0 Register	00101C _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_FLT_FE (i=0-2;x=0-7)	TIMi Channel x Filter Parameter 1 Register	001020 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_CTRL (i=0;x=0-7) (i=1-2;x=0-7)	TIMi Channel x Control Register	001024 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	68 and Family Spec
GTM_TIMi_CHx_ECTRL (i=0-2;x=0-7)	TIMi Channel x Extended Control Register	001028 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_IRQ_NOTIFY (i=0-2;x=0-7)	TIMi Channel x Interrupt Notification Register	00102C _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_IRQ_EN (i=0-2;x=0-7)	TIMi Channel x Interrupt Enable Register	001030 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_IRQ_FORCINT (i=0-2;x=0-7)	TIMi Channel x Force Interrupt Register	001034 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_IRQ_MODE (i=0-2;x=0-7)	TIMi Channel x Interrupt Mode Configuration Register	001038 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_CHx_IRQ_EN (i=0-2;x=0-7)	TIMi Channel x Error Interrupt Enable Register	00103C _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_INP_VAL (i=0-2)	TIMi Input Value Observation Register	001074 _H +i*800 _H	U,SV,32		Application Reset	See Family Spec
GTM_TIMi_IN_SRC (i=0-2)	TIMi AUX IN Source Selection Register	001078 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TIMi_RST (i=0-2)	TIMi Global Software Reset Register	00107C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TOMi_CHx_CTRL (i=0-1;x=0-15)	TOMi Channel x Control Register	008000 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_SR0 (i=0-1;x=0-15)	TOMi Channel x CCU0 Compare Shadow Register	008004 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_SR1 (i=0-1;x=0-15)	TOMi Channel x CCU1 Compare Shadow Register	008008 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CM0 (i=0-1;x=0-15)	TOMi Channel x CCU0 Compare Register	00800C _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CM1 (i=0-1;x=0-15)	TOMi Channel x CCU1 Compare Register	008010 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_CN0 (i=0-1;x=0-15)	TOMi Channel x CCU0 Counter Register	008014 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_STAT (i=0-1;x=0-15)	TOMi Channel x Status Register	008018 _H +i*800 _H x*40 _H	U,SV,32		Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_NOTIFY (i=0-1;x=0-15)	TOMi Channel x Interrupt Notification Register	00801C _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_EN (i=0-1;x=0-15)	TOMi Channel x Interrupt Enable Register	008020 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_FORCINT (i=0-1;x=0-15)	TOMi Channel x Force Interrupt Register	008024 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_CHx_IRQ_MODE (i=0-1;x=0-15)	TOMi Channel x Interrupt Mode Register	008028 _H +i*800 _H x*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_GLB_CTRL (i=0-1)	TOMi TGC0 Global Control Register	008030 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_ACT_TB (i=0-1)	TOMi TGC0 Action Time Base Register	008034 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_FUPD_CTRL (i=0-1)	TOMi TGC0 Force Update Control Register	008038 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_TOMi_TGC0_INT_TRIG (i=0-1)	TOMi TGC0 Internal Trigger Control Register	00803C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_ENDIS_CTRL (i=0-1)	TOMi TGC0 Enable/Disable Control Register	008070 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_ENDIS_STAT (i=0-1)	TOMi TGC0 Enable/Disable Status Register	008074 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_OUTEN_CTRL (i=0-1)	TOMi TGC0 Output Enable Control Register	008078 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC0_OUTEN_STAT (i=0-1)	TOMi TGC0 Output Enable Status Register	00807C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_GLB_CTRL (i=0-1)	TOMi TGC1 Global Control Register	008230 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_ACT_TB (i=0-1)	TOMi TGC1 Action Time Base Register	008234 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_FUPD_CTRL (i=0-1)	TOMi TGC1 Force Update Control Register	008238 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_INT_TRIG (i=0-1)	TOMi TGC1 Internal Trigger Control Register	00823C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_ENDIS_CTRL (i=0-1)	TOMi TGC1 Enable/Disable Control Register	008270 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_ENDIS_STAT (i=0-1)	TOMi TGC1 Enable/Disable Status Register	008274 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_OUTEN_CTRL (i=0-1)	TOMi TGC1 Output Enable Control Register	008278 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_TOMi_TGC1_OUTEN_STAT (i=0-1)	TOMi TGC1 Output Enable Status Register	00827C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_F2Ai_CHz_ARU_RD_FIFO (i=0;z=0-7)	F2Ai Stream z Read Address Register	018000 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_F2Ai_CHz_STR_CFG (i=0;z=0-7)	F2Ai Stream z Configuration Register	018020 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_F2Ai_ENABLE (i=0)	F2Ai Stream Activation Register	018040 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_F2Ai_CTRL (i=0)	F2Ai Stream Control Register	018044 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_AFDi_CHx_BUF_ACC (i=0;x=0-7)	AFD i FIFO x Buffer Access Register	018080 _H +x*10 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_CTRL (i=0;z=0-7)	FIFOi Channel z Control Register	018400 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_END_ADDR (i=0;z=0-7)	FIFOi Channel z End Address Register	018404 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_START_ADDR (i=0;z=0-7)	FIFOi Channel z Start Address Register	018408 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_UPPER_WM (i=0;z=0-7)	FIFOi Channel z Upper Watermark Register	01840C _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_LOWER_WM (i=0;z=0-7)	FIFOi Channel z Lower Watermark Register	018410 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_STATUS (i=0;z=0-7)	FIFOi Channel z Status Register	018414 _H +z*40 _H	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_FILL_LEVEL (i=0;z=0-7)	FIFOi Channel z Fill Level Register	018418 _H +z*40 _H	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_WR_PTR (i=0;z=0-7)	FIFOi Channel z Write Pointer Register	01841C _H +z*40 _H	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_RD_PTR (i=0;z=0-7)	FIFOi Channel z Read Pointer Register	018420 _H +z*40 _H	U,SV,32		Application Reset	See Family Spec
GTM_FIFOi_CHz_IRQ_NOTIFY (i=0;z=0-7)	FIFOi Channel z Interrupt Notification Register	018424 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_FIFOi_CHz_IRQ_EN (i=0;z=0-7)	FIFOi Channel z Interrupt Enable Register	018428 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_IRQ_FORCINT (i=0;z=0-7)	FIFOi Channel z Force Interrupt Register	01842C _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_IRQ_MODE (i=0;z=0-7)	FIFOi Channel z Interrupt Mode Control Register	018430 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_FIFOi_CHz_EIRQ_EN (i=0;z=0-7)	FIFOi Channel z Error Interrupt Enable Register	018434 _H +z*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_PSM_FIFOi_MEMORY (i=0)	Mapped section of FIFO RAM (001000 _H Byte)	019000 _H	U,SV	U,SV		
GTM_DPLL_CTRL_0	DPLL Control Register 0	028000 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_1	DPLL Control Register 1	028004 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_2	DPLL Control Register 2	028008 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_3	DPLL Control Register 3	02800C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_4	DPLL Control Register 4	028010 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_5	DPLL Control Register 5	028014 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ACT_STA	DPLL ACTION Status Register with Connected Shadow Register	028018 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_OSW	DPLL Offset and Switch Old/New Address Register	02801C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_AOSV_2	DPLL Address Offset Register of RAM 2 Regions	028020 _H	U,SV,32		Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_APT	DPLL Actual RAM Pointer Address for TRIGGER	028024 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APS	DPLL Actual RAM Pointer Address for STATE	028028 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APT_2C	DPLL Actual RAM Pointer for Region 2C	02802C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APS_1C3	DPLL Actual RAM Pointer for RAM Region 1C3	028030 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NUT_C	DPLL Number of Recent TRIGGER Events Used for Calculations	028034 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NUS_C	DPLL Number of Recent STATE Events Used for Calculations	028038 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NTICNT	DPLL Number of Active TRIGGER Events to Interrupt	02803C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_NOTIFY	DPLL Interrupt Notification Register	028040 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_EN	DPLL Interrupt Enable Register	028044 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_FORCINT	DPLL Interrupt Force Register	028048 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_IRQ_MODE	DPLL Interrupt Mode Register	02804C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_EIRQ_EN	DPLL Error Interrupt Enable Register	028050 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_INC_CNT1	DPLL Counter for Pulses for TBU_CH1_BASE to be Sent in Automatic End Mode	0280B0 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_INC_CNT2	DPLL Counter for Pulses for TBU_TS2 to be Sent in Automatic End Mode	0280B4 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_APT_SYNC	DPLL Old RAM Pointer and Offset Value for TRIGGER	0280B8 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APS_SYNC	DPLL Old RAM Pointer and Offset Value for STATE	0280BC _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_TBU_TS0_T	DPLL TBU_TS0 Value at Last TRIGGER Event	0280C0 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_TBU_TS0_S	DPLL TBU_TS0 Value at Last STATE Event	0280C4 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ADD_IN_LD1	DPLL Direct Load Input Value for SUB_INC1	0280C8 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ADD_IN_LD2	DPLL Direct Load Input Value for SUB_INC2	0280CC _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_STAT_US	DPLL Status Register	0280FC _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ID_P_MTR_z (z=0-31)	DPLL ID Information for Input Signal PMT z Register	028100 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_0_SHADOW_TRIGGER	DPLL Control 0 Shadow Trigger Register	0281E0 _H	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_CTRL_0_SHADOW_STATE	DPLL Control 0 Shadow STATE Register	0281E4 _H	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_CTRL_1_SHADOW_TRIGGER	DPLL Control 1 Shadow TRIGGER Register	0281E8 _H	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_CTRL_1_SHADOW_STATE	DPLL Control 1 Shadow STATE Register	0281EC _H	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_RAM_INI	DPLL RAM Initialization Register	0281FC _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_PSAi (i=0-31)	DPLL ACTION_i Position/Value Request	028200 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_DLAi (i=0-31)	DPLL ACTION_i Time to React before PSAi	028280 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NAi (i=0-31)	DPLL Calculated Number of TRIGGER/STATE Increments to ACTION_i	028300 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DTAi (i=0-31)	DPLL Calculated Relative TIME to ACTION_i	028380 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_T	DPLL Actual TRIGGER Time Stamp Value	028400 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_T_OLD	DPLL Previous TRIGGER Time Stamp Value	028404 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_FTV_T	DPLL Actual TRIGGER Filter Value	028408 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_S	DPLL Actual STATE Time Stamp	028410 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TS_S_OLD	DPLL Previous STATE Time Stamp	028414 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_FTV_S	DPLL Actual STATE Filter Value	028418 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_THMI	DPLL TRIGGER Hold Time Minimum Value	028420 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_THM_A	DPLL TRIGGER Hold Time Maximum Value	028424 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_THVAL	DPLL Measured TRIGGER Hold Time Value	028428 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TOV	DPLL Time Out Value of Active TRIGGER Slope	028430 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TOV_S	DPLL Time Out Value of Active STATE Slope	028434 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_ADD_IN_CAL1	DPLL Calculated ADD_IN Value for SUB_INC1 Generation	028438 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_ADD_IN_CAL2	DPLL Calculated ADD_IN Value for SUB_INC2 Generation	02843C _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MPV_AL1	DPLL Missing Pulses to be Added or Subtracted Directly 1	028440 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MPV_AL2	DPLL Missing Pulses to be Added or Subtracted Directly 2	028444 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_T_TAR	DPLL Target Number of Pulses to be Sent in Normal Mode	028448 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_T_TAR_OLD	DPLL Last but One Target Number of Pulses to be Sent in Normal Mode	02844C _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_S_TAR	DPLL Target Number of Pulses to be Sent in Emergency Mode	028450 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_S_TAR_OLD	DPLL Last but One Target Number of Pulses to be Sent in Emergency Mode	028454 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCD_T_TX	DPLL Reciprocal Value of the Expected Increment Duration of TRIGGER	028460 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCD_T_SX	DPLL Reciprocal Value of the Expected Increment Duration of STATE	028464 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCD_T_TX_NOM	DPLL Reciprocal Value of the Expected Nominal Increment Duration of TRIGGER	028468 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RCD_T_SX_NOM	DPLL Reciprocal Value of the Expected Nominal Increment Duration of STATE	02846C _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_RDT_T_ACT	DPLL Reciprocal Value of the Last Increment of TRIGGER	028470 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_RDT_S_ACT	DPLL Reciprocal Value of the Last Increment of STATE	028474 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DT_T_ACT	DPLL Duration of the Last TRIGGER Increment	028478 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DT_S_ACT	DPLL Duration of the Last STATE Increment	02847C _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_EDT_T	DPLL Difference of Prediction to Actual Value of the Last TRIGGER Increment	028480 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MED_T_T	DPLL Weighted Difference of Prediction Errors of TRIGGER	028484 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_EDT_S	DPLL Difference of Prediction to Actual Value of the Last STATE Increment	028488 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MED_T_S	DPLL Weighted Difference of Prediction Errors of STATE	02848C _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_TX	DPLL Prediction of the Actual TRIGGER Increment Duration	028490 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_SX	DPLL Prediction of the Actual STATE Increment Duration	028494 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_TX_NOM	DPLL Prediction of the Nominal TRIGGER Increment Duration	028498 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CDT_SX_NOM	DPLL Prediction of the Nominal STATE Increment Duration	02849C _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TLR	DPLL TRIGGER Locking Range	0284A0 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_SLR	DPLL STATE Locking Range	0284A4 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PDT_z (z=0-31)	DPLL Projected Increment Sum Relations for Action z	028500 _H +z*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_MLS1	DPLL Calculated Number of Sub-Pulses between two Nominal STATE Events for SMC = 0	0285C0 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_MLS2	DPLL Calculated Number of Sub-Pulses between two Nominal STATE Events for SMC = 1 and RMO = 1	0285C4 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CNT_NUM_1	DPLL Number of Sub-Pulses of SUB_INC1 in Continuous Mode	0285C8 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_CNT_NUM_2	DPLL Number of Sub-Pulses of SUB_INC2 in Continuous Mode	0285CC _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PVT	DPLL Plausibility Value of Next TRIGGER Slope	0285D0 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSTC	DPLL Actual Calculated Position Stamp of TRIGGER	0285E0 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSSC	DPLL Actual Calculated Position Stamp of STATE	0285E4 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSTM	DPLL Measured Position Stamp at Last TRIGGER Input	0285E8 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSTM_OLD	DPLL Measured Position Stamp at Last but One TRIGGER Input	0285EC _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSSM	DPLL Measured Position Stamp at Last STATE Input	0285F0 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_PSSM_OLD	DPLL Measured Position Stamp at Last but One STATE Input	0285F4 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_T	DPLL Number of Pulses to be Sent in Normal Mode	0285F8 _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_NMB_S	DPLL Number of Pulses to be Sent in Emergency Mode	0285FC _H	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_RDT_Si (i=0-63)	DPLL Reciprocal Values of the Nominal STATE i Increment Duration in FULL_SCALE	028600 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TSF_Si (i=0-63)	DPLL Time Stamp Values of the Nominal STATE i Events in FULL_SCALE	028700 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_ADT_Si (i=0-63)	DPLL Adapt and Profile Values of the STATE i Increments in FULL_SCALE	028800 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_DT_Si (i=0-63)	DPLL Nominal STATE i Increment Duration in FULL_SCALE	028900 _H +i*4	U,SV,32	U,SV,32,P	See Family Spec	See Family Spec
GTM_DPLL_TSACz (z=0-31)	DPLL Calculated Time Value to start Action z Register	028E00 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_PSACz (z=0-31)	DPLL ACTION Position/Value Action z Request Register	028E80 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_ACBz (z=0-7)	DPLL Control Bits Register z for up to 32 Actions	028F00 _H +z*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_11	DPLL Control Register 11	028F20 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_THVAL2	DPLL Immediate THVAL Value Register	028F24 _H	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_TIDEL	DPLL Additional TRIGGER Input Delay Register	028F28 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_SIDE_L	DPLL Additional STATE Input Delay Register	028F2C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APS_SYNC_EXT	DPLL Extension Register for DPLL_APS_SYNC	028F30 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTRL_EXT	DPLL Extension Register for DPLL_CTRL	028F34 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_APS_EXT	DPLL Extension Register for DPLL_APS	028F38 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_APS_1C3_EXT	DPLL Extension Register for DPLL_APS_1C3	028F3C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_STA	DPLL Status of the State Machine States Register	028F40 _H	U,SV,32		Application Reset	See Family Spec
GTM_DPLL_INCF_1_OFFSET	DPLL Start Value of the ADD_IN_ADDER1 Register	028F44 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_INCF_2_OFFSET	DPLL Start Value of the ADD_IN_ADDER2 Register	028F48 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_DT_T_START	DPLL Start Value of DPLL_DT_T_ACT for the First Increment after SIP1 is Set to 1	028F4C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_DT_S_START	DPLL Start Value of DPLL_DT_S_ACT for the First Increment after SIP2 is Set to 1	028F50 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_STA_MASK	DPLL Trigger Masks for Signals DPLL_STA_T and DPLL_STA_S	028F54 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_STA_FLAG	DPLL STA Flag Register	028F58 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_INC_CNT1_MASK	DPLL INC_CNT1 Trigger Mask	028F5C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_INC_CNT2_MASK	DPLL INC_CNT2 Trigger Mask	028F60 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NUSC_EXT1	DPLL Extension Register Number 1 for DPLL_NUSC 4	028F64 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_NUSC_EXT2	DPLL Extension Register Number 2 for DPLL_NUSC 4	028F68 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CTN_MIN	DPLL Minimum CDT_T Nominal Value Register	028F6C _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_DPLL_CTN_MAX	DPLL Maximum CDT_T Nominal Value Register	028F70 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CSN_MIN	DPLL Minimum CDT_S Nominal Value Register	028F74 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_CSN_MAX	DPLL Maximum CDT_S Nominal Value Register	028F78 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_DPLL_RR2	RAM based TRIGGER data (001000 _H Byte)	02C000 _H	U,SV	U,SV		
GTM_MCSi_MEM (i=0-2)	Mapped section of embedded RAM 0 (002000 _H Byte)	038000 _H +i*8000 H	U,SV	U,SV		
GTM_MCSi_MEM 1 (i=0-2)	Mapped section of embedded RAM 1 (001000 _H Byte)	03A000 _H +i*8000 H	U,SV	U,SV		
GTM_CLC	Clock Control Register	09FD00 _H	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_RESET_CLR	Kernel Reset Status Clear Register	09FD04 _H	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_RESET1	Kernel Reset Register 0	09FD08 _H	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_RESET2	Kernel Reset Register 1	09FD0C _H	U,SV	SV,E,P	Application Reset	See Family Spec
GTM_ACCEN0	Access Enable Register 0	09FD10 _H	U,SV	SV,SE	Application Reset	See Family Spec
GTM_ACCEN1	Access Enable Register 1	09FD14 _H	U,SV	SV,SE	Application Reset	See Family Spec
GTM_OTBU0T	OCDS TBU0 Trigger Register	09FD18 _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTBU1T	OCDS TBU1 Trigger Register	09FD1C _H	U,SV	SV,P	Debug Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_OTBU2T	OCDS TBU2 Trigger Register	09FD20 _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTBU3T	OCDS TBU3 Trigger Register	09FD24 _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTSS	OCDS Trigger Set Select Register	09FD28 _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTSC0	OCDS Trigger Set Control 0 Register	09FD2C _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OTSC1	OCDS Trigger Set Control 1 Register	09FD30 _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_ODA	OCDS Debug Access Register	09FD34 _H	U,SV	SV,P	Debug Reset	See Family Spec
GTM_OCS	OCDS Control and Status	09FD38 _H	U,SV	SV,P,OEN	Debug Reset	See Family Spec
GTM_TIMnINSEL (n=0-2)	TIMn Input Select Register	09FD40 _H +n*4	U,SV	U,SV,P	Application Reset	55
GTM_TOUTSELn (n=0-16)	Timer Output Select Register	09FD60 _H +n*4	U,SV	U,SV,P	Application Reset	73
GTM_DSADCINSELi (i=0-2)	DSADC Input Select i Register	09FE00 _H +i*4	U,SV	U,SV,P	Application Reset	185
GTM_DSADCOUTSELi0 (i=0-3)	DSADC Output Select i0 Register	09FE20 _H +i*8	U,SV	U,SV,P	Application Reset	195
GTM_ADCTRIGi0 (i=0-4)	ADC Trigger i Output Select 0 Register	09FE40 _H +i*8	U,SV	U,SV,P	Application Reset	202
GTM_ADCTRIGi0 (i=0-4)	ADC Trigger i Output Select 1 Register	09FE44 _H +i*8	U,SV	U,SV,P	Application Reset	205
GTM_DXOUTCON	Data Exchange Output Control Register	09FE70 _H	U,SV	U,SV,P	Application Reset	49
GTM_TRIGOUTn (n=0-2)	Trigger Output Register n	09FE74 _H +n*4	U,SV	U,SV,P	Application Reset	50

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_INTOUTn (n=0-2)	Interrupt Output Register n	09FE9CH +n*4	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_MCSTRIGOUTSEL	Trigger Output Select Register	09FEC4H	U,SV	U,SV,P	Application Reset	51
GTM_MCSINTSTAT	MCS Interrupt Status Register	09FEC8H	U,SV	U,SV,P	Application Reset	50
GTM_MCSINTCLR	MCS Interrupt Clear Register	09FECC H	U,SV	U,SV,P	Application Reset	51
GTM_DXINCON	Data Exchange Input Control Register	09FED0H	U,SV	U,SV,P	Application Reset	52
GTM_DATAINn (n=0-2)	Data Input n Register	09FED4H +n*4	U,SV	U,SV,P	Application Reset	See Family Spec
GTM_MSCSETiCONj (i=0;j=0-3) (i=1;j=0-3) (i=2;j=0-3) (i=3;j=0-3)	MSC Set i Control j Register	09FF00 _H +i*10 _H +j*4	U,SV	U,SV,P	Application Reset	162
GTM_MSCiINLCON (i=0)	MSCi Input Low Control Register	09FF90 _H	U,SV	U,SV,P	Application Reset	182
GTM_MSCiINHCON (i=0)	MSCi Input High Control Register	09FF94 _H	U,SV	U,SV,P	Application Reset	182
GTM_MSCiINLEXCON (i=0)	MSCi Input Low Extended Control Register	09FF98 _H	U,SV	U,SV,P	Application Reset	183
GTM_PSI5OUTSEL	PSI5 Output Select Register	09FFCCH	U,SV	U,SV,P	Application Reset	222
GTM_PSI5SOUTSEL	PSI5-S Output Select Register	09FFD0H	U,SV	U,SV,P	Application Reset	223
GTM_LCDCDCOUTSEL	LCD CDC Output Select Register	09FFD4H	U,SV	U,SV,P	Application Reset	225
GTM_DTMAUXINSEL	DTM_AUX Input Selection Register	09FFD8H	U,SV	U,SV,P	Application Reset	157
GTM_CANOUTSEL0	CAN0/CAN1 Output Select Register	09FFDC H	U,SV	U,SV,P	Application Reset	218
GTM_CCMi_ARPz_CTRL (i=0-2;z=0-9)	CCMi Address Range Protector z Control Register	0E2000 _H +i*200 _H +z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_CCMi_ARPz_PROT (i=0-2;z=0-9)	CCMi Address Range Protector z Protection Register	0E2004 _H +i*200 _H z*8	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_AEIM_STA (i=0-2)	CCMi MCS Bus Master Status Register	0E21D8 _H +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_HW_CONF (i=0-3)	CCMi Hardware Configuration Register	0E21DC _H +i*200 _H	U,SV,32		Application Reset	See Family Spec
GTM_CCMi_TIM_AUX_IN_SRC (i=0-2)	CCMi TIM Module AUX_IN Source Selection Register	0E21E0 _H +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_EXT_CAP_EN (i=0-2)	CCMi External Capture Trigger Enable Register	0E21E4 _H +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	44 and Family Spec
GTM_CCMi_TOM_OUT (i=0-1)	CCMi TOM Output Level Register	0E21E8 _H +i*200 _H	U,SV,32		Application Reset	45
GTM_CCMi_ATOM_OUT (i=0-3)	CCMi ATOM Output Level Register	0E21ECh +i*200 _H	U,SV,32		Application Reset	See Family Spec
GTM_CCMi_CMU_CLK_CFG (i=0-3)	CCMi CMU Clock Configuration Register	0E21F0 _H +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_CMU_FXCLK_CFG (i=0-3)	CCMi CMU Fixed Clock Configuration Register	0E21F4 _H +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CCMi_CFG (i=0-3)	CCMi Configuration Register	0E21F8 _H +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	38
GTM_CCMi_PROT (i=0-3)	CCMi Protection Register	0E21FCh +i*200 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_CTRL (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Global Configuration and Control Register	0E4000 _H +i*400 _H j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_CH_CTRL1 (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Channel Control Register 1	0E4004 _H +i*400 _H j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_CDTMi_DT Mj_CH_CTRL2 (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Channel Control Register 2	0E4008 _H +i*400 _H + j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_CH_CTRL2_S R (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Channel Control Register 2 Shadow R	0E400C _H +i*400 _H + j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_PS_CTRL (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Phase Shift Unit Configuration and Control Register	0E4010 _H +i*400 _H + j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_CHz_DTV (i=0-1;j=0-1,4- 5;z=0-3) (i=2-3;j=4-5;z=0- 3)	CDTMi DTMj Channel z Dead Time Reload Values	0E4014 _H +i*400 _H + j*40 _H +z* 4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_CH_SR (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Channel Shadow Register	0E4024 _H +i*400 _H + j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_CDTMi_DT Mj_CH_CTRL3 (i=0-1;j=0-1,4-5) (i=2-3;j=4-5)	CDTMi DTMj Channel Control Register 3	0E4028 _H +i*400 _H + j*40 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx _RDADDR (i=0-3;x=0-7)	ATOMi Channel x ARU read address Register	0E8000 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx _CTRL (i=0-3;x=0-7)	ATOMi Channel x Control Register	0E8004 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx _SOMB (i=0-3;x=0-7)	ATOMi Channel x Control Register in SOMB Mode	0E8004 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx _SOMC (i=0-3;x=0-7)	ATOMi Channel x Control Register in SOMC Mode	0E8004 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx _SOMI (i=0-3;x=0-7)	ATOMi Channel x Control Register in SOMI Mode	0E8004 _H +i*800 _H + x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ATOMi_CHx_SOMP (i=0-3;x=0-7)	ATOMi Channel x Control Register in SOMP Mode	0E8004 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SOMS (i=0-3;x=0-7)	ATOMi Channel x Control Register in SOMS Mode	0E8004 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SR0 (i=0-3;x=0-7)	ATOMi Channel x CCU0 Compare Shadow Register	0E8008 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_SR1 (i=0-3;x=0-7)	ATOMi Channel x CCU1 Compare Shadow Register	0E800C _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CM0 (i=0-3;x=0-7)	ATOMi Channel x CCU0 Compare Register	0E8010 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CM1 (i=0-3;x=0-7)	ATOMi Channel x CCU1 Compare Register	0E8014 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_CN0 (i=0-3;x=0-7)	ATOMi Channel x CCU0 Counter Register	0E8018 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_STAT (i=0-3;x=0-7)	ATOMi Channel x Status Register	0E801C _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_NOTIFY (i=0-3;x=0-7)	ATOMi Channel x Interrupt Notification Register	0E8020 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_EN (i=0-3;x=0-7)	ATOMi Channel x Interrupt Enable Register	0E8024 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_FORCINT (i=0-3;x=0-7)	ATOMi Channel x Software Interrupt Generation Register	0E8028 _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_CHx_IRQ_MODE (i=0-3;x=0-7)	ATOMi Channel x Interrupt Mode Configuration Register	0E802C _H +i*800 _H x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_GLB_CTRL (i=0-3)	ATOMi AGC Global Control Register	0E8040 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG_C_ENDIS_CTRL (i=0-3)	ATOMi AGC Enable/Disable Control Register	0E8044 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_ATOMi_AG C_ENDIS_STAT (i=0-3)	ATOMi AGC Enable/Disable Status Register	0E8048 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG C_ACT_TB (i=0-3)	ATOMi AGC Action Time Base Register	0E804C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG C_OUTEN_CTRL (i=0-3)	ATOMi AGC Output Enable Control Register	0E8050 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG C_OUTEN_STAT (i=0-3)	ATOMi AGC Output Enable Status Register	0E8054 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG C_FUPD_CTRL (i=0-3)	ATOMi AGC Force Update Control Register	0E8058 _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_ATOMi_AG C_INT_TRIG (i=0-3)	ATOMi AGC Internal Trigger Control Register	0E805C _H +i*800 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_ Ry (i=0-2;x=0-7;y=0- 7)	MCSi Channel x General Purpose Register y	0F0000 _H +i*1000 H+x*80 _H +y*4	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_ CTRL (i=0-2;x=0-7)	MCSi Channel x Control Register	0F0020 _H +i*1000 H+x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_ ACB (i=0-2;x=0-7)	MCSi Channel x ARU Control Bit Register	0F0024 _H +i*1000 H+x*80 _H	U,SV,32		Application Reset	See Family Spec
GTM_MCSi_CTRG (i=0-2)	MCSi Clear Trigger Control Register	0F0028 _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_STRG (i=0-2)	MCSi Set Trigger Control Register	0F002C _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_ MHB (i=0-2;x=0-7)	MCSi Channel x Memory High Byte Register	0F003C _H +i*1000 H+x*80 _H	U,SV,32		Application Reset	See Family Spec
GTM_MCSi_CHx_ PC (i=0-2;x=0-7)	MCSi Channel x Program Counter Register	0F0040 _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	53
GTM_MCSi_CHx_ IRQ_NOTIFY (i=0-2;x=0-7)	MCSi Channel x Interrupt Notification Register	0F0044 _H +i*1000 H+x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

Table 219 Register Overview - GTM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GTM_MCSi_CHx_IRQ_EN (i=0-2;x=0-7)	MCSi Channel x Interrupt Enable Register	0F0048 _H +i*1000 H+x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_IRQ_FORCINT (i=0-2;x=0-7)	MCSi Channel x Force Interrupt Register	0F004C _H +i*1000 H+x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_IRQ_MODE (i=0-2;x=0-7)	MCSi Channel x Interrupt Mode Configuration Register	0F0050 _H +i*1000 H+x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CHx_EIRQ_EN (i=0-2;x=0-7)	MCSi Channel x Error Interrupt Enable Register	0F0054 _H +i*1000 H+x*80 _H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_REG_PROT (i=0-2)	MCSi Write Protection Register	0F0060 _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CTRL_STAT (i=0-2)	MCSi Control and Status Register	0F0064 _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_RESET (i=0-2)	MCSi Reset Register	0F0068 _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CAT (i=0-2)	MCSi Cancel ARU Transfer Instruction Register	0F006C _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_CWT (i=0-2)	MCSi Cancel WURM Instruction Register	0F0070 _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec
GTM_MCSi_ERR (i=0-2)	MCSi error register	0F007C _H +i*1000 H	U,SV,32	U,SV,32,P	Application Reset	See Family Spec

Generic Timer Module (GTM)

26.3 TC36x Specific Registers

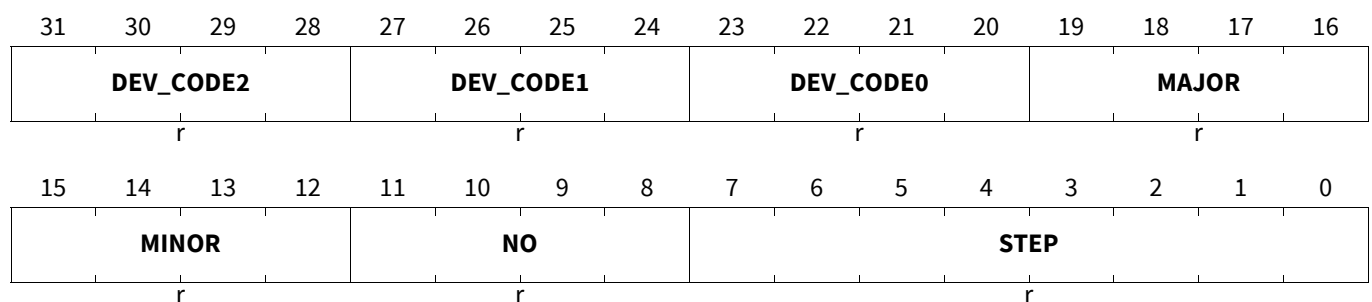
26.3.1 GTM IP Registers Specific Settings

GTM Version Control Register

Note: The numbers are encoded in BCD. Values "A" - "F" are characters.

GTM_REV

GTM Version Control Register (000000_H) Application Reset Value: 3123 15BD_H



Field	Bits	Type	Description
STEP	7:0	r	Release step GTM Release step
NO	11:8	r	Delivery number Define delivery number of GTM specification.
MINOR	15:12	r	Minor version number Define minor version number of GTM specification.
MAJOR	19:16	r	Major version number Define major version number of GTM specification.
DEV_CODE0	23:20	r	Device encoding digit 0 Device encoding digit 0.
DEV_CODE1	27:24	r	Device encoding digit 1 Device encoding digit 1.
DEV_CODE2	31:28	r	Device encoding digit 2 Device encoding digit 2.

GTM Cluster Clock Configuration

Note: For clusters greater than 4 (only MAX 100 MHz capable), the allowed setting for the CLS_CLK_DIV are 00_B and 10_B (clock divider 2). For clusters < 5, 200 MHz is available. In case a device has a single 100 MHz cluster, the ARU will run with 100 MHz.

Note: Writing a value to a bit field CLS[c]_CLK_DIV that is not available in the device, an AEI status 10_B is returned.

Note: The availability of configuration bits is indicated by value of bit CFG_CLOCK_RATE in register CCM[c]_HW_CFG. If CFG_CLOCK_RATE=0, only the values 00_B and 01_B are valid for bit fields CLS[c]_CLK_DIV.

Generic Timer Module (GTM)

GTM_CLS_CLK_CFG

GTM Cluster Clock Configuration

(0000B0_H)

Application Reset Value: 0000 00AA_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			0					0		0		0		0	
			r					r		r		r		r	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	CLS3_CLK_DI	CLS2_CLK_DI	CLS1_CLK_DI	CLS0_CLK_DI				
								V	V	V	V				
r	r	r	r	r	r	r	r	rw	rw	rw	rw				

Field	Bits	Type	Description
CLSc_CLK_DI V (c=0-3)	2*c+1:2*c	rw	Cluster c Clock Divider This bit is only writable if bit field RF_PROT of register GTM_CTRL is cleared. 00 _B Cluster c is disabled 01 _B Cluster c is enabled without clock divider 10 _B Cluster c is enabled with clock divider 11 _B Reserved, do not use.
0	23:22, 21:20, 19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 31:24	r	Reserved Read as zero, shall be written as zero.

Monitor Status Register

The MCS can be programmed to generate an error, when the comparison of signal values (duty time, cycle time) fails or also when the cycle time of the ARU (checking of the TBU_TS0 between two periodic accesses) is out of the expected range.

GTM_MON_STATUS

Monitor Status Register

(000180_H)

Application Reset Value: 0000 4000_H

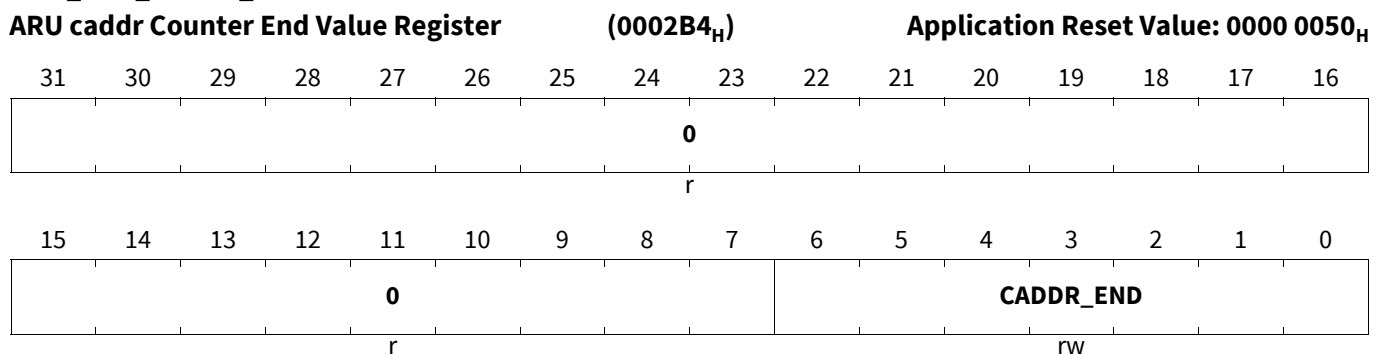
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	MCS2_ERR	MCS1_ERR	MCS0_ERR		0		CMP_ERR
r	r	r	r	r	r	r	r	r	r	r	r		r		r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ACT_C MU8	0	ACT_C MUFX 4	ACT_C MUFX 3	ACT_C MUFX 2	ACT_C MUFX 1	ACT_C MUFX 0	ACT_C MU7	ACT_C MU6	ACT_C MU5	ACT_C MU4	ACT_C MU3	ACT_C MU2	ACT_C MU1	ACT_C MU0
r	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Generic Timer Module (GTM)

Field	Bits	Type	Description
ACT_CMUx (x=0-7)	x	rw	CMU_CLKx activity This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged. Bits is set, when a rising edge is detected at the considered clock.
ACT_CMUFx (x=0-4)	x+8	rw	CMU_CLKFx activity This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged. Bits is set, when a rising edge is detected at the considered clock.
ACT_CMU8	14	rw	CMU_CLK8 activity This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged. Bit is set, when a rising edge is detected at the considered clock.
CMP_ERR	16	r	Error detected at CMP This bit will be readable only. Bits is set, when the corresponding unit reports an error.
MCSx_ERR (x=0-2)	x+20	r	Error detected at MCSx This bit will be readable only. Bits is set, when the corresponding unit reports an error.
0	13, 15, 19:17, 29, 28, 27, 26, 25, 24, 23, 31:30	r	Reserved Read as zero, shall be written as zero.

ARU caddr Counter End Value Register

GTM_ARU_CADDR_END



Generic Timer Module (GTM)

Field	Bits	Type	Description
CADDR_END	6:0	rw	<p>Set end value of ARU caddr counter</p> <p>The ARU roundtrip counter aru_caddr runs from zero to caddr_end value.</p> <p>Shorten the ARU roundtrip cycle by setting a smaller number than the defined reset value will cause that not all ARU-connected modules will be served.</p> <p>Making the roundtrip cycle longer than the reset value would cause longer ARU roundtrip time and as a result some ARU-connected modules will not be served as fast as possible for this device.</p> <p>This bit is write protected by bit RF_PROT of register GTM_CTRL</p>
0	31:7	r	<p>Reserved</p> <p>Read as zero, shall be written as zero.</p>

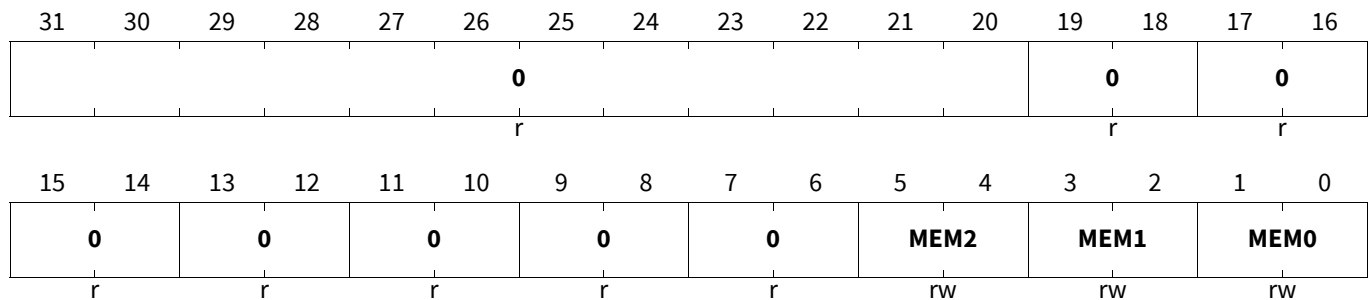
MCFG Memory Layout Configuration Register

This register is only writable if the bit **RF_PROT** in register **GTM_CTRL** is cleared.

GTM_MCFG_CTRL

MCFG Memory Layout Configuration Register (000F40_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
MEMx (x=0-2)	2*x+1:2*x	rw	<p>Configure Memory pages for MCS-instance MCSx</p> <p>00_B DEFAULT configuration</p> <p>01_B SWAP configuration</p> <p>10_B BORROW configuration</p> <p>11_B Reserved, do not use.</p>
0	19:18, 17:16, 15:14, 13:12, 11:10, 9:8, 7:6, 31:20	r	<p>Reserved</p> <p>Read as zero, shall be written as zero.</p>

CCMi Configuration Register

NOTE: The module specific clock enable registers (bit field **EN_***) are only implemented if the corresponding module is available in the i-th cluster.

Generic Timer Module (GTM)

NOTE: For the Clusters greater than 4, (only 100MHz capable), the only allowed settings for the CLS_CLK_DIV are 00 and 10 (clock divider 2).

GTM_CCMi_CFG (i=0)

CCMi Configuration Register

(0E21F8_H+i*200_H)

Application Reset Value: 0002 007F_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
TBU_D IR2	TBU_D IR1	0												CLS_CLK_DIV		
r	r	r												r		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0							0	EN_PS M	EN_BR C	EN_DP LL_MA P	EN_M CS	EN_AT OM_A DTM	EN_TO M_SPE _TDT M	EN_TI M		
r							r	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EN_TIM	0	rw	Enable TIM This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for sub module TIM 1 _B Enable clock signal for sub module TIM
EN_TOM_SPE_TDTM	1	rw	Enable TOM, SPE and TDTM This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for modules TOM, SPE, and their related DTM modules 1 _B Enable clock signal for modules TOM, SPE, and their related DTM modules.
EN_ATOM_AD TM	2	rw	Enable ATOM and ADTM This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for modules ATOM and their related DTM modules. 1 _B Enable clock signal for modules ATOM and their related DTM modules.
EN_MCS	3	rw	Enable MCS This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for module MCS 1 _B Enable clock signal for module MCS
EN_DPLL_MA P	4	rw	Enable DPLL and MAP This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for modules DPLL and MAP 1 _B Enable clock signal for modules DPLL and MAP

Generic Timer Module (GTM)

Field	Bits	Type	Description
EN_TIM	0	rw	<p>Enable TIM</p> <p>This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared.</p> <p>0_B Disable clock signal for sub module TIM</p> <p>1_B Enable clock signal for sub module TIM</p>
EN_TOM_SPE_TDTM	1	rw	<p>Enable TOM, SPE and TDTM</p> <p>This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared.</p> <p>0_B Disable clock signal for modules TOM, SPE, and their related DTM modules</p> <p>1_B Enable clock signal for modules TOM, SPE, and their related DTM modules.</p>
EN_ATOM_AD_TM	2	rw	<p>Enable ATOM and ADTM</p> <p>This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared.</p> <p>0_B Disable clock signal for modules ATOM and their related DTM modules.</p> <p>1_B Enable clock signal for modules ATOM and their related DTM modules.</p>
EN_MCS	3	rw	<p>Enable MCS</p> <p>This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared.</p> <p>0_B Disable clock signal for module MCS</p> <p>1_B Enable clock signal for module MCS</p>
EN_CMP_MON	7	rw	<p>Enable CMP and MON</p> <p>This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared.</p> <p>0_B Disable clock signal for modules CMP and MON</p> <p>1_B Enable clock signal for modules CMP and MON</p>
CLS_CLK_DIV	17:16	r	<p>Cluster Clock Divider</p> <p>The value of this bit field mirrors the bit field CLS[i]_CLK_DIV of register GTM_CLS_CLK_CFG, whereas i equals the cluster index.</p> <p>00_B Cluster is disabled</p> <p>01_B Cluster is enabled without clock divider</p> <p>10_B Cluster is enabled with clock divider 2</p> <p>11_B Reserved, do not use.</p>
TBU_DIR1	30	r	<p>DIR1 input signal of module TBU</p> <p>0_B Indicating forward direction</p> <p>1_B Indicating backward direction</p>
TBU_DIR2	31	r	<p>DIR2 input signal of module TBU</p> <p>0_B Indicating forward direction</p> <p>1_B Indicating backward direction</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
0	4, 5, 6, 15:8, 29:18	r	Reserved Read as zero, shall be written as zero.

GTM_CCMi_CFG (i=2)

CCMi Configuration Register

(0E21F8_H+i*200_H)

Application Reset Value: 0002 000D_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBU_D IR2	TBU_D IR1						0								CLS_CLK_DIV
r	r						r								r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			0					0	0	0	0	EN_M CS	EN_ATOM_A DTM	0	EN_T M
			r					r	r	r	r	rw	rw	r	rw

Field	Bits	Type	Description
EN_TIM	0	rw	Enable TIM This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for sub module TIM 1 _B Enable clock signal for sub module TIM
EN_ATOM_AD TM	2	rw	Enable ATOM and ADTM This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for modules ATOM and their related DTM modules. 1 _B Enable clock signal for modules ATOM and their related DTM modules.
EN_MCS	3	rw	Enable MCS This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for module MCS 1 _B Enable clock signal for module MCS
CLS_CLK_DIV	17:16	r	Cluster Clock Divider The value of this bit field mirrors the bit field CLS[i]_CLK_DIV of register GTM_CLS_CLK_CFG , whereas i equals the cluster index. 00 _B Cluster is disabled 01 _B Cluster is enabled without clock divider 10 _B Cluster is enabled with clock divider 2 11 _B Reserved, do not use.

Generic Timer Module (GTM)

Field	Bits	Type	Description
TBU_DIR1	30	r	DIR1 input signal of module TBU 0 _B Indicating forward direction 1 _B Indicating backward direction
TBU_DIR2	31	r	DIR2 input signal of module TBU 0 _B Indicating forward direction 1 _B Indicating backward direction
0	1, 4, 5, 6, 7, 15:8, 29:18	r	Reserved Read as zero, shall be written as zero.

GTM_CCMi_CFG (i=3)

CCMi Configuration Register

(0E21F8_H+i*200_H)

Application Reset Value: 0002 0004_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
TBU_D IR2	TBU_D IR1	0										CLS_CLK_DIV							
r	r	r										r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0											0	0	0	0	0	0	EN_ATOM_A DTM	0	0
r											r	r	r	r	r	r	rw	r	r

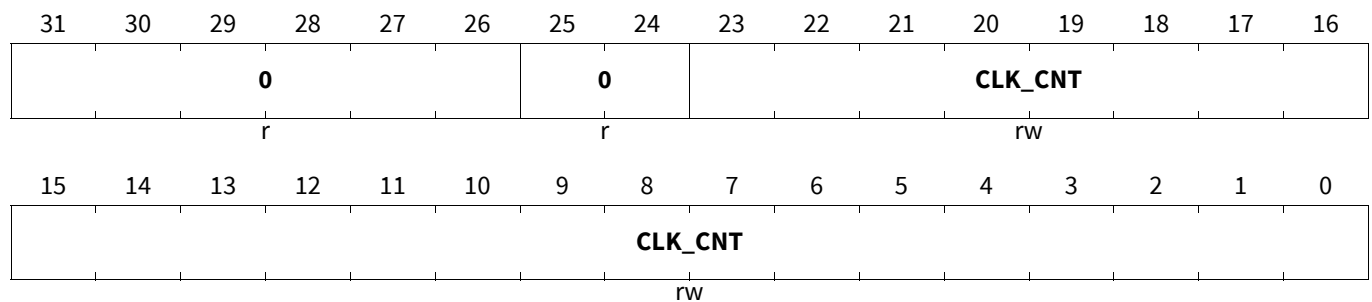
Field	Bits	Type	Description
EN_ATOM_ADTM	2	rw	Enable ATOM and ADTM This bit is only writable if bit field CLS_PROT of register CCM[i]_PROT is cleared. 0 _B Disable clock signal for modules ATOM and their related DTM modules. 1 _B Enable clock signal for modules ATOM and their related DTM modules.
CLS_CLK_DIV	17:16	r	Cluster Clock Divider The value of this bit field mirrors the bit field CLS[i]_CLK_DIV of register GTM_CLS_CLK_CFG , whereas i equals the cluster index. 00 _B Cluster is disabled 01 _B Cluster is enabled without clock divider 10 _B Cluster is enabled with clock divider 2 11 _B Reserved, do not use.
TBU_DIR1	30	r	DIR1 input signal of module TBU 0 _B Indicating forward direction 1 _B Indicating backward direction

Generic Timer Module (GTM)

CMU Control for Clock Source z

GTM_CMU_CLK_z_CTRL (z=0-5)

CMU Control for Clock Source z (00030C_H+z*4) Application Reset Value: 0000 0000_H

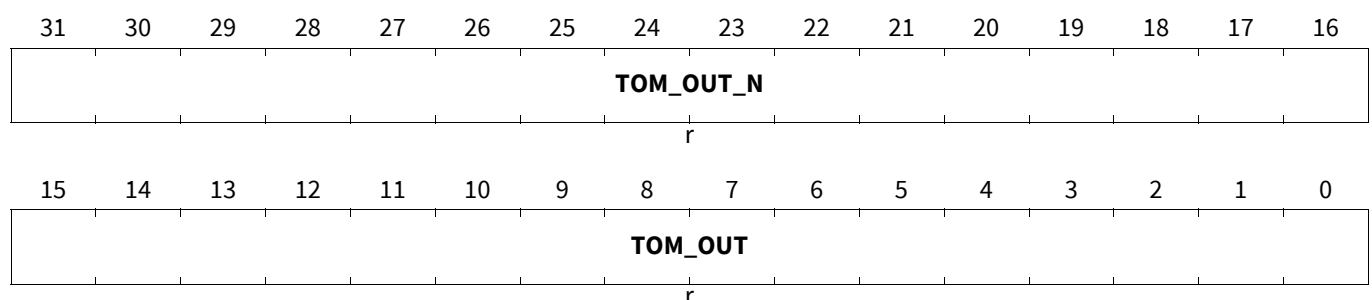


Field	Bits	Type	Description
CLK_CNT	23:0	rw	Clock count Defines count value for the clock divider. Value can only be modified when clock enable EN_CLKz and EN_ECLK1 are disabled.
0	25:24, 31:26	r	Reserved Read as zero, shall be written as zero.

CCMi TOM Output Level Register

GTM_CCMi_TOM_OUT (i=0-1)

CCMi TOM Output Level Register (0E21E8_H+i*200_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
TOM_OUT	15:0	r	Output level snapshot of TOM[i]_OUT all channels
TOM_OUT_N	31:16	r	Output level snapshot of TOM[i]_OUT_N all channels

Generic Timer Module (GTM)

GTM TIM i Module AUX_IN Source Selection Register

GTM_TIMi_AUX_IN_SRC (i=0-2)

GTM TIM i Module AUX_IN Source Selection Register(000040_H+i*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SEL_O UT_N_ CH7	SEL_O UT_N_ CH6	SEL_O UT_N_ CH5	SEL_O UT_N_ CH4	SEL_O UT_N_ CH3	SEL_O UT_N_ CH2	SEL_O UT_N_ CH1	SEL_O UT_N_ CH0
r								rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SRC_C H7	SRC_C H6	SRC_C H5	SRC_C H4	SRC_C H3	SRC_C H2	SRC_C H1	SRC_C H0
r								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SRC_CH0	0	rw	Defines AUX_IN source of TIM[i] channel 0 SEL_OUT_N_CH0 / SEL_OUT_N_CH0 = 1: 0 _B CDTM[i].DTM0 output DTM_OUT0 selected / CDTM[i].DTM0 output DTM_OUT1_N selected 1 _B CDTM[i].DTM4 output DTM_OUT0 selected / CDTM[i].DTM4 output DTM_OUT1_N selected
SRC_CH1	1	rw	Defines AUX_IN source of TIM[i] channel 1 SEL_OUT_N_CH1 = 0 / SEL_OUT_N_CH1 = 1: 0 _B CDTM[i].DTM0 output DTM_OUT1 selected / CDTM[i].DTM0 output DTM_OUT2_N selected 1 _B CDTM[i].DTM4 output DTM_OUT1 selected / CDTM[i].DTM4 output DTM_OUT2_N selected
SRC_CH2	2	rw	Defines AUX_IN source of TIM[i] channel 2 SEL_OUT_N_CH2 = 0 / SEL_OUT_N_CH2 = 1: 0 _B CDTM[i].DTM0 output DTM_OUT2 selected / CDTM[i].DTM0 output DTM_OUT3_N selected 1 _B CDTM[i].DTM4 output DTM_OUT2 selected / CDTM[i].DTM4 output DTM_OUT3_N selected
SRC_CH3	3	rw	Defines AUX_IN source of TIM[i] channel 3 SEL_OUT_N_CH3 = 0 / SEL_OUT_N_CH3 = 1: 0 _B CDTM[i].DTM0 output DTM_OUT3 selected / CDTM[i].DTM1 output DTM_OUT0_N selected 1 _B CDTM[i].DTM4 output DTM_OUT3 selected / CDTM[i].DTM5 output DTM_OUT0_N selected
SRC_CH4	4	rw	Defines AUX_IN source of TIM[i] channel 4 SEL_OUT_N_CH4 = 0 / SEL_OUT_N_CH4 = 1: 0 _B CDTM[i].DTM1 output DTM_OUT0 selected / CDTM[i].DTM1 output DTM_OUT1_N selected 1 _B CDTM[i].DTM5 output DTM_OUT0 selected / CDTM[i].DTM5 output DTM_OUT1_N selected

Generic Timer Module (GTM)

Field	Bits	Type	Description
SRC_CH5	5	rw	Defines AUX_IN source of TIM[i] channel 5 SEL_OUT_N_CH5 = 0 / SEL_OUT_N_CH5 = 1: 0 _B CDTM[i].DTM1 output DTM_OUT1 selected / CDTM[i].DTM1 output DTM_OUT2_N selected 1 _B CDTM[i].DTM5 output DTM_OUT1 selected / CDTM[i].DTM5 output DTM_OUT2_N selected
SRC_CH6	6	rw	Defines AUX_IN source of TIM[i] channel 6 SEL_OUT_N_CH6 = 0 / SEL_OUT_N_CH6 = 1: 0 _B CDTM[i].DTM1 output DTM_OUT2 selected / CDTM[i].DTM1 output DTM_OUT3_N selected 1 _B CDTM[i].DTM5 output DTM_OUT2 selected / CDTM[i].DTM5 output DTM_OUT3_N selected
SRC_CH7	7	rw	Defines AUX_IN source of TIM[i] channel 7 SEL_OUT_N_CH7 = 0 / SEL_OUT_N_CH7 = 1: 0 _B CDTM[i].DTM1 output DTM_OUT3 selected / CDTM[i].DTM0 output DTM_OUT0_N selected 1 _B CDTM[i].DTM5 output DTM_OUT3 selected / CDTM[i].DTM4 output DTM_OUT0_N selected
SEL_OUT_N_CH0	16	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 0 0 _B Use DTM_OUT signal as AUX_IN source of TIM[i] 1 _B Use DTM_OUT_N signal as AUX_IN source of TIM[i]
SEL_OUT_N_CH1	17	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 1
SEL_OUT_N_CH2	18	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 2
SEL_OUT_N_CH3	19	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 3
SEL_OUT_N_CH4	20	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 4
SEL_OUT_N_CH5	21	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 5
SEL_OUT_N_CH6	22	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 6
SEL_OUT_N_CH7	23	rw	Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel 7
0	15:8, 31:24	r	Reserved Read as zero, shall be written as zero.

Generic Timer Module (GTM)

ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm

GTM_ICM_IRQG_CLS_k_MEI (k=0)

ICM Interrupt Group k for Module Error Interrupt Information for each TIMm, MCSm, SPEm, FIFOm

(000710_H)

Application Reset Value: 0000 0000_H

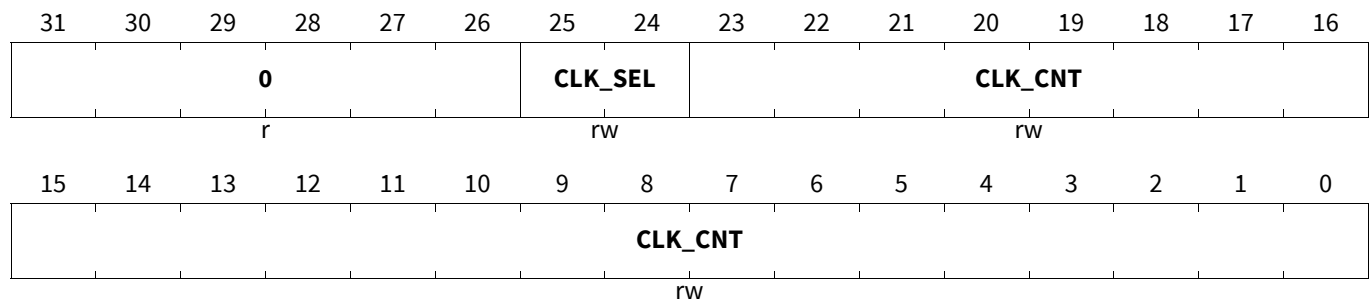
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0			0	0	0	0			0		0	0	MCS_M2_EIRQ	TIM_M2_EIRQ
	r			r	r	r	r			r		r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0			0	SPE_M1_EIRQ	MCS_M1_EIRQ	TIM_M1_EIRQ			0		FIFO_M0_EIRQ	SPE_M0_EIRQ	MCS_M0_EIRQ	TIM_M0_EIRQ
	r			r	r	r	r			r		r	r	r	r

Field	Bits	Type	Description
TIM_Mj_EIRQ (j=0-2)	8*j	r	Error interrupt TIMm_EIRQ (m=4*0+j) This bit is only set when the error interrupt is enabled in the error interrupt enable register of the corresponding sub-module. 0 _B No error interrupt occurred 1 _B Error interrupt was raised by the corresponding sub-module
MCS_Mj_EIRQ (j=0-2)	8*j+1	r	Error interrupt MCSm_EIRQ (m=4*0+j) Coding see bit 0.
SPE_Mj_EIRQ (j=0-1)	8*j+2	r	Error interrupt SPEm_EIRQ (m=4*0+j) Coding see bit 0.
FIFO_Mj_EIRQ (j=0)	8*j+3	r	Error interrupt FIFOm_EIRQ (m=4*0+j) Coding see bit 0.
0	24, 25, 26, 18, 27, 19, 11, 31:28, 23:20, 15:12, 7:4	r	Reserved Read as zero, shall be written as zero.

Generic Timer Module (GTM)

GTM_CMU_CLK_z_CTRL (z=6)

CMU Control for Clock Source z (00030C_H+z*4) Application Reset Value: 0000 0000_H

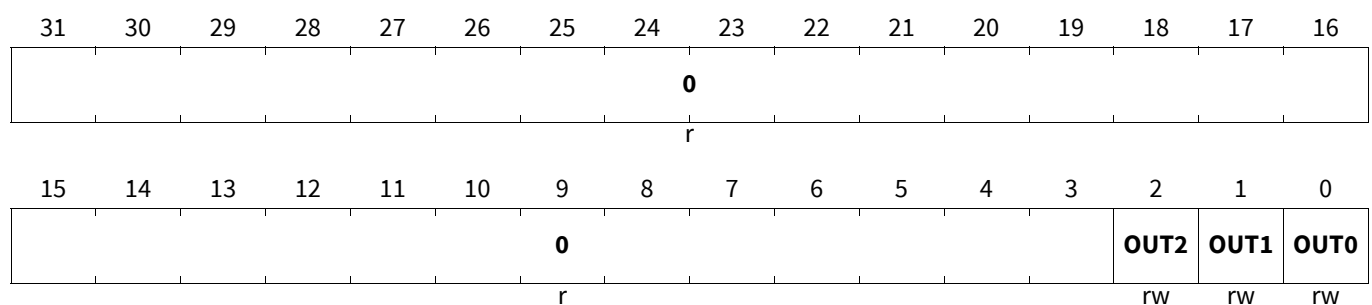


Field	Bits	Type	Description
CLK_CNT	23:0	rw	Clock count Defines count value for the clock divider. Value can only be modified when clock enable EN_CLKz and EN_ECLK1 are disabled.
CLK_SEL	25:24	rw	Clock source selection for CMU_CLKz Value can only be modified when clock enable EN_CLKz and EN_ECLK1 are disabled. <i>Note: The existence and interpretation of this bit field depends on z. z>5</i> 00 _B Use Clock Source 6 Divider 01 _B Use signal SUB_INC2 of module DPLL / If no DPLL: Reserved, do not use. 10 _B Use signal SUB_INC1c of module DPLL / If no DPLL: Reserved, do not use 11 _B Use signal CCM0_CMU_CLK6 of sub-module CCM0
0	31:26	r	Reserved Read as zero, shall be written as zero.

Data Exchange Output Control Register

GTM_DXOUTCON

Data Exchange Output Control Register (09FE70_H) Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
OUTx (x=0-2)	x	rw	Output 0x Control This bit defines whether register TRIGOUTx/INTOUTx is accessible from the MCS instead of RAM0 or not. 0 _B RAM0 memory is accessed 1 _B Register TRIGOUTx/INTOUTx is accessed
0	31:3	r	Reserved Read as 0, shall be written with 0.

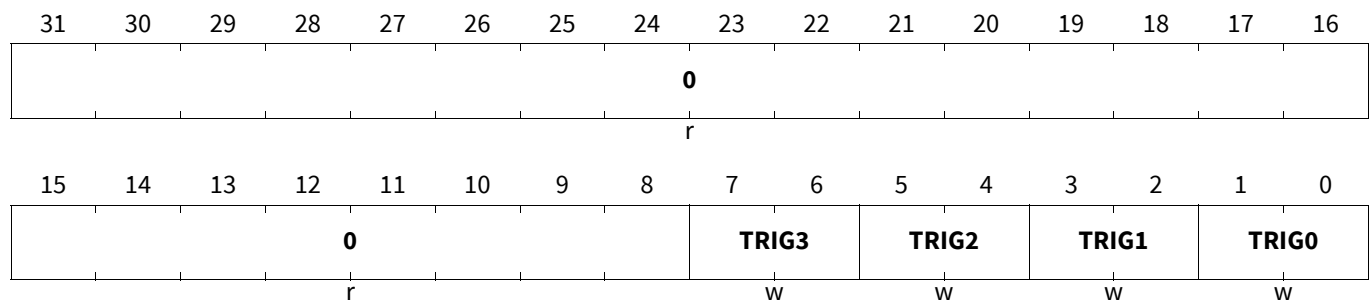
Trigger Output Register n

GTM_TRIGOUTn (n=0-2)

Trigger Output Register n

(09FE74_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
TRIGx (x=0-3)	2*x+1:2*x	w	Trigger x This bit field defines whether a trigger x request is generated or not. In case of read, the value 0x00000000 is returned. 00 _B No modification of current state 01 _B Pending trigger x is cleared 10 _B Trigger x is set 11 _B No modification of current state
0	31:8	r	Reserved Read as 0, shall be written with 0.

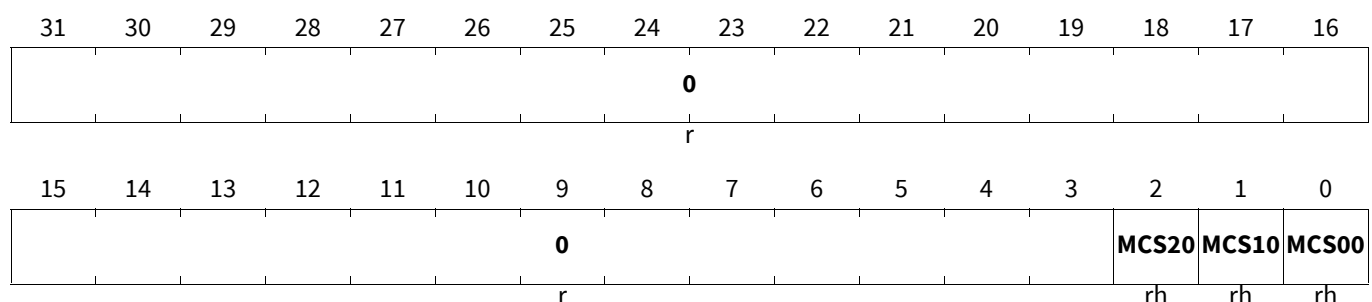
MCS Interrupt Status Register

GTM_MCSINTSTAT

MCS Interrupt Status Register

(09FEC8_H)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
MCSn0 (n=0-2)	n	rh	MCSn RAM0 Interrupt 0 Status Flag The requested interrupt is SRC_GTMMCSWn0. This bit is cleared when bit MCSINTCLR.MCSn is set. 0 _B No interrupt was requested 1 _B An interrupt was requested
0	31:3	r	Reserved Read as 0, shall be written with 0.

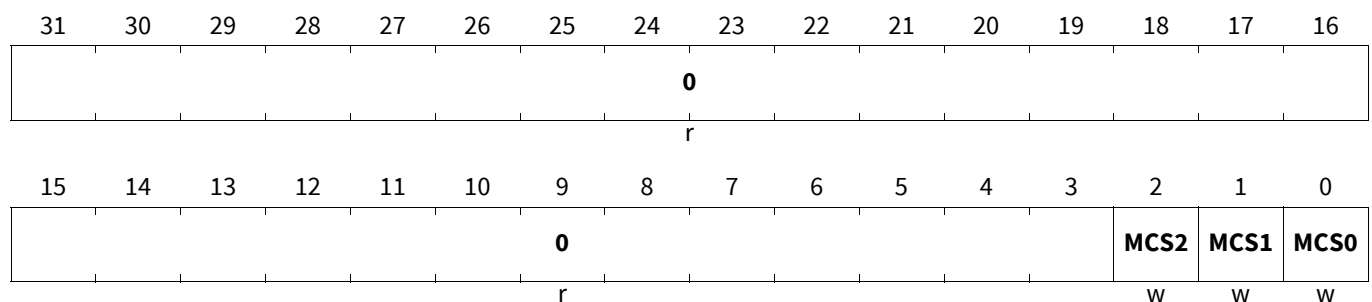
MCS Interrupt Clear Register

GTM_MCSINTCLR

MCS Interrupt Clear Register

(09FECC_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
MCSx (x=0-2)	x	w	MCSn RAM0 Interrupt 0 Status Clear Bit This bit is always read as zero. 0 _B No action 1 _B Bit MCSINTSTAT.MCSn0 is cleared
0	31:3	r	Reserved Read as 0, shall be written with 0.

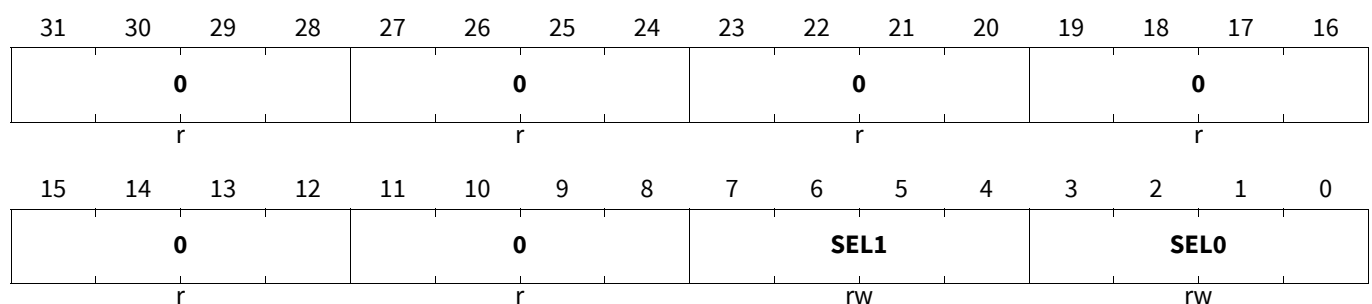
Trigger Output Select Register

GTM_MCSTRIGOUTSEL

Trigger Output Select Register

(09FEC4_H)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELk (k=0)	4*k+3:4*k	rw	Selects which MCS triggers go to FCKBFDAT/SEL 0 _H TRG0_01 , TRIGOUT0_TRIG0/1 1 _H TRG1_01 , TRIGOUT1_TRIG0/1 2 _H TRG2_01 , TRIGOUT2_TRIG0/1 3 _H TRG3_01 , TRIGOUT3_TRIG0/1 4 _H TRG4_01 , TRIGOUT4_TRIG0/1 5 _H Reserved, do not use ... F _H Reserved, do not use
SELk (k=1)	4*k+3:4*k	rw	Selects which MCS triggers go to FCKBFDAT/SEL 0 _H TRG0_23 , TRIGOUT0_TRIG2/3 1 _H TRG1_23 , TRIGOUT1_TRIG2/3 2 _H TRG2_23 , TRIGOUT2_TRIG2/3 3 _H TRG3_23 , TRIGOUT3_TRIG2/3 4 _H TRG4_23 , TRIGOUT4_TRIG2/3 5 _H Reserved, do not use ... F _H Reserved, do not use
0	31:28, 27:24, 23:20, 19:16, 15:12, 11:8	r	Reserved Read as 0, shall be written with 0.

Data Exchange Input Control Register

GTM_DXINCON

Data Exchange Input Control Register (09FED0_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												DSS2	DSS1	DSS0	
r												rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												IN2	IN1	IN0	
r												rw	rw	rw	

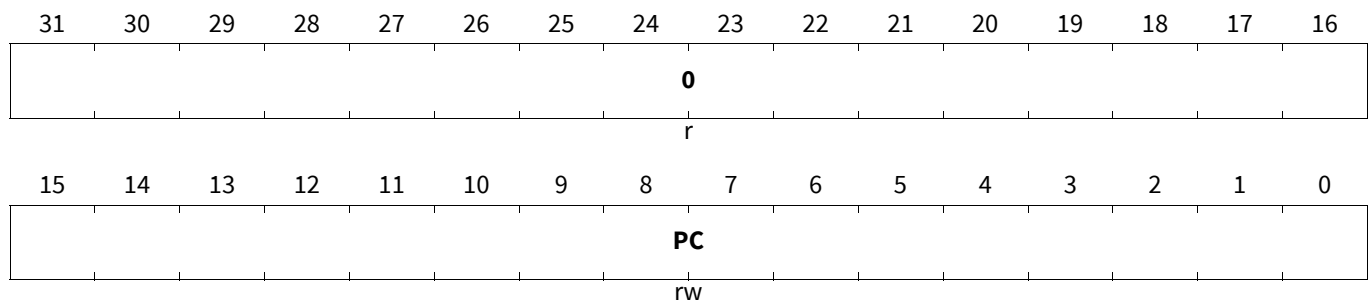
Field	Bits	Type	Description
INx (x=0-2)	x	rw	Input 0x Control This bit defines whether register DATAINx is read from the MCS instead of RAM0 or not. 0 _B RAM0 memory is read 1 _B Register DATAINx is read

Generic Timer Module (GTM)

Field	Bits	Type	Description
DSSx (x=0-2)	x+16	rw	Data Source Select 0x Control This bit defines whether the 12 LSB of the read operation directed to register DATAIN0x deliver the register content or the state of 12 inputs. 0 _B Register DATAINx[11:0] is read 1 _B MCS_STATx[11:0] is read
0	15:3, 31:19	r	Reserved Read as 0, shall be written with 0.

MCS0 Channel 0 Program Counter Register

- GTM_MCSi_CH0_PC (i=0-2)
MCSi Channel 0 Program Counter Register(0F0040_H+i*1000_H) Application Reset Value: 0000 0000_H
- GTM_MCSi_CH1_PC (i=0-2)
MCSi Channel 1 Program Counter Register(0F0040_H+i*1000_H+80_H) Application Reset Value: 0000 0004_H
- GTM_MCSi_CH2_PC (i=0-2)
MCSi Channel 2 Program Counter Register(0F0040_H+i*1000_H+100_H) Application Reset Value: 0000 0008_H
- GTM_MCSi_CH3_PC (i=0-2)
MCSi Channel 3 Program Counter Register(0F0040_H+i*1000_H+180_H) Application Reset Value: 0000 000C_H
- GTM_MCSi_CH4_PC (i=0-2)
MCSi Channel 4 Program Counter Register(0F0040_H+i*1000_H+200_H) Application Reset Value: 0000 0010_H
- GTM_MCSi_CH5_PC (i=0-2)
MCSi Channel 5 Program Counter Register(0F0040_H+i*1000_H+280_H) Application Reset Value: 0000 0014_H
- GTM_MCSi_CH6_PC (i=0-2)
MCSi Channel 6 Program Counter Register(0F0040_H+i*1000_H+300_H) Application Reset Value: 0000 0018_H
- GTM_MCSi_CH7_PC (i=0-2)
MCSi Channel 7 Program Counter Register(0F0040_H+i*1000_H+380_H) Application Reset Value: 0000 001C_H



Field	Bits	Type	Description
PC	15:0	rw	Current Program Counter <i>Note: The program counter is only writable if the corresponding MCS-channel is disabled. The bits 0 and 1 are always written as zeros.</i> <i>Note: The actual width of the program counter depends on the MCS configuration. The actual width is RAW+USR+2 bits meaning that only the bits 0 to RAW+USR+1 are available and the other bits (RAW+USR+2 to 31) are reserved.</i>
0	31:16	r	Reserved Read as zero, shall be written as zero.

Generic Timer Module (GTM)

26.3.2 Port to GTM TIM Connections

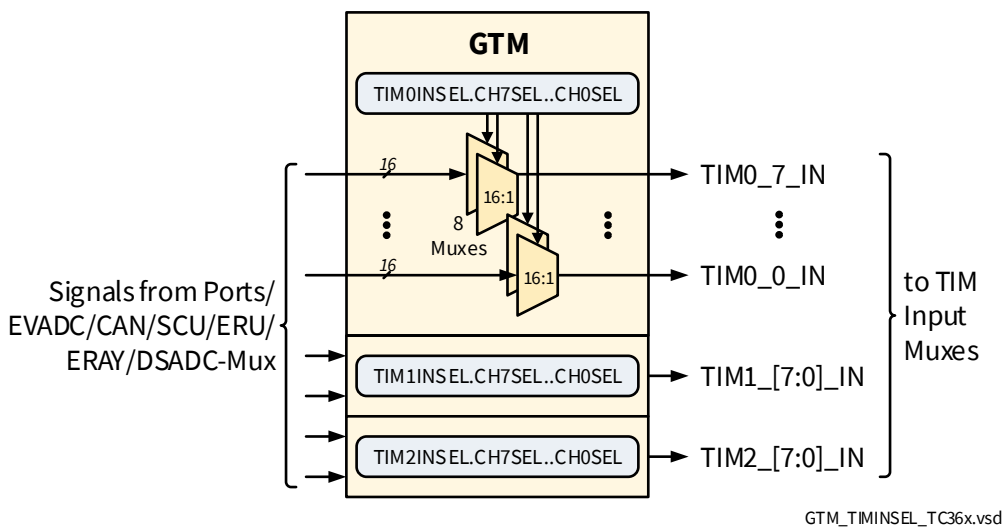


Figure 6 Port to GTM TIM Connections Overview

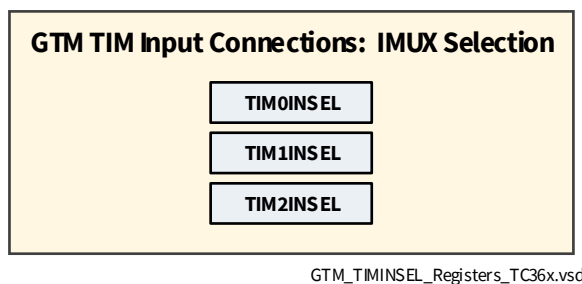


Figure 7 Port to GTM TIM Connections Registers Overview

Table 220 Port to GTM TIM Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
TIM0INSEL	TIM0 Input Select Register (n=0)	CH0SEL..CH7SEL	Page 55
TIM1INSEL	TIM1 Input Select Register (n=1)	CH0SEL..CH7SEL	Page 59
TIM2INSEL	TIM2 Input Select Register (n=2)	CH0SEL..CH7SEL	Page 63
TIMi_CHx_CTRL	TIMi Channel x Control Register (i=1-2;x=0-7)		Page 68

Generic Timer Module (GTM)

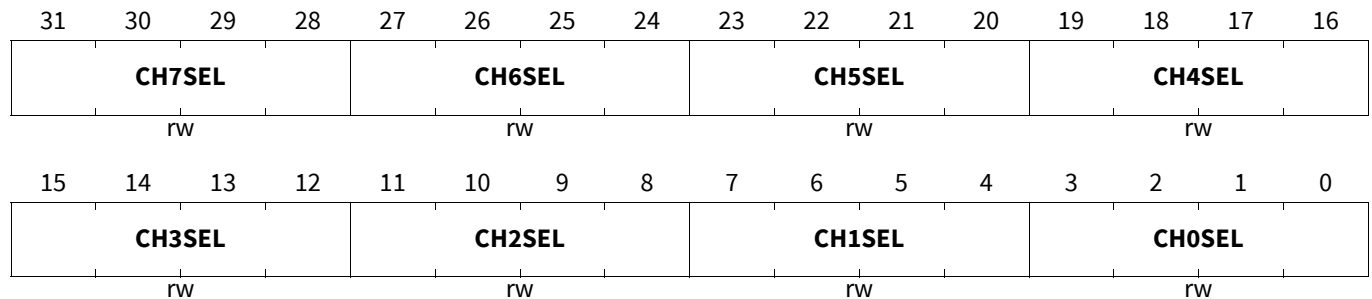
TIMn Input Select Register

GTM_TIMnINSEL (n=0)

TIMn Input Select Register

(09FD40_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H FC0BFL, EVADC boundary flag level of FC channel 0</p> <p>1_H P00.9, Port pad input</p> <p>2_H P02.0, Port pad input</p> <p>3_H P10.7, Port pad input (no TQFP144/LQFP144)</p> <p>4_H P14.5, Port pad input</p> <p>5_H P14.7, Port pad input (no TQFP144/LQFP144)</p> <p>6_H P15.6, Port pad input</p> <p>7_H P21.2, Port pad input</p> <p>8_H P22.1, Port pad input</p> <p>9_H P33.10, Port pad input</p> <p>A_H P33.4, Port pad input</p> <p>B_H Reserved, do not use</p> <p>C_H PDOUT0, SCU/ERU pattern detection output 0</p> <p>D_H Reserved, do not use</p> <p>E_H IMUX0_0, DSADC input IMUX0_OUT0</p> <p>F_H COSR0, EVADC service request 0 of common block 0</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=1)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H FC1BFL, EVADC boundary flag level of FC channel 1 1_H P00.10, Port pad input (no TQFP144/LQFP144) 2_H P02.1, Port pad input 3_H P10.1, Port pad input 4_H P14.6, Port pad input 5_H P15.7, Port pad input 6_H P21.3, Port pad input 7_H P22.0, Port pad input 8_H P33.5, Port pad input 9_H P33.9, Port pad input A_H Reserved, do not use B_H Reserved, do not use C_H PDOUT1, SCU/ERU pattern detection output 1 D_H INT_O12, CAN interrupt output INT_O12 E_H IMUX0_1, DSADC input IMUX0_OUT1 F_H C1SR0, EVADC service request 0 of common block 1</p>
CHxSEL (x=2)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.11, Port pad input (no TQFP144/LQFP144) 2_H P02.2, Port pad input 3_H P10.2, Port pad input 4_H P10.5, Port pad input 5_H P15.8, Port pad input 6_H P21.4, Port pad input 7_H P23.5, Port pad input (no TQFP144/LQFP144) 8_H P33.11, Port pad input 9_H P33.6, Port pad input A_H Reserved, do not use B_H Reserved, do not use C_H PDOUT2, SCU/ERU pattern detection output 2 D_H INT_O13, CAN interrupt output INT_O13 E_H IMUX0_2, DSADC input IMUX0_OUT2 F_H COSR1, EVADC service request 1 of common block 0</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=3)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.12, Port pad input 2_H P02.3, Port pad input 3_H P10.3, Port pad input 4_H P10.6, Port pad input 5_H P14.0, Port pad input 6_H P21.5, Port pad input 7_H P22.2, Port pad input 8_H P32.2, Port pad input (no TQFP144/LQFP144) 9_H P33.7, Port pad input A_H Reserved, do not use B_H Reserved, do not use C_H PDOUT3, SCU/ERU pattern detection output 3 D_H INT_O14, CAN interrupt output INT_O14 E_H IMUX0_3, DSADC input IMUX0_OUT3 F_H C1SR1, EVADC service request 1 of common block 1</p>
CHxSEL (x=4)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.4, Port pad input 2_H P10.0, Port pad input (no TQFP144/LQFP144) 3_H P14.1, Port pad input 4_H P22.3, Port pad input 5_H P32.3, Port pad input (no TQFP144/LQFP144) 6_H P33.0, Port pad input (no TQFP144/LQFP144) 7_H P33.8, Port pad input 8_H P21.6, Port pad input 9_H Reserved, do not use ... B_H Reserved, do not use C_H PDOUT4, SCU/ERU pattern detection output 4 D_H INT_O15, CAN interrupt output INT_O15 E_H IMUX0_4, DSADC input IMUX0_OUT4 F_H COSR2, EVADC service request 2 of common block 0</p>

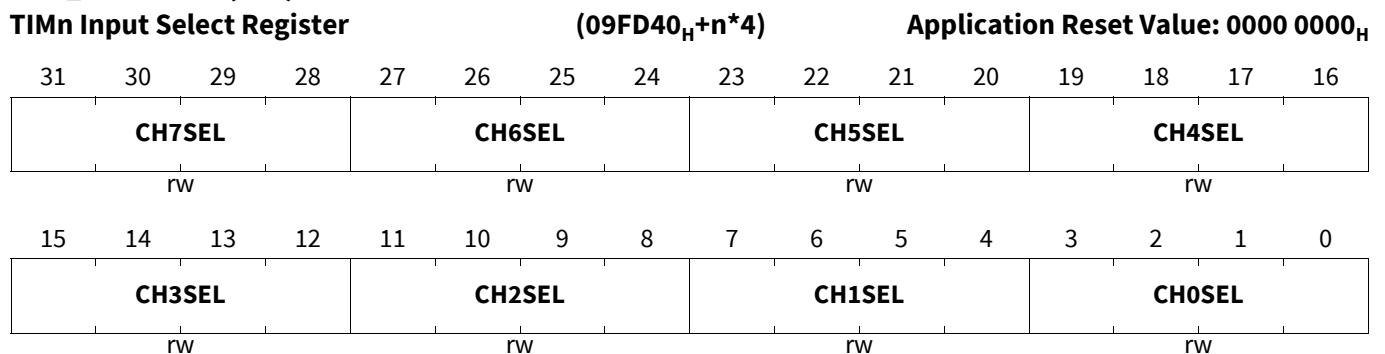
Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=5)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.5, Port pad input 2_H P10.8, Port pad input (no TQFP144/LQFP144) 3_H P14.2, Port pad input 4_H P23.0, Port pad input (no TQFP144/LQFP144) 5_H P32.4, Port pad input 6_H P33.1, Port pad input (no TQFP144/LQFP144) 7_H P21.7, Port pad input 8_H Reserved, do not use ... B_H Reserved, do not use C_H PDOUT5, SCU/ERU pattern detection output 5 D_H Reserved, do not use E_H IMUX0_5, DSADC input IMUX0_OUT5 F_H C1SR2, EVADC service request 2 of common block 1</p>
CHxSEL (x=6)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.6, Port pad input 2_H P10.4, Port pad input (no TQFP144/LQFP144) 3_H P14.3, Port pad input 4_H P23.1, Port pad input 5_H P23.2, Port pad input (no TQFP144/LQFP144) 6_H P33.2, Port pad input (no TQFP144/LQFP144) 7_H P20.0, Port pad input 8_H Reserved, do not use ... B_H Reserved, do not use C_H PDOUT6, SCU/ERU pattern detection output 6 D_H Reserved, do not use E_H IMUX0_6, DSADC input IMUX0_OUT6 F_H C0SR3, EVADC service request 3 of common block 0</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=7)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.7, Port pad input 2_H P14.4, Port pad input 3_H P20.8, Port pad input 4_H P23.3, Port pad input (no TQFP144/LQFP144) 5_H P23.4, Port pad input (no TQFP144/LQFP144) 6_H P33.3, Port pad input (no TQFP144/LQFP144) 7_H Reserved, do not use 8_H P11.15, Port pad input (no QFP) 9_H WUTUFLOW, PMS: Underflow output to support WUT calibration A_H Reserved, do not use B_H Reserved, do not use C_H PDOU7, SCU/ERU pattern detection output 7 D_H MT0, ERAY0 macrotick clock from CC E_H IMUX0_7, DSADC input IMUX0_OUT7 F_H C1SR3, EVADC service request 3 of common block 1</p>

GTM_TIMnINSEL (n=1)



Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H FC0BFL, EVADC boundary flag level of FC channel 0 1_H P00.9, Port pad input 2_H P02.0, Port pad input 3_H P10.7, Port pad input (no TQFP144/LQFP144) 4_H P14.5, Port pad input 5_H P14.7, Port pad input (no TQFP144/LQFP144) 6_H P15.6, Port pad input 7_H P21.2, Port pad input 8_H P22.1, Port pad input 9_H P33.10, Port pad input A_H P33.4, Port pad input B_H IMUX1_0, DSADC input IMUX1_OUT0 C_H COSR2, EVADC service request 2 of common block 0 D_H CBFLOUT0, EVADC common boundary flag output 0 E_H Reserved, do not use F_H Reserved, do not use</p>
CHxSEL (x=1)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H FC1BFL, EVADC boundary flag level of FC channel 1 1_H P00.10, Port pad input (no TQFP144/LQFP144) 2_H P02.1, Port pad input 3_H P10.1, Port pad input 4_H P14.6, Port pad input 5_H P15.7, Port pad input 6_H P21.3, Port pad input 7_H P22.0, Port pad input 8_H P33.5, Port pad input 9_H P33.9, Port pad input A_H Reserved, do not use B_H IMUX1_1, DSADC input IMUX1_OUT1 C_H C1SR2, EVADC service request 2 of common block 1 D_H INT_O12, CAN interrupt output INT_O12 E_H CBFLOUT1, EVADC common boundary flag output 1 F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=2)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.11, Port pad input (no TQFP144/LQFP144) 2_H P02.2, Port pad input 3_H P10.2, Port pad input 4_H P10.5, Port pad input 5_H P15.8, Port pad input 6_H P21.4, Port pad input 7_H P23.5, Port pad input (no TQFP144/LQFP144) 8_H P33.11, Port pad input 9_H P33.6, Port pad input A_H Reserved, do not use B_H IMUX1_2, DSADC input IMUX1_OUT2 C_H C0SR3, EVADC service request 3 of common block 0 D_H INT_O13, CAN interrupt output INT_O13 E_H CBFLOUT2, EVADC common boundary flag output 2 F_H Reserved, do not use</p>
CHxSEL (x=3)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.12, Port pad input 2_H P02.3, Port pad input 3_H P10.3, Port pad input 4_H P10.6, Port pad input 5_H P14.0, Port pad input 6_H P21.5, Port pad input 7_H P22.2, Port pad input 8_H P32.2, Port pad input (no TQFP144/LQFP144) 9_H P33.7, Port pad input A_H Reserved, do not use B_H CBFLOUT3, EVADC common boundary flag output 3 C_H Reserved, do not use D_H INT_O14, CAN interrupt output INT_O14 E_H IMUX1_3, DSADC input IMUX1_OUT3 F_H C1SR3, EVADC service request 3 of common block 1</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=4)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.4, Port pad input 2_H P10.0, Port pad input (no TQFP144/LQFP144) 3_H P14.1, Port pad input 4_H P22.3, Port pad input 5_H P32.3, Port pad input (no TQFP144/LQFP144) 6_H P33.0, Port pad input (no TQFP144/LQFP144) 7_H P33.8, Port pad input 8_H P21.6, Port pad input 9_H P20.0, Port pad input A_H C0SR0, EVADC service request 0 of common block 0 B_H CBFLOUT0, EVADC common boundary flag output 0 C_H Reserved, do not use D_H INT_O15, CAN interrupt output INT_O15 E_H IMUX1_4, DSADC input IMUX1_OUT4 F_H Reserved, do not use</p>
CHxSEL (x=5)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.5, Port pad input 2_H P10.8, Port pad input (no TQFP144/LQFP144) 3_H P14.2, Port pad input 4_H P23.0, Port pad input (no TQFP144/LQFP144) 5_H P32.4, Port pad input 6_H P33.1, Port pad input (no TQFP144/LQFP144) 7_H P21.7, Port pad input 8_H P20.7, Port pad input 9_H CBFLOUT1, EVADC common boundary flag output 1 A_H C1SR0, EVADC service request 0 of common block 1 B_H Reserved, do not use ... D_H Reserved, do not use E_H IMUX1_5, DSADC input IMUX1_OUT5 F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=6)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.6, Port pad input 2_H P10.4, Port pad input (no TQFP144/LQFP144) 3_H P14.3, Port pad input 4_H P23.1, Port pad input 5_H P23.2, Port pad input (no TQFP144/LQFP144) 6_H P33.2, Port pad input (no TQFP144/LQFP144) 7_H P20.0, Port pad input 8_H CBFLOUT2, EVADC common boundary flag output 2 9_H Reserved, do not use A_H C0SR1, EVADC service request 1 of common block 0 B_H Reserved, do not use ... D_H Reserved, do not use E_H IMUX1_6, DSADC input IMUX1_OUT6 F_H Reserved, do not use</p>
CHxSEL (x=7)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P02.7, Port pad input 2_H P14.4, Port pad input 3_H P20.8, Port pad input 4_H P23.3, Port pad input (no TQFP144/LQFP144) 5_H P23.4, Port pad input (no TQFP144/LQFP144) 6_H P33.3, Port pad input (no TQFP144/LQFP144) 7_H CBFLOUT3, EVADC common boundary flag output 3 8_H Reserved, do not use 9_H Reserved, do not use A_H C1SR1, EVADC service request 1 of common block 1 B_H Reserved, do not use C_H Reserved, do not use D_H MT0, ERAY0 macrotick clock from CC E_H IMUX1_7, DSADC input IMUX1_OUT7 F_H Reserved, do not use</p>

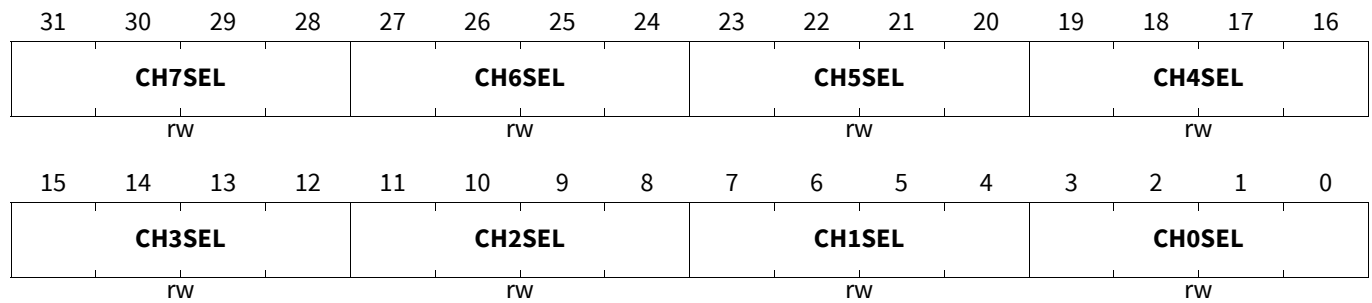
Generic Timer Module (GTM)

GTM_TIMnINSEL (n=2)

TIMn Input Select Register

(09FD40_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
CHxSEL (x=0)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H FC0BFL, EVADC boundary flag level of FC channel 0</p> <p>1_H P00.0, Port pad input</p> <p>2_H P02.8, Port pad input</p> <p>3_H P13.3, Port pad input</p> <p>4_H P15.5, Port pad input</p> <p>5_H P20.12, Port pad input</p> <p>6_H P33.12, Port pad input</p> <p>7_H P11.0, Port pad input (no QFP)</p> <p>8_H Reserved, do not use</p> <p>9_H P11.10, Port pad input</p> <p>A_H COSR0, EVADC service request 0 of common block 0</p> <p>B_H IMUX2_0, DSADC input IMUX2_OUT0</p> <p>C_H Reserved, do not use</p> <p>...</p> <p>E_H Reserved, do not use</p> <p>F_H CBFLOUT0, EVADC common boundary flag output 0</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=1)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H FC1BFL, EVADC boundary flag level of FC channel 1 1_H P00.1, Port pad input 2_H P00.2, Port pad input 3_H P11.2, Port pad input 4_H P20.13, Port pad input 5_H P33.13, Port pad input 6_H P11.1, Port pad input (no QFP) 7_H Reserved, do not use ... 9_H Reserved, do not use A_H C1SR0, EVADC service request 0 of common block 1 B_H IMUX2_1, DSADC input IMUX2_OUT1 C_H Reserved, do not use D_H INT_O12, CAN interrupt output INT_O12 E_H Reserved, do not use F_H CBFLOUT1, EVADC common boundary flag output 1</p>
CHxSEL (x=2)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.3, Port pad input 2_H P11.3, Port pad input 3_H P14.8, Port pad input (no TQFP144/LQFP144) 4_H P20.14, Port pad input 5_H P32.0, Port pad input 6_H P11.4, Port pad input (no QFP) 7_H Reserved, do not use ... 9_H Reserved, do not use A_H C0SR1, EVADC service request 1 of common block 0 B_H IMUX2_2, DSADC input IMUX2_OUT2 C_H Reserved, do not use D_H INT_O13, CAN interrupt output INT_O13 E_H P15.6, Port pad input F_H CBFLOUT2, EVADC common boundary flag output 2</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=3)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.4, Port pad input 2_H P11.6, Port pad input 3_H P14.9, Port pad input (no TQFP144/LQFP144) 4_H P15.0, Port pad input 5_H P20.1, Port pad input (no TQFP144/LQFP144) 6_H Reserved, do not use 7_H Reserved, do not use 8_H P11.5, Port pad input (no QFP) 9_H Reserved, do not use A_H C1SR1, EVADC service request 1 of common block 1 B_H IMUX2_3, DSADC input IMUX2_OUT3 C_H Reserved, do not use D_H INT_O14, CAN interrupt output INT_O14 E_H Reserved, do not use F_H CBFLOUT3, EVADC common boundary flag output 3</p>
CHxSEL (x=4)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.5, Port pad input 2_H P11.9, Port pad input 3_H P14.10, Port pad input (no TQFP144/LQFP144) 4_H P15.1, Port pad input 5_H P20.3, Port pad input 6_H P21.0, Port pad input (no TQFP144/LQFP144) 7_H P11.7, Port pad input (no QFP) 8_H Reserved, do not use 9_H Reserved, do not use A_H C0SR2, EVADC service request 2 of common block 0 B_H IMUX2_4, DSADC input IMUX2_OUT4 C_H Reserved, do not use D_H INT_O15, CAN interrupt output INT_O15 E_H Reserved, do not use F_H CBFLOUT0, EVADC common boundary flag output 0</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=5)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.6, Port pad input 2_H P11.10, Port pad input 3_H P13.0, Port pad input 4_H P15.2, Port pad input 5_H P20.9, Port pad input 6_H P21.1, Port pad input (no TQFP144/LQFP144) 7_H Reserved, do not use 8_H P11.8, Port pad input (no TQFP144/LQFP176) 9_H Reserved, do not use A_H C1SR2, EVADC service request 2 of common block 1 B_H IMUX2_5, DSADC input IMUX2_OUT5 C_H Reserved, do not use ... E_H Reserved, do not use F_H CBFLOUT1, EVADC common boundary flag output 1</p>
CHxSEL (x=6)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.7, Port pad input 2_H P11.11, Port pad input 3_H P13.1, Port pad input 4_H P15.3, Port pad input 5_H P20.6, Port pad input 6_H P20.10, Port pad input 7_H P11.13, Port pad input (no QFP) 8_H Reserved, do not use 9_H Reserved, do not use A_H C0SR3, EVADC service request 3 of common block 0 B_H IMUX2_6, DSADC input IMUX2_OUT6 C_H Reserved, do not use ... E_H Reserved, do not use F_H CBFLOUT2, EVADC common boundary flag output 2</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
CHxSEL (x=7)	4*x+3:4*x	rw	<p>TIM Channel x Input Selection</p> <p>This bit defines which input is connected for TIMn channel x of the GTM. The input is either derived from a port pad or from an on-chip module.</p> <p>0_H Reserved, do not use 1_H P00.8, Port pad input 2_H P11.12, Port pad input 3_H P13.2, Port pad input 4_H P15.4, Port pad input 5_H P20.7, Port pad input 6_H P20.11, Port pad input 7_H Reserved, do not use 8_H P11.14, Port pad input (no QFP) 9_H Reserved, do not use A_H C1SR3, EVADC service request 3 of common block 1 B_H IMUX2_7, DSADC input IMUX2_OUT7 C_H Reserved, do not use D_H MT0, ERAY0 macrotick clock from CC E_H Reserved, do not use F_H CBFLOUT3, EVADC common boundary flag output 3</p>

TIMi Channel x Control Register

GTM_TIMi_CHx_CTRL (i=1-2;x=0-7)

TIMi Channel x Control Register (001024_H+i*800_H+x*80_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOCTRL		EGPR1_SEL	EGPRO_SEL	FR_EC NT_OF L	CLK_SEL			FLT_C TR_FE	FLT_M ODE_F E	FLT_C TR_RE	FLT_M ODE_R E	EXT_C AP_EN	FLT_CNT_FR Q	FLT_E N	
rw		rw	rw	rw	rw			rw	rw	rw	rw	rw	rw		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECNT_ RESET	ISL	DSL	CNTS_ SEL	GPR1_SEL	GPR0_SEL	0	CICTR L	ARU_E N	OSM	TIM_MODE			TIM_E N		
rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
TIM_EN	0	rw	<p>TIM channel x enable</p> <p>Enabling of the channel resets the registers ECNT, TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_GPR0, and TIM[i]_CH[x]_GPR1 to their reset values. After finishing the action in one-shot mode the TIM_EN bit is cleared automatically. Otherwise, the bit must be cleared manually.</p> <p>0_B Channel disabled 1_B Channel enabled</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
TIM_MODE	3:1	rw	<p>TIM channel x mode</p> <p>If an undefined value is written to the TIM_MODE register, the hardware switches automatically to TIM_MODE = 0b000 (TPWM mode). The TIM_MODE register should not be changed while the TIM channel is enabled.</p> <p>If the TIM channel is enabled and operating in TPWM or TPIM mode after the first valid edge defined by DSL has occurred, a reconfiguration of DSL, ISL, TIM_MODE will not change the channel behavior. Reading these bit fields after reconfiguration will show the newly configured settings but the initial channel behavior will not change. Only a disabling of the TIM channel by setting TIM_EN= 0 and reenabling with TIM_EN= 1 will change the channel operation mode.</p> <p>000_B PWM Measurement Mode (TPWM) 001_B Pulse Integration Mode (TPIM) 010_B Input Event Mode (TIEM) 011_B Input Prescaler Mode (TIPM) 100_B Bit Compression Mode (TBCM) 101_B Gated Periodic Sampling Mode (TGPS) 110_B Serial Shift Mode (TSSM)</p>
OSM	4	rw	<p>One-shot mode</p> <p>After finishing the action in one-shot mode the TIM_EN bit is cleared automatically.</p> <p>0_B Continuous operation mode 1_B One-shot mode</p>
ARU_EN	5	rw	<p>GPR0 and GPR1 register values routed to ARU</p> <p>0_B Registers content not routed 1_B Registers content routed</p>
CICTRL	6	rw	<p>Channel Input Control</p> <p>0_B Use signal TIM_IN(x) as input for channel x 1_B Use signal TIM_IN(x-1) as input for channel x (or TIM_IN(m-1) if x is 0)</p>
GPR0_SEL	9:8	rw	<p>Selection for GPR0 register</p> <p>If EGPR0_SEL =0 / EGPR0_SEL =1 :</p> <p>If a reserved value is written to the EGPR0_SEL, GPR0_SEL bit fields, the hardware will use TBU_TS0 input.</p> <p>00_B Use TBU_TS0 as input / use ECNT as input 01_B Use TBU_TS1 as input / use TIM_INP_VAL as input 10_B Use TBU_TS2 as input / reserved 11_B Use CNTS as input; if TGPS mode in channel = 0 is selected, use TIM Filter F_OUT as input / reserved</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
GPR1_SEL	11:10	rw	<p>Selection for GPR1 register</p> <p>If EGPR1_SEL =0 / EGPR1_SEL =1: If a reserved value is written to the EGPR1_SEL, GPR1_SEL bit fields, the hardware will use TBU_TS0 input. Note: In TBCM mode: EGPR1_SEL=1, GPR1_SEL=01 selects TIM_INP_VAL as input; in all other cases, TIM Filter F_OUT is used.</p> <p>00_B Use TBU_TS0 as input / use ECNT as input 01_B Use TBU_TS1 as input / use TIM_INP_VAL as input 10_B Use TBU_TS2 as input / reserved 11_B Use CNT as input / reserved</p>
CNTS_SEL	12	rw	<p>Selection for CNTS register</p> <p>The functionality of the CNTS_SEL is disabled in the modes TIPM, TGPS and TBCM.</p> <p>CNTS_SEL in TSSM mode selects the source signal for registered or latched shift out operation.</p> <p>0_B use F_OUTx 1_B use TIM_INx 0_B Use CNT register as input 1_B Use TBU_TS0 as input</p>
DSL	13	rw	<p>Signal level control</p> <p>In TIM_MODE=0b110 (TSSM), the bit field DSL defines the shift direction.</p> <p>0_B Shift left 1_B Shift right 0_B Measurement starts with falling edge (low level measurement) 1_B Measurement starts with rising edge (high level measurement)</p>
ISL	14	rw	<p>Ignore signal level</p> <p>This bit is mode dependent and will have different meanings (see details in the TIM Channel mode description).</p> <p>0_B Use DSL bit for selecting active signal level (TIEM) 1_B Ignore DSL and treat both edges as active edge (TIEM)</p>
ECNT_RESET	15	rw	<p>Enables resetting of counter in certain modes</p> <p>If TIM_MODE=0b101 (TGPS) / TIM_MODE=0b000 (TPWM) else ECNT counter operating in wrap around mode; In TIM_MODE=0b110 (TSSM), the bit field ECNT_RESET defines the initial polarity for the shift register.</p> <p>0_B ECNT counter operating in wrap around mode / ECNT counter operating in wrap around mode, CNT is reset on active input edge defined by DSL 1_B ECNT counter is reset with periodic sampling / ECNT counter operating in wrap around mode, CNT is reset on active and inactive input edge</p>
FLT_EN	16	rw	<p>Filter enable for channel x</p> <p>If the filter is disabled, all filter related units (including CSU) are bypassed, which means that the signal F_IN is directly routed to signal F_OUT.</p> <p>0_B Filter disabled and internal states are reset 1_B Filter enabled</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
FLT_CNT_FRQ	18:17	rw	Filter counter frequency select 00 _B FLT_CNT counts with CMU_CLK0 01 _B FLT_CNT counts with CMU_CLK1 10 _B FLT_CNT counts with CMU_CLK6 11 _B FLT_CNT counts with CMU_CLK7
EXT_CAP_EN	19	rw	Enables external capture mode The selected TIM mode is only sensitive to external capture pulses the input event changes are ignored. 0 _B External capture disabled 1 _B External capture enabled
FLT_MODE_RE	20	rw	Filter mode for rising edge Coding see Family Spec.
FLT_CTR_RE	21	rw	Filter counter mode for rising edge Coding see Family Spec.
FLT_MODE_FE	22	rw	Filter mode for falling edge Coding see Family Spec.
FLT_CTR_FE	23	rw	Filter counter mode for falling edge Coding see Family Spec.
CLK_SEL	26:24	rw	CMU clock source select for channel If ECLK_SEL = 0 / ECLK_SEL = 1: 000 _B CMU_CLK0 selected / tdu_sample_evt of TDU selected 001 _B CMU_CLK1 selected / reserved 010 _B CMU_CLK2 selected / reserved 011 _B CMU_CLK3 selected / reserved 100 _B CMU_CLK4 selected / reserved 101 _B CMU_CLK5 selected / reserved 110 _B CMU_CLK6 selected / reserved 111 _B CMU_CLK7 selected / reserved
FR_ECNT_OFL	27	rw	Extended Edge counter overflow behavior 0 _B Overflow will be signaled on ECNT bit width = 8 1 _B Overflow will be signaled on EECNT bit width (full range)
EGPRO_SEL	28	rw	Extension of GPR0_SEL bit field Details described in GPR0_SEL bit field.
EGPR1_SEL	29	rw	Extension of GPR1_SEL bit field Details described in GPR1_SEL bit field.
TOCTRL	31:30	rw	Timeout control It has to be mentioned that writing of TOCTRL= 0 will every time stop the TDU, independent of the previous state of TOCTRL. 00 _B Timeout feature disabled 01 _B Timeout feature enabled for rising edge only 10 _B Timeout feature enabled for falling edge only 11 _B Timeout feature enabled for both edges
0	7	r	Reserved Read as zero, shall be written as zero.

Generic Timer Module (GTM)

26.3.3 GTM to Port Connections

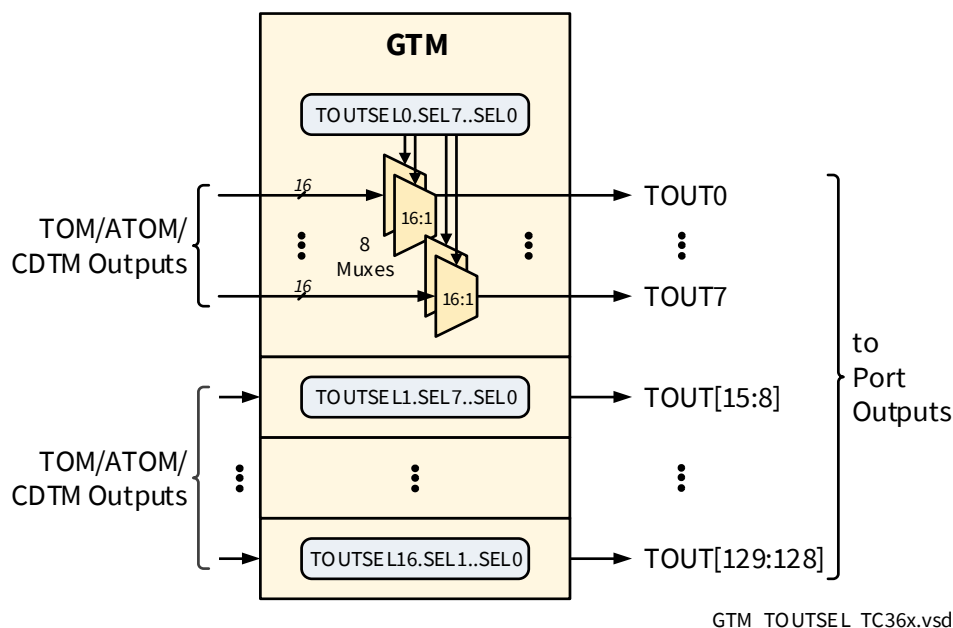


Figure 8 GTM to Port Connections Overview

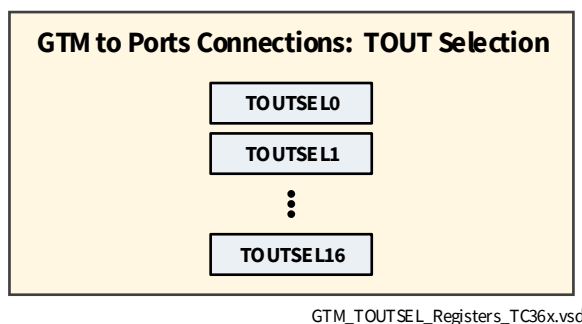


Figure 9 GTM to Port Connections Registers Overview

Table 221 Assignment of TOUTSELn Registers and SELx Bitfields to TOUTy Outputs

Register	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TOUTSEL0, Page 73	TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0
TOUTSEL1, Page 79	TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8
TOUTSEL2, Page 87	TOUT23 ¹⁾	TOUT22 ¹⁾	TOUT21	TOUT20 ²⁾	TOUT19 ²⁾	TOUT18	TOUT17	TOUT16
TOUTSEL3, Page 92	TOUT31	TOUT30	TOUT29	TOUT28	TOUT27	TOUT26	TOUT25 ¹⁾	TOUT24 ¹⁾
TOUTSEL4, Page 100	TOUT39 ²⁾	TOUT38 ²⁾	TOUT37	TOUT36	TOUT35 ³⁾	TOUT34	TOUT33	TOUT32
TOUTSEL5, Page 105	TOUT47	TOUT46 ²⁾	TOUT45 ²⁾	TOUT44 ¹⁾ 3)	TOUT43 ²⁾	TOUT42	TOUT41 ²⁾	TOUT40 ³⁾
TOUTSEL6, Page 110	TOUT55	TOUT54	TOUT53	TOUT52 ²⁾	TOUT51 ¹⁾ 3)	TOUT50	TOUT49	TOUT48
TOUTSEL7, Page 114	TOUT63	TOUT62	TOUT61	TOUT60 ²⁾	TOUT59	TOUT58	TOUT57	TOUT56

Generic Timer Module (GTM)

Table 221 Assignment of TOUTSELn Registers and SELx Bitfields to TOUTy Outputs (cont'd)

Register	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
TOUTSEL8, Page 119	TOUT71	TOUT70	TOUT69	TOUT68	TOUT67	TOUT66	TOUT65	TOUT64
TOUTSEL9, Page 123	TOUT79	TOUT78	TOUT77	TOUT76	TOUT75	TOUT74	TOUT73	TOUT72
TOUTSEL10, Page 128	TOUT87 ²⁾	TOUT86	TOUT85	TOUT84	TOUT83	TOUT82	TOUT81	TOUT80
TOUTSEL11, Page 132	TOUT95	TOUT94	TOUT93	TOUT92	TOUT91	TOUT90 ¹⁾ ³⁾	TOUT89 ²⁾	TOUT88 ¹⁾ ³⁾
TOUTSEL12, Page 138	TOUT103	TOUT102 ¹⁾³⁾	TOUT101	TOUT100	TOUT99	TOUT98	TOUT97	TOUT96
TOUTSEL13, Page 143	-	TOUT110 ²⁾	TOUT109 ²⁾	TOUT108	TOUT107	TOUT106 ¹⁾³⁾	TOUT105	TOUT104
TOUTSEL14, Page 147	TOUT119 ⁴⁾	-	-	-	-	-	-	-
TOUTSEL15, Page 151				TOUT124 ¹⁾³⁾⁵⁾	TOUT123 ⁴⁾		TOUT121 ⁴⁾	TOUT120 ⁴⁾
TOUTSEL16, Page 151	-	-	-	-	-	-	TOUT129 ⁴⁾	TOUT128 ⁴⁾

- 1) Not available in LQFP144.
- 2) Only available in LQFP176 and LFBGA292 packages
- 3) Not available in TQFP144.
- 4) Only available in LFBGA292 package
- 5) Not available LQFP176 packages

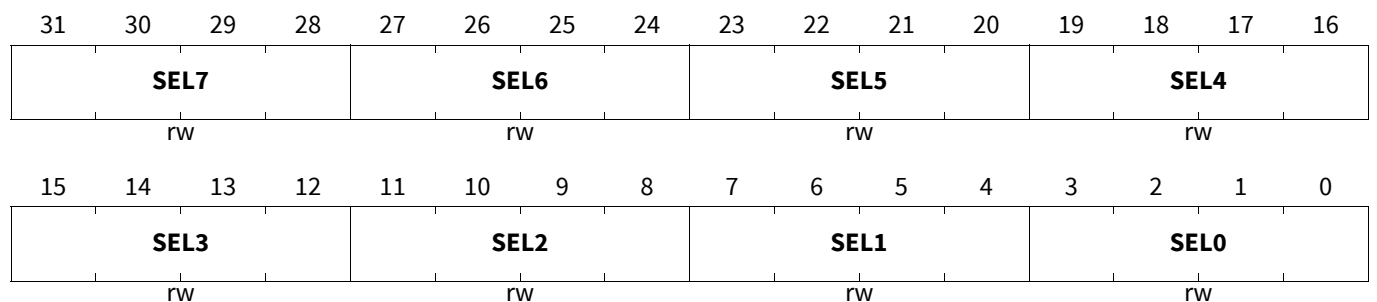
Timer Output Select Register

GTM_TOUTSELn (n=0)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H TOM1_8, Output of TOM1, channel 8 2_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 3_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 4_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 5_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 6_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 8_H CDTM0_DTM5_1_N, ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5 9_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_9, Output of TOM0, channel 9 1_H TOM1_9, Output of TOM1, channel 9 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 4_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 6_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 8_H CDTM0_DTM5_2_N, ATOM0_6_N, Inverted dead-time output of ATOM0, channel 6 9_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_10, Output of TOM0, channel 10 1_H TOM1_10, Output of TOM1, channel 10 2_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 3_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 4_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 5_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 6_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 8_H CDTM0_DTM5_3_N, ATOM0_7_N, Inverted dead-time output of ATOM0, channel 7 9_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_11, Output of TOM0, channel 11 1_H TOM1_11, Output of TOM1, channel 11 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 4_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 5_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM0_DTM5_0_N, ATOM0_4_N, Inverted dead-time output of ATOM0, channel 4 9_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_12, Output of TOM0, channel 12 1_H TOM1_12, Output of TOM1, channel 12 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 6_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 8_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 9_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_13, Output of TOM0, channel 13 1_H TOM1_13, Output of TOM1, channel 13 2_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 3_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H CDTM1_DTM0_2_N, TOM1_2_N, Inverted dead-time output of TOM1, channel 2 6_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 8_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 9_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2 A_H Reserved, do not use B_H Reserved, do not use</p>

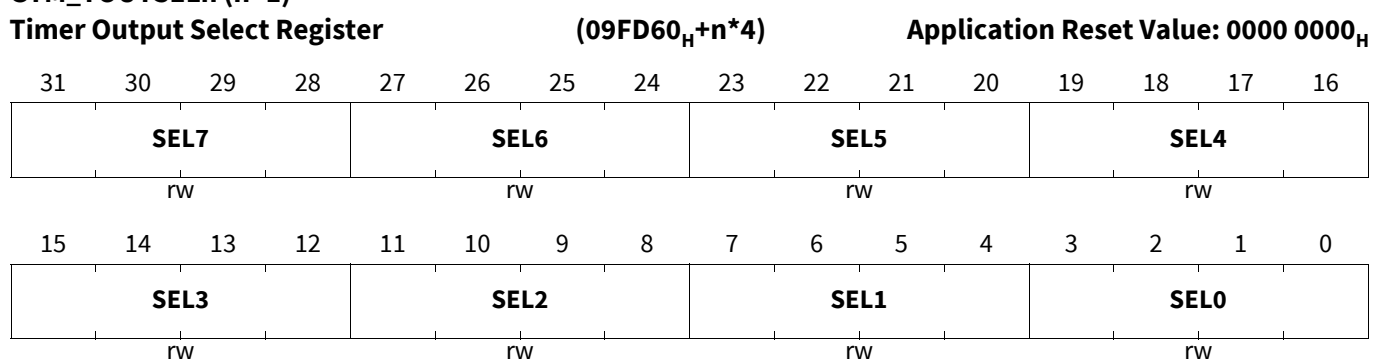
Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_14, Output of TOM0, channel 14 1_H TOM1_14, Output of TOM1, channel 14 2_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 3_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H CDTM1_DTM0_3_N, TOM1_3_N, Inverted dead-time output of TOM1, channel 3 6_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 8_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 9_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_15, Output of TOM0, channel 15 1_H TOM1_15, Output of TOM1, channel 15 2_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 3_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H CDTM1_DTM0_0_N, TOM1_0_N, Inverted dead-time output of TOM1, channel 0 6_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 8_H CDTM0_DTM4_0_N, ATOM0_0_N, Inverted dead-time output of ATOM0, channel 0 9_H CDTM1_DTM4_0_N, ATOM1_0_N, Inverted dead-time output of ATOM1, channel 0 A_H Reserved, do not use B_H Reserved, do not use</p>

GTM_TOUTSELn (n=1)



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 3_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 4_H Reserved, do not use 5_H Reserved, do not use 6_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 8_H CDTM0_DTM5_1_N, ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5 9_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 3_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 6_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 8_H CDTM0_DTM5_1_N, ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5 9_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 A_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_9, Output of TOM0, channel 9 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 8_H CDTM0_DTM5_2_N, ATOM0_6_N, Inverted dead-time output of ATOM0, channel 6 9_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6 A_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_9, Output of TOM0, channel 9 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 8_H CDTM0_DTM5_2_N, ATOM0_6_N, Inverted dead-time output of ATOM0, channel 6 9_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6 A_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_10, Output of TOM0, channel 10 1_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 2_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 3_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM0_DTM5_3_N, ATOM0_7_N, Inverted dead-time output of ATOM0, channel 7 9_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7 A_H CDTM2_DTM4_0_N, ATOM2_0_N, Inverted dead-time output of ATOM2, channel 0 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_11, Output of TOM0, channel 11 1_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 4_H Reserved, do not use 5_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 6_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 8_H CDTM0_DTM5_0_N, ATOM0_4_N, Inverted dead-time output of ATOM0, channel 4 9_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_12, Output of TOM0, channel 12 1_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 6_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 8_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 9_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1 A_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_13, Output of TOM0, channel 13 1_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 2_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 3_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H CDTM1_DTM0_2_N, TOM1_2_N, Inverted dead-time output of TOM1, channel 2 6_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 8_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 9_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2 A_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 B_H Reserved, do not use</p>

GTM_TOUTSELn (n=2)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw				rw			

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_14, Output of TOM0, channel 14 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 3_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H CDTM1_DTM0_3_N, TOM1_3_N, Inverted dead-time output of TOM1, channel 3 6_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 8_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 9_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3 A_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_15, Output of TOM0, channel 15 1_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 2_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 3_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H CDTM1_DTM0_0_N, TOM1_0_N, Inverted dead-time output of TOM1, channel 0 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM0_DTM4_0_N, ATOM0_0_N, Inverted dead-time output of ATOM0, channel 0 9_H CDTM1_DTM4_0_N, ATOM1_0_N, Inverted dead-time output of ATOM1, channel 0 A_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0 B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 3_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 4_H Reserved, do not use 5_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 3_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 4_H Reserved, do not use 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM3_DTM5_2_N, ATOM3_6_N, Inverted dead-time output of ATOM3, channel 6 9_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 2_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 3_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 4_H Reserved, do not use 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM3_DTM5_3_N, ATOM3_7_N, Inverted dead-time output of ATOM3, channel 7 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 2_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 3_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 4_H Reserved, do not use 5_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM3_DTM5_0_N, ATOM3_4_N, Inverted dead-time output of ATOM3, channel 4 9_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 2_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 3_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 9_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 1_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 2_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 3_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H CDTM1_DTM0_2_N, TOM1_2_N, Inverted dead-time output of TOM1, channel 2 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 9_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 A_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 B_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2</p>

GTM_TOUTSELn (n=3)

Timer Output Select Register (09FD60_H+n*4) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw				rw			

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 3_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H CDTM1_DTM0_3_N, TOM1_3_N, Inverted dead-time output of TOM1, channel 3 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 9_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 A_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 B_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 1_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 2_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 3_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H CDTM1_DTM0_0_N, TOM1_0_N, Inverted dead-time output of TOM1, channel 0 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_0_N, ATOM2_0_N, Inverted dead-time output of ATOM2, channel 0 9_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 3_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 4_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 5_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM5_1_N, ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 9_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 A_H CDTM0_DTM5_1_N, ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5 B_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 3_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 8_H CDTM2_DTM5_2_N, ATOM2_6_N, Inverted dead-time output of ATOM2, channel 6 9_H CDTM3_DTM5_2_N, ATOM3_6_N, Inverted dead-time output of ATOM3, channel 6 A_H CDTM0_DTM5_2_N, ATOM0_6_N, Inverted dead-time output of ATOM0, channel 6 B_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 2_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 3_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM2_DTM5_3_N, ATOM2_7_N, Inverted dead-time output of ATOM2, channel 7 9_H CDTM3_DTM5_3_N, ATOM3_7_N, Inverted dead-time output of ATOM3, channel 7 A_H CDTM0_DTM5_3_N, ATOM0_7_N, Inverted dead-time output of ATOM0, channel 7 B_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 2_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 3_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 4_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 5_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 6_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 8_H CDTM2_DTM5_0_N, ATOM2_4_N, Inverted dead-time output of ATOM2, channel 4 9_H CDTM3_DTM5_0_N, ATOM3_4_N, Inverted dead-time output of ATOM3, channel 4 A_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 B_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 2_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 3_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 6_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 8_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 9_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

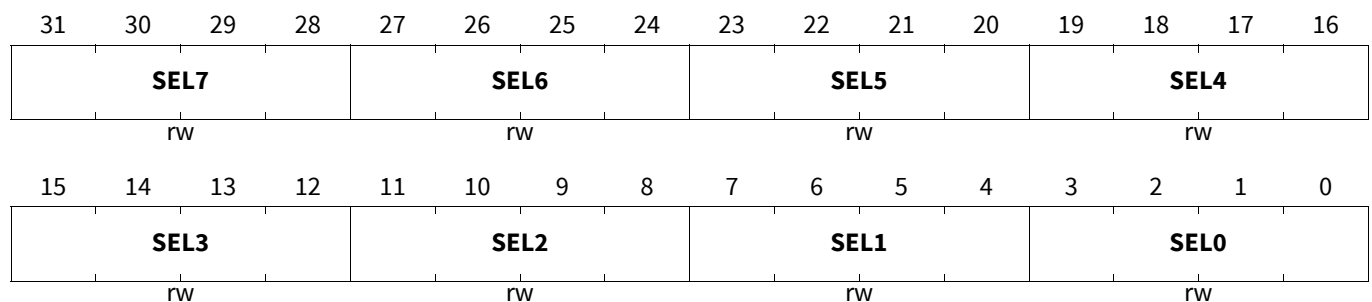
Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 8_H Reserved, do not use 9_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 A_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 B_H Reserved, do not use</p>

GTM_TOUTSELn (n=4)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 3_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 4_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 5_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 6_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 8_H CDTM2_DTM4_0_N, ATOM2_0_N, Inverted dead-time output of ATOM2, channel 0 9_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 2_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 3_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 9_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_12, Output of TOM1, channel 12 1_H Reserved, do not use 2_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 3_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H CDTM1_DTM0_0_N, TOM1_0_N, Inverted dead-time output of TOM1, channel 0 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 9_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_13, Output of TOM1, channel 13 1_H Reserved, do not use 2_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 3_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 9_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_14, Output of TOM1, channel 14 1_H Reserved, do not use 2_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 3_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 4_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 5_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 9_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_15, Output of TOM1, channel 15 1_H Reserved, do not use 2_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 3_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 4_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 5_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 9_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 A_H CDTM2_DTM4_0_N, ATOM2_0_N, Inverted dead-time output of ATOM2, channel 0 B_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 7_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 8_H Reserved, do not use 9_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 A_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1 B_H Reserved, do not use</p>

GTM_TOUTSELn (n=5)

Timer Output Select Register (09FD60_H+n*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw				rw			

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 1_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 2_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 3_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 7_H CDTM1_DTM0_2_N, TOM1_2_N, Inverted dead-time output of TOM1, channel 2 8_H Reserved, do not use 9_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 A_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_10, TOM0_10, Output of TOM0, channel 10 1_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 2_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 3_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 4_H Reserved, do not use 5_H CDTM1_DTM0_2_N, TOM1_2_N, Inverted dead-time output of TOM1, channel 2 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 9_H Reserved, do not use A_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 B_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H TOM0_15, Output of TOM0, channel 15 2_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 3_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 7_H Reserved, do not use 8_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 9_H Reserved, do not use A_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 B_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_11, Output of TOM0, channel 11 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 3_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 4_H Reserved, do not use 5_H Reserved, do not use 6_H CDTM1_DTM0_3_N, TOM1_3_N, Inverted dead-time output of TOM1, channel 3 7_H Reserved, do not use 8_H CDTM0_DTM4_0_N, ATOM0_0_N, Inverted dead-time output of ATOM0, channel 0 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_12, Output of TOM0, channel 12 1_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 2_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 3_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 4_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 9_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 1_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 2_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 3_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 4_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_10, Output of TOM0, channel 10 1_H Reserved, do not use 2_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 3_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_9, Output of TOM0, channel 9 1_H Reserved, do not use 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H Reserved, do not use ... B_H Reserved, do not use</p>

GTM_TOUTSELn (n=6)

Timer Output Select Register (09FD60_H+n*4) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw				rw			

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H Reserved, do not use 2_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 3_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 8_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_11, Output of TOM0, channel 11 1_H Reserved, do not use 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 8_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_12, Output of TOM0, channel 12 1_H Reserved, do not use 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 8_H Reserved, do not use 9_H Reserved, do not use A_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 B_H Reserved, do not use</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H Reserved, do not use 2_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 3_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 4_H Reserved, do not use 5_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 9_H Reserved, do not use A_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_9, Output of TOM0, channel 9 1_H Reserved, do not use 2_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 3_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 4_H Reserved, do not use 5_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 9_H Reserved, do not use A_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 B_H Reserved, do not use</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H Reserved, do not use 2_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 3_H Reserved, do not use 4_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 5_H Reserved, do not use 6_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 8_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H Reserved, do not use 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H Reserved, do not use 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H Reserved, do not use 6_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 8_H CDTM0_DTM4_0_N, ATOM0_0_N, Inverted dead-time output of ATOM0, channel 0 9_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H Reserved, do not use 2_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 3_H Reserved, do not use 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H Reserved, do not use 6_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 8_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 9_H Reserved, do not use ... B_H Reserved, do not use</p>

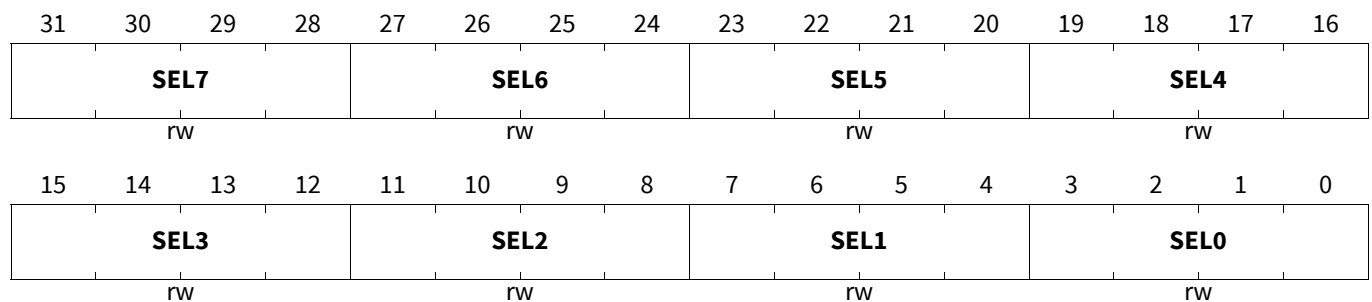
Generic Timer Module (GTM)

GTM_TOUTSELn (n=7)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H Reserved, do not use 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H Reserved, do not use 4_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 5_H Reserved, do not use 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H Reserved, do not use 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H Reserved, do not use 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_0_N, ATOM2_4_N, Inverted dead-time output of ATOM2, channel 4 9_H CDTM3_DTM5_0_N, ATOM3_4_N, Inverted dead-time output of ATOM3, channel 4 A_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 1_H Reserved, do not use 2_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 3_H Reserved, do not use 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 9_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H Reserved, do not use 2_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 3_H Reserved, do not use 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_1_N, ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 9_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 A_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_11, Output of TOM1, channel 11 1_H Reserved, do not use 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_2_N, ATOM2_6_N, Inverted dead-time output of ATOM2, channel 6 9_H CDTM3_DTM5_2_N, ATOM3_6_N, Inverted dead-time output of ATOM3, channel 6 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_12, Output of TOM1, channel 12 1_H Reserved, do not use 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 4_H Reserved, do not use 5_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 6_H Reserved, do not use 7_H Reserved, do not use 8_H CDTM2_DTM5_3_N, ATOM2_7_N, Inverted dead-time output of ATOM2, channel 7 9_H CDTM3_DTM5_3_N, ATOM3_7_N, Inverted dead-time output of ATOM3, channel 7 A_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 B_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_10, Output of TOM1, channel 10 1_H Reserved, do not use 2_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 3_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 4_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 9_H Reserved, do not use A_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 B_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3</p>

Generic Timer Module (GTM)

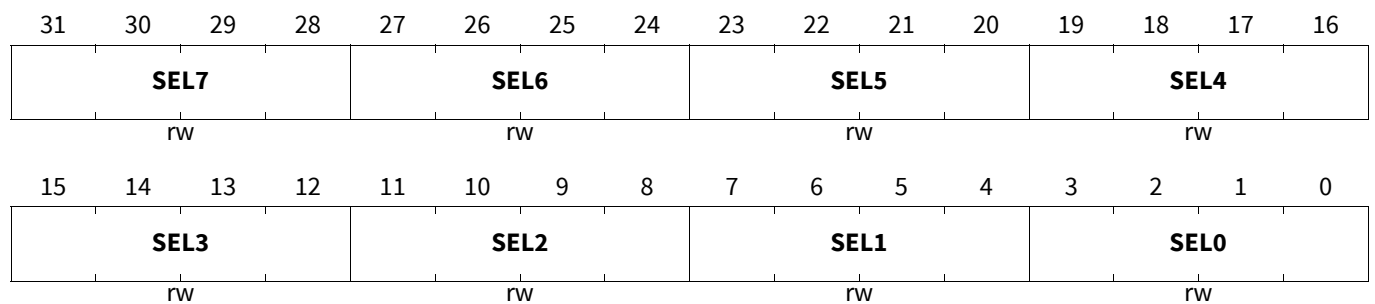
Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_11, TOM1_11, Output of TOM1, channel 11 1_H Reserved, do not use 2_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 3_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 4_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 9_H Reserved, do not use A_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0 B_H Reserved, do not use</p>

GTM_TOUTSELn (n=8)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 1_H Reserved, do not use 2_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 6_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 7_H Reserved, do not use 8_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 9_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_13, Output of TOM1, channel 13 1_H Reserved, do not use 2_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 6_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 7_H Reserved, do not use 8_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 9_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 A_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_14, Output of TOM1, channel 14 1_H Reserved, do not use 2_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 6_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 7_H Reserved, do not use ... 9_H Reserved, do not use A_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 B_H Reserved, do not use</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_15, Output of TOM1, channel 15 1_H Reserved, do not use 2_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 6_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 7_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 1_H Reserved, do not use 2_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 6_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 7_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 1_H Reserved, do not use 2_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 6_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 7_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 1_H Reserved, do not use 2_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 6_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 7_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 1_H Reserved, do not use 2_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 3_H Reserved, do not use 4_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 5_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 6_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 8_H Reserved, do not use 9_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 A_H Reserved, do not use B_H Reserved, do not use</p>

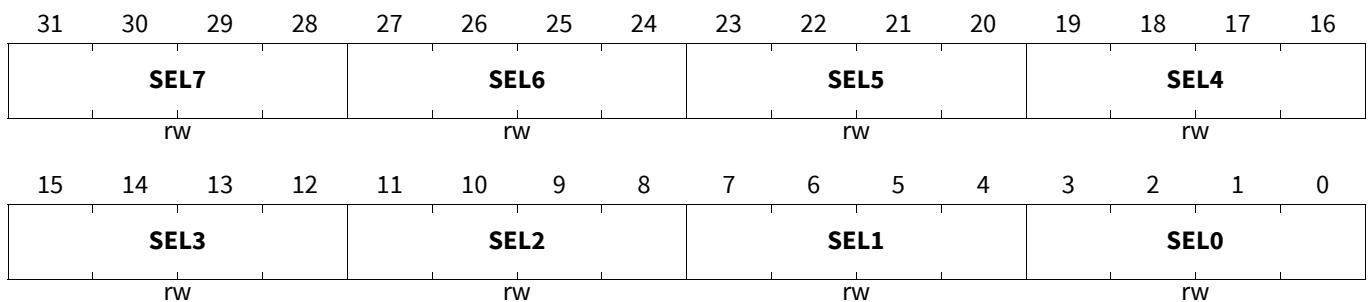
Generic Timer Module (GTM)

GTM_TOUTSELn (n=9)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 1_H Reserved, do not use 2_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 3_H Reserved, do not use 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H CDTM1_DTM0_1_N, TOM1_1_N, Inverted dead-time output of TOM1, channel 1 6_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 8_H Reserved, do not use 9_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 1_H Reserved, do not use 2_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 3_H Reserved, do not use 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H CDTM1_DTM0_2_N, TOM1_2_N, Inverted dead-time output of TOM1, channel 2 6_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 8_H Reserved, do not use 9_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 1_H Reserved, do not use 2_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 3_H Reserved, do not use 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H CDTM1_DTM0_3_N, TOM1_3_N, Inverted dead-time output of TOM1, channel 3 6_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 8_H Reserved, do not use 9_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 1_H Reserved, do not use 2_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 3_H Reserved, do not use 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H CDTM1_DTM0_0_N, TOM1_0_N, Inverted dead-time output of TOM1, channel 0 6_H Reserved, do not use ... 8_H Reserved, do not use 9_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 3_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0 9_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 6_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 7_H Reserved, do not use 8_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 9_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 6_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 7_H Reserved, do not use 8_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 9_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

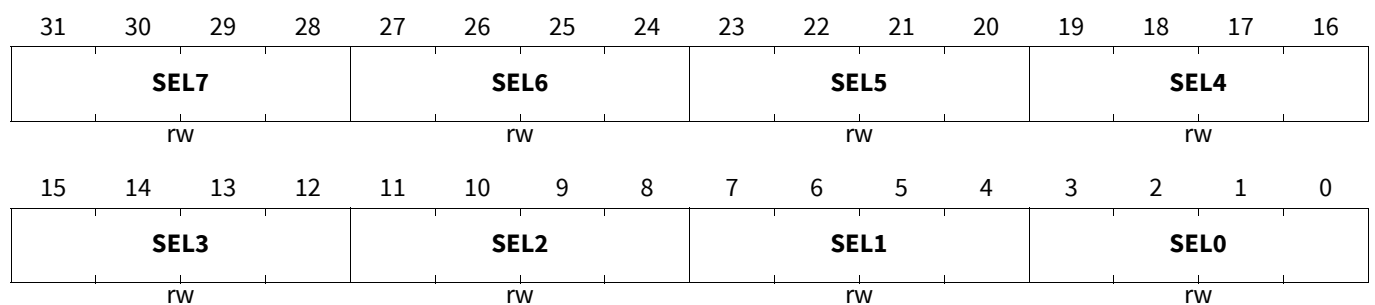
Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 2_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 3_H Reserved, do not use 4_H Reserved, do not use 5_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 6_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 7_H Reserved, do not use 8_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 9_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7 A_H Reserved, do not use B_H Reserved, do not use</p>

GTM_TOUTSELn (n=10)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 2_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 3_H Reserved, do not use 4_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 5_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 6_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 2_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 3_H Reserved, do not use 4_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 5_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 6_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 1_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 2_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 3_H Reserved, do not use 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 6_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 3_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 1_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 2_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 3_H Reserved, do not use 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 6_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 2_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 3_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 2_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 3_H Reserved, do not use 4_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_0_N, ATOM2_4_N, Inverted dead-time output of ATOM2, channel 4 9_H CDTM3_DTM5_0_N, ATOM3_4_N, Inverted dead-time output of ATOM3, channel 4 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H Reserved, do not use 2_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 3_H Reserved, do not use 4_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_1_N, ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 9_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 A_H Reserved, do not use B_H Reserved, do not use</p>

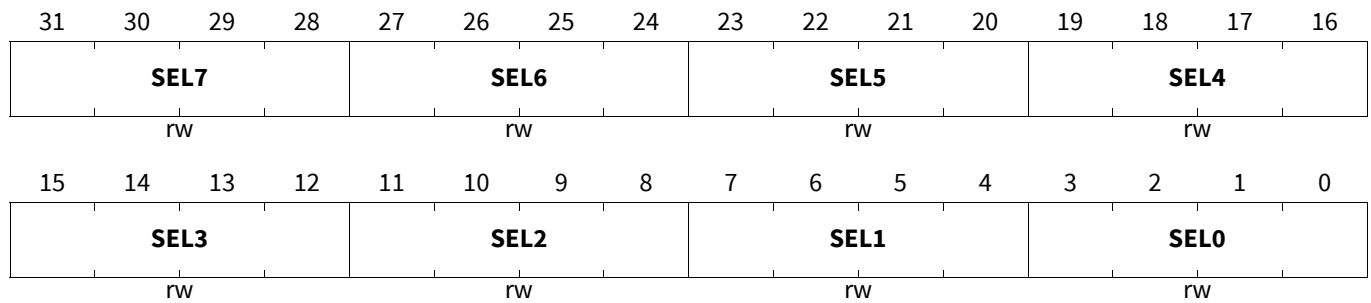
Generic Timer Module (GTM)

GTM_TOUTSELn (n=11)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H Reserved, do not use 2_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 3_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 4_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_2_N, ATOM2_6_N, Inverted dead-time output of ATOM2, channel 6 9_H CDTM3_DTM5_2_N, ATOM3_6_N, Inverted dead-time output of ATOM3, channel 6 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H Reserved, do not use 2_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 3_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 4_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM5_3_N, ATOM2_7_N, Inverted dead-time output of ATOM2, channel 7 9_H CDTM3_DTM5_3_N, ATOM3_7_N, Inverted dead-time output of ATOM3, channel 7 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H Reserved, do not use 2_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 3_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 9_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 A_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 B_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 1_H Reserved, do not use 2_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 3_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H Reserved, do not use 6_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 8_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 9_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 A_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 B_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H Reserved, do not use 2_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 3_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H Reserved, do not use 6_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 8_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 9_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 A_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 B_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 1_H Reserved, do not use 2_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 3_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H Reserved, do not use 6_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 7_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 8_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 9_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H Reserved, do not use 2_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 3_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H Reserved, do not use 6_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 8_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 9_H CDTM2_DTM5_1_N, ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 A_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_8, Output of TOM0, channel 8 1_H Reserved, do not use 2_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 3_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 4_H Reserved, do not use 5_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 6_H Reserved, do not use 7_H CDTM1_DTM1_0_N, TOM1_4_N, Inverted dead-time output of TOM1, channel 4 8_H CDTM3_DTM5_2_N, ATOM3_6_N, Inverted dead-time output of ATOM3, channel 6 9_H CDTM2_DTM5_2_N, ATOM2_6_N, Inverted dead-time output of ATOM2, channel 6 A_H Reserved, do not use B_H Reserved, do not use</p>

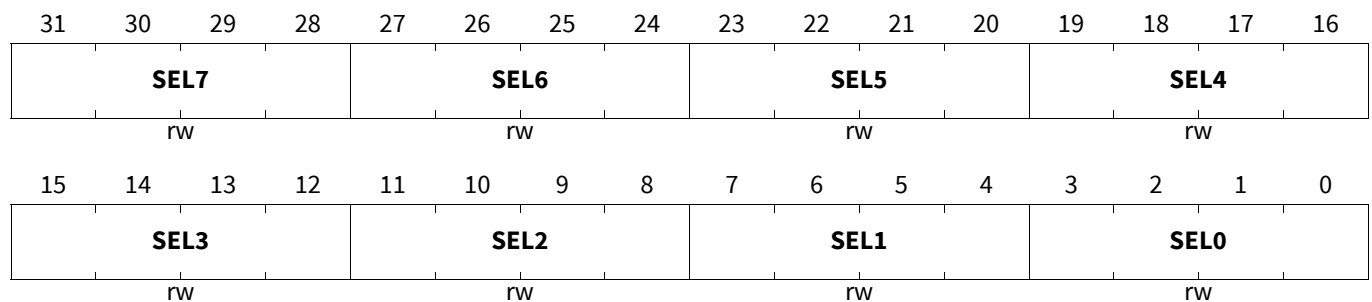
Generic Timer Module (GTM)

GTM_TOUTSELn (n=12)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H TOM0_10, Output of TOM0, channel 10 1_H Reserved, do not use 2_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 3_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 4_H Reserved, do not use 5_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 6_H CDTM0_DTM1_0_N, TOM0_4_N, Inverted dead-time output of TOM0, channel 4 7_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 8_H CDTM3_DTM5_3_N, ATOM3_7_N, Inverted dead-time output of ATOM3, channel 7 9_H CDTM2_DTM5_3_N, ATOM2_7_N, Inverted dead-time output of ATOM2, channel 7 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_11, Output of TOM0, channel 11 1_H Reserved, do not use 2_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 3_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 4_H Reserved, do not use 5_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 6_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 7_H CDTM1_DTM1_1_N, TOM1_5_N, Inverted dead-time output of TOM1, channel 5 8_H CDTM3_DTM5_0_N, ATOM3_4_N, Inverted dead-time output of ATOM3, channel 4 9_H CDTM2_DTM5_0_N, ATOM2_4_N, Inverted dead-time output of ATOM2, channel 4 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_12, Output of TOM0, channel 12 1_H Reserved, do not use 2_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 3_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 4_H Reserved, do not use 5_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 6_H Reserved, do not use 7_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 8_H CDTM3_DTM4_1_N, ATOM3_1_N, Inverted dead-time output of ATOM3, channel 1 9_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_13, Output of TOM0, channel 13 1_H Reserved, do not use 2_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 3_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 4_H Reserved, do not use 5_H CDTM0_DTM1_2_N, TOM0_6_N, Inverted dead-time output of TOM0, channel 6 6_H Reserved, do not use 7_H CDTM1_DTM1_2_N, TOM1_6_N, Inverted dead-time output of TOM1, channel 6 8_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2 9_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_14, Output of TOM0, channel 14 1_H Reserved, do not use 2_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 3_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 4_H Reserved, do not use 5_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 6_H Reserved, do not use 7_H CDTM1_DTM1_3_N, TOM1_7_N, Inverted dead-time output of TOM1, channel 7 8_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3 9_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM0_15, Output of TOM0, channel 15 1_H Reserved, do not use 2_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 3_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 4_H Reserved, do not use 5_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 6_H Reserved, do not use 7_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 8_H CDTM3_DTM4_0_N, ATOM3_0_N, Inverted dead-time output of ATOM3, channel 0 9_H CDTM2_DTM4_0_N, ATOM2_0_N, Inverted dead-time output of ATOM2, channel 0 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 1_H Reserved, do not use 2_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 3_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1 9_H Reserved, do not use A_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

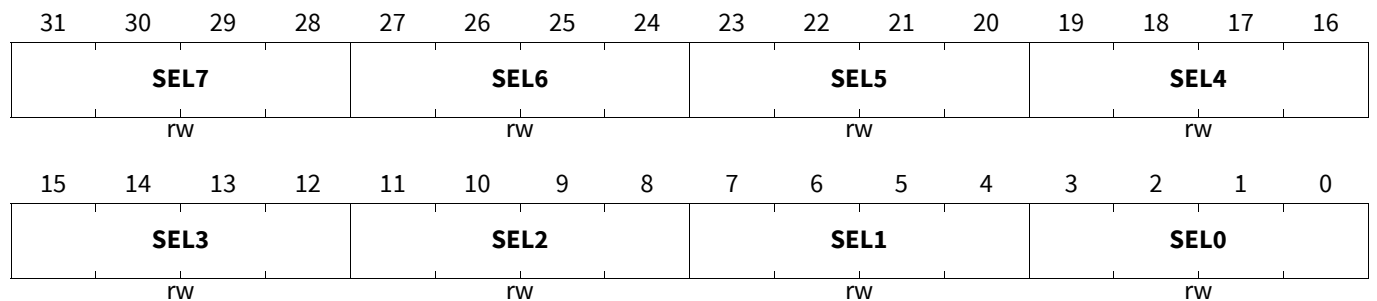
Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 1_H Reserved, do not use 2_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 3_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6 9_H Reserved, do not use A_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 B_H Reserved, do not use</p>

GTM_TOUTSELn (n=13)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H Reserved, do not use 2_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 3_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7 9_H Reserved, do not use A_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H Reserved, do not use 2_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 3_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 9_H Reserved, do not use A_H CDTM2_DTM4_1_N, ATOM2_1_N, Inverted dead-time output of ATOM2, channel 1 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H Reserved, do not use 2_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 3_H Reserved, do not use 4_H CDTM0_DTM0_0_N, TOM0_0_N, Inverted dead-time output of TOM0, channel 0 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3 9_H Reserved, do not use A_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 B_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 1_H Reserved, do not use 2_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 3_H Reserved, do not use 4_H CDTM0_DTM0_1_N, TOM0_1_N, Inverted dead-time output of TOM0, channel 1 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7 9_H Reserved, do not use A_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 1_H Reserved, do not use 2_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 3_H Reserved, do not use 4_H CDTM0_DTM0_2_N, TOM0_2_N, Inverted dead-time output of TOM0, channel 2 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 9_H Reserved, do not use A_H CDTM2_DTM4_0_N, ATOM2_0_N, Inverted dead-time output of ATOM2, channel 0 B_H Reserved, do not use</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 1_H Reserved, do not use 2_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 3_H Reserved, do not use 4_H CDTM0_DTM0_3_N, TOM0_3_N, Inverted dead-time output of TOM0, channel 3 5_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM5_1_N, ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 9_H Reserved, do not use A_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

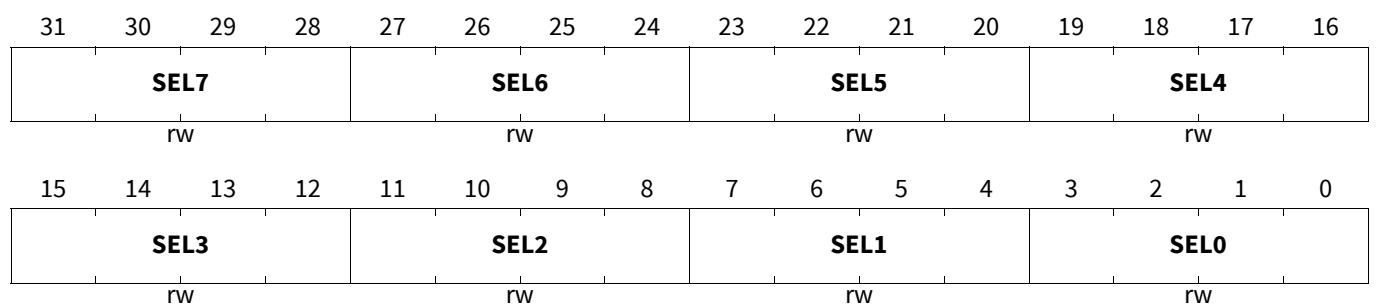
Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 1_H Reserved, do not use 2_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 3_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2 9_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use 1_H Reserved, do not use 2_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 3_H Reserved, do not use ... B_H Reserved, do not use</p>

GTM_TOUTSELn (n=14)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_0_N, ATOM0_0_N, Inverted dead-time output of ATOM0, channel 0 9_H CDTM1_DTM4_0_N, ATOM1_0_N, Inverted dead-time output of ATOM1, channel 0 A_H Reserved, do not use B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_1_N, ATOM0_1_N, Inverted dead-time output of ATOM0, channel 1 9_H CDTM1_DTM4_1_N, ATOM1_1_N, Inverted dead-time output of ATOM1, channel 1 A_H Reserved, do not use B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_2_N, ATOM0_2_N, Inverted dead-time output of ATOM0, channel 2 9_H CDTM1_DTM4_2_N, ATOM1_2_N, Inverted dead-time output of ATOM1, channel 2 A_H CDTM2_DTM4_2_N, ATOM2_2_N, Inverted dead-time output of ATOM2, channel 2 B_H CDTM3_DTM4_2_N, ATOM3_2_N, Inverted dead-time output of ATOM3, channel 2</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1_H Reserved, do not use ... 7_H Reserved, do not use 8_H CDTM0_DTM4_3_N, ATOM0_3_N, Inverted dead-time output of ATOM0, channel 3 9_H CDTM1_DTM4_3_N, ATOM1_3_N, Inverted dead-time output of ATOM1, channel 3 A_H CDTM2_DTM4_3_N, ATOM2_3_N, Inverted dead-time output of ATOM2, channel 3 B_H CDTM3_DTM4_3_N, ATOM3_3_N, Inverted dead-time output of ATOM3, channel 3</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... 3_H Reserved, do not use 4_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 5_H Reserved, do not use 6_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 7_H Reserved, do not use 8_H CDTM0_DTM5_2_N, ATOM0_6_N, Inverted dead-time output of ATOM0, channel 6 9_H CDTM1_DTM5_2_N, ATOM1_6_N, Inverted dead-time output of ATOM1, channel 6 A_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 B_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... 3_H Reserved, do not use 4_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 5_H Reserved, do not use 6_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 7_H Reserved, do not use 8_H CDTM0_DTM5_3_N, ATOM0_7_N, Inverted dead-time output of ATOM0, channel 7 9_H CDTM1_DTM5_3_N, ATOM1_7_N, Inverted dead-time output of ATOM1, channel 7 A_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 B_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2</p>

Generic Timer Module (GTM)

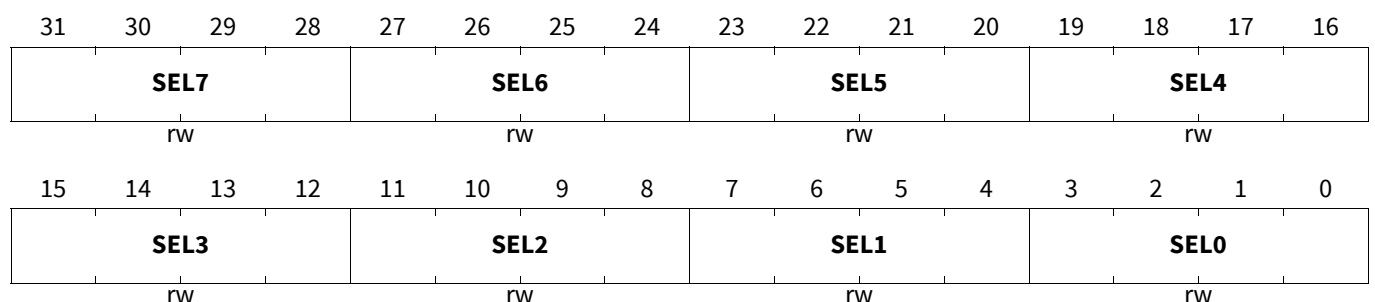
Field	Bits	Type	Description
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... 3_H Reserved, do not use 4_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 5_H Reserved, do not use 6_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 7_H Reserved, do not use 8_H CDTM0_DTM5_0_N, ATOM0_4_N, Inverted dead-time output of ATOM0, channel 4 9_H CDTM1_DTM5_0_N, ATOM1_4_N, Inverted dead-time output of ATOM1, channel 4 A_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 B_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 7_H Reserved, do not use ... B_H Reserved, do not use</p>

GTM_TOUTSELn (n=15)

Timer Output Select Register

(09FD60_H+n*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... 6_H Reserved, do not use 7_H ,, Reserved, do not use 8_H Reserved, do not use 9_H CDTM2_DTM5_1_N, ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 A_H CDTM3_DTM5_1_N, ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 B_H Reserved, do not use</p>
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_1_N, TOM0_5_N, Inverted dead-time output of TOM0, channel 5 7_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>

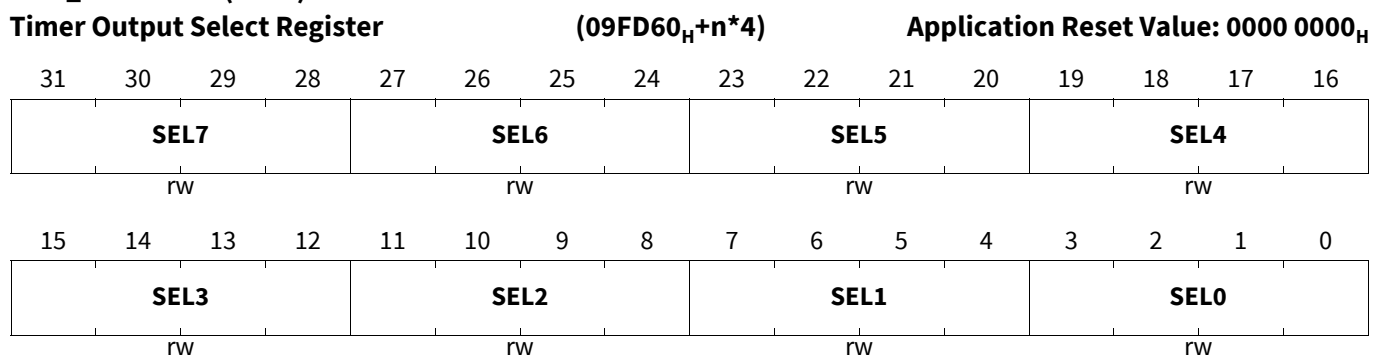
Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_3_N, TOM0_7_N, Inverted dead-time output of TOM0, channel 7 7_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... 4_H Reserved, do not use 5_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 6_H Reserved, do not use 7_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 8_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>

GTM_TOUTSELn (n=16)



Field	Bits	Type	Description
SELx (x=0)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H TOM1_8, Output of TOM1, channel 8 1_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 7_H Reserved, do not use ... 9_H Reserved, do not use A_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H TOM1_9, Output of TOM1, channel 9 1_H Reserved, do not use ... 5_H Reserved, do not use 6_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 7_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=2)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=3)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=4)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note: SELx values not explicitly defined here are equivalent to the last defined SELx setting.</i></p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=6)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>
SELx (x=7)	4*x+3:4*x	rw	<p>TOUT(n*8 + x) Output Selection This bit field defines which timer output is connected as TOUT(n*8+x).</p> <p><i>Note:</i> SELx values not explicitly defined here are equivalent to the last defined SELx setting.</p> <p>0_H Reserved, do not use ... B_H Reserved, do not use</p>

Generic Timer Module (GTM)

26.3.4 GTM DTMAUXINSEL Connections

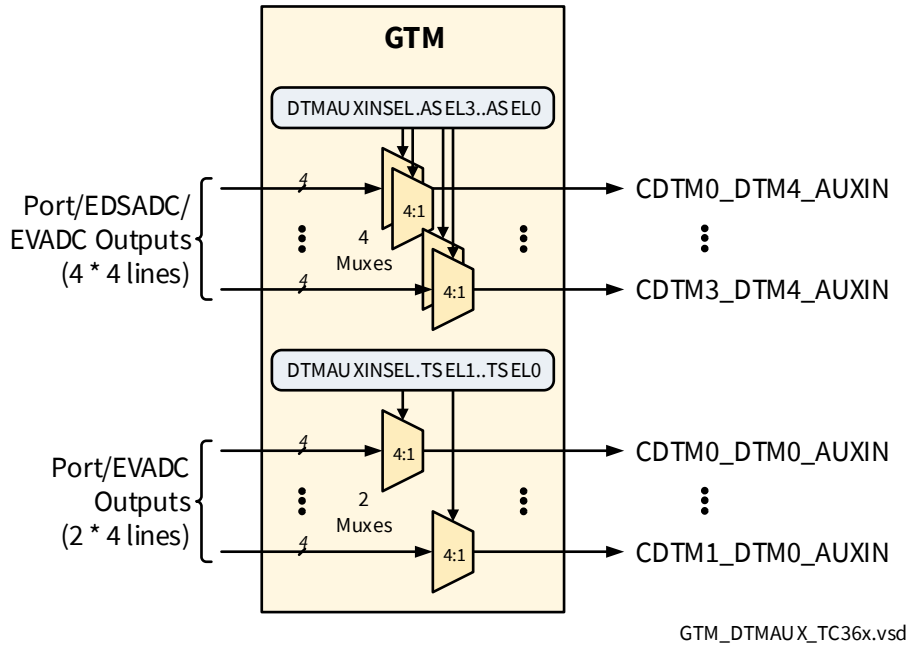


Figure 10 DTM_AUXIN Connections Overview



GTM_DTMAUXINSEL_Registers_TC36x.vsd

Figure 11 DTM_AUXIN Connections Registers Overview

DTM_AUX Input Selection Register

GTM_DTMAUXINSEL

DTM_AUX Input Selection Register

(09FFD8_H)

Application Reset Value: 0000 0000_H

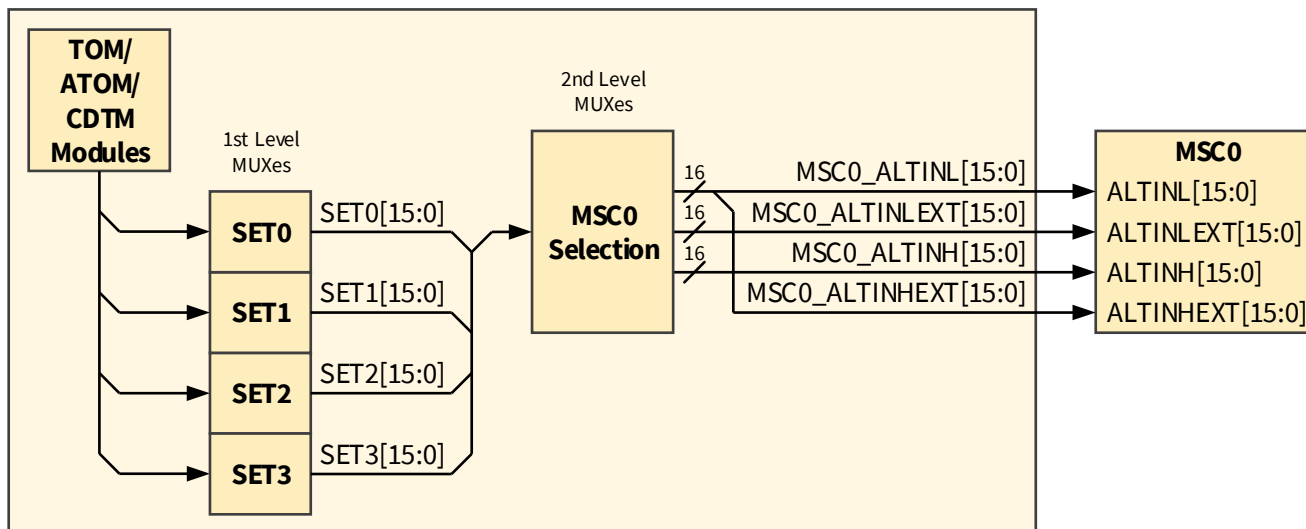
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												TSEL1		TSEL0	
r												rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								ASEL3		ASEL2		ASEL1		ASEL0	
r								rw		rw		rw		rw	

Generic Timer Module (GTM)

Field	Bits	Type	Description
ASELx (x=0)	2*x+1:2*x	rw	CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3) This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 _B P02.0 , Port pad input 01 _B P02.8 , Port pad input 10 _B SWIB0 , EDSADC within-band signal 0 11 _B CBFLOUT0 , EVADC common boundary flag output 0
ASELx (x=1)	2*x+1:2*x	rw	CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3) This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 _B P21.2 , Port pad input 01 _B P20.1 , Port pad input 10 _B SWIB1 , EDSADC within-band signal 1 11 _B CBFLOUT1 , EVADC common boundary flag output 1
ASELx (x=2)	2*x+1:2*x	rw	CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3) This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 _B P14.5 , Port pad input 01 _B P11.0 , Port pad input (BGA only) 10 _B SWIB2 , EDSADC within-band signal 2 11 _B CBFLOUT2 , EVADC common boundary flag output 2
ASELx (x=3)	2*x+1:2*x	rw	CDTMx_DTM4_AUX Input Selection (ATOMx_CH0...3) This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM4_AUX input. 00 _B P22.4 , Port pad input (BGA only) 01 _B P22.9 , Port pad input (BGA only) 10 _B SWIB3 , EDSADC within-band signal 3 11 _B CBFLOUT3 , EVADC common boundary flag output 3
TSELx (x=0)	2*x+17:2*x+16	rw	CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3) This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 _B P14.4 , Port pad input 01 _B P10.1 , Port pad input (FC1BFLOUT) 10 _B P00.7 , Port pad input (FC2BFLOUT) 11 _B CBFLOUT0 , EVADC common boundary flag output 0
TSELx (x=1)	2*x+17:2*x+16	rw	CDTMx_DTM0_AUX Input Selection (TOMx_CH0...3) This bit field defines which GPIO/DSADC/EVADC signal is connected to the CDTMx_DTM0_AUX input. 00 _B P34.0 , Reserved, do not use (TC33x only) 01 _B P00.5 , Port pad input (FC0BFLOUT) 10 _B P33.0 , Port pad input (not QFP144) (FC2BFLOUT) 11 _B CBFLOUT1 , EVADC common boundary flag output 1
0	15:8, 31:20	r	Reserved Read as 0, shall be written with 0.

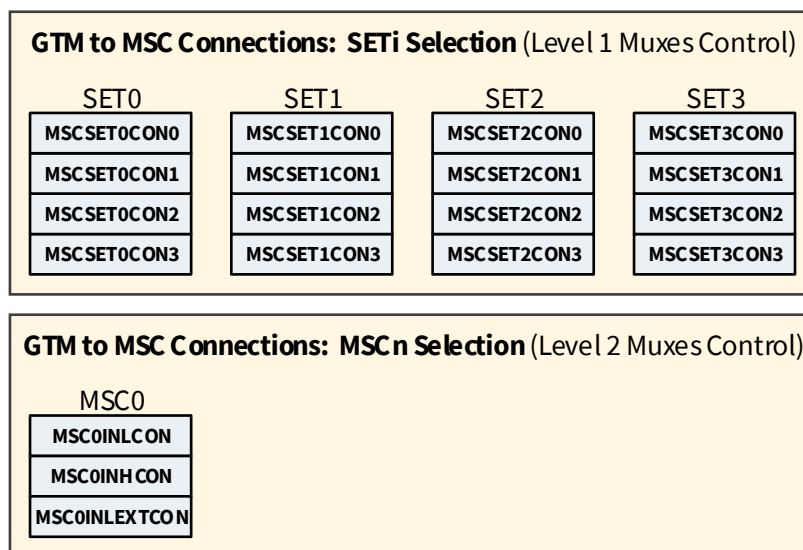
Generic Timer Module (GTM)

26.3.5 GTM to MSC (Micro Second Channel) Connections



GTM_MSC_Connections_Overview_TC36x.vsd

Figure 12 GTM to MSC Connections Overview



GTM_MSC_Registers_TC36x.vsd

Figure 13 GTM to MSC Connections Registers Overview

Generic Timer Module (GTM)

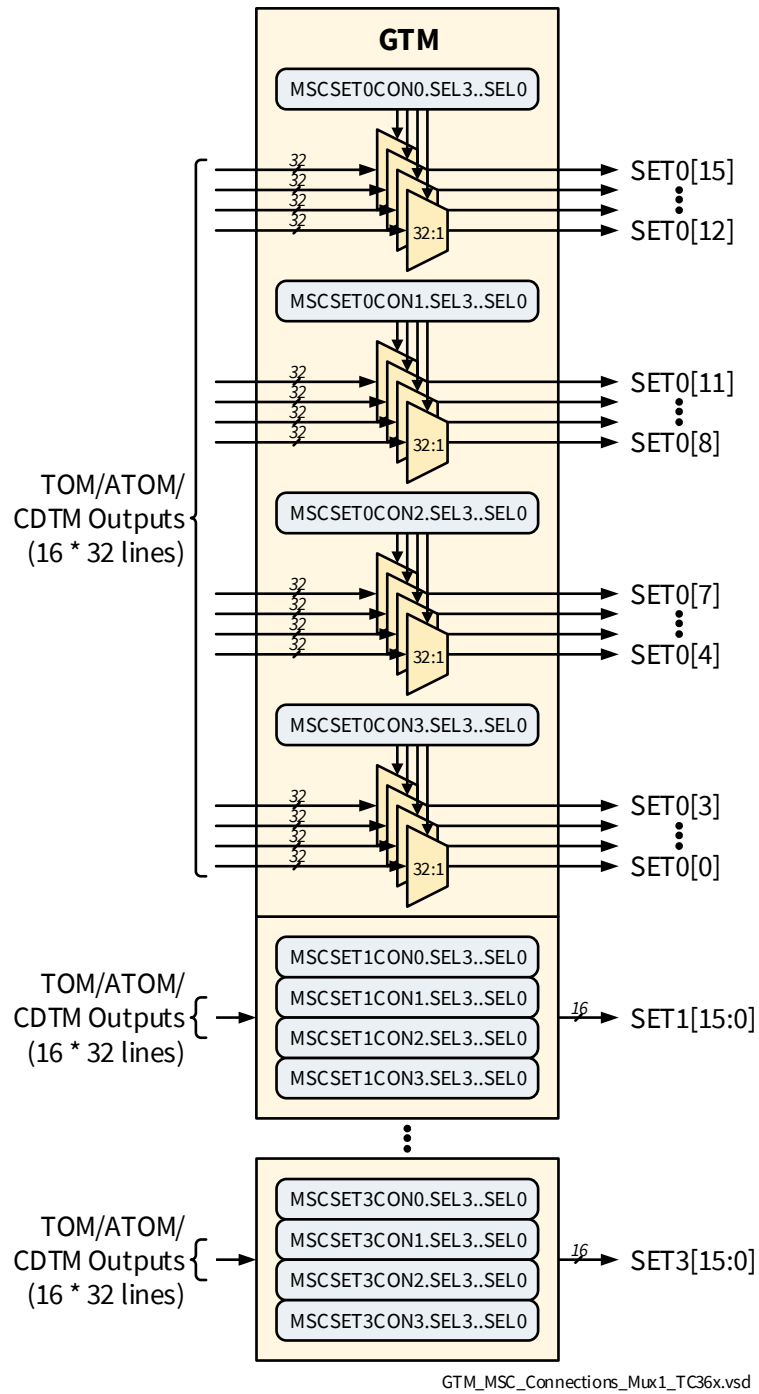


Figure 14 GTM to MSC Connections, 1st Level Muxes Overview

Generic Timer Module (GTM)

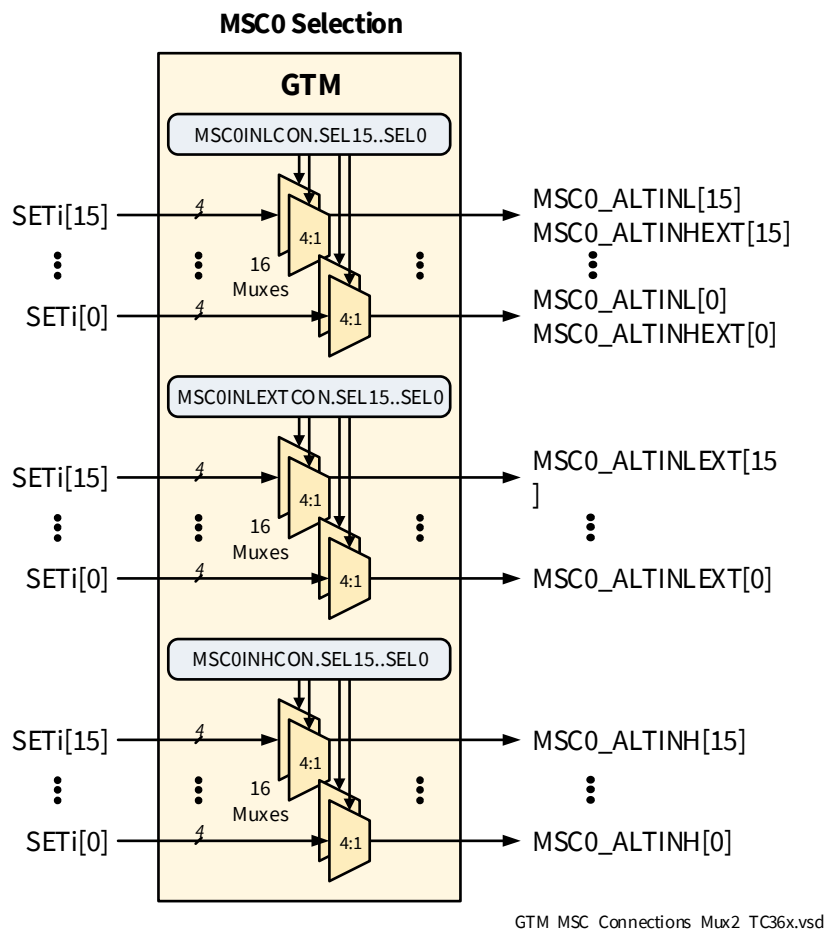


Figure 15 GTM to MSC Connections, 2nd Level Muxes Overview

Table 222 GTM to MSC Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
MSCSET0CON0	MSC Set 0 Control 0 Register (i=0;j=0)	SEL0..SEL3	Page 162
MSCSET0CON1	MSC Set 0 Control 1 Register (i=0;j=1)	SEL4..SEL7	Page 164
MSCSET0CON2	MSC Set 0 Control 2 Register (i=0;j=2)	SEL8..SEL11	Page 165
MSCSET0CON3	MSC Set 0 Control 3 Register (i=0;j=3)	SEL12..SEL15	Page 167
MSCSET1CON0	MSC Set 1 Control 0 Register (i=1;j=0)	SEL0..SEL3	Page 168
MSCSET1CON1	MSC Set 1 Control 1 Register (i=1;j=1)	SEL4..SEL7	Page 170
MSCSET1CON2	MSC Set 1 Control 2 Register (i=1;j=2)	SEL8..SEL11	Page 171
MSCSET1CON3	MSC Set 1 Control 3 Register (i=1;j=3)	SEL12..SEL15	Page 173
MSCSET2CON0	MSC Set 2 Control 0 Register (i=2;j=0)	SEL0..SEL3	Page 174
MSCSET2CON1	MSC Set 2 Control 1 Register (i=2;j=1)	SEL4..SEL7	Page 175
MSCSET2CON2	MSC Set 2 Control 2 Register (i=2;j=2)	SEL8..SEL11	Page 176
MSCSET2CON3	MSC Set 2 Control 3 Register (i=2;j=3)	SEL12..SEL15	Page 177
MSCSET3CON0	MSC Set 3 Control 0 Register (i=3;j=0)	SEL0..SEL3	Page 178

Generic Timer Module (GTM)

Table 222 GTM to MSC Connections Registers Overview (cont'd)

Register	Long Name	Selection Bitfields	Page
MSCSET3CON1	MSC Set 3 Control 1 Register (i=3;j=1)	SEL4..SEL7	Page 179
MSCSET3CON2	MSC Set 3 Control 2 Register (i=3;j=2)	SEL8..SEL11	Page 180
MSCSET3CON3	MSC Set 3 Control 3 Register (i=3;j=3)	SEL12..SEL15	Page 181
MSC0INLCON	MSC0 Input Low Control Register	SEL0..SEL15	Page 182
MSC0INHCON	MSC0 Input High Control Register	SEL0..SEL15	Page 182
MSC0INLEXTCON	MSC0 Input Low Extended Control Register	SEL0..SEL15	Page 183

MSC Set i Control j Register

GTM_MSCSETiCONj (i=0;j=0)

MSC Set i Control j Register (09FF00_H+i*10_H+j*4) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL3				0		SEL2							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL1				0		SEL0							
r		rw				r		rw							

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELk (k=0-3)	8*k+4:8*k	rw	<p>Set 0[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 01_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 02_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 03_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 04_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 05_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 06_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 07_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 08_H TOM0_8, Output of TOM0, channel 8 09_H TOM0_9, Output of TOM0, channel 9 0A_H TOM0_10, Output of TOM0, channel 10 0B_H TOM0_11, Output of TOM0, channel 11 0C_H TOM0_12, Output of TOM0, channel 12 0D_H TOM0_13, Output of TOM0, channel 13 0E_H TOM0_14, Output of TOM0, channel 14 0F_H TOM0_15, Output of TOM0, channel 15 10_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 11_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 12_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 13_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 14_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 15_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 16_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 17_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 18_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 19_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 1A_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 1B_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 1C_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 1D_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 1E_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 1F_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=0;j=1)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL7				0		SEL6							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL5				0		SEL4							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p>Set 0[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 01_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 02_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 03_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 04_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 05_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 06_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 07_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 08_H TOM0_8, Output of TOM0, channel 8 09_H TOM0_9, Output of TOM0, channel 9 0A_H TOM0_10, Output of TOM0, channel 10 0B_H TOM0_11, Output of TOM0, channel 11 0C_H TOM0_12, Output of TOM0, channel 12 0D_H TOM0_13, Output of TOM0, channel 13 0E_H TOM0_14, Output of TOM0, channel 14 0F_H TOM0_15, Output of TOM0, channel 15 10_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 11_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 12_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 13_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 14_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 15_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 16_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 17_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 18_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 19_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 1A_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 1B_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 1C_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 1D_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 1E_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 1F_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
0	31:29, 23:21, 15:13, 7:5	r	Reserved Read as 0, shall be written with 0.

GTM_MSCSETiCONj (i=0;j=2)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL11				0		SEL10							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL9				0		SEL8							
r		rw				r		rw							

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELk (k=8-11)	8*k-60:8*k-64	rw	<p>Set 0[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 01_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 02_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 03_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 04_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 05_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 06_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 07_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 08_H TOM0_8, Output of TOM0, channel 8 09_H TOM0_9, Output of TOM0, channel 9 0A_H TOM0_10, Output of TOM0, channel 10 0B_H TOM0_11, Output of TOM0, channel 11 0C_H TOM0_12, Output of TOM0, channel 12 0D_H TOM0_13, Output of TOM0, channel 13 0E_H TOM0_14, Output of TOM0, channel 14 0F_H TOM0_15, Output of TOM0, channel 15 10_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 11_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 12_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 13_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 14_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 15_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 16_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 17_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 18_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 19_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 1A_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 1B_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 1C_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 1D_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 1E_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 1F_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=0;j=3)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL15				0		SEL14							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL13				0		SEL12							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=12-15)	8*k-92:8*k-96	rw	<p>Set 0[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM0_0, TOM0_0, Dead-time output of TOM0, channel 0 01_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1 02_H CDTM0_DTM0_2, TOM0_2, Dead-time output of TOM0, channel 2 03_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 04_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 05_H CDTM0_DTM1_1, TOM0_5, Dead-time output of TOM0, channel 5 06_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 07_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 08_H TOM0_8, Output of TOM0, channel 8 09_H TOM0_9, Output of TOM0, channel 9 0A_H TOM0_10, Output of TOM0, channel 10 0B_H TOM0_11, Output of TOM0, channel 11 0C_H TOM0_12, Output of TOM0, channel 12 0D_H TOM0_13, Output of TOM0, channel 13 0E_H TOM0_14, Output of TOM0, channel 14 0F_H TOM0_15, Output of TOM0, channel 15 10_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0 11_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1 12_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2 13_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 14_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 15_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 16_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 17_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 18_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0 19_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1 1A_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2 1B_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 1C_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 1D_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 1E_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 1F_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
0	31:29, 23:21, 15:13, 7:5	r	Reserved Read as 0, shall be written with 0.

GTM_MSCSETiCONj (i=1;j=0)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL3				0		SEL2							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL1				0		SEL0							
r		rw				r		rw							

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELk (k=0-3)	8*k+4:8*k	rw	<p>Set 1[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 01_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 02_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 03_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 04_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 05_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 06_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 07_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 08_H TOM1_8, Output of TOM1, channel 8 09_H TOM1_9, Output of TOM1, channel 9 0A_H TOM1_10, Output of TOM1, channel 10 0B_H TOM1_11, Output of TOM1, channel 11 0C_H TOM1_12, Output of TOM1, channel 12 0D_H TOM1_13, Output of TOM1, channel 13 0E_H TOM1_14, Output of TOM1, channel 14 0F_H TOM1_15, Output of TOM1, channel 15 10_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 11_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 12_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 13_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 14_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 15_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 16_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 17_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=1;j=1)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL7				0		SEL6							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL5				0		SEL4							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p>Set 1[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 01_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 02_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 03_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 04_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 05_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 06_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 07_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 08_H TOM1_8, Output of TOM1, channel 8 09_H TOM1_9, Output of TOM1, channel 9 0A_H TOM1_10, Output of TOM1, channel 10 0B_H TOM1_11, Output of TOM1, channel 11 0C_H TOM1_12, Output of TOM1, channel 12 0D_H TOM1_13, Output of TOM1, channel 13 0E_H TOM1_14, Output of TOM1, channel 14 0F_H TOM1_15, Output of TOM1, channel 15 10_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 11_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 12_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 13_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 14_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 15_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 16_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 17_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
0	31:29, 23:21, 15:13, 7:5	r	Reserved Read as 0, shall be written with 0.

GTM_MSCSETiCONj (i=1;j=2)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL11				0		SEL10							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL9				0		SEL8							
r		rw				r		rw							

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELk (k=8-11)	8*k-60:8*k-64	rw	<p>Set 1[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 01_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 02_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 03_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 04_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 05_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 06_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 07_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 08_H TOM1_8, Output of TOM1, channel 8 09_H TOM1_9, Output of TOM1, channel 9 0A_H TOM1_10, Output of TOM1, channel 10 0B_H TOM1_11, Output of TOM1, channel 11 0C_H TOM1_12, Output of TOM1, channel 12 0D_H TOM1_13, Output of TOM1, channel 13 0E_H TOM1_14, Output of TOM1, channel 14 0F_H TOM1_15, Output of TOM1, channel 15 10_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 11_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 12_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 13_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 14_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 15_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 16_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 17_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=1;j=3)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL15				0		SEL14							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL13				0		SEL12							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=12-15)	8*k-92:8*k-96	rw	<p>Set 1[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM1_DTM0_0, TOM1_0, Dead-time output of TOM1, channel 0 01_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1 02_H CDTM1_DTM0_2, TOM1_2, Dead-time output of TOM1, channel 2 03_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 04_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 05_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5 06_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 07_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 08_H TOM1_8, Output of TOM1, channel 8 09_H TOM1_9, Output of TOM1, channel 9 0A_H TOM1_10, Output of TOM1, channel 10 0B_H TOM1_11, Output of TOM1, channel 11 0C_H TOM1_12, Output of TOM1, channel 12 0D_H TOM1_13, Output of TOM1, channel 13 0E_H TOM1_14, Output of TOM1, channel 14 0F_H TOM1_15, Output of TOM1, channel 15 10_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0 11_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1 12_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2 13_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 14_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 15_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 16_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 17_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
0	31:29, 23:21, 15:13, 7:5	r	Reserved Read as 0, shall be written with 0.

GTM_MSCSETiCONj (i=2;j=0)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL3				0		SEL2							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL1				0		SEL0							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=0-3)	8*k+4:8*k	rw	Set 2[k] Input Selection This bit field defines the GTM timer source configured as Set i signal k out. 00 _H Reserved, do not use ... 17 _H Reserved, do not use 18 _H CDTM3_DTM4_0, ATOM3_0 , Dead-time output of ATOM3, channel 0 19 _H CDTM3_DTM4_1, ATOM3_1 , Dead-time output of ATOM3, channel 1 1A _H CDTM3_DTM4_2, ATOM3_2 , Dead-time output of ATOM3, channel 2 1B _H CDTM3_DTM4_3, ATOM3_3 , Dead-time output of ATOM3, channel 3 1C _H CDTM3_DTM5_0, ATOM3_4 , Dead-time output of ATOM3, channel 4 1D _H CDTM3_DTM5_1, ATOM3_5 , Dead-time output of ATOM3, channel 5 1E _H CDTM3_DTM5_2, ATOM3_6 , Dead-time output of ATOM3, channel 6 1F _H CDTM3_DTM5_3, ATOM3_7 , Dead-time output of ATOM3, channel 7
0	31:29, 23:21, 15:13, 7:5	r	Reserved Read as 0, shall be written with 0.

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=2;j=1)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL7				0		SEL6							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL5				0		SEL4							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p>Set 2[k] Input Selection This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H Reserved, do not use ... 17_H Reserved, do not use 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=2;j=2)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL11				0		SEL10							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL9				0		SEL8							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=8-11)	8*k-60:8*k-64	rw	<p>Set 2[k] Input Selection This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H Reserved, do not use ... 17_H Reserved, do not use 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=2;j=3)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL15				0		SEL14							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL13				0		SEL12							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=12-15)	8*k-92:8*k-96	rw	<p>Set 2[k] Input Selection This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H Reserved, do not use ... 17_H Reserved, do not use 18_H CDTM3_DTM4_0, ATOM3_0, Dead-time output of ATOM3, channel 0 19_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1 1A_H CDTM3_DTM4_2, ATOM3_2, Dead-time output of ATOM3, channel 2 1B_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 1C_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 1D_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 1E_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 1F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=3;j=0)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			SEL3				0			SEL2					
r			rw				r			rw					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			SEL1				0			SEL0					
r			rw				r			rw					

Field	Bits	Type	Description
SELk (k=0-3)	8*k+4:8*k	rw	<p>Set 3[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0</p> <p>01_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1</p> <p>02_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2</p> <p>03_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3</p> <p>04_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>05_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>06_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>07_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>08_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0</p> <p>09_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1</p> <p>0A_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2</p> <p>0B_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p> <p>0C_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>0D_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>0E_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>0F_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>10_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0</p> <p>11_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1</p> <p>12_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2</p> <p>13_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>14_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>15_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5</p> <p>16_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6</p> <p>17_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>18_H Reserved, do not use</p> <p>...</p> <p>1F_H Reserved, do not use</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=3;j=1)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL7				0		SEL6							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL5				0		SEL4							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=4-7)	8*k-28:8*k-32	rw	<p>Set 3[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0</p> <p>01_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1</p> <p>02_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2</p> <p>03_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3</p> <p>04_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>05_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>06_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>07_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>08_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0</p> <p>09_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1</p> <p>0A_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2</p> <p>0B_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p> <p>0C_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>0D_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>0E_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>0F_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>10_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0</p> <p>11_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1</p> <p>12_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2</p> <p>13_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>14_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>15_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5</p> <p>16_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6</p> <p>17_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>18_H Reserved, do not use</p> <p>...</p> <p>1F_H Reserved, do not use</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=3;j=2)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL11				0		SEL10							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL9				0		SEL8							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=8-11)	8*k-60:8*k-64	rw	<p>Set 3[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0</p> <p>01_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1</p> <p>02_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2</p> <p>03_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3</p> <p>04_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>05_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>06_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>07_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>08_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0</p> <p>09_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1</p> <p>0A_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2</p> <p>0B_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p> <p>0C_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>0D_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>0E_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>0F_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>10_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0</p> <p>11_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1</p> <p>12_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2</p> <p>13_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>14_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>15_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5</p> <p>16_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6</p> <p>17_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>18_H Reserved, do not use</p> <p>...</p> <p>1F_H Reserved, do not use</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

GTM_MSCSETiCONj (i=3;j=3)

MSC Set i Control j Register

(09FF00_H+i*10_H+j*4)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		SEL15				0		SEL14							
r		rw				r		rw							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SEL13				0		SEL12							
r		rw				r		rw							

Field	Bits	Type	Description
SELk (k=12-15)	8*k-92:8*k-96	rw	<p>Set 3[k] Input Selection</p> <p>This bit field defines the GTM timer source configured as Set i signal k out.</p> <p>00_H CDTM0_DTM4_0, ATOM0_0, Dead-time output of ATOM0, channel 0</p> <p>01_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1</p> <p>02_H CDTM0_DTM4_2, ATOM0_2, Dead-time output of ATOM0, channel 2</p> <p>03_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3</p> <p>04_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>05_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>06_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>07_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>08_H CDTM1_DTM4_0, ATOM1_0, Dead-time output of ATOM1, channel 0</p> <p>09_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1</p> <p>0A_H CDTM1_DTM4_2, ATOM1_2, Dead-time output of ATOM1, channel 2</p> <p>0B_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p> <p>0C_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>0D_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>0E_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>0F_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>10_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0</p> <p>11_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1</p> <p>12_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2</p> <p>13_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>14_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>15_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5</p> <p>16_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6</p> <p>17_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>18_H Reserved, do not use</p> <p>...</p> <p>1F_H Reserved, do not use</p>
0	31:29, 23:21, 15:13, 7:5	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

MSCi Input Low Control Register

GTM_MSCiINLCON (i=0)

MSCi Input Low Control Register

(09FF90_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL15		SEL14		SEL13		SEL12		SEL11		SEL10		SEL9		SEL8	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL7		SEL6		SEL5		SEL4		SEL3		SEL2		SEL1		SEL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
SELx (x=0-15)	2*x+1:2*x	rw	<p>GTM MSCq Low x Output Selection</p> <p>GTM output gtm_mscq[low][x] is controlled by the timer output.</p> <p>00_B SET0, Outputs SET0[15:0] selected</p> <p>01_B SET1, Outputs SET1[15:0] selected</p> <p>10_B SET2, Outputs SET2[15:0] selected</p> <p>11_B SET3, Outputs SET3[15:0] selected</p>

MSCi Input High Control Register

GTM_MSCiINHCON (i=0)

MSCi Input High Control Register

(09FF94_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL15		SEL14		SEL13		SEL12		SEL11		SEL10		SEL9		SEL8	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL7		SEL6		SEL5		SEL4		SEL3		SEL2		SEL1		SEL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
SELx (x=0-15)	2*x+1:2*x	rw	<p>GTM MSCq High x Output Selection</p> <p>GTM output gtm_mscq[high][x] is controlled by the timer output.</p> <p>00_B SET0, Outputs SET0[15:0] selected</p> <p>01_B SET1, Outputs SET1[15:0] selected</p> <p>10_B SET2, Outputs SET2[15:0] selected</p> <p>11_B SET3, Outputs SET3[15:0] selected</p>

Generic Timer Module (GTM)

MSCi Input Low Extended Control Register

GTM_MSCiINLEXTCON (i=0)

MSCi Input Low Extended Control Register (09FF98_H)

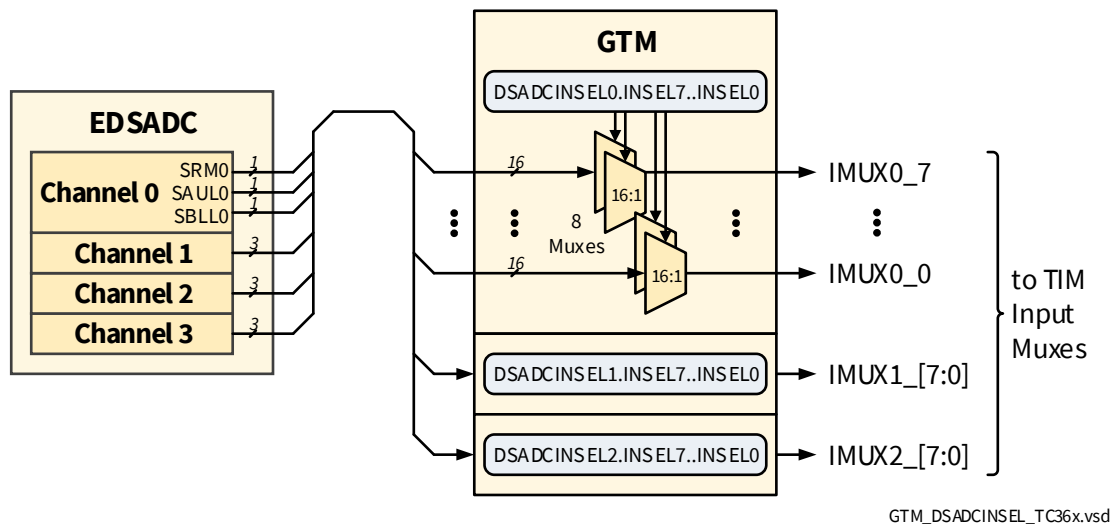
Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL15		SEL14		SEL13		SEL12		SEL11		SEL10		SEL9		SEL8	
rw		rw		rw		rw		rw		rw		rw		rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL7		SEL6		SEL5		SEL4		SEL3		SEL2		SEL1		SEL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
SELx (x=0-15)	2*x+1:2*x	rw	<p>GTM MSCq LowExtended x Output Selection</p> <p>GTM output gtm_mscqaltinext[x] is controlled by the timer output.</p> <p>00_B SET0, Outputs SET0[15:0] selected</p> <p>01_B SET1, Outputs SET1[15:0] selected</p> <p>10_B SET2, Outputs SET2[15:0] selected</p> <p>11_B SET3, Outputs SET3[15:0] selected</p>

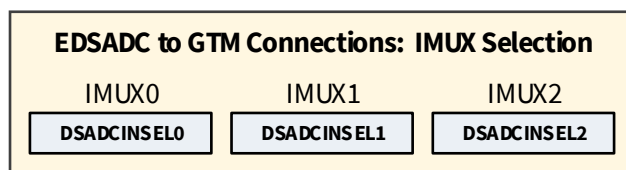
Generic Timer Module (GTM)

26.3.6 EDSADC to GTM TIM Connections



GTM_DSADCINSEL_TC36x.vsd

Figure 16 EDSADC to GTM Connections Overview



GTM_DSADCINSEL_Registers_TC36x.vsd

Figure 17 EDSADC to GTM Connections Registers Overview

Table 223 EDSADC to GTM Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
DSADCINSEL0	DSADC Input Select 0 Register (i=0)	INSEL0..INSEL7	Page 185
DSADCINSEL1	DSADC Input Select 1 Register (i=1)	INSEL0..INSEL7	Page 187
DSADCINSEL2	DSADC Input Select 2 Register (i=2)	INSEL0..INSEL7	Page 190

Generic Timer Module (GTM)

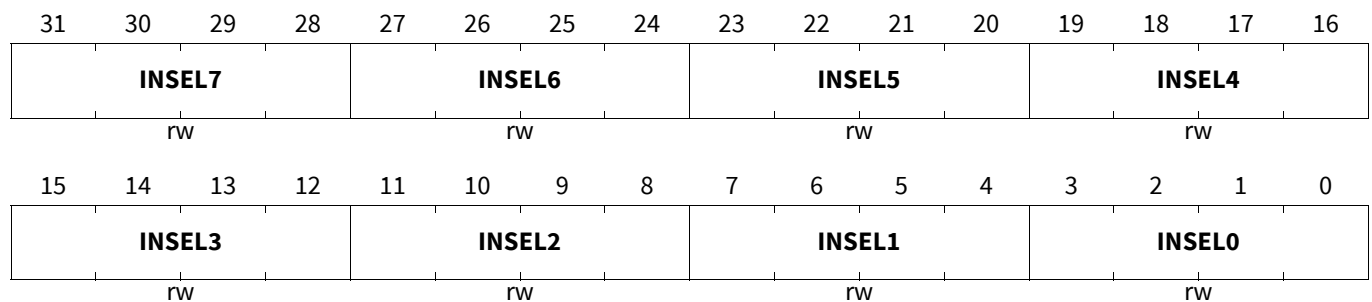
DSADC Input Select i Register

GTM_DSADCINSELi (i=0)

DSADC Input Select i Register

(09FE00_H+i*4)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
INSELj (j=0)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAULO, Input signal is DSADC_SAULO B_H SBLLO, Input signal is DSADC_SBLLO C_H SAUL1, Input signal is DSADC_SAUL1 D_H SBLL1, Input signal is DSADC_SBLL1 E_H Reserved, do not use F_H Reserved, do not use</p>
INSELj (j=1)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL1, Input signal is DSADC_SAUL1 B_H SBLL1, Input signal is DSADC_SBLL1 C_H SAULO, Input signal is DSADC_SAULO D_H SBLLO, Input signal is DSADC_SBLLO E_H Reserved, do not use F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
INSELj (j=2)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL2, Input signal is DSADC_SAUL2 B_H SBLL2, Input signal is DSADC_SBLL2 C_H SAUL3, Input signal is DSADC_SAUL3 D_H SBLL3, Input signal is DSADC_SBLL3 E_H Reserved, do not use F_H Reserved, do not use</p>
INSELj (j=3)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL3, Input signal is DSADC_SAUL3 B_H SBLL3, Input signal is DSADC_SBLL3 C_H SAUL2, Input signal is DSADC_SAUL2 D_H SBLL2, Input signal is DSADC_SBLL2 E_H Reserved, do not use F_H Reserved, do not use</p>
INSELj (j=4)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>

Generic Timer Module (GTM)

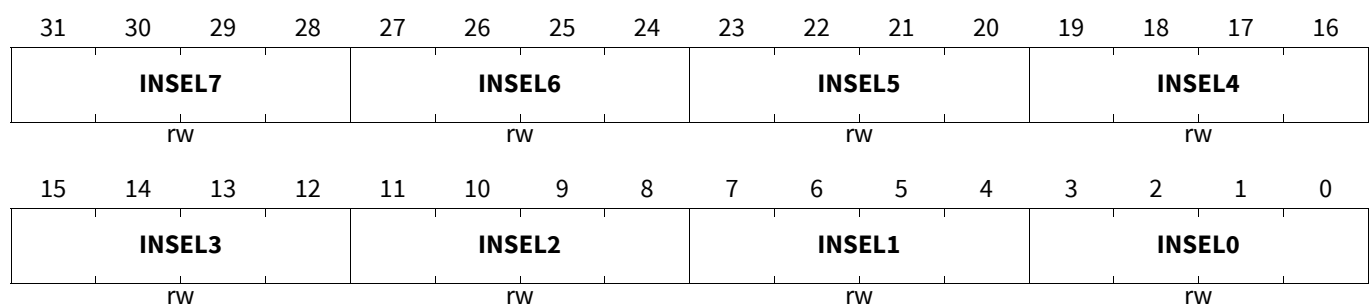
Field	Bits	Type	Description
INSELj (j=5)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=6)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=7)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>

GTM_DSADCINSELi (i=1)

DSADC Input Select i Register

(09FE00_H+i*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
INSELj (j=0)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAULO, Input signal is DSADC_SAULO B_H SBLLO, Input signal is DSADC_SBLLO C_H SAUL1, Input signal is DSADC_SAUL1 D_H SBLL1, Input signal is DSADC_SBLL1 E_H Reserved, do not use F_H Reserved, do not use</p>
INSELj (j=1)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL1, Input signal is DSADC_SAUL1 B_H SBLL1, Input signal is DSADC_SBLL1 C_H SAULO, Input signal is DSADC_SAULO D_H SBLLO, Input signal is DSADC_SBLLO E_H Reserved, do not use F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
INSELj (j=2)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL2, Input signal is DSADC_SAUL2 B_H SBLL2, Input signal is DSADC_SBLL2 C_H SAUL3, Input signal is DSADC_SAUL3 D_H SBLL3, Input signal is DSADC_SBLL3 E_H Reserved, do not use F_H Reserved, do not use</p>
INSELj (j=3)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL3, Input signal is DSADC_SAUL3 B_H SBLL3, Input signal is DSADC_SBLL3 C_H SAUL2, Input signal is DSADC_SAUL2 D_H SBLL2, Input signal is DSADC_SBLL2 E_H Reserved, do not use F_H Reserved, do not use</p>
INSELj (j=4)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>

Generic Timer Module (GTM)

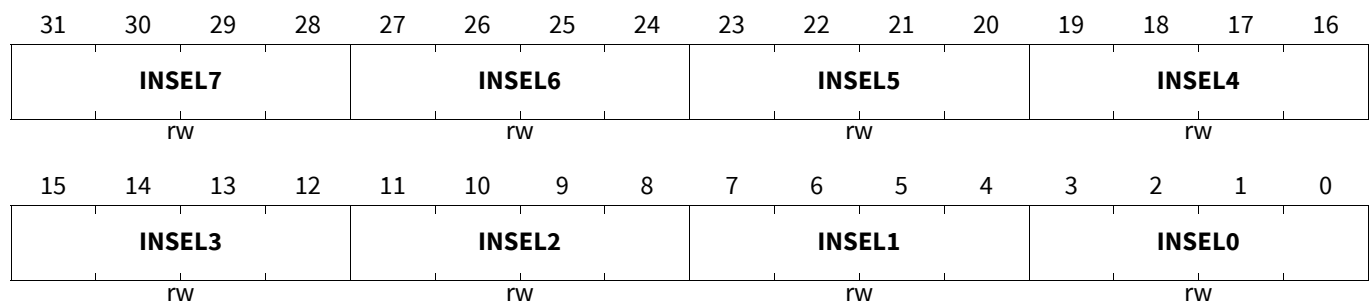
Field	Bits	Type	Description
INSELj (j=5)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=6)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=7)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>

GTM_DSADCINSELi (i=2)

DSADC Input Select i Register

(09FE00_H+i*4)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
INSELj (j=0)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=1)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=2)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=3)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>

Generic Timer Module (GTM)

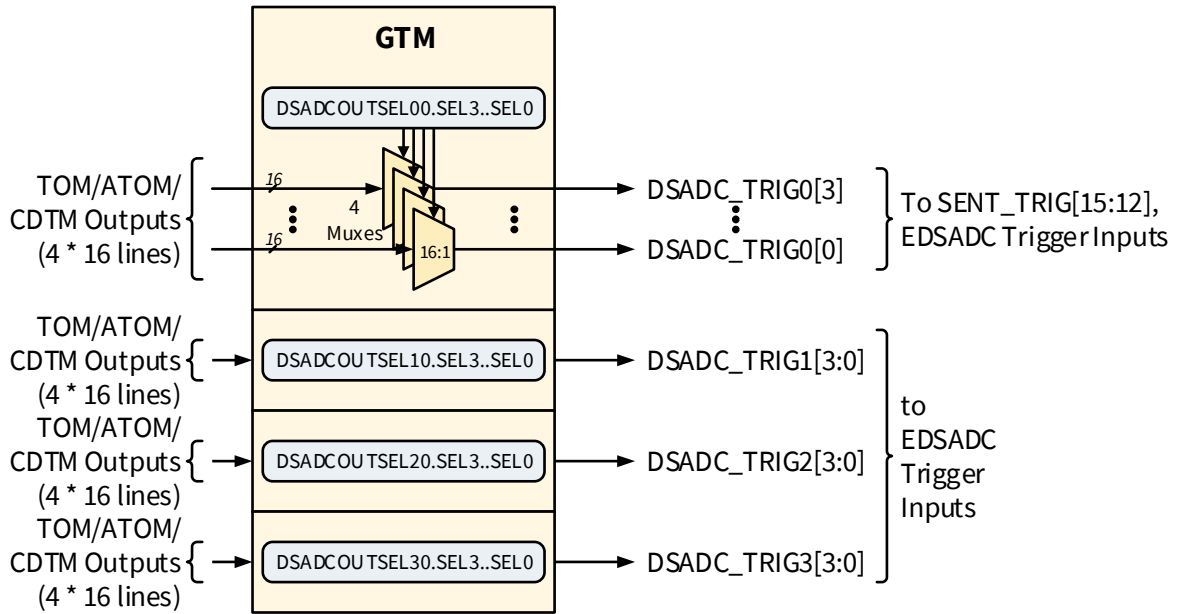
Field	Bits	Type	Description
INSELj (j=4)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=5)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... F_H Reserved, do not use</p>
INSELj (j=6)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAULO, Input signal is DSADC_SAULO B_H SBLLO, Input signal is DSADC_SBLLO C_H SAUL1, Input signal is DSADC_SAUL1 D_H SBLL1, Input signal is DSADC_SBLL1 E_H Reserved, do not use F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
INSELj (j=7)	4*j+3:4*j	rw	<p>In Selection for DSADCn GTM connection</p> <p>This bit field defines which DSADCn output is connected if the channel input mux is configured as DSADC input for TIMi channel j.</p> <p>0_H SRM0, Input signal is DSADC_SRM0 1_H SRM1, Input signal is DSADC_SRM1 2_H SRM2, Input signal is DSADC_SRM2 3_H SRM3, Input signal is DSADC_SRM3 4_H Reserved, do not use ... 9_H Reserved, do not use A_H SAUL1, Input signal is DSADC_SAUL1 B_H SBL11, Input signal is DSADC_SBL11 C_H SAULO, Input signal is DSADC_SAULO D_H SBLLO, Input signal is DSADC_SBLLO E_H Reserved, do not use F_H Reserved, do not use</p>

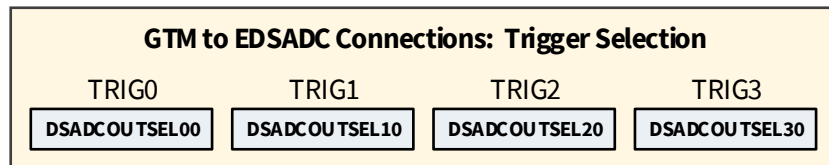
Generic Timer Module (GTM)

26.3.7 GTM to EDSADC Connections



GTM_DSADCOUTSEL_TC36x.vsd

Figure 18 GTM to EDSADC Connections Overview



GTM_DSADCOUTSEL_Registers_TC36x.vsd

Figure 19 GTM to EDSADC Connections Registers Overview

Table 224 GTM to EDSADC Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
DSADCOUTSEL00	DSADC Output Select 00 Register (i=0)	SEL0..SEL3	Page 195
DSADCOUTSEL10	DSADC Output Select 10 Register (i=1)	SEL0..SEL3	Page 196
DSADCOUTSEL20	DSADC Output Select 20 Register (i=2)	SEL0..SEL3	Page 197
DSADCOUTSEL30	DSADC Output Select 30 Register (i=3)	SEL0..SEL3	Page 198

Generic Timer Module (GTM)

Table 225 GTM to EDSADC Connections Overview

Signal	SELi	EDSADC/SENT Trigger Inputs			
		x = 0	x = 1	x = 2	x = 3
DSADC_TRIGx_0	SEL0	ITR0A SENT: TRIG12	ITR0B	ITR0M	ITR0N
DSADC_TRIGx_1	SEL1	ITR1A SENT: TRIG13	ITR1B	ITR1M	ITR1N
DSADC_TRIGx_2	SEL2	ITR2A SENT: TRIG14	ITR2B	ITR2M	ITR2N
DSADC_TRIGx_3	SEL3	ITR3A SENT: TRIG15	ITR3B	ITR3M	ITR3N

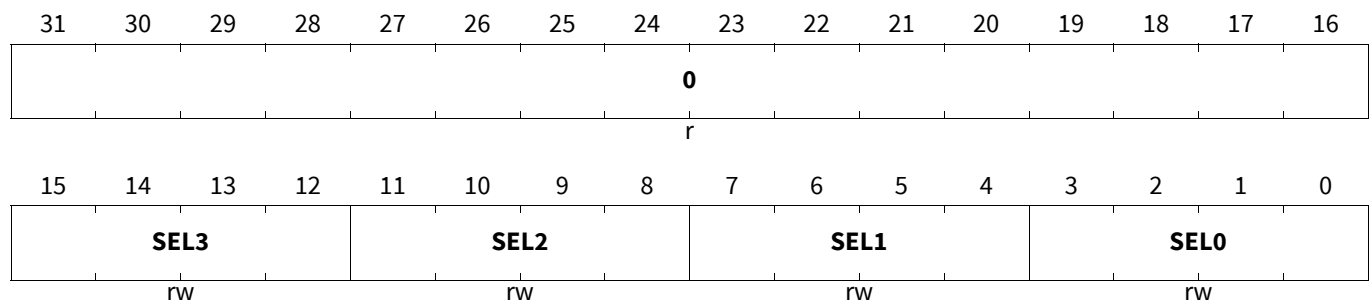
DSADC Output Select i0 Register

GTM_DSADCOUTSELi0 (i=0)

DSADC Output Select i0 Register

(09FE20_H+i*8)

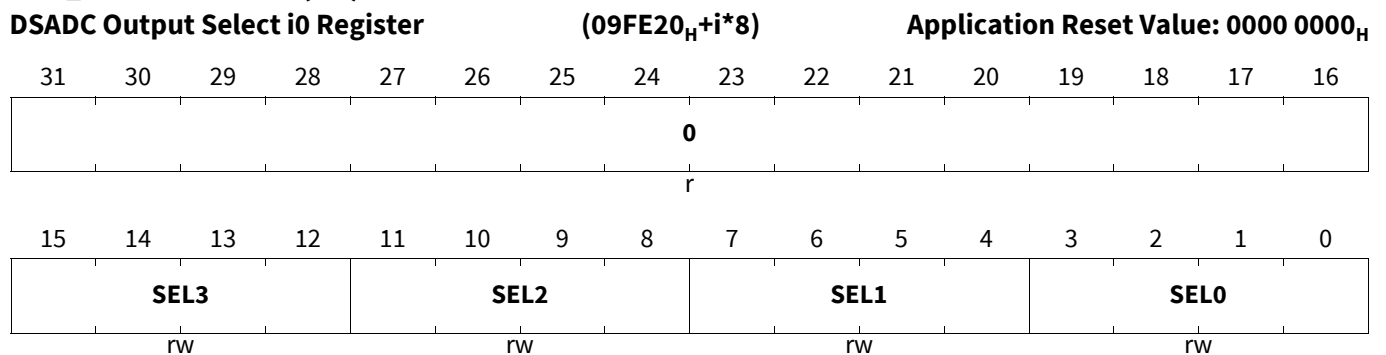
Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p>Output Selection for DSADCx GTM connection This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <p>0_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 1_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 2_H TOM0_13, Output of TOM0, channel 13 3_H TOM0_14, Output of TOM0, channel 14 4_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 5_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 6_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 7_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 8_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 9_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 A_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 B_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 C_H Reserved, do not use ... F_H Reserved, do not use</p>
0	31:16	r	<p>Reserved Read as 0, shall be written with 0.</p>

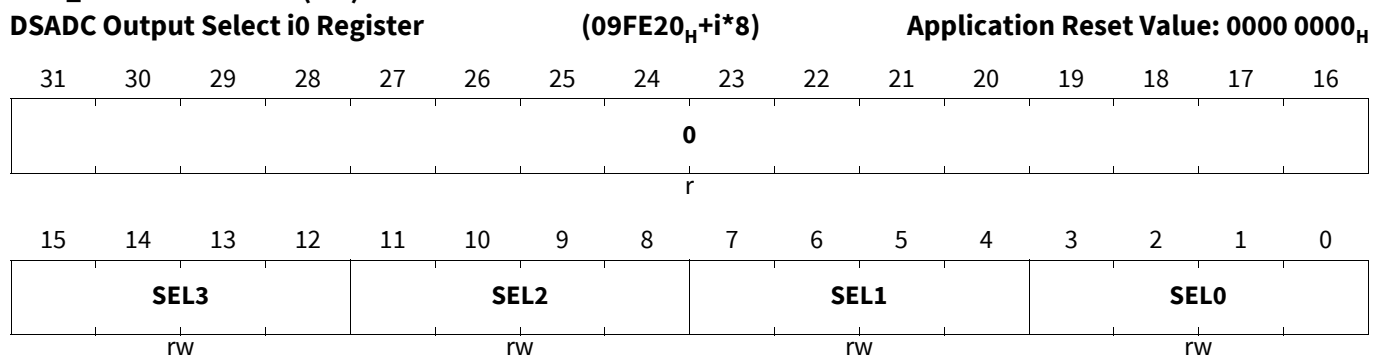
GTM_DSADCOUTSELi0 (i=1)



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p>Output Selection for DSADCx GTM connection This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i.</p> <p>0_H Reserved, do not use ... 3_H Reserved, do not use 4_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4 5_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5 6_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6 7_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 8_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 9_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 A_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 B_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 C_H Reserved, do not use ... F_H Reserved, do not use</p>
0	31:16	r	<p>Reserved Read as 0, shall be written with 0.</p>

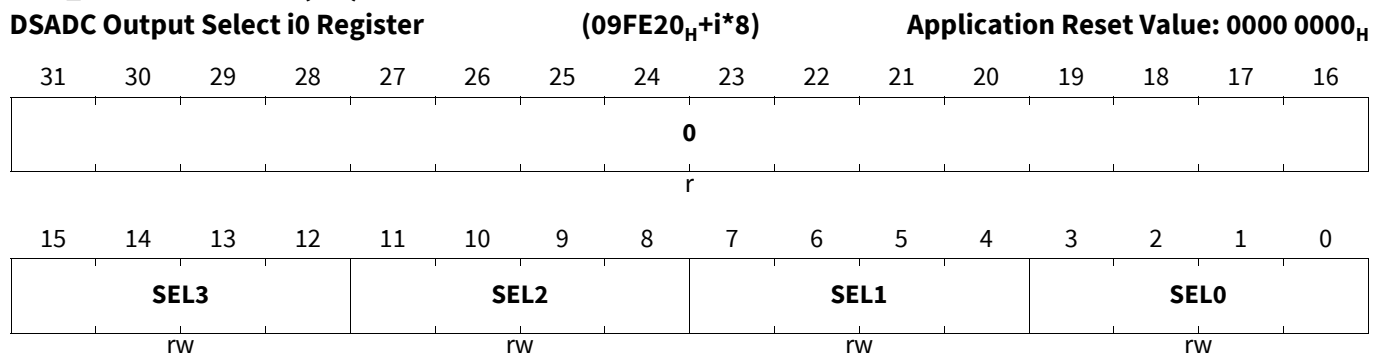
GTM_DSADCOUTSELi0 (i=2)



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	Output Selection for DSADCx GTM connection This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i. 0 _H CDTM1_DTM1_3, TOM1_7 , Dead-time output of TOM1, channel 7 1 _H TOM1_14 , Output of TOM1, channel 14 2 _H Reserved, do not use ... F _H Reserved, do not use
0	31:16	r	Reserved Read as 0, shall be written with 0.

GTM_DSADCOUTSELi0 (i=3)



Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	Output Selection for DSADCx GTM connection This bit field defines which TOM/ATOM channel output is used as DSADCx trigger i. 0 _H CDTM1_DTM1_2, TOM1_6 , Dead-time output of TOM1, channel 6 1 _H Reserved, do not use ... F _H Reserved, do not use
0	31:16	r	Reserved Read as 0, shall be written with 0.

Generic Timer Module (GTM)
26.3.8 EVADC to GTM Connections

The number of FCxBFL and CBFL0UTx signals from the EVADC to the MCS data inputs is product specific. See the following table for the connections available in this device.

Table 226 MCS Data Input Signal Connections

MCS Status Input	Input
MCSSTAT0	FC0BFL
MCSSTAT1	FC1BFL
MCSSTAT2	Reserved
MCSSTAT3	Reserved
MCSSTAT4	Reserved
MCSSTAT5	Reserved
MCSSTAT6	Reserved
MCSSTAT7	Reserved
MCSSTAT8	CBFL0UT0
MCSSTAT9	CBFL0UT1
MCSSTAT10	CBFL0UT2
MCSSTAT11	CBFL0UT3
all other	Reserved

Generic Timer Module (GTM)

26.3.9 GTM to EVADC Connections

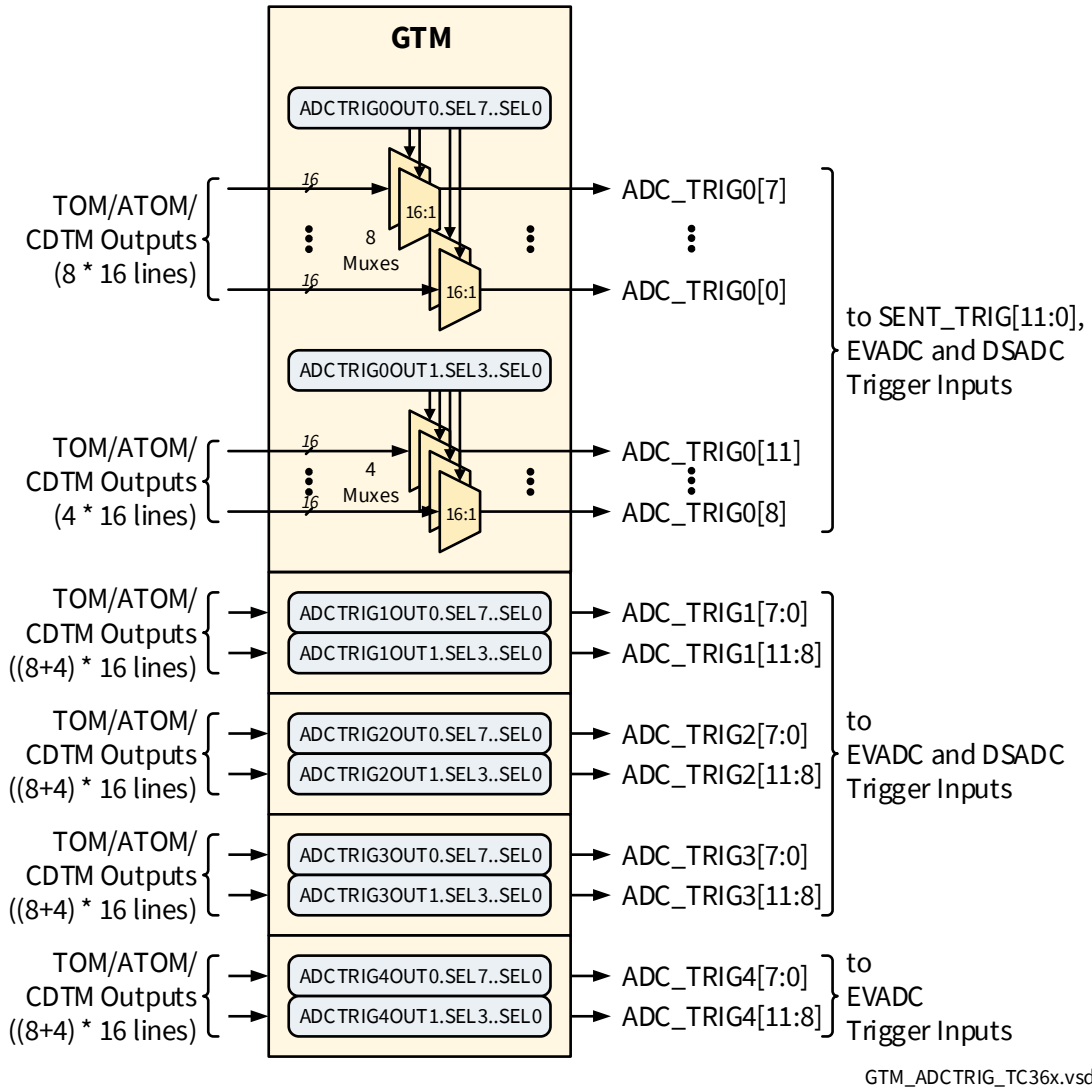


Figure 20 GTM to EVADC Connections Overview

GTM to EVADC Connections: Trigger Selection				
TRIG0	TRIG1	TRIG2	TRIG3	TRIG4
ADCTRIG0OUT0	ADCTRIG1OUT0	ADCTRIG2OUT0	ADCTRIG3OUT0	ADCTRIG4OUT0
ADCTRIG0OUT1	ADCTRIG1OUT1	ADCTRIG2OUT1	ADCTRIG3OUT1	ADCTRIG4OUT1

GTM_ADCTRIG_Registers_TC36x.vsd

Figure 21 GTM to EVADC Connections Registers Overview

Generic Timer Module (GTM)

Table 227 GTM to EVADC Connections Registers Overview

Register	Long Name	Selection Bitfields	Page
ADCTRIG0OUT0	ADC Trigger 0 Output Select 0 Register (i=0)	SEL0..SEL7	Page 202
ADCTRIG0OUT1	ADC Trigger 0 Output Select 1 Register (i=0)	SEL0..SEL3	Page 205
ADCTRIG1OUT0	ADC Trigger 1 Output Select 0 Register (i=1)	SEL0..SEL7	Page 206
ADCTRIG1OUT1	ADC Trigger 1 Output Select 1 Register (i=1)	SEL0..SEL3	Page 209
ADCTRIG2OUT0	ADC Trigger 2 Output Select 0 Register (i=2)	SEL0..SEL7	Page 210
ADCTRIG2OUT1	ADC Trigger 2 Output Select 1 Register (i=2)	SEL0..SEL3	Page 212
ADCTRIG3OUT0	ADC Trigger 3 Output Select 0 Register (i=3)	SEL0..SEL7	Page 213
ADCTRIG3OUT1	ADC Trigger 3 Output Select 1 Register (i=3)	SEL0..SEL3	Page 215
ADCTRIG4OUT0	ADC Trigger 4 Output Select 0 Register (i=4)	SEL0..SEL7	Page 216
ADCTRIG4OUT1	ADC Trigger 4 Output Select 1 Register (i=4)	SEL0..SEL3	Page 216

Table 228 Connections of ADC_TRIGx Signals to ADC/SENT Modules

GTM Trigger Signal	EVADC			EDSADC	SENT
ADC_TRIG0					
ADC_TRIG0_[1:0]	FC[1:0]REQTRI	G[1:0]REQGTA	G[1:0]REQTRI	ITR[1:0]C	TRIG[1:0]
ADC_TRIG0_[3:2]	-	G[3:2]REQGTA	G[3:2]REQTRI	ITR[3:2]C	TRIG[3:2]
ADC_TRIG0_[7:4]	-	-	-	-	TRIG[7:4]
ADC_TRIG0_[9:8]	-	G[9:8]REQGTA	G[9:8]REQTRI	-	TRIG[9:8]
ADC_TRIG0_[11:10]	-	-	-	-	TRIG[11:10]
ADC_TRIG1					
ADC_TRIG1_[1:0]	FC[1:0]REQTRJ	G[1:0]REQGTB	G[1:0]REQTRJ	ITR[1:0]D	-
ADC_TRIG1_[3:2]	-	G[3:2]REQGTB	G[3:2]REQTRJ	ITR[3:2]D	-
ADC_TRIG1_[7:4]	-	-	-	-	-
ADC_TRIG1_[9:8]	-	G[9:8]REQGTB	G[9:8]REQTRJ	-	-
ADC_TRIG1_[11:10]	-	-	-	-	-
ADC_TRIG2					
ADC_TRIG2_[1:0]	FC[1:0]REQTRK	G[1:0]REQGTK	G[1:0]REQTRK	ITR[1:0]K	-
ADC_TRIG2_[3:2]	-	G[3:2]REQGTK	G[3:2]REQTRK	ITR[3:2]K	-
ADC_TRIG2_[7:4]	-	-	-	-	-
ADC_TRIG2_[9:8]	-	G[9:8]REQGTK	G[9:8]REQTRK	-	-
ADC_TRIG2_[11:10]	-	-	-	-	-
ADC_TRIG3					
ADC_TRIG3_[3:0]	-	G[3:0]REQGTL	G[3:0]REQTRL	ITR[3:0]L	-
ADC_TRIG3_[7:4]	-	-	-	-	-
ADC_TRIG3_[9:8]	FC[1:0]REQTRL	G[9:8]REQGTL	G[9:8]REQTRL	-	-
ADC_TRIG3_[11:10]	-	-	-	-	-

Generic Timer Module (GTM)

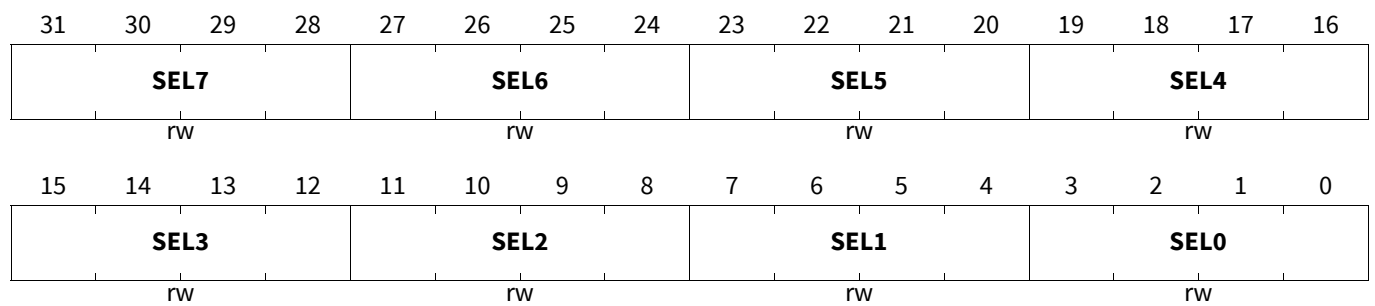
Table 228 Connections of ADC_TRIGx Signals to ADC/SENT Modules (cont'd)

GTM Trigger Signal	EVADC	EDSADC	SENT
ADC_TRIG4			
ADC_TRIG4_[3:0]	-	G[3:0]REQGTL	G[3:0]REQTRL
ADC_TRIG4_[7:4]	-	-	-
ADC_TRIG4_[9:8]	FC[1:0]REQTRM	G[9:8]REQGTL	G[9:8]REQTRL
ADC_TRIG4_[11:10]	-	-	-

ADC Trigger i Output Select 0 Register

GTM_ADCTRIGiOUT0 (i=0)

ADC Trigger i Output Select 0 Register (09FE40_H+i*8) Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-2)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection</p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger</p> <p>1_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6</p> <p>2_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7</p> <p>3_H TOM0_13, Output of TOM0, channel 13</p> <p>4_H TOM0_14, Output of TOM0, channel 14</p> <p>5_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>6_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>7_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>8_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>9_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>A_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>B_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>C_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>D_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>E_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3-4)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection</p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger</p> <p>1_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6</p> <p>2_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7</p> <p>3_H TOM0_13, Output of TOM0, channel 13</p> <p>4_H TOM0_14, Output of TOM0, channel 14</p> <p>5_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>6_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>7_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>8_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>9_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6</p> <p>A_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7</p> <p>B_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>C_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5</p> <p>D_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4</p> <p>E_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5</p> <p>F_H Reserved, do not use</p>

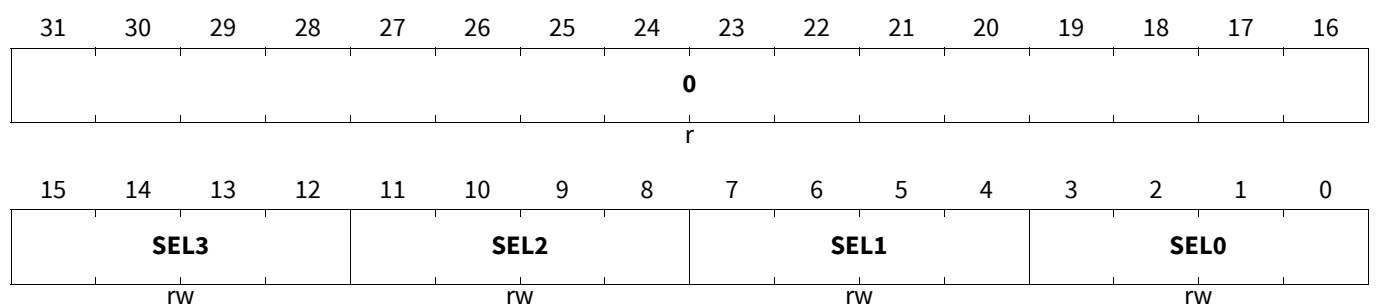
Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5-7)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H Reserved, do not use 2_H Reserved, do not use 3_H TOM0_13, Output of TOM0, channel 13 4_H TOM0_14, Output of TOM0, channel 14 5_H Reserved, do not use ... 8_H Reserved, do not use 9_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 A_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 B_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 C_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 D_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 E_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 F_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p>

ADC Trigger i Output Select 1 Register

GTM_ADCTRIGiOUT1 (i=0)

ADC Trigger i Output Select 1 Register (09FE44_H+i*8) Application Reset Value: 0000 0000_H

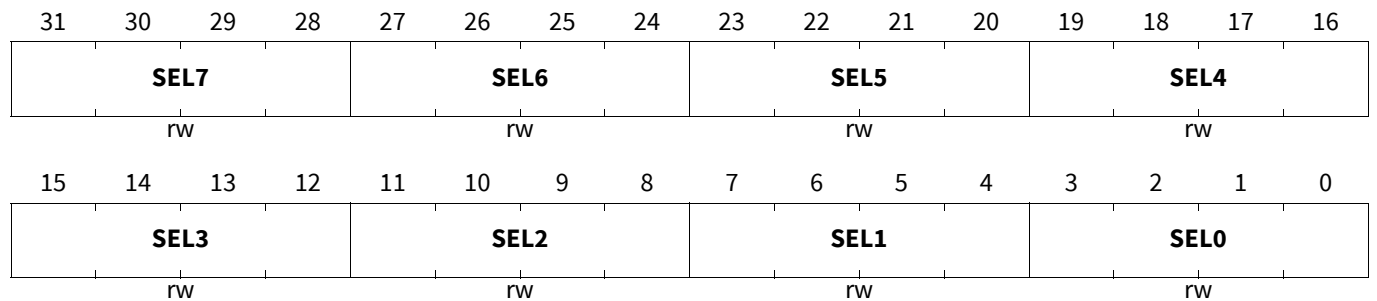


Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 2_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 3_H TOM0_13, Output of TOM0, channel 13 4_H TOM0_14, Output of TOM0, channel 14 5_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4 6_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5 7_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6 8_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7 9_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6 A_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 B_H Reserved, do not use C_H Reserved, do not use D_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 E_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 F_H TOM0_15, Output of TOM0, channel 15</p>
0	31:16	r	<p>Reserved Read as 0, shall be written with 0.</p>

GTM_ADCTRIGiOUT0 (i=1)

ADC Trigger i Output Select 0 Register (09FE40_H+i*8) Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-2)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection</p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger</p> <p>1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6</p> <p>2_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7</p> <p>3_H TOM1_13, Output of TOM1, channel 13</p> <p>4_H TOM1_14, Output of TOM1, channel 14</p> <p>5_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>6_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>7_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>8_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>9_H TOM0_14, Output of TOM0, channel 14</p> <p>A_H TOM0_15, Output of TOM0, channel 15</p> <p>B_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>C_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>D_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>E_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>F_H Reserved, do not use</p>

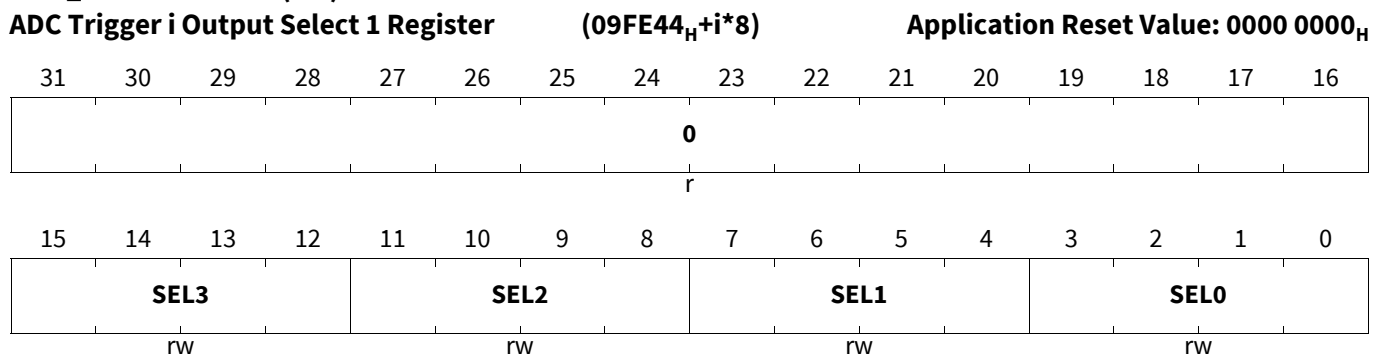
Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3-4)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection</p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger</p> <p>1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6</p> <p>2_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7</p> <p>3_H TOM1_13, Output of TOM1, channel 13</p> <p>4_H TOM1_14, Output of TOM1, channel 14</p> <p>5_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4</p> <p>6_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5</p> <p>7_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6</p> <p>8_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7</p> <p>9_H TOM1_14, Output of TOM1, channel 14</p> <p>A_H TOM1_15, Output of TOM1, channel 15</p> <p>B_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6</p> <p>C_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>D_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6</p> <p>E_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p> <p>F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5-7)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H Reserved, do not use 2_H Reserved, do not use 3_H TOM1_13, Output of TOM1, channel 13 4_H TOM1_14, Output of TOM1, channel 14 5_H Reserved, do not use ... 8_H Reserved, do not use 9_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 A_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 B_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 C_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 D_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 E_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 F_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p>

GTM_ADCTRIGiOUT1 (i=1)

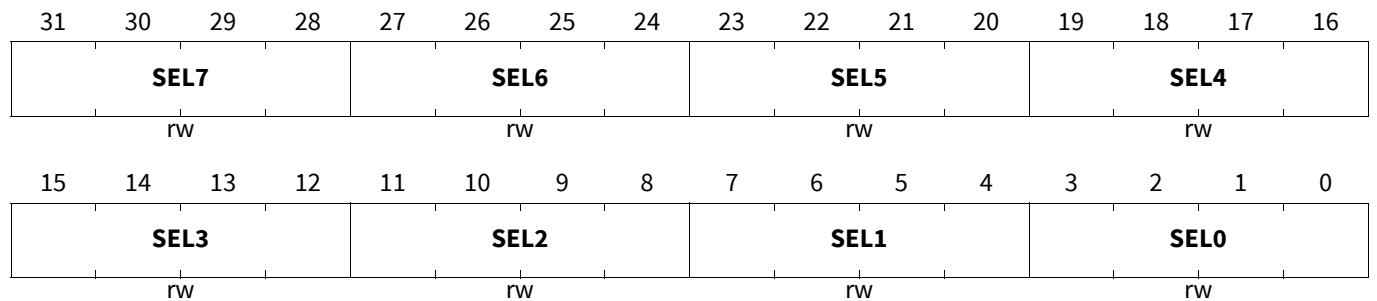


Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <p>0_H No trigger 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 3_H TOM1_13, Output of TOM1, channel 13 4_H TOM1_14, Output of TOM1, channel 14 5_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 6_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 7_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 8_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 9_H TOM0_14, Output of TOM0, channel 14 A_H TOM0_15, Output of TOM0, channel 15 B_H Reserved, do not use C_H Reserved, do not use D_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 E_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 F_H Reserved, do not use</p>
0	31:16	r	<p>Reserved Read as 0, shall be written with 0.</p>

GTM_ADCTRIGiOUT0 (i=2)

ADC Trigger i Output Select 0 Register (09FE40_H+i*8) Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

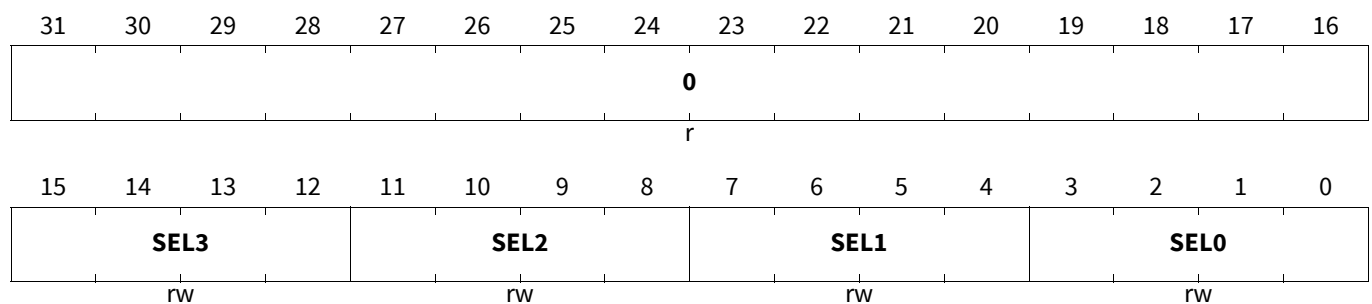
Field	Bits	Type	Description
SELx (x=0-2)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 2_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 3_H CDTM0_DTM1_1(_N), TOM0_5_N, Inverted dead-time output of TOM0, channel 5 4_H CDTM0_DTM1_2(_N), TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 6_H TOM0_11, Output of TOM0, channel 11 7_H TOM0_15, Output of TOM0, channel 15 8_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 9_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 A_H CDTM1_DTM1_1(_N), TOM1_5_N, Inverted dead-time output of TOM1, channel 5 B_H CDTM1_DTM1_2(_N), TOM1_6_N, Inverted dead-time output of TOM1, channel 6 C_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 D_H TOM1_11, Output of TOM1, channel 11 E_H TOM1_15, Output of TOM1, channel 15 F_H Reserved, do not use</p>
SELx (x=3-4)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 2_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 3_H CDTM0_DTM1_1(_N), TOM0_5_N, Inverted dead-time output of TOM0, channel 5 4_H CDTM0_DTM1_2(_N), TOM0_6_N, Inverted dead-time output of TOM0, channel 6 5_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7 6_H TOM0_11, Output of TOM0, channel 11 7_H TOM0_15, Output of TOM0, channel 15 8_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 9_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 A_H CDTM1_DTM1_1(_N), TOM1_5_N, Inverted dead-time output of TOM1, channel 5 B_H CDTM1_DTM1_2(_N), TOM1_6_N, Inverted dead-time output of TOM1, channel 6 C_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 D_H TOM1_11, Output of TOM1, channel 11 E_H TOM1_15, Output of TOM1, channel 15 F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=5-7)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 2_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 3_H CDTM0_DTM1_1(_N), TOM0_5_N, Inverted dead-time output of TOM0, channel 5 4_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 5_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 6_H CDTM1_DTM1_1(_N), TOM1_5_N, Inverted dead-time output of TOM1, channel 5 7_H Reserved, do not use ... F_H Reserved, do not use</p>

GTM_ADCTRIGiOUT1 (i=2)

ADC Trigger i Output Select 1 Register (09FE44_H+i*8) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM0_3, TOM0_3, Dead-time output of TOM0, channel 3 2_H CDTM0_DTM1_0, TOM0_4, Dead-time output of TOM0, channel 4 3_H CDTM0_DTM1_1(_N), TOM0_5_N, Inverted dead-time output of TOM0, channel 5 4_H CDTM1_DTM0_3, TOM1_3, Dead-time output of TOM1, channel 3 5_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4 6_H CDTM1_DTM1_1(_N), TOM1_5_N, Inverted dead-time output of TOM1, channel 5 7_H Reserved, do not use ... F_H Reserved, do not use</p>
0	31:16	r	<p>Reserved Read as 0, shall be written with 0.</p>

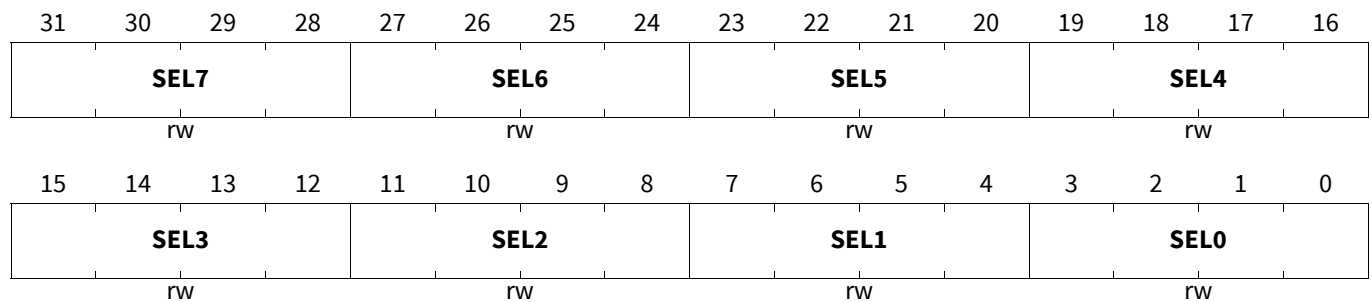
Generic Timer Module (GTM)

GTM_ADCTRIGiOUT0 (i=3)

ADC Trigger i Output Select 0 Register

(09FE40_H+i*8)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0-2)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection</p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger</p> <p>1_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3</p> <p>2_H CDTM0_DTM5_1(_N), ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5</p> <p>3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p> <p>4_H CDTM1_DTM5_1(_N), ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5</p> <p>5_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>6_H CDTM2_DTM5_1(_N), ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5</p> <p>7_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3</p> <p>8_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4</p> <p>9_H CDTM3_DTM5_1(_N), ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5</p> <p>A_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7</p> <p>B_H Reserved, do not use</p> <p>... ..</p> <p>F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=3-4)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 2_H CDTM0_DTM5_1(_N), ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5 3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 4_H CDTM1_DTM5_1(_N), ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 5_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 6_H CDTM2_DTM5_1(_N), ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 7_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7 8_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 9_H CDTM3_DTM5_1(_N), ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 A_H Reserved, do not use ... F_H Reserved, do not use</p>
SELx (x=5-7)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i.</p> <p>0_H No trigger 1_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3 2_H CDTM0_DTM5_1(_N), ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5 3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3 4_H CDTM1_DTM5_1(_N), ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5 5_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3 6_H CDTM2_DTM5_1(_N), ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5 7_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3 8_H CDTM3_DTM5_1(_N), ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5 9_H Reserved, do not use ... F_H Reserved, do not use</p>

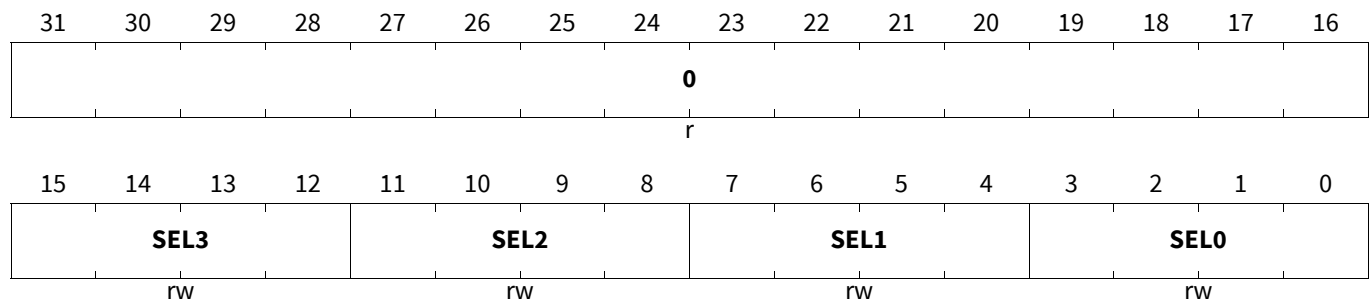
Generic Timer Module (GTM)

GTM_ADCTRIGiOUT1 (i=3)

ADC Trigger i Output Select 1 Register

(09FE44_H+i*8)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	<p>Output Selection for GTM to ADCx connection</p> <p>This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i.</p> <p>0_H No trigger</p> <p>1_H CDTM0_DTM4_3, ATOM0_3, Dead-time output of ATOM0, channel 3</p> <p>2_H CDTM0_DTM5_1(_N), ATOM0_5_N, Inverted dead-time output of ATOM0, channel 5</p> <p>3_H CDTM1_DTM4_3, ATOM1_3, Dead-time output of ATOM1, channel 3</p> <p>4_H CDTM1_DTM5_1(_N), ATOM1_5_N, Inverted dead-time output of ATOM1, channel 5</p> <p>5_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>6_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>7_H CDTM2_DTM5_1(_N), ATOM2_5_N, Inverted dead-time output of ATOM2, channel 5</p> <p>8_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>9_H CDTM3_DTM4_3, ATOM3_3, Dead-time output of ATOM3, channel 3</p> <p>A_H CDTM3_DTM5_1(_N), ATOM3_5_N, Inverted dead-time output of ATOM3, channel 5</p> <p>B_H Reserved, do not use</p> <p>...</p> <p>F_H Reserved, do not use</p>
0	31:16	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

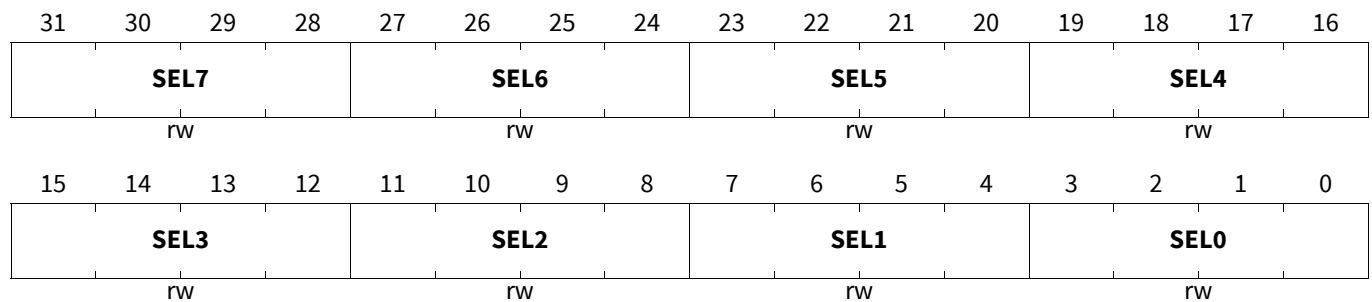
Generic Timer Module (GTM)

GTM_ADTRIGiOUT0 (i=4)

ADC Trigger i Output Select 0 Register

(09FE40_H+i*8)

Application Reset Value: 0000 0000_H



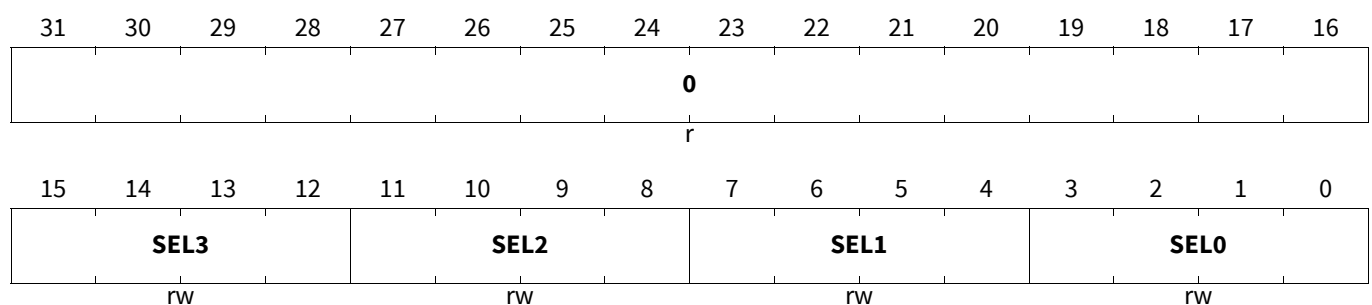
Field	Bits	Type	Description
SELx (x=0-2)	4*x+3:4*x	rw	Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i. 0 _H No trigger 1 _H Reserved, do not use ... F _H Reserved, do not use
SELx (x=3-4)	4*x+3:4*x	rw	Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i. 0 _H No trigger 1 _H Reserved, do not use ... F _H Reserved, do not use
SELx (x=5-7)	4*x+3:4*x	rw	Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx trigger i. 0 _H No trigger 1 _H Reserved, do not use ... F _H Reserved, do not use

GTM_ADTRIGiOUT1 (i=4)

ADC Trigger i Output Select 1 Register

(09FE44_H+i*8)

Application Reset Value: 0000 0000_H



Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-3)	4*x+3:4*x	rw	Output Selection for GTM to ADCx connection This bit field defines which TOM/ATOM channel output is used as ADCx+8 trigger i. 0 _H No trigger 1 _H Reserved, do not use ... F _H Reserved, do not use
0	31:16	r	Reserved Read as 0, shall be written with 0.

Generic Timer Module (GTM)

26.3.10 GTM to CAN/TTCAN Connections

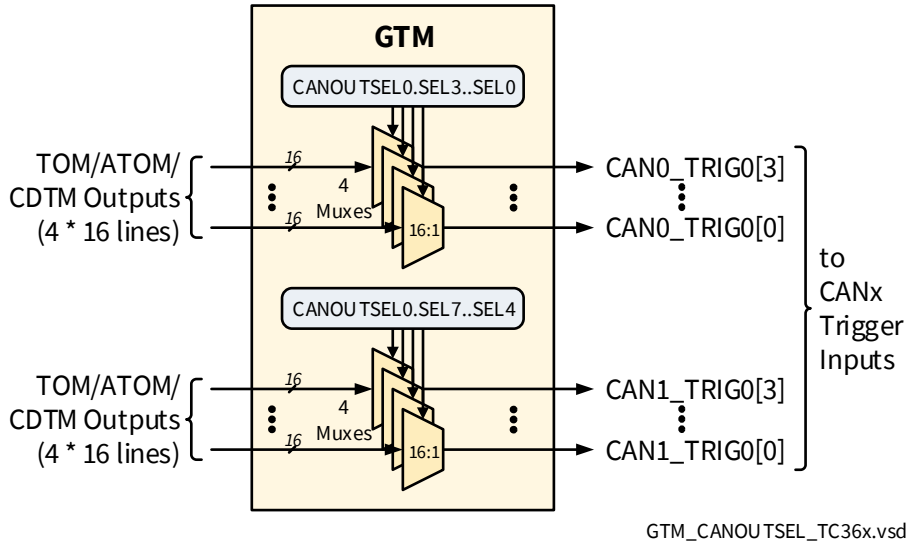


Figure 22 GTM to CAN/TTCAN Connections Overview

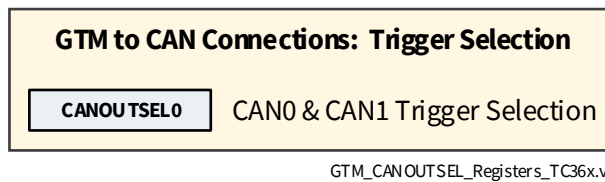


Figure 23 GTM to CAN/TTCAN Connections Registers Overview

CAN0/CAN1 Output Select Register

This register holds the selection for the trigger outputs to the CAN0/CAN1 modules. Bit fields SEL0..3 define the selection for triggers 0..3 for CAN0, while bit fields SEL4..7 define the selection for triggers 0..3 for CAN1.

GTM_CANOUTSEL0
CAN0/CAN1 Output Select Register (09FFDC_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SEL7				SEL6				SEL5				SEL4			
rw				rw				rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL3				SEL2				SEL1				SEL0			
rw				rw				rw				rw			

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=0-1)	4*x+3:4*x	rw	Output Selection for GTM to CAN connection x This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.
SELx (x=2-3)	4*x+3:4*x	rw	Output Selection for GTM to CAN connection x This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x. 0 _H CDTM1_DTM1_0, TOM1_4 , Dead-time output of TOM1, channel 4 1 _H CDTM1_DTM1_1, TOM1_5 , Dead-time output of TOM1, channel 5 2 _H TOM1_11 , Output of TOM1, channel 11 3 _H TOM1_12 , Output of TOM1, channel 12 4 _H CDTM2_DTM4_0, ATOM2_0 , Dead-time output of ATOM2, channel 0 5 _H CDTM2_DTM4_1, ATOM2_1 , Dead-time output of ATOM2, channel 1 6 _H CDTM2_DTM4_2, ATOM2_2 , Dead-time output of ATOM2, channel 2 7 _H CDTM2_DTM4_3, ATOM2_3 , Dead-time output of ATOM2, channel 3 8 _H Reserved, do not use ... F _H Reserved, do not use
SELx (x=4-5)	4*x+3:4*x	rw	Output Selection for GTM to CAN connection x This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x. 0 _H CDTM1_DTM1_0, TOM1_4 , Dead-time output of TOM1, channel 4 1 _H CDTM1_DTM1_1, TOM1_5 , Dead-time output of TOM1, channel 5 2 _H TOM1_11 , Output of TOM1, channel 11 3 _H TOM1_12 , Output of TOM1, channel 12 4 _H CDTM2_DTM4_0, ATOM2_0 , Dead-time output of ATOM2, channel 0 5 _H CDTM2_DTM4_1, ATOM2_1 , Dead-time output of ATOM2, channel 1 6 _H CDTM2_DTM4_2, ATOM2_2 , Dead-time output of ATOM2, channel 2 7 _H CDTM2_DTM4_3, ATOM2_3 , Dead-time output of ATOM2, channel 3 8 _H Reserved, do not use ... F _H Reserved, do not use

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=6-7)	4*x+3:4*x	rw	<p>Output Selection for GTM to CAN connection x</p> <p>This bit field defines which TOM/ATOM channel output is used as CAN0/CAN1 node trigger x.</p> <p>0_H CDTM1_DTM1_0, TOM1_4, Dead-time output of TOM1, channel 4</p> <p>1_H CDTM1_DTM1_1, TOM1_5, Dead-time output of TOM1, channel 5</p> <p>2_H TOM1_11, Output of TOM1, channel 11</p> <p>3_H TOM1_12, Output of TOM1, channel 12</p> <p>4_H CDTM2_DTM4_0, ATOM2_0, Dead-time output of ATOM2, channel 0</p> <p>5_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1</p> <p>6_H CDTM2_DTM4_2, ATOM2_2, Dead-time output of ATOM2, channel 2</p> <p>7_H CDTM2_DTM4_3, ATOM2_3, Dead-time output of ATOM2, channel 3</p> <p>8_H Reserved, do not use</p> <p>... F_H Reserved, do not use</p>

Generic Timer Module (GTM)

26.3.11 GTM to PSI5(S) Connections

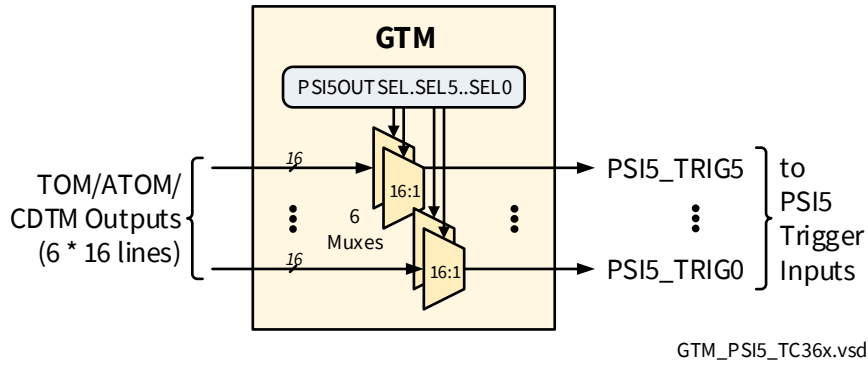


Figure 24 GTM to PSI5 Connections Overview

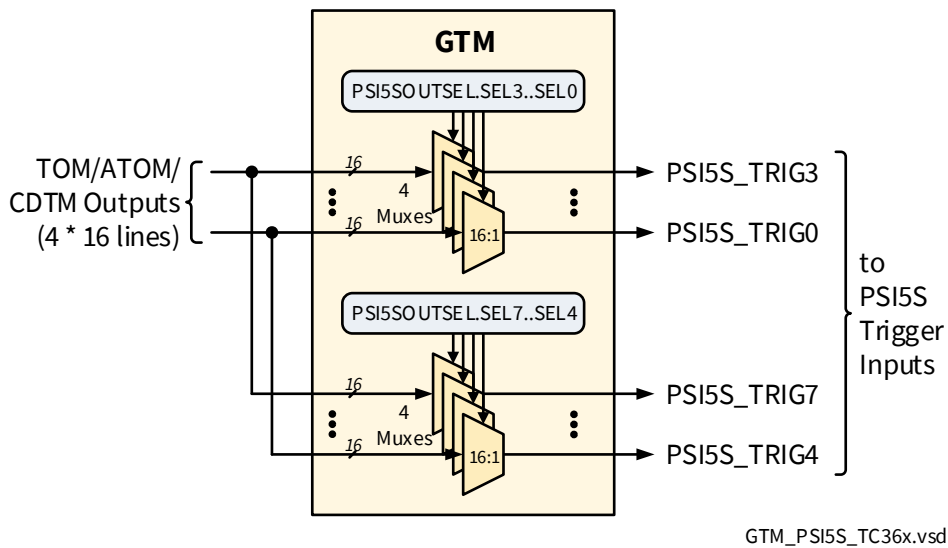


Figure 25 GTM to PSI5S Connections Overview

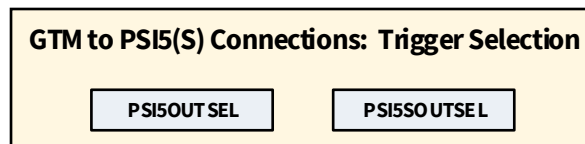


Figure 26 GTM to PSI5(S) Connections Registers Overview

Generic Timer Module (GTM)

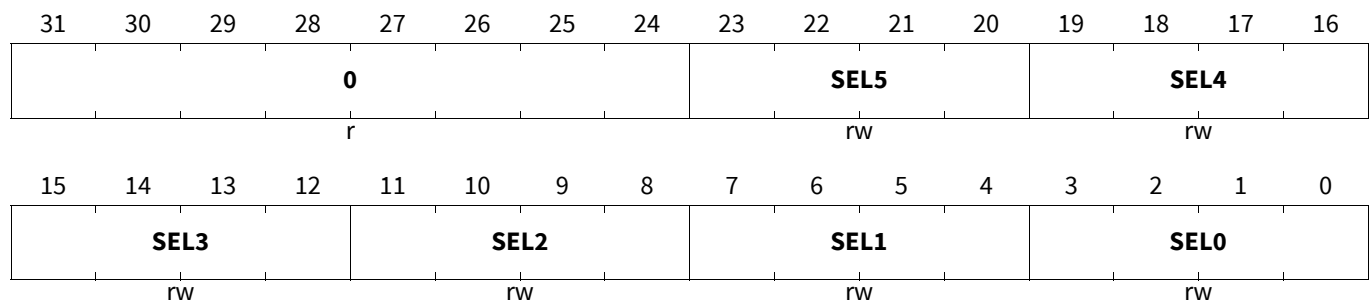
PSI5 Output Select Register

GTM_PSI5OUTSEL

PSI5 Output Select Register

(09FFCC_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0-5)	4*x+3:4*x	rw	<p>Output Selection for GTM to PSI5x connection</p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5 trigger x.</p> <p>0_H No trigger</p> <p>1_H Reserved, do not use</p> <p>...</p> <p>4_H Reserved, do not use</p> <p>5_H CDTM2_DTM5_0, ATOM2_4, Dead-time output of ATOM2, channel 4</p> <p>6_H CDTM2_DTM5_1, ATOM2_5, Dead-time output of ATOM2, channel 5</p> <p>7_H CDTM2_DTM5_2, ATOM2_6, Dead-time output of ATOM2, channel 6</p> <p>8_H CDTM2_DTM5_3, ATOM2_7, Dead-time output of ATOM2, channel 7</p> <p>9_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6</p> <p>A_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7</p> <p>B_H TOM0_13, Output of TOM0, channel 13</p> <p>C_H TOM0_14, Output of TOM0, channel 14</p> <p>D_H Reserved, do not use</p> <p>...</p> <p>F_H Reserved, do not use</p>
0	31:24	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

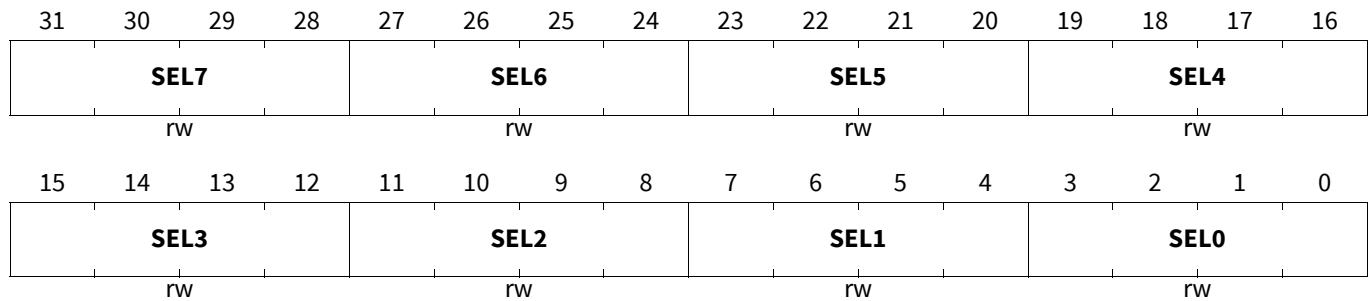
PSI5-S Output Select Register

GTM_PSI5SOUTSEL

PSI5-S Output Select Register

(09FFD0_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SELx (x=0,4)	4*x+3:4*x	rw	<p>Output Selection for GTM to PSI5-S connection</p> <p>This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <p>0_H No trigger</p> <p>1_H CDTM0_DTM1_2, TOM0_6, Dead-time output of TOM0, channel 6</p> <p>2_H CDTM0_DTM1_3, TOM0_7, Dead-time output of TOM0, channel 7</p> <p>3_H TOM0_13, Output of TOM0, channel 13</p> <p>4_H TOM0_14, Output of TOM0, channel 14</p> <p>5_H CDTM0_DTM5_0, ATOM0_4, Dead-time output of ATOM0, channel 4</p> <p>6_H CDTM0_DTM5_1, ATOM0_5, Dead-time output of ATOM0, channel 5</p> <p>7_H CDTM0_DTM5_2, ATOM0_6, Dead-time output of ATOM0, channel 6</p> <p>8_H CDTM0_DTM5_3, ATOM0_7, Dead-time output of ATOM0, channel 7</p> <p>9_H Reserved, do not use</p> <p>... Reserved, do not use</p> <p>F_H Reserved, do not use</p>

Generic Timer Module (GTM)

Field	Bits	Type	Description
SELx (x=1,5)	4*x+3:4*x	rw	<p>Output Selection for GTM to PSI5-S connection This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <p>0_H No trigger 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 3_H TOM1_13, Output of TOM1, channel 13 4_H TOM1_14, Output of TOM1, channel 14 5_H CDTM1_DTM5_0, ATOM1_4, Dead-time output of ATOM1, channel 4 6_H CDTM1_DTM5_1, ATOM1_5, Dead-time output of ATOM1, channel 5 7_H CDTM1_DTM5_2, ATOM1_6, Dead-time output of ATOM1, channel 6 8_H CDTM1_DTM5_3, ATOM1_7, Dead-time output of ATOM1, channel 7 9_H Reserved, do not use ... F_H Reserved, do not use</p>
SELx (x=2,6)	4*x+3:4*x	rw	<p>Output Selection for GTM to PSI5-S connection This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <p>0_H No trigger 1_H CDTM1_DTM1_2, TOM1_6, Dead-time output of TOM1, channel 6 2_H CDTM1_DTM1_3, TOM1_7, Dead-time output of TOM1, channel 7 3_H TOM1_13, Output of TOM1, channel 13 4_H TOM1_14, Output of TOM1, channel 14 5_H CDTM3_DTM5_0, ATOM3_4, Dead-time output of ATOM3, channel 4 6_H CDTM3_DTM5_1, ATOM3_5, Dead-time output of ATOM3, channel 5 7_H CDTM3_DTM5_2, ATOM3_6, Dead-time output of ATOM3, channel 6 8_H CDTM3_DTM5_3, ATOM3_7, Dead-time output of ATOM3, channel 7 9_H Reserved, do not use ... F_H Reserved, do not use</p>
SELx (x=3,7)	4*x+3:4*x	rw	<p>Output Selection for GTM to PSI5-S connection This bit field defines which TOM/ATOM channel output is used as PSI5-S trigger x.</p> <p>0_H No trigger 1_H Reserved, do not use ... F_H Reserved, do not use</p>

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26.3.12 GTM to LCDCDC Connection

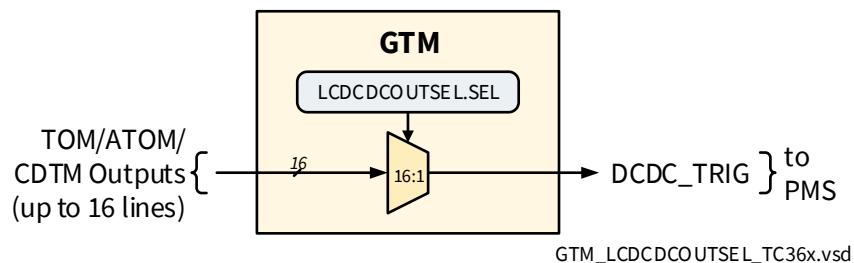


Figure 27 GTM to LCDCDC Connections Overview

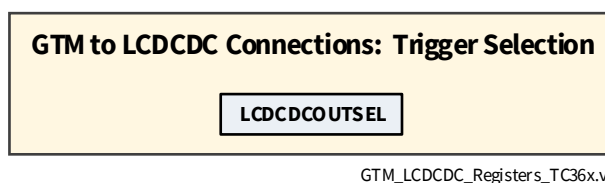


Figure 28 GTM to LCDCDC Connections Registers Overview

LCDCDC Output Select Register

GTM_LCDCDCOUTSEL
LCDCDC Output Select Register (09FFD4_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												SEL			
r												rw			

Generic Timer Module (GTM)

Field	Bits	Type	Description
SEL	3:0	rw	<p>Output Selection for GTM to LCDCDC connection</p> <p>This bit field defines which TOM/ATOM channel output is used as LCDCDC signal.</p> <p>0_H No trigger</p> <p>1_H CDTM0_DTM4_1, ATOM0_1, Dead-time output of ATOM0, channel 1</p> <p>2_H CDTM1_DTM4_1, ATOM1_1, Dead-time output of ATOM1, channel 1</p> <p>3_H CDTM2_DTM4_1, ATOM2_1, Dead-time output of ATOM2, channel 1</p> <p>4_H CDTM3_DTM4_1, ATOM3_1, Dead-time output of ATOM3, channel 1</p> <p>5_H Reserved, do not use</p> <p>6_H CDTM0_DTM0_1, TOM0_1, Dead-time output of TOM0, channel 1</p> <p>7_H CDTM1_DTM0_1, TOM1_1, Dead-time output of TOM1, channel 1</p> <p>8_H Reserved, do not use</p> <p>...</p> <p>F_H Reserved, do not use</p>
0	31:4	r	<p>Reserved</p> <p>Read as 0, shall be written with 0.</p>

Generic Timer Module (GTM)

26.4 ARU Parameters

The following sections list the device-specific parameters of the ARU.

26.4.1 ARU Write Address Overview

The ARU write address map for the TC36x is specified in the following table.

Table 229 ARU Write Addresses

GTM Data Source	ARU Address
ARU_ACCESS	0x000
TIM0_WRADDR[0..7]	0x001..0x008
TIM1_WRADDR[0..7]	0x009..0x010
TIM2_WRADDR[0..7]	0x011..0x018
unused	0x019..0x050
F2A0_WRADDR[0..7]	0x051..0x058
unused	0x059..0x060
BRC_WRADDR[0..21]	0x061..0x076
MCS0_WRADDR[0..23]	0x077..0x08E
MCS1_WRADDR[0..23]	0x08F..0x0A6
MCS2_WRADDR[0..23]	0x0A7..0x0BE
unused	0x0BF..0x11E
ATOM0_WRADDR[0..7]	0x11F..0x126
ATOM1_WRADDR[0..7]	0x127..0x12E
ATOM2_WRADDR[0..7]	0x12F..0x136
ATOM3_WRADDR[0..7]	0x137..0x13E
unused	0x13F..0x17E
DPLL_WRADDR[0..31]	0x17F..0x19E
unused	0x19F..0x1FD
ARU_EMPTY_ADDR	0x1FE
ARU_FULL_ADDR	0x1FF

26.4.2 ARU Port Partitioning

All GTM sub-modules which are reading from ARU can be connected to one of two ARU read ports. Therefore, it can be read from two different ARU addresses in parallel.

Table 230 GTM ARU Partitioning

Modules	ARU-0 port	ARU-1 port
ATOM0	X	
ATOM1		X
ATOM2	X	

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Table 230 GTM ARU Partitioning (cont'd)

Modules	ARU-0 port	ARU-1 port
ATOM3		X
MCS0	X	
MCS1		X
MCS2	X	
DPLL		X
BRC	X	
PSM0	X	

26.4.3 ARU Read ID

Each ARU connected data destination is defined by a combination of ARU port (ARU0 or ARU1) and an ARU read ID. The two ARU counter are addressing two ARU read IDs in parallel. Depending on the ARU mode, both counter may have different values at different point in time (i.e. in dynamic routing mode). The maximum ARU round-trip time is determined by the value of the last ARU read ID. The following table describes the detailed addressing of GTM sub-modules by ARU read IDs.

The following table shows the ARU read IDs for TC36x silicon. The unused IDs are marked with “-”.

Table 231 GTM Read IDs for TC36x

ARU read ID (dec)	ARU0	ARU1	GTM read ID (dec)	ARU0	ARU1
0	reserved	reserved	64	-	DPLL action 31
1	ARU0	ARU1	65	-	-
2	BRC channel 0	DPLL action0	66	-	ATOM3 channel 0
3	PSM0 channel 0	-	67	-	-
4	BRC channel 1	DPLL action 1	68	-	ATOM3 channel 1
5	PSM0 channel 1	-	69	-	-
6	BRC channel 2	DPLL action 2	70	-	ATOM3 channel 2
7	PSM0 channel 2	-	71	-	-
8	BRC channel 3	DPLL action 3	72	-	ATOM3 channel 3
9	PSM0 channel 3	-	73	-	-
10	BRC channel 4	DPLL action 4	74	-	ATOM3 channel 4
11	PSM0 channel 4	-	75	-	-
12	BRC channel 5	DPLL action 5	76	-	ATOM3 channel 5
13	PSM0 channel 5	-	77	-	-
14	BRC channel 6	DPLL action 6	78	-	ATOM3 channel 6
15	PSM0 channel 6	-	79	-	-
16	BRC channel 7	DPLL action 7	80	-	ATOM3 channel 7
17	PSM0 channel 7	-	81	-	-
18	BRC channel 8	DPLL action 8	82	-	-

Generic Timer Module (GTM)

Table 231 GTM Read IDs for TC36x (cont'd)

ARU read ID (dec)	ARU0	ARU1	GTM read ID (dec)	ARU0	ARU1
19	MCS0 channel 0	MCS1 channel 0	83	-	-
20	BRC channel 9	DPLL action 9	84	-	-
21	MCS0 channel 1	MCS1 channel 1	85	-	-
22	BRC channel 10	DPLL action 10	86	-	-
23	MCS0 channel 2	MCS1 channel 2	87	-	-
24	BRC channel 11	DPLL action 11	88	-	-
25	MCS0 channel 3	MCS1 channel 3	89	-	-
26	ATOM0 channel 0	DPLL action 12	90	-	-
27	MCS0 channel 4	MCS1 channel 4	91	-	-
28	ATOM0 channel 1	DPLL action 13	92	-	-
29	MCS0 channel 5	MCS1 channel 5	93	-	-
30	ATOM0 channel 2	DPLL action 14	94	-	-
31	MCS0 channel 6	MCS1 channel 6	95	-	-
32	ATOM0 channel 3	DPLL action 15	96	-	-
33	MCS0 channel 7	MCS1 channel 7	97	-	-
34	ATOM0 channel 4	DPLL action 16	98	-	-
35	MCS2 channel 0	ATOM1 channel 0	99	-	-
36	ATOM0 channel 5	DPLL action 17	100	-	-
37	MCS2 channel 1	ATOM1 channel 1	101	-	-
38	ATOM0 channel 6	DPLL action 18	102	-	-
39	MCS2 channel 2	ATOM1 channel 2	103	-	-
40	ATOM0 channel 7	DPLL action 19	104	-	-
41	MCS2 channel 3	ATOM1 channel 3	105	-	-
42	ATOM2 channel 0	DPLL action 20	106	-	-
43	MCS2 channel 4	ATOM1 channel 4	107	-	-
44	ATOM2 channel 1	DPLL action 21	108	-	-
45	MCS2 channel 5	ATOM1 channel 5	109	-	-
46	ATOM2 channel 2	DPLL action 22	110	-	-
47	MCS2 channel 6	ATOM1 channel 6	111	-	-
48	ATOM2 channel 3	DPLL action 23	112	-	-
49	MCS2 channel 7	ATOM1 channel 7	113	-	-
50	ATOM2 channel 4	DPLL action 24	114	-	-
51	-	-	115	-	-
52	ATOM2 channel 5	DPLL action 25	116	-	-
53	-	-	117	-	-
54	ATOM2 channel 6	DPLL action 26	118	-	-
55	-	-	119	-	-

Generic Timer Module (GTM)**Table 231** GTM Read IDs for TC36x (cont'd)

ARU read ID (dec)	ARU0	ARU1	GTM read ID (dec)	ARU0	ARU1
56	ATOM2 channel 7	DPLL action 27	120	-	-
57	-	-	121	-	-
58	-	DPLL action 28	122	-	-
59	-	-	123	-	-
60	-	DPLL action 29	124	-	-
61	-	-	125	-	-
62	-	DPLL action 30	126	-	-
63	-	-	127	-	-

Generic Timer Module (GTM)

26.5 Revision History

Table 232 Revision History

Reference	Change to Previous Version	Comment
V2.2.10	Initial release	
V2.2.11		
Page 49	Added missing registers GTM_ICM_IRQG_CLS_k_MEI	
Page 154, Page 72	Added missing register GTM_TOUTSELn (n=16); corrected Figure 9 and Table 221	
Table 221	Added package information to TOUTy table	
Table 225	Added GTM to EDSADC connection information	
Table 228	Added GTM to EVADC/EDSADC/SENT connection information	
Figure 18, Figure 20	Updated figures regarding EVADC/EDSADC/SENT connections	
V2.2.11		
Page 35	Register Overview - GTM Protection Mechanism corrected	
Page 35	GTM_CCMi_CFG register now only includes EN_CMP_MON for cluster 1, therefore changed reset value.	
	GTM_CMU_CLK_z_CTRL remark that certain bitfields are only valid, if a DPLL is existent, as TC33x has no DPLL.	
	GTM_TIMnINSEL removed TINxx information	
	Changed TOUTSEL registers.	
V2.2.12		
	no changes relevant for TC36x	
V2.2.13		
Page 218	correcting CANOUTSEL	
	Adding registers, which are changing among AURIX family members, but were missing inside the TC36x appendix.	
V2.2.15		
	Remarks inside OCDS Registers, concerning status, if TBU channel 3, DPLL or MCS do not exist on a device.	
	CCMi_HW_CONF gets proper bit descriptions, as constants have been all 0x0.	
V2.2.18		
	IRQ_NOTIFY registers: Remark, that due to bit property rw, these registers have to be written to reset.	
	DTMAUXINSEL: Corrected. Non existing sideband signals and pins are out of this list.	
Page 218	CANOUTSEL corrected to be matching with design.	
V2.2.19		
	CCMi_CFG registers completely listed	

Generic Timer Module (GTM)**Table 232 Revision History** (cont'd)

Reference	Change to Previous Version	Comment
V2.2.20	CMU_CLK_z_CTRL registers completely listed	
V2.2.21	Changes have no impact on this document.	
V2.2.22	Changes have no impact on this document.	
V2.2.23	Changes have no impact on this document.	
V2.2.24	TOUT table corrected.	

Capture/Compare Unit 6 (CCU6)

27 Capture/Compare Unit 6 (CCU6)

This chapter describes the specific properties of the product TC36x, which is a member of the product family TC3XX.

The functionality of the CCU6 is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

27.1 TC36x Specific Register Set

Table 233 Register Address Space - CCU6

Module	Base Address	End Address	Note
CCU60	F0002A00 _H	F0002AFF _H	FPI slave interface
CCU61	F0002B00 _H	F0002BFF _H	FPI slave interface

Note: Register MOSEL controls the trigger signals from both CCU6 kernels (CCU60 and CCU61) of the CCU6 module, and is only available in the address space of kernel CCU60.

Register Overview Tables of CCU6

Table 234 Register Overview - CCU60 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_CLC	Clock Control Register	0000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_MCFG	Module Configuration Register	0004 _H	U,SV	U,SV,P	See Family Spec	See Family Spec
CCU60_ID	Module Identification Register	0008 _H	U,SV	BE	See Family Spec	See Family Spec
CCU60_MOSEL	CCU60 Module Output Select Register	000C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PISEL0	Port Input Select Register 0	0010 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PISEL2	Port Input Select Register 2	0014 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_KSCSR	Kernel State Control Sensitivity Register	001C _H	U,SV	U,SV,P,OEN	See Family Spec	See Family Spec
CCU60_T12	Timer T12 Counter Register	0020 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Capture/Compare Unit 6 (CCU6)

Table 234 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_T12PR	Timer 12 Period Register	0024 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T12DTC	Dead-Time Control Register for Timer12	0028 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC6xR (x=0-2)	Capture/Compare Register for Channel CC6x	0030 _H +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC6xSR (x=0-2)	Capture/Compare Shadow Reg. for Channel CC6x	0040 _H +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T13	Timer T13 Counter Register	0050 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T13PR	Timer 13 Period Register	0054 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC63R	Compare Register for T13	0058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC63SR	Compare Shadow Register for T13	005C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CMPSTAT	Compare State Register	0060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CMPMOD IF	Compare State Modification Register	0064 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T12MSEL	T12 Mode Select Register	0068 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR0	Timer Control Register 0	0070 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR2	Timer Control Register 2	0074 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR4	Timer Control Register 4	0078 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Capture/Compare Unit 6 (CCU6)

Table 234 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_MODCTR	Modulation Control Register	0080 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TRPCTR	Trap Control Register	0084 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PSLR	Passive State Level Register	0088 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMOUT S	Multi-Channel Mode Output Shadow Register	008C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMOUT	Multi-Channel Mode Output Register	0090 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMCTR	Multi-Channel Mode Control Register	0094 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IMON	Input Monitoring Register	0098 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_LI	Lost Indicator Register	009C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IS	Interrupt Status Register	00A0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_ISS	Interrupt Status Set Register	00A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_ISR	Interrupt Status Reset Register	00A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_INP	Interrupt Node Pointer Register	00AC _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IEN	Interrupt Enable Register	00B0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_OCS	OCDS Control and Status Register	00E8 _H	U,SV	SV,P,OEN	See Family Spec	See Family Spec

Capture/Compare Unit 6 (CCU6)
Table 234 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_KRSTCLR	Kernel Reset Status Clear Register	00EC _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_KRST1	Kernel Reset Register 1	00F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_KRST0	Kernel Reset Register 0	00F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_ACCENO	Access Enable Register 0	00FC _H	U,SV	SV,SE	Application Reset	See Family Spec

Table 235 Register Overview - CCU61 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_CLC	Clock Control Register	0000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_MCFG	Module Configuration Register	0004 _H	U,SV	U,SV,P	See Family Spec	See Family Spec
CCU61_ID	Module Identification Register	0008 _H	U,SV	BE	See Family Spec	See Family Spec
CCU61_PISEL0	Port Input Select Register 0	0010 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_PISEL2	Port Input Select Register 2	0014 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_KSCSR	Kernel State Control Sensitivity Register	001C _H	U,SV	U,SV,P,OEN	See Family Spec	See Family Spec
CCU61_T12	Timer T12 Counter Register	0020 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T12PR	Timer 12 Period Register	0024 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Capture/Compare Unit 6 (CCU6)

Table 235 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_T12DTC	Dead-Time Control Register for Timer12	0028 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC6xR (x=0-2)	Capture/Compare Register for Channel CC6x	0030 _H +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC6xSR (x=0-2)	Capture/Compare Shadow Reg. for Channel CC6x	0040 _H +x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T13	Timer T13 Counter Register	0050 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T13PR	Timer 13 Period Register	0054 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC63R	Compare Register for T13	0058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC63SR	Compare Shadow Register for T13	005C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CMPSTAT	Compare State Register	0060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CMPMOD IF	Compare State Modification Register	0064 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T12MSEL	T12 Mode Select Register	0068 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR0	Timer Control Register 0	0070 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR2	Timer Control Register 2	0074 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR4	Timer Control Register 4	0078 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MODCTR	Modulation Control Register	0080 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Capture/Compare Unit 6 (CCU6)

Table 235 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_TRPCTR	Trap Control Register	0084 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_PSLR	Passive State Level Register	0088 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMOUT S	Multi-Channel Mode Output Shadow Register	008C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMOUT	Multi-Channel Mode Output Register	0090 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMCTR	Multi-Channel Mode Control Register	0094 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IMON	Input Monitoring Register	0098 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_LI	Lost Indicator Register	009C _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IS	Interrupt Status Register	00A0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_ISS	Interrupt Status Set Register	00A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_ISR	Interrupt Status Reset Register	00A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_INP	Interrupt Node Pointer Register	00AC _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IEN	Interrupt Enable Register	00B0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_OCS	OCDS Control and Status Register	00E8 _H	U,SV	SV,P,OEN	See Family Spec	See Family Spec
CCU61_KRSTCLR	Kernel Reset Status Clear Register	00EC _H	U,SV	SV,E,P	Application Reset	See Family Spec

Capture/Compare Unit 6 (CCU6)

Table 235 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_KRST1	Kernel Reset Register 1	00F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_KRST0	Kernel Reset Register 0	00F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_ACCEN0	Access Enable Register 0	00FC _H	U,SV	SV,SE	Application Reset	See Family Spec

27.2 TC36x Specific Registers

No deviations from the Family Spec

27.3 Connectivity

Table 236 Connections of CCU60

Interface Signals	connects		Description
CCU60:CC60	to	IOM:MON1(2)	T12 PWM channel 60
		IOM:REF1(6)	
		P02.0:ALT(7)	
		P02.6:ALT(7)	
		P11.12:ALT(7)	
		P15.6:ALT(7)	
CCU60:CC61	to	IOM:MON1(1)	T12 PWM channel 61
		IOM:REF1(5)	
		P02.2:ALT(7)	
		P02.7:ALT(7)	
		P11.11:ALT(7)	
		P15.5:ALT(7)	
CCU60:CC62	to	IOM:MON1(0)	T12 PWM channel 62
		IOM:REF1(4)	
		P02.4:ALT(7)	
		P02.8:ALT(7)	
		P11.10:ALT(7)	
		P15.4:ALT(7)	
CCU60:CC60INA	from	P02.0:IN	T12 capture input 60
CCU60:CC61INA	from	P02.2:IN	T12 capture input 61
CCU60:CC62INA	from	P02.4:IN	T12 capture input 62
CCU60:CC60INB	from	P00.1:IN	T12 capture input 60

Capture/Compare Unit 6 (CCU6)

Table 236 Connections of CCU60 (cont'd)

Interface Signals	connects		Description
CCU60:CC61INB	from	P00.3:IN	T12 capture input 61
CCU60:CC62INB	from	P00.5:IN	T12 capture input 62
CCU60:CC60INC	from	P02.6:IN	T12 capture input 60
CCU60:CC61INC	from	P02.7:IN	T12 capture input 61
CCU60:CC62INC	from	P02.8:IN	T12 capture input 62
CCU60:CC60IND	from	PMS:pms_wut_underflow	T12 capture input 60
CCU60:CC62IND	from	SCU:E_PDOOUT(4)	T12 capture input 62
CCU60:CCPOS0A	from	P02.6:IN	Hall capture input 0
CCU60:CCPOS1A	from	P02.7:IN	Hall capture input 1
CCU60:CCPOS2A	from	P02.8:IN	Hall capture input 2
CCU60:CCPOS0B	from	CCU61:SR(2)	Hall capture input 0
CCU60:CCPOS1B	from	P40.1:IN	Hall capture input 1
CCU60:CCPOS2B	from	P40.3:IN	Hall capture input 2
CCU60:CCPOS0C	from	P10.4:IN	Hall capture input 0
CCU60:CCPOS1C	from	P10.7:IN	Hall capture input 1
CCU60:CCPOS2C	from	P10.8:IN	Hall capture input 2
CCU60:CCPOS0D	from	P40.0:IN	Hall capture input 0
CCU60:CCPOS1D	from	P40.2:IN	Hall capture input 1
CCU60:CCPOS2D	from	P40.4:IN	Hall capture input 2
CCU60:COOUT60	to	SCU:E_REQ0(1) IOM:MON1(3) IOM:REF1(3) P02.1:ALT(7) P11.9:ALT(7) P15.7:ALT(7)	T12 PWM channel 60
CCU60:COOUT61	to	IOM:MON1(4) IOM:REF1(2) P02.3:ALT(7) P11.6:ALT(7) P15.8:ALT(7)	T12 PWM channel 61
CCU60:COOUT62	to	IOM:MON1(5) IOM:REF1(1) P02.5:ALT(7) P11.3:ALT(7) P14.0:ALT(7)	T12 PWM channel 62

Capture/Compare Unit 6 (CCU6)
Table 236 Connections of CCU60 (cont'd)

Interface Signals	connects		Description
CCU60:COUT63	to	IOM:MON1(6)	T13 PWM channel 63
		IOM:REF1(0)	
		P00.0:ALT(7)	
		P11.2:ALT(7)	
		P14.1:ALT(7)	
		P32.4:ALT(7)	
		PMS:dcdc_sync_ccu6	
CCU60:CTRAPA	from	P00.11:IN	Trap input capture
CCU60:CTRAPB	from	CCU60:WHE_N	Trap input capture
CCU60:CTRAPC	from	EVADC:FC0BFLOUT	Trap input capture
CCU60:CTRAPD	from	SCU:E_PDOUT(0)	Trap input capture
CCU60:SR(0)	to	HSM:EXT_INT(10)	Service request
CCU60:SR(1)	to	CCU60:T13HRH	Service request
CCU60:SR(2)	to	CCU61:CCPOS0B	Service request
		CCU61:T12HRG	
		CCU61:T13HRG	
CCU60:SR(3)	to	EVADC:G0REQTRA	Service request
		EVADC:G1REQTRA	
		EVADC:G2REQTRA	
		EVADC:G3REQTRA	
		EVADC:G8REQTRA	
		EVADC:G9REQTRA	
CCU60:T12HRA	from	SCU:scu_cctrig0	External timer start 12
CCU60:T13HRA	from	SCU:scu_cctrig0	External timer start 13
CCU60:T12HRB	from	P00.7:IN	External timer start 12
CCU60:T13HRB	from	P00.8:IN	External timer start 13
CCU60:T12HRC	from	P00.9:IN	External timer start 12
CCU60:T13HRC	from	P00.9:IN	External timer start 13
CCU60:T12HRD	from	GTM:CCU6_TRIG(0)	External timer start 12
CCU60:T13HRD	from	GTM:CCU6_TRIG(1)	External timer start 13
CCU60:T12HRE	from	P00.0:IN	External timer start 12
CCU60:T12HRF	from	GPT120:T6OFL	External timer start 12
CCU60:T13HRF	from	GPT120:T6OFL	External timer start 13
CCU60:T12HRG	from	CCU61:SR(2)	External timer start 12
CCU60:T13HRG	from	CCU61:SR(2)	External timer start 13
CCU60:T12HRH	from	SCU:E_PDOUT(0)	External timer start 12
CCU60:T13HRH	from	CCU60:SR(1)	External timer start 13

Capture/Compare Unit 6 (CCU6)
Table 236 Connections of CCU60 (cont'd)

Interface Signals	connects		Description
CCU60:TRIG(0)	to	EVADC:G0REQGTC	Output select trigger
		EVADC:G1REQGTC	
		EVADC:G2REQGTC	
		EVADC:G3REQGTC	
		EVADC:G8REQGTC	
		EVADC:G9REQGTC	
CCU60:TRIG(1)	to	EVADC:G0REQGTD	Output select trigger
		EVADC:G1REQGTD	
		EVADC:G2REQGTD	
		EVADC:G3REQGTD	
		EVADC:G8REQGTD	
		EVADC:G9REQGTD	
CCU60:TRIG(2)	to	EVADC:G0REQGTE	Output select trigger
		EVADC:G1REQGTE	
		EVADC:G2REQGTE	
		EVADC:G3REQGTE	
		EVADC:G8REQGTE	
		EVADC:G9REQGTE	
CCU60:WHE_N	to	CCU60:CTRAPB	Set wrong hall event negative

Table 237 Connections of CCU61

Interface Signals	connects		Description
CCU61:CC60	to	IOM:MON1(8)	T12 PWM channel 60
		IOM:REF1(13)	
		P00.1:ALT(7)	
		P00.7:ALT(7)	
		P20.8:ALT(7)	
		P33.13:ALT(7)	
CCU61:CC61	to	IOM:MON1(9)	T12 PWM channel 61
		IOM:REF1(12)	
		P00.3:ALT(7)	
		P00.8:ALT(7)	
		P20.9:ALT(7)	
		P33.11:ALT(7)	

Capture/Compare Unit 6 (CCU6)
Table 237 Connections of CCU61 (cont'd)

Interface Signals	connects		Description
CCU61:CC62	to	IOM:MON1(10)	T12 PWM channel 62
		IOM:REF1(11)	
		P00.5:ALT(7)	
		P00.9:ALT(7)	
		P20.10:ALT(7)	
		P33.9:ALT(7)	
CCU61:CC60INA	from	P00.1:IN	T12 capture input 60
CCU61:CC61INA	from	P00.3:IN	T12 capture input 61
CCU61:CC62INA	from	P00.5:IN	T12 capture input 62
CCU61:CC60INB	from	P02.0:IN	T12 capture input 60
CCU61:CC61INB	from	P02.2:IN	T12 capture input 61
CCU61:CC62INB	from	P02.4:IN	T12 capture input 62
CCU61:CC60INC	from	P00.7:IN	T12 capture input 60
CCU61:CC61INC	from	P00.8:IN	T12 capture input 61
CCU61:CC62INC	from	P00.9:IN	T12 capture input 62
CCU61:CC60IND	from	PMS:pms_wut_underflow	T12 capture input 60
CCU61:CC61IND	from	CAN0:INT(12)	T12 capture input 61
CCU61:CC62IND	from	SCU:E_PDOOUT(5)	T12 capture input 62
CCU61:CCPOS0A	from	P00.7:IN	Hall capture input 0
CCU61:CCPOS1A	from	P00.8:IN	Hall capture input 1
CCU61:CCPOS2A	from	P00.9:IN	Hall capture input 2
CCU61:CCPOS0B	from	CCU60:SR(2)	Hall capture input 0
CCU61:CCPOS1B	from	P40.6:IN	Hall capture input 1
CCU61:CCPOS2B	from	P40.8:IN	Hall capture input 2
CCU61:CCPOS0C	from	P33.7:IN	Hall capture input 0
CCU61:CCPOS1C	from	P33.6:IN	Hall capture input 1
CCU61:CCPOS2C	from	P33.5:IN	Hall capture input 2
CCU61:CCPOS0D	from	P40.5:IN	Hall capture input 0
CCU61:CCPOS1D	from	P40.7:IN	Hall capture input 1
CCU61:CCPOS2D	from	P40.9:IN	Hall capture input 2
CCU61:COU60	to	SCU:E_REQ1(1)	T12 PWM channel 60
		IOM:MON1(11)	
		IOM:REF1(10)	
		P00.2:ALT(7)	
		P20.11:ALT(7)	
		P33.12:ALT(7)	

Capture/Compare Unit 6 (CCU6)

Table 237 Connections of CCU61 (cont'd)

Interface Signals	connects		Description
CCU61:COUT61	to	IOM:MON1(12)	T12 PWM channel 61
		IOM:REF1(9)	
		P00.4:ALT(7)	
		P20.12:ALT(7)	
		P33.10:ALT(7)	
CCU61:COUT62	to	IOM:MON1(13)	T12 PWM channel 62
		IOM:REF1(8)	
		P00.6:ALT(7)	
		P20.13:ALT(7)	
		P33.8:ALT(7)	
CCU61:COUT63	to	IOM:MON1(7)	T13 PWM channel 63
		IOM:REF1(7)	
		P00.10:ALT(7)	
		P00.12:ALT(7)	
		P20.7:ALT(7)	
CCU61:CTRAPA	from	P00.0:IN	Trap input capture
CCU61:CTRAPB	from	CCU61:WHE_N	Trap input capture
CCU61:CTRAPC	from	P33.4:IN	Trap input capture
CCU61:CTRAPD	from	SCU:E_PDOOUT(1)	Trap input capture
CCU61:SR(0)	to	HSM:EXT_INT(11)	Service request
CCU61:SR(1)	to	CCU61:T13HRH	Service request
CCU61:SR(2)	to	CCU60:CCPOS0B	Service request
		CCU60:T12HRG	
		CCU60:T13HRG	
CCU61:SR(3)	to	EVADC:G0REQTRB	Service request
		EVADC:G1REQTRB	
		EVADC:G2REQTRB	
		EVADC:G3REQTRB	
		EVADC:G8REQTRB	
		EVADC:G9REQTRB	
CCU61:T12HRA	from	SCU:scu_cctrig0	External timer start 12
CCU61:T13HRA	from	SCU:scu_cctrig0	External timer start 13
CCU61:T12HRB	from	P02.6:IN	External timer start 12
CCU61:T13HRB	from	P02.7:IN	External timer start 13
CCU61:T12HRC	from	P02.8:IN	External timer start 12
CCU61:T13HRC	from	P02.8:IN	External timer start 13
CCU61:T12HRD	from	GTM:CCU6_TRIG(2)	External timer start 12
CCU61:T13HRD	from	GTM:CCU6_TRIG(3)	External timer start 13

Capture/Compare Unit 6 (CCU6)
Table 237 Connections of CCU61 (cont'd)

Interface Signals	connects		Description
CCU61:T12HRE	from	P00.11:IN	External timer start 12
CCU61:T13HRE	from	CAN0:INT(15)	External timer start 13
CCU61:T12HRF	from	GPT120:T6OFL	External timer start 12
CCU61:T13HRF	from	GPT120:T6OFL	External timer start 13
CCU61:T12HRG	from	CCU60:SR(2)	External timer start 12
CCU61:T13HRG	from	CCU60:SR(2)	External timer start 13
CCU61:T12HRH	from	SCU:E_PDOUT(1)	External timer start 12
CCU61:T13HRH	from	CCU61:SR(1)	External timer start 13
CCU61:WHE_N	to	CCU61:CTRAPB	Set wrong hall event negative

27.4 Revision History**Table 238 Revision History**

Reference	Change to Previous Version	Comment
V3.0.0		
Page 7	Connectivity table updated.	

General Purpose Timer Unit (GPT12)

28 General Purpose Timer Unit (GPT12)

This chapter describes the specific properties of the product TC36x, which is a member of the product family TC3XX.

The functionality of the GPT12 is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

28.1 TC36x Specific Register Set

Table 239 Register Address Space - GPT12

Module	Base Address	End Address	Note
GPT120	F0001800 _H	F00018FF _H	FPI slave interface

Register Overview Table

See corresponding AURIX™ TC3xx Platform family specification.

28.2 TC36x Specific Registers

No deviations from the Family Spec

General Purpose Timer Unit (GPT12)

28.3 Connectivity

Table 240 Connections of GPT120

Interface Signals	connects		Description
GPT120:CAPINA	from	P13.2:IN	Trigger input to capture value of timer T5 into CAPREL register
GPT120:CAPINB	from	SCU:E_PDOOUT(6)	Trigger input to capture value of timer T5 into CAPREL register
GPT120:T2EUDA	from	P00.8:IN	Count direction control input of timer T2
GPT120:T3EUDA	from	P02.7:IN	Count direction control input of core timer T3
GPT120:T4EUDA	from	P00.9:IN	Count direction control input of timer T4
GPT120:T5EUDA	from	P21.6:IN	Count direction control input of timer T5
GPT120:T6EUDA	from	P20.0:IN	Count direction control input of core timer T6
GPT120:T2EUDB	from	P33.6:IN	Count direction control input of timer T2
GPT120:T3EUDB	from	P10.7:IN	Count direction control input of core timer T3
GPT120:T4EUDB	from	P33.5:IN	Count direction control input of timer T4
GPT120:T5EUDB	from	P10.1:IN	Count direction control input of timer T5
GPT120:T6EUDB	from	P10.0:IN	Count direction control input of core timer T6
GPT120:T2INA	from	P00.7:IN	Trigger/gate input of timer T2
GPT120:T3INA	from	P02.6:IN	Trigger/gate input of core timer T3
GPT120:T4INA	from	P02.8:IN	Trigger/gate input of timer T4
GPT120:T5INA	from	P21.7:IN	Trigger/gate input of timer T5
GPT120:T6INA	from	P20.3:IN	Trigger/gate input of core timer T6
GPT120:T2INB	from	P33.7:IN	Trigger/gate input of timer T2
GPT120:T3INB	from	P10.4:IN	Trigger/gate input of core timer T3
GPT120:T4INB	from	P10.8:IN	Trigger/gate input of timer T4
GPT120:T5INB	from	P10.3:IN	Trigger/gate input of timer T5
GPT120:T6INB	from	P10.2:IN	Trigger/gate input of core timer T6
GPT120:T3INC	from	SCU:E_PDOOUT(4)	Trigger/gate input of core timer T3
GPT120:T6OFL	to	CCU60:T12HRF	Overflow/underflow signal of timer T6
		CCU60:T13HRF	
		CCU61:T12HRF	
		CCU61:T13HRF	
GPT120:T3OUT	to	SCU:E_REQ4(2)	External output for overflow/underflow detection of core timer T3
		P10.6:ALT(4)	
		P21.6:ALT(7)	
GPT120:T6OUT	to	SCU:E_REQ5(2)	External output for overflow/underflow detection of core timer T6
		P10.5:ALT(5)	
		P21.7:ALT(7)	
GPT120:CIRQ_INT	to	INT:gpt120.CIRQ_INT	GPT120 CAPREL Service Request

General Purpose Timer Unit (GPT12)

Table 240 Connections of GPT120 (cont'd)

Interface Signals	connects		Description
GPT120:T2_INT	to	INT:gpt120.T2_INT	GPT120 T2 Overflow/Underflow Service Request
GPT120:T3_INT	to	INT:gpt120.T3_INT	GPT120 T3 Overflow/Underflow Service Request
GPT120:T4_INT	to	INT:gpt120.T4_INT	GPT120 T4 Overflow/Underflow Service Request
GPT120:T5_INT	to	INT:gpt120.T5_INT	GPT120 T5 Overflow/Underflow Service Request
GPT120:T6_INT	to	INT:gpt120.T6_INT	GPT120 T6 Overflow/Underflow Service Request

28.4 Revision History

Table 241 Revision History

Reference	Change to Previous Version	Comment
V2.2.3		
---	No change	
V3.0.0		
Page 2	Connections table changed (no functional change).	-
V3.0.1		
-	No functional changes.	-
V3.0.2		
	No functional changes.	

Converter Control Block (CONVCTRL)

29 Converter Control Block (CONVCTRL)

This chapter describes the specific properties of the product TC36x, which is a member of the product family TC3xx.

The functionality of the CONVCTRL is described in the TC3xx family documentation. The complete product description consists of the family documentation and this product-specific appendix.

29.1 TC36x-Specific IP Configuration

The functional description describes the features and operating modes of the converter control block in a general way. This section summarizes the configuration that is available in a specific product.

Table 242 TC36x specific configuration of CONVERTER

Parameter	CONVCTRL
FPI base address	F0025000 _H
FPI address range	100 _H
Application Reset and Kernel Reset	Application Reset
Name of the config sector value	CFS Value
CFS value for register VRCFG	000000C3 _H

29.2 TC36x Specific Register Set

Table 243 Register Address Space - CONVERTER

Module	Base Address	End Address	Note
CONVCTRL	F0025000 _H	F00250FF _H	FPI slave interface

Register Overview Table

See main family chapter.

29.3 TC36x Specific Registers

No deviations from the Family Spec

Converter Control Block (CONVCTRL)

29.4 Connectivity

The CONVCTRL is connected to its environment through a number of input and output signals.

Table 244 Digital Connections for Product TC36x

Signal	Dir.	Source/Destin.	Description
General			
PHSYNC	O	EVADC, EDSADC	Synchronization signal for analog clocks
CC_ALARM	O	SMU	Alarm signal from safety logic

Table 245 List of CONVERTER Interface Signals

Interface Signals	I/O	Description
PHSYNC	out	Phase synchronization signal
CC_ALARM	out	Safety Alarm Signal

29.5 Revision History

Table 246 Revision History for the Appendix

Reference	Change to Previous Version	Comment
V3.0.0		
-	No change	
V3.0.1		
	No functional change.	

Enhanced Versatile Analog-to-Digital Converter (EVADC)

30 Enhanced Versatile Analog-to-Digital Converter (EVADC)

This chapter describes the specific properties of the product TC36x, which is a member of the product family TC3XX.

The functionality of the EVADC is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

30.1 TC36x-Specific IP Configuration

The functional description describes the features and operating modes of the A/D Converters in a general way. This section summarizes the configuration that is available in a specific product.

Each converter group is equipped with a separate analog converter module and a dedicated analog input multiplexer.

Table 247 General Converter Configuration TC36x

Converter Group	Input Channels	Converter Cluster	Common Service Req. Group	Associated Standard Reference Pins
Primary Groups				
G0	CH0 ... CH7	Primary	C0	V_{AREF1} , V_{AGND1}
G1	CH0 ... CH7	Primary	C1	V_{AREF1} , V_{AGND1}
G2	CH0 ... CH7	Primary	C0	V_{AREF1} , V_{AGND1}
G3	CH0 ... CH7	Primary	C1	V_{AREF1} , V_{AGND1}
Secondary Groups				
G8	CH0 ... CH15	Secondary	C0	V_{AREF1} , V_{AGND1}
G9	CH0 ... CH15	Secondary	C1	V_{AREF1} , V_{AGND1}
Fast Compare Channels				
FC0	CH0	FastCompare	C0	V_{AREF1} , V_{AGND1}
FC1	CH0	FastCompare	C1	V_{AREF1} , V_{AGND1}

Synchronization Groups

Up to 4 converter kernels can be connected to synchronization groups to achieve parallel conversion of several input channels.

Not all channels can be synchronized to each other, but certain groups can be formed.

Table 248 summarizes which kernels can be synchronized for parallel conversions.

Table 248 Synchronization Groups

ADC Kernel	Synchr. Group	Master selected by control input C1x ¹⁾			
		C10 ²⁾	C11	C12	C13
G0 (Prim.)	A	G0	G1	G2	G3
G1 (Prim.)	A	G1	G0	G2	G3
G2 (Prim.)	A	G2	G0	G1	G3
G3 (Prim.)	A	G3	G0	G1	G2
G8 (Sec.)	C	G8	G9	---	---
G9 (Sec.)	C	G9	G8	---	---

Enhanced Versatile Analog-to-Digital Converter (EVADC)

- 1) The control input is selected by bitfield STSEL in register GxSYNCTR.
Select the corresponding ready inputs accordingly by bits EVALRx.
- 2) Control input CI0 always selects the own control signals of the corresponding ADC kernel. This selection is meant for the synchronization master or for stand-alone operation.

Hardware Connections Between Groups

Certain groups can forward their result values to Fast Compare channels via the HDI. [Table 249](#) shows these connections.

Table 249 Hardware Connections to Fast Compare Channels

Source Group	Target Channel
G0 (Prim.)	FC0CH0
G1 (Prim.)	FC1CH0

Table 250 TC36x specific configuration of EVADC

Parameter	EVADC
Number of available primary groups	4
Number of available secondary groups	2
Number of available Fast Compare channels	2
FPI base address	F0020000 _H
FPI address range	4000 _H

30.2 TC36x Specific Register Set

Table 251 Register Address Space - EVADC

Module	Base Address	End Address	Note
EVADC	F0020000 _H	F0023FFF _H	FPI slave interface

Register Overview Table

See main family chapter.

Enhanced Versatile Analog-to-Digital Converter (EVADC)

30.3 Connectivity

The EVADC is connected to its environment through a number of analog input signals and also digital input and output signals. These connections establish communication with other peripherals, with the system blocks, and with external components. The following tables list:

- [Analog Module Connections](#)
- [Digital Module Connections](#)

30.3.1 Analog Module Connections

The EVADC module accepts a number of analog input signals. The analog input multiplexers select the input channels to be converted from the signals available in this product.

Note: If an analog input channel is connected to an I/O port pin, make sure the output driver and/or pull devices and/or the digital input path are disabled during normal operation (Px_PDISC.PDISy = 1). For diagnostic functions (MD, PDD) ports must be configured differently (see family description).

The exact number of analog input channels and the available connection to port pins depend on the employed product type and package (refer to [Table 247](#) and to the corresponding Data Sheets).

A summary of channels can be found in the table below.

Note: Most analog input pins are also connected either to other channels of the EVADC or to channels of the EDSADC. These connections are listed in column “Overlay”

Special Markings

- Input channels marked “PDD” provide a pull-down device for pull-down diagnostics.
Note: G9CH3: No PDD because of IO pads.
- Input channels marked “MD” can activate the pullup and pulldown devices for multiplexer diagnostics.
- Input channels marked “AltRef” can be selected as an alternate reference voltage for conversions on channels of the same group.
- Input channels marked “FixRef” cannot select an alternate reference voltage, but only the corresponding standard reference voltage.

Table 252 Analog Input Connections for Product TC36x

Signal	Source	Overlay	Description
Reference Inputs			
V _{AREF}	VAREF1	-	positive analog reference
V _{AGND}	VAGND1	-	negative analog reference
Analog Inputs for Group 0 (Primary)			
G0CH0 (AltRef)	AN0	EDS3PA	analog input channel 0 of group 0
G0CH1 (MD)	AN1	EDS3NA	analog input channel 1 of group 0
G0CH2 (MD)	AN2	EDS0PA	analog input channel 2 of group 0
G0CH3	AN3	EDS0NA	analog input channel 3 of group 0
G0CH4 (FixRef)	AN4	-	analog input channel 4 of group 0
G0CH5 (FixRef)	AN5	-	analog input channel 5 of group 0
G0CH6 (FixRef)	AN6	-	analog input channel 6 of group 0

Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 252 Analog Input Connections for Product TC36x (cont'd)

Signal	Source	Overlay	Description
G0CH7 (PDD, FixRef)	AN7	-	analog input channel 7 of group 0
Analog Inputs for Group 1 (Primary)			
G1CH0 (AltRef)	AN8	-	analog input channel 0 of group 1
G1CH1 (MD)	AN9	-	analog input channel 1 of group 1
G1CH2 (MD)	AN10	-	analog input channel 2 of group 1
G1CH3 (PDD)	AN11	-	analog input channel 3 of group 1
G1CH4	AN12	EDS0PB	analog input channel 4 of group 1
G1CH5	AN13	EDS0NB	analog input channel 5 of group 1
G1CH6	AN14	EDS3PB	analog input channel 6 of group 1
G1CH7	AN15	EDS3NB	analog input channel 7 of group 1
Analog Inputs for Group 2 (Primary)			
G2CH0 (AltRef)	AN16	FC0CH0	analog input channel 0 of group 2
G2CH1 (MD)	AN17	FC1CH0	analog input channel 1 of group 2
G2CH2 (MD)	AN18	SENT11A	analog input channel 2 of group 2
G2CH3 (PDD)	AN19	SENT12A	analog input channel 3 of group 2
G2CH4	AN20	EDS2PA	analog input channel 4 of group 2
G2CH5	AN21	EDS2NA	analog input channel 5 of group 2
G2CH6	AN22	-	analog input channel 6 of group 2
G2CH7	AN23	-	analog input channel 7 of group 2
Analog Inputs for Group 3 (Primary)			
G3CH0 (AltRef)	AN24	EDS2PB/SENT0A	analog input channel 0 of group 3
G3CH1 (MD)	AN25	EDS2NB/SENT1A	analog input channel 1 of group 3
G3CH2 (MD)	AN26	SENT2A	analog input channel 2 of group 3
G3CH3 (PDD)	AN27	SENT3A	analog input channel 3 of group 3
G3CH4	AN28	SENT13A	analog input channel 4 of group 3
G3CH5	AN29	SENT14A	analog input channel 5 of group 3
G3CH6	AN30	-	analog input channel 6 of group 3
G3CH7	AN31	-	analog input channel 7 of group 3
Analog Inputs for Group 8 (Secondary)			
G8CH0 (AltRef)	AN32	SENT4A	analog input channel 0 of group 8
G8CH1 (MD)	AN33	SENT5A	analog input channel 1 of group 8
G8CH2 (MD)	AN34	-	analog input channel 2 of group 8
G8CH3 (PDD)	AN35	-	analog input channel 3 of group 8
G8CH4	AN36	EDS1PA/SENT6A	analog input channel 4 of group 8
G8CH5	AN37	EDS1NA/SENT7A	analog input channel 5 of group 8
G8CH6	AN38	EDS1PB/SENT8A	analog input channel 6 of group 8
G8CH7	AN39	EDS1NB/SENT9A	analog input channel 7 of group 8
G8CH8	AN40	-	analog input channel 8 of group 8

Enhanced Versatile Analog-to-Digital Converter (EVADC)
Table 252 Analog Input Connections for Product TC36x (cont'd)

Signal	Source	Overlay	Description
G8CH9	AN41	-	analog input channel 9 of group 8
G8CH10	AN42	-	analog input channel 10 of group 8
G8CH11	AN43	-	analog input channel 11 of group 8
G8CH12	AN44	EDS1PC	analog input channel 12 of group 8
G8CH13	AN45	EDS1NC	analog input channel 13 of group 8
G8CH14	AN46	EDS1PD	analog input channel 14 of group 8
G8CH15	AN47	EDS1ND	analog input channel 15 of group 8

Analog Inputs for Group 9 (Secondary)

G9CH0 (AltRef)	P00.12	-	analog input channel 0 of group 9
G9CH1 (MD)	P00.11	-	analog input channel 1 of group 9
G9CH2 (MD)	P00.10	-	analog input channel 2 of group 9
G9CH3	P00.9	-	analog input channel 3 of group 9
G9CH4	P00.8	-	analog input channel 4 of group 9
G9CH5	P00.7	-	analog input channel 5 of group 9
G9CH6	P00.6	-	analog input channel 6 of group 9
G9CH7	P00.5	-	analog input channel 7 of group 9
G9CH8	P00.4	-	analog input channel 8 of group 9
G9CH9	P00.3	-	analog input channel 9 of group 9
G9CH10	P00.2	-	analog input channel 10 of group 9
G9CH11	P00.1	-	analog input channel 11 of group 9
G9CH12	-	-	analog input channel 12 of group 10
G9CH13	-	-	analog input channel 13 of group 10
G9CH14	-	-	analog input channel 14 of group 10
G9CH15	V_{EDSADC}	-	Selected supervision signal from the EDSADC

Analog Inputs for Fast Compare Channels

FC0CH0	AN16	-	analog input channel of FC channel 0
FC1CH0	AN17	-	analog input channel of FC channel 1

Common Input Signals (x = 0-3, 8-9, z = 0-1)

GxCH28, FCzCH28	$V_{ANACOMM}$	-	common reference signal, available to all converters, used for production testing, can be fed to the converters through pin AN11
GxCH29, FCzCH29	V_{MTS}	-	module test signal, comparator supply voltage V_{DDK}

Enhanced Versatile Analog-to-Digital Converter (EVADC)**Table 252 Analog Input Connections for Product TC36x (cont'd)**

Signal	Source	Overlay	Description
GxCH30, FCzCH30	V_{AGND}	-	negative reference voltage
GxCH31, FCzCH31	V_{AREF}	-	positive reference voltage

Enhanced Versatile Analog-to-Digital Converter (EVADC)

30.3.2 Digital Module Connections

The EVADC module accepts a number of digital input signals and generates a number of output signals. This section summarizes the connection of these signals to other on-chip modules or to external resources via port pins.

Table 253 Digital Connections for Product TC36x

Signal	Dir.	Source/Destin.	Description
Gate Inputs for Primary and Secondary Groups (x = 0-3, 8-9, input line selected via bitfield GTSEL = [yyyy_B])			
GxREQGTA	I	GTM_adc _x _trig0	[0000 _B] GTM ADC trigger 0
GxREQGTB	I	GTM_adc _x _trig1	[0001 _B] GTM ADC trigger 1
GxREQGTC	I	CCU6061 TRIG0	[0010 _B] CCU6061 trigger output 0
GxREQGTD	I	CCU6061 TRIG1	[0011 _B] CCU6061 trigger output 1
GxREQGTE	I	CCU6061 TRIG2	[0100 _B] CCU6061 trigger output 2
GxREQGTF	I	-	[0101 _B] Gating input F, group x
GxREQGTG	I	GTM_adc _x _trig4	[0110 _B] GTM ADC trigger 4
GxREQGTH	I	-	[0111 _B] Gating input H, group x
GxREQGTI	I	-	[1000 _B] Gating input I, group x
GxREQGTJ	I	-	[1001 _B] Gating input J, group x
GxREQGTK	I	GTM_adc _x _trig2	[1010 _B] GTM ADC trigger 2
GxREQGTL	I	GTM_adc _x _trig3	[1011 _B] GTM ADC trigger 3
GyREQGTM	I	eru_pdout _y	[1100 _B] ERU pattern detection output y (y = 0 - 3)
G8REQGTM	I	eru_pdout_0	[1100 _B] ERU pattern detection output 0
G9REQGTM	I	eru_pdout_1	[1100 _B] ERU pattern detection output 1
GxREQGTN	I	-	[1101 _B] Gating input N, group x
GxREQGTO	I	-	[1110 _B] Gating input O, group x
GxREQGTP	I	[internal]	[1111 _B] Extend inputs to the selected internal trigger source (see GxTRCTR)
GxREQGTySEL	O	GxREQTRyP ¹⁾	Selected gating signal of the respective source
Trigger Inputs for Primary and Secondary Groups (x = 0-3, 8-9, input line selected via bitfield XTSEL = [yyyy_B])			
GxREQTRA	I	CCU60_SR3	[0000 _B] CCU60 service request output 3
GxREQTRB	I	CCU61_SR3	[0001 _B] CCU61 service request output 3
GxREQTRC	I	HSPDM_adc_trig	[0010 _B] HSPDM chirp trigger
GxREQTRD	I	-	[0011 _B] Trigger input D, group x
GxREQTRE	I	-	[0100 _B] Trigger input E, group x
GxREQTRF	I	-	[0101 _B] Trigger input F, group x
GxREQTRG	I	GTM_adc _x _trig4	[0110 _B] GTM ADC trigger 4
GyREQTRH	I	eru_iout _y	[0111 _B] ERU interrupt output y (y = 0 - 7)
G8REQTRH	I	eru_iout_0	[0111 _B] ERU interrupt output 0

Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 253 Digital Connections for Product TC36x (cont'd)

Signal	Dir.	Source/Destin.	Description
G9REQTRH	I	eru_iout_1	[0111 _B] ERU interrupt output 1
GxREQTRI	I	GTM_adcx_trig0	[1000 _B] GTM ADC trigger 0
GxREQTRJ	I	GTM_adcx_trig1	[1001 _B] GTM ADC trigger 1
GxREQTRK	I	GTM_adcx_trig2	[1010 _B] GTM ADC trigger 2
GxREQTRL	I	GTM_adcx_trig3	[1011 _B] GTM ADC trigger 3
GxREQTRM	I	vadc_gxsr1	[1100 _B] Service request 1, group x
GxREQTRN	I	vadc_c0sr1	[1101 _B] Service request 1, common group 0
GxREQTRO	I	vadc_c1sr1	[1110 _B] Service request 1, common group 1
GxREQTRyP	I	GxREQGTySEL ¹⁾	[1111 _B] Extend triggers to selected gating input of the respective source
GxREQTRySEL	O	-	Selected trigger signal of the respective source

Trigger/Gate Inputs for Fast Compare Channels (z = 0-1, input line selected via bitfield XTSEL = [yyyy_B])

FCzREQTRA	I	-	[0000 _B] Trigger input A
FCzREQTRB	I	-	[0001 _B] Trigger input B
FCzREQTRC	I	-	[0010 _B] Trigger input C
FCzREQTRD	I	-	[0011 _B] Trigger input D
FCzREQTRE	I	-	[0100 _B] Trigger input E
FCzREQTRF	I	-	[0101 _B] Trigger input F
FCzREQTRG	I	-	[0110 _B] Trigger input G
FCzREQTRH	I	-	[0111 _B] Trigger input H
FCzREQTRI	I	GTM_adcz_trig0	[1000 _B] GTM ADCz trigger 0
FCzREQTRJ	I	GTM_adcz_trig1	[1001 _B] GTM ADCz trigger 1
FCzREQTRK	I	GTM_adcz_trig2	[1010 _B] GTM ADCz trigger 2
FC0REQTRL	I	GTM_adc8_trig3	[1011 _B] GTM ADC8 trigger 3
FC1REQTRL	I	GTM_adc9_trig3	[1011 _B] GTM ADC9 trigger 3
FC0REQTRM	I	GTM_adc8_trig4	[1100 _B] GTM ADC8 trigger 4
FC1REQTRM	I	GTM_adc9_trig4	[1100 _B] GTM ADC9 trigger 4
FCzREQTRN	I	-	[1101 _B] Trigger input N
FCzREQTRO	I	-	[1110 _B] Trigger input O
FCzREQTRP	I	-	[1111 _B] Trigger input P

Global Signals and Service Request Lines For Primary/Secondary Groups: x = 0-3, 8-9, for Fast Compare Channels: z = 0-1

GxDATA[20:0]	O	Fast Compare channel, RIF, GTM	Result values written to RES15
GxWR	O	Fast Compare channel, RIF, GTM	Write signal for GxDATA
EMUX00	O	P02.6, P33.3	Control of external analog multiplexer interface 0
EMUX01	O	P02.7, P33.2	
EMUX02	O	P02.8, P33.1	

Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 253 Digital Connections for Product TC36x (cont'd)

Signal	Dir.	Source/Destin.	Description
EMUX10	O	P00.6, P33.6	Control of external analog multiplexer interface 1
EMUX11	O	P00.7, P33.5	
EMUX12	O	P00.8, P33.4	
CBFLOUT0	O	GTM_CDTM0_DTM03, GTM_CDTM0_DTM43, GTM_MCSSTAT8, GTM_TIM1_CH0, GTM_TIM1_CH4, GTM_TIM2_CH0, GTM_TIM2_CH4	Common boundary flag output 0
CBFLOUT1	O	GTM_CDTM1_DTM03, GTM_CDTM1_DTM43, GTM_MCSSTAT9, GTM_TIM1_CH1, GTM_TIM1_CH5, GTM_TIM2_CH1, GTM_TIM2_CH5	Common boundary flag output 1
CBFLOUT2	O	GTM_CDTM2_DTM03, GTM_CDTM2_DTM43, GTM_MCSSTAT10, GTM_TIM1_CH2, GTM_TIM1_CH6, GTM_TIM2_CH2, GTM_TIM2_CH6	Common boundary flag output 2
CBFLOUT3	O	GTM_CDTM3_DTM03, GTM_CDTM3_DTM43, GTM_MCSSTAT11, GTM_TIM1_CH3, GTM_TIM1_CH7, GTM_TIM2_CH3, GTM_TIM2_CH7	Common boundary flag output 3
FC0BFLOUT	O	CCU60_CTRAPC, P00.5, P33.4	Boundary flag output of FC channel 0
FC0BFL	O	GTM_MCSSTAT0, GTM_tim_0_muxin_0_0 GTM_tim_1_muxin_0_0 GTM_tim_2_muxin_0_0 GTM_tim_4_muxin_0_0	Boundary flag level of FC channel 0
FC0BFSEL	I	GTM_MCSTRIG1	Boundary flag (FC channel 0) source select
FC0BFDAT	I	GTM_MCSTRIG0	Boundary flag (FC channel 0) alternate data
FC1BFLOUT	O	P10.1, P33.6	Boundary flag output of FC channel 1

Enhanced Versatile Analog-to-Digital Converter (EVADC)

Table 253 Digital Connections for Product TC36x (cont'd)

Signal	Dir.	Source/Destin.	Description
FC1BFL	O	GTM_MCSSTAT1, GTM_tim_0_muxin_1_0 GTM_tim_1_muxin_1_0 GTM_tim_2_muxin_1_0 GTM_tim_4_muxin_1_0	Boundary flag level of FC channel 1
FC1BFSEL	I	GTM_MCSTRIG3	Boundary flag (FC channel 1) source select
FC1BFDAT	I	GTM_MCSTRIG2	Boundary flag (FC channel 1) alternate data
GxSR0	O	ICU	Service request 0 of group x
GxSR1	O	ICU	Service request 1 of group x
GxSR2	O	ICU	Service request 2 of group x
GxSR3	O	ICU	Service request 3 of group x
FCzSR0	O	ICU	Service request 0 of FC channel z
C0SR0	O	ICU, GTM_TIM0_CH0, GTM_TIM1_CH4, GTM_TIM2_CH0	Service request 0 of common block 0
C0SR1	O	ICU, GTM_TIM0_CH2, GTM_TIM1_CH6, GTM_TIM2_CH2	Service request 1 of common block 0
C0SR2	O	ICU, GTM_TIM0_CH4, GTM_TIM1_CH0, GTM_TIM2_CH4	Service request 2 of common block 0
C0SR3	O	ICU, GTM_TIM0_CH6, GTM_TIM1_CH2, GTM_TIM2_CH6	Service request 3 of common block 0
C1SR0	O	ICU, GTM_TIM0_CH1, GTM_TIM1_CH5, GTM_TIM2_CH1	Service request 0 of common block 1
C1SR1	O	ICU, GTM_TIM0_CH3, GTM_TIM1_CH7, GTM_TIM2_CH3	Service request 1 of common block 1
C1SR2	O	ICU, GTM_TIM0_CH5, GTM_TIM1_CH1, GTM_TIM2_CH5	Service request 2 of common block 1
C1SR3	O	ICU, GTM_TIM0_CH7, GTM_TIM1_CH3, GTM_TIM2_CH7	Service request 3 of common block 1

System-Internal Connections (x = 0-3, 8-9)

PHSYNC	I	Phase synchronizer	Synchronization signal for analog clocks
otgb0[15:0]	O	OTGM	Alternate trigger buses for additional trace signals indicating the input signal sample phase (see OCS)
otgb1[15:0]	O	OTGM	

1) Internal signal connection.

Enhanced Versatile Analog-to-Digital Converter (EVADC)

30.4 Revision History

This is a summary of the modifications that have been applied to this chapter.

Table 254 Revision History

Reference	Change to Previous Version	Comment
V3.0.0		
Page 3	Clarify functionality of channel CH29 (see end of table)	
V3.0.1		
-	No functional changes.	-
V3.0.2		
-	No functional changes.	-
V3.0.3		
Page 3	Changed source values.	
V3.0.4		
-	No functional changes.	-
V3.0.5		
-	No functional changes.	-

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

31 Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

This chapter describes the specific properties of the product TC36x, which is a member of the product family TC3XX.

The functionality of the EDSADC is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

31.1 TC36x-Specific IP Configuration

The functional description describes the features and operating modes of the A/D Converters in a general way. This section summarizes the configuration that is available in a specific product.

The EDSADC features a number of channels, some with an analog input multiplexer.

Table 255 General Converter Configuration TC36x

Channel	Analog Inputs	Digital Inputs	Reference Pins	Notes
0	2	2	V_{AREF1} , V_{AGND1}	2:1 analog multiplexer
1	4	2	V_{AREF1} , V_{AGND1}	4:1 analog multiplexer
2	2	2	V_{AREF1} , V_{AGND1}	2:1 analog multiplexer
3	2	2	V_{AREF1} , V_{AGND1}	2:1 analog multiplexer

Table 256 TC36x specific configuration of EDSADC

Parameter	EDSADC
Number of available channels	4
FPI base address	F0024000 _H
FPI address range	1000 _H
Application- or Kernel Reset	Application Reset

31.2 TC36x Specific Register Set

Table 257 Register Address Space - EDSADC

Module	Base Address	End Address	Note
EDSADC	F0024000 _H	F0024FFF _H	FPI slave interface

Register Overview Table

See main family chapter.

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

31.3 Connectivity

The EDSADC is connected to its environment through a number of analog input signals and also digital input and output signals. These connections establish communication with other peripherals, with the system blocks, and with external components. The following tables list:

- [Analog Module Connections](#)
- [Digital Module Connections](#)

31.3.1 Analog Module Connections

The EDSADC module accepts a positive and a negative analog input signal to be used as a differential input. Each analog input can also be used in single-ended mode.

Note: If an analog input channel is connected to an I/O port pin, make sure the output driver and/or the digital input path are disabled during normal operation (Px_PDISC.PDISy = 1).

The exact number of analog input channels and the available connection to port pins depend on the employed product type and package (refer to [Table 255](#) and to the corresponding Data Sheets).

A summary of channels can be found in the table below.

Note: Most analog input pins are also connected to channels of the EVADC. These connections are listed in column “Overlay”

Table 258 Analog Input Connections for Product TC36x

Signal	Source	Overlay	Description
Reference Inputs			
V _{AREF}	VAREF1	-	positive analog reference
V _{AGND}	VAGND1	-	negative analog reference
Analog Inputs (input line selected via bitfield INMUX = [yy_B])			
EDS0PA	AN2	G0CH2 (MD)	[00 _B] positive analog input of channel 0, pin A
EDS0NA	AN3	G0CH3	[00 _B] negative analog input of channel 0, pin A
EDS0PB	AN12	G1CH4	[01 _B] positive analog input of channel 0, pin B
EDS0NB	AN13	G1CH5	[01 _B] negative analog input of channel 0, pin B
EDS1PA	AN36	G8CH4/SENT6A	[00 _B] positive analog input of channel 1, pin A
EDS1NA	AN37	G8CH5/SENT7A	[00 _B] negative analog input of channel 1, pin A
EDS1PB	AN38	G8CH6/SENT8A	[01 _B] positive analog input of channel 1, pin B
EDS1NB	AN39	G8CH7/SENT9A	[01 _B] negative analog input of channel 1, pin B
EDS1PC	AN44	G8CH12	[10 _B] positive analog input of channel 1, pin C
EDS1NC	AN45	G8CH13	[10 _B] negative analog input of channel 1, pin C
EDS1PD	AN46	G8CH14	[11 _B] positive analog input of channel 1, pin D
EDS1ND	AN47	G8CH15	[11 _B] negative analog input of channel 1, pin D
EDS2PA	AN20	G2CH4	[00 _B] positive analog input of channel 2, pin A
EDS2NA	AN21	G2CH5	[00 _B] negative analog input of channel 2, pin A
EDS2PB	AN24	G3CH0 (AltRef)/ SENT0A	[01 _B] positive analog input of channel 2, pin B

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**Table 258 Analog Input Connections for Product TC36x (cont'd)**

Signal	Source	Overlay	Description
EDS2NB	AN25	G3CH1 (MD) / SENT1A	[01 _B] negative analog input of channel 2, pin B
EDS3PA	AN0	G0CH0 (AltRef)	[00 _B] positive analog input of channel 3, pin A
EDS3NA	AN1	G0CH1 (MD)	[00 _B] negative analog input of channel 3, pin A
EDS3PB	AN14	G1CH6	[01 _B] positive analog input of channel 3, pin B
EDS3NB	AN15	G1CH7	[01 _B] negative analog input of channel 3, pin B

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

31.3.2 Digital Module Connections

The EDSADC module accepts a number of digital input signals and generates a number of output signals. This section summarizes the connection of these signals to other on-chip modules or to external resources via port pins.

Note: The input signals ITRxA ... ITRxP can be used for both trigger functions and gating functions. The trigger input line is selected via bitfield TRSEL = [yyyy]_B, the data input line (DSDIN...) is selected via bitfield DSRCEX = [yyy]_B, the clock input line (DSCIN...) is selected via bitfield CSRCEX = [yyy]_B.

Table 259 Digital Connections for Product TC36x

Signal	Dir.	Source/Destin.	Description
Channel 0			
DSDIN0A	I	P00.12	[00X] _B Data bitstream channel 0 input A
DSDIN0B	I	P33.6	[01X] _B Data bitstream channel 0 input B
DSDIN0C	I	-	[10X] _B Data bitstream channel 0 input C
DSDIN0D	I	-	[11X] _B Data bitstream channel 0 input D
DSCIN0A	I	P00.11	[011] _B Modulator clock channel 0 input A
DSCIN0B	I	P33.5	[100] _B Modulator clock channel 0 input B
DSCIN0C	I	-	[101] _B Modulator clock channel 0 input C
DSCOUT0	O	P00.11, P33.5	Modulator clock channel 0 output
ITR0A	I	GTM:DSADC_TRIG0(0)	[0000] _B GTM DSADC trigger 0
ITR0B	I	GTM:DSADC_TRIG1(0)	[0001] _B GTM DSADC trigger 1
ITR0C	I	GTM:ADC_TRIG0(0)	[0010] _B GTM ADC trigger 0
ITR0D	I	GTM:ADC_TRIG1(0)	[0011] _B GTM ADC trigger 1
ITR0E	I	P33.0	[0100] _B Trigger/gate via port input
ITR0F	I	P33.4	[0101] _B Trigger/gate via port input
ITR0G	I	SCU_PDOUT0	[0110] _B ERU pattern detection output 0
ITR0H	I	-	[0111] _B Trigger/gate, channel 0, input H
ITR0I	I	-	[1000] _B Trigger/gate, channel 0, input I
ITR0J	I	-	[1001] _B Trigger/gate, channel 0, input J
ITR0K	I	GTM:ADC_TRIG2(0)	[1010] _B GTM ADC trigger 2
ITR0L	I	GTM:ADC_TRIG3(0)	[1011] _B GTM ADC trigger 3
ITR0M	I	GTM:DSADC_TRIG2(0)	[1100] _B GTM DSADC trigger 2
ITR0N	I	GTM:DSADC_TRIG3(0)	[1101] _B GTM DSADC trigger 3
ITR0O	I	-	[1110] _B Trigger/gate, channel 0, input O
ITR0P	I	-	[1111] _B Trigger/gate, channel 0, input P
SRM0	O	ICU, GTM:DSADC_SRM(0)	Service request output main channel 0
SRA0	O	ICU	Service request output aux. channel 0
SAUL0	O	GTM:DSADC_SAUL(0)	Signal above upper limit ind., channel 0
SBLLO	O	GTM:DSADC_SBLL(0)	Signal below lower limit ind., channel 0
SWIB0	O	GTM:DTMA0(2)	Signal within band ind., channel 0

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 259 Digital Connections for Product TC36x (cont'd)

Signal	Dir.	Source/Destin.	Description
DATA0[16:0]	O	GTM	Result values of channel 0
WRO	O	GTM	Write signal for DATA0
Channel 1			
DSDIN1A	I	P00.10	[00X _B] Data bitstream channel 1 input A
DSDIN1B	I	P33.4	[01X _B] Data bitstream channel 1 input B
DSDIN1C	I	-	[10X _B] Data bitstream channel 1 input C
DSDIN1D	I	-	[11X _B] Data bitstream channel 1 input D
DSCIN1A	I	P00.9	[011 _B] Modulator clock channel 1 input A
DSCIN1B	I	P33.3	[100 _B] Modulator clock channel 1 input B
DSCIN1C	I	-	[101 _B] Modulator clock channel 1 input C
DSCOUT1	O	P00.9, P33.3	Modulator clock channel 1 output
ITR1A	I	GTM:DSADC_TRIG0(1)	[0000 _B] GTM DSADC trigger 0
ITR1B	I	GTM:DSADC_TRIG1(1)	[0001 _B] GTM DSADC trigger 1
ITR1C	I	GTM:ADC_TRIG0(1)	[0010 _B] GTM ADC trigger 0
ITR1D	I	GTM:ADC_TRIG1(1)	[0011 _B] GTM ADC trigger 1
ITR1E	I	P33.1	[0100 _B] Trigger/gate via port input
ITR1F	I	P33.5	[0101 _B] Trigger/gate via port input
ITR1G	I	SCU_PDOUT1	[0110 _B] ERU pattern detection output 1
ITR1H	I	-	[0111 _B] Trigger/gate, channel 1, input H
ITR1I	I	-	[1000 _B] Trigger/gate, channel 1, input I
ITR1J	I	-	[1001 _B] Trigger/gate, channel 1, input J
ITR1K	I	GTM:ADC_TRIG2(1)	[1010 _B] GTM ADC trigger 2
ITR1L	I	GTM:ADC_TRIG3(1)	[1011 _B] GTM ADC trigger 3
ITR1M	I	GTM:DSADC_TRIG2(1)	[1100 _B] GTM DSADC trigger 2
ITR1N	I	GTM:DSADC_TRIG3(1)	[1101 _B] GTM DSADC trigger 3
ITR1O	I	-	[1110 _B] Trigger/gate, channel 1, input O
ITR1P	I	-	[1111 _B] Trigger/gate, channel 1, input P
SRM1	O	ICU, GTM:DSADC_SRM(1)	Service request output main channel 1
SRA1	O	ICU	Service request output aux. channel 1
SAUL1	O	GTM:DSADC_SAUL(1)	Signal above upper limit ind., channel 1
SBLL1	O	GTM:DSADC_SBLL(1)	Signal below lower limit ind., channel 1
SWIB1	O	GTM:DTMA1(2)	Signal within band ind., channel 1
DATA1[16:0]	O	GTM	Result values of channel 1
WR1	O	GTM	Write signal for DATA1
Channel 2			
DSDIN2A	I	P00.6	[00X _B] Data bitstream channel 2 input A
DSDIN2B	I	P33.2	[01X _B] Data bitstream channel 2 input B
DSDIN2C	I	-	[10X _B] Data bitstream channel 2 input C

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 259 Digital Connections for Product TC36x (cont'd)

Signal	Dir.	Source/Destin.	Description
DSDIN2D	I	-	[11X _B] Data bitstream channel 2 input D
DSCIN2A	I	P00.5	[011 _B] Modulator clock channel 2 input A
DSCIN2B	I	P33.1	[100 _B] Modulator clock channel 2 input B
DSCIN2C	I	-	[101 _B] Modulator clock channel 2 input C
DSCOUT2	O	P00.5, P33.1	Modulator clock channel 2 output
ITR2A	I	GTM:DSADC_TRIG0(2)	[0000 _B] GTM DSADC trigger 0
ITR2B	I	GTM:DSADC_TRIG1(2)	[0001 _B] GTM DSADC trigger 1
ITR2C	I	GTM:ADC_TRIG0(2)	[0010 _B] GTM ADC trigger 0
ITR2D	I	GTM:ADC_TRIG1(2)	[0011 _B] GTM ADC trigger 1
ITR2E	I	P33.2	[0100 _B] Trigger/gate via port input
ITR2F	I	P33.6	[0101 _B] Trigger/gate via port input
ITR2G	I	SCU_PDOUT2	[0110 _B] ERU pattern detection output 2
ITR2H	I	-	[0111 _B] Trigger/gate, channel 2, input H
ITR2I	I	-	[1000 _B] Trigger/gate, channel 2, input I
ITR2J	I	-	[1001 _B] Trigger/gate, channel 2, input J
ITR2K	I	GTM:ADC_TRIG2(2)	[1010 _B] GTM ADC trigger 2
ITR2L	I	GTM:ADC_TRIG3(2)	[1011 _B] GTM ADC trigger 3
ITR2M	I	GTM:DSADC_TRIG2(2)	[1100 _B] GTM DSADC trigger 2
ITR2N	I	GTM:DSADC_TRIG3(2)	[1101 _B] GTM DSADC trigger 3
ITR2O	I	-	[1110 _B] Trigger/gate, channel 2, input O
ITR2P	I	-	[1111 _B] Trigger/gate, channel 2, input P
SRM2	O	ICU, GTM:DSADC_SRM(2)	Service request output main channel 2
SRA2	O	ICU	Service request output aux. channel 2
SAUL2	O	GTM:DSADC_SAUL(2)	Signal above upper limit ind., channel 2
SBLL2	O	GTM:DSADC_SBLL(2)	Signal below lower limit ind., channel 2
SWIB2	O	GTM:DTMA2(2)	Signal within band ind., channel 2
DATA2[16:0]	O	GTM	Result values of channel 2
WR2	O	GTM	Write signal for DATA2

Channel 3

DSDIN3A	I	P00.4	[00X _B] Data bitstream channel 3 input A
DSDIN3B	I	P02.8	[01X _B] Data bitstream channel 3 input B
DSDIN3C	I	-	[10X _B] Data bitstream channel 3 input C
DSDIN3D	I	-	[11X _B] Data bitstream channel 3 input D
DSCIN3A	I	P00.3	[011 _B] Modulator clock channel 3 input A
DSCIN3B	I	P02.7	[100 _B] Modulator clock channel 3 input B
DSCIN3C	I	-	[101 _B] Modulator clock channel 3 input C
DSCOUT3	O	P00.3, P02.7	Modulator clock channel 3 output
ITR3A	I	GTM:DSADC_TRIG0(3)	[0000 _B] GTM DSADC trigger 0

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

Table 259 Digital Connections for Product TC36x (cont'd)

Signal	Dir.	Source/Destin.	Description
ITR3B	I	GTM:DSADC_TRIG1(3)	[0001 _B] GTM DSADC trigger 1
ITR3C	I	GTM:ADC_TRIG0(3)	[0010 _B] GTM ADC trigger 0
ITR3D	I	GTM:ADC_TRIG1(3)	[0011 _B] GTM ADC trigger 1
ITR3E	I	P02.8	[0100 _B] Trigger/gate via port input
ITR3F	I	P00.9	[0101 _B] Trigger/gate via port input
ITR3G	I	SCU_PDOOUT3	[0110 _B] ERU pattern detection output 3
ITR3H	I	-	[0111 _B] Trigger/gate, channel 3, input H
ITR3I	I	-	[1000 _B] Trigger/gate, channel 3, input I
ITR3J	I	-	[1001 _B] Trigger/gate, channel 3, input J
ITR3K	I	GTM:ADC_TRIG2(3)	[1010 _B] GTM ADC trigger 2
ITR3L	I	GTM:ADC_TRIG3(3)	[1011 _B] GTM ADC trigger 3
ITR3M	I	GTM:DSADC_TRIG2(3)	[1100 _B] GTM DSADC trigger 2
ITR3N	I	GTM:DSADC_TRIG3(3)	[1101 _B] GTM DSADC trigger 3
ITR3O	I	-	[1110 _B] Trigger/gate, channel 3, input O
ITR3P	I	-	[1111 _B] Trigger/gate, channel 3, input P
SRM3	O	ICU, GTM:DSADC_SRM(3), HSM_EXT_INT23	Service request output main channel 3
SRA3	O	ICU	Service request output aux. channel 3
SAUL3	O	GTM:DSADC_SAUL(3)	Signal above upper limit ind., channel 3
SBLL3	O	GTM:DSADC_SBLL(3)	Signal below lower limit ind., channel 3
SWIB3	O	GTM:DTMA3(2)	Signal within band ind., channel 3
DATA3[16:0]	O	GTM	Result values of channel 3
WR3	O	GTM	Write signal for DATA3

General

PHSYNC	I	Phase synchronizer	Synchronization signal for analog clocks
MODCLK	I	SCU: f_{SPB}	Module clock
RESET	I	SCU	Reset signal (general)
SGNA	I	P00.4	Sign input A (carrier signal)
SGNB	I	P33.13	Sign input B (carrier signal)
CGPWMP	O	P00.6, P02.1, P33.12	Positive PWM signal of carrier generator
CGPWMN	O	P00.5, P02.0, P33.11	Negative PWM signal of carrier generator

31.4 Revision History

This is a summary of the modifications that have been applied to this chapter.

Table 260 Revision History

Reference	Change to Previous Version	Comment
V3.0.0		
-	No change.	

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)**Table 260 Revision History (cont'd)**

Reference	Change to Previous Version	Comment
V3.0.1		
-	No functional change.	
V3.0.2		
-	No functional change.	
V3.0.3		
-	No functional change.	
V3.0.4		
-	No functional change.	
V3.0.5		
-	No functional change.	
V3.0.6		
-	No functional change.	

Inter-Integrated Circuit (I2C)

32 Inter-Integrated Circuit (I2C)

This chapter describes the Inter-Integrated Circuit (short I2C) Module of the TC36x.

32.1 TC36x Specific IP Configuration

See features in family spec.

No product specific configuration for I2C

32.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

Table 261 Register Address Space - I2C

Module	Base Address	End Address	Note
I2C0	F00C0000 _H	F00D00FF _H	FPI slave interface

Register Overview Table

There are no product specific register for this module.

32.3 TC36x Specific Registers

There are no product specific register for this module.

32.4 Connectivity

The tables below list all the connections of I2C instances.

Table 262 Connections of I2C0

Interface Signals	connects		Description
I2C0:SCL	to	P02.5:ALT(5)	Serial Clock Output
		P13.1:ALT(6)	
		P15.4:ALT(6)	
I2C0:SDA	to	P02.4:ALT(5)	Serial Data Output
		P13.2:ALT(6)	
		P15.5:ALT(6)	
I2C0:SDAA	from	P02.4:IN	Serial Data Input 0
I2C0:SDAB	from	P13.2:IN	Serial Data Input 1
I2C0:SDAC	from	P15.5:IN	Serial Data Input 2
I2C0:SLEEP	from	SCU:scu_syst_sleep_n	Sleep Request
I2C0:DTR_INT	to	INT:i2c0.DTR_INT	I2C Data Transfer Request
I2C0:ERR_INT	to	INT:i2c0.ERR_INT	I2C Error Service Request
I2C0:P_INT	to	INT:i2c0.P_INT	I2C Kernel Service Request

Inter-Integrated Circuit (I2C)**32.5 Revision History****Table 263 Revision History**

Reference	Change to Previous Version	Comment
V2.3.4		
Page 1	No functional changes. Formal changes in Connectivity tables.	
V2.3.5		
–	No functional changes.	
V2.3.6		
–	No functional changes.	

High Speed Serial Link (HSSL)

33 High Speed Serial Link (HSSL)

This section provides information regarding the implementation of the module HSSL specifically for device TC36x.

33.1 TC36x Specific IP Configuration

See features in family spec.

No product specific configuration for HSSL

33.2 TC36x Specific Register Set

33.2.1 Address Map

Table 264 Register Address Space - HSSL

Module	Base Address	End Address	Note
HSSL0	F0080000 _H	F00803FF _H	FPI slave interface

Note: The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

33.3 TC36x Specific Registers

There are no device specific registers in TC36x.

33.4 Connectivity

Table 265 Connections of HSSL0

Interface Signals	connects		Description
HSSL0:READ_PH_ERR_ALARM	to	SMU:hssl0_READ_PH_ERR_ALARM	SRI read phase error
HSSL0:COK_INT(3:0)	to	INT:hssl0_COK_INT(3:0)	Channel OK Service Request
HSSL0:RDI_INT(3:0)	to	INT:hssl0_RDI_INT(3:0)	Channel Read Data Service Request
HSSL0:ERR_INT(3:0)	to	INT:hssl0_ERR_INT(3:0)	Channel Error Service Request
HSSL0:TRG_INT(3:0)	to	INT:hssl0_TRG_INT(3:0)	Channel Trigger Interrupt Service Request m
HSSL0:EXI_INT	to	INT:hssl0_EXI_INT	HSSL Exception Service Request

High Speed Serial Link (HSSL)**33.5 Revision History****Table 266 Revision History**

Reference	Change to Previous Version	Comment
V3.0.16		
-	Initial version for TC36X	
V3.0.17		
-	No functional changes.	
V3.0.18		
-	No changes.	
V3.0.19		
-	No changes.	

33.6 High Speed Communication Tunnel (HSCT)

This section provides information regarding the implementation of the module HSCT specifically for device TC36x.

33.6.1 TC36x Specific IP Configuration

See features in family spec.

No product specific configuration for HSCT

No differences between the instances of the HSCT in TC36x.

33.6.2 TC36x Specific Register Set

There are no device specific registers in TC36x.

33.6.2.1 Address Map

Table 267 Register Address Space - HSCT

Module	Base Address	End Address	Note
HSCT0	F0090000 _H	F009FFFF _H	FPI slave interface

Note: The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

33.6.3 TC36x Specific Registers

There are no module specific registers for the HSCT.

33.6.4 Connectivity

The LVDS TX output of HSCT0 is connected to P21.4 and P21.5, the LVDS RX input to P21.2 and P21.3.

The SYSCLK input/output is connected to P20.0. For more details see the pinning chapter.

Table 268 Connections of HSCT0

Interface Signals	connects		Description
HSCT0:RXDN	from	TC36x:P21.2	Rx data
HSCT0:RXDP	from	TC36x:P21.3	Rx data
HSCT0:SYSCLK_IN	from	CCU:CLKA_REF_HSCT	Reference clock
HSCT0:SYSCLK_OUT	to	P20.0:ALT(5)	sys clock output
HSCT0:TXDN	to	TC36x:P21.4	Tx data
HSCT0:TXDP	to	TC36x:P21.5	Tx data
HSCT0:INT	to	INT:hsct0.INT	HSCT Service Request

33.6.5 Revision History

Table 269 Revision History

Reference	Change to Previous Version	Comment
V2.3.11		
-	Initial version.	
V2.3.12		
Page 3	Formal changes in connections table, no functional changes.	
V2.3.13		
-	No functional changes.	
V2.3.14		
Page 3	Updated headline.	
V2.3.15		
-	No functional changes.	

Asynchronous Serial Interface (ASCLIN)

34 Asynchronous Serial Interface (ASCLIN)

Text with reference to family spec.

34.1 TC36x Specific IP Configuration

No product specific configuration for ASCLIN

Asynchronous Serial Interface (ASCLIN)

34.2 TC36x Specific Register Set

Register Address Space Table

Table 270 Register Address Space - ASCLIN

Module	Base Address	End Address	Note
ASCLIN0	F0000600 _H	F00006FF _H	FPI slave interface
ASCLIN1	F0000700 _H	F00007FF _H	FPI slave interface
ASCLIN2	F0000800 _H	F00008FF _H	FPI slave interface
ASCLIN3	F0000900 _H	F00009FF _H	FPI slave interface
ASCLIN4	F0000A00 _H	F0000AFF _H	FPI slave interface
ASCLIN5	F0000B00 _H	F0000BFF _H	FPI slave interface
ASCLIN6	F0000C00 _H	F0000CFF _H	FPI slave interface
ASCLIN7	F0000D00 _H	F0000DFF _H	FPI slave interface
ASCLIN8	F0000E00 _H	F0000EFF _H	FPI slave interface
ASCLIN9	F0000F00 _H	F0000FFF _H	FPI slave interface
ASCLIN10	F02C0A00 _H	F02C0AFF _H	FPI slave interface
ASCLIN11	F02C0B00 _H	F02C0BFF _H	FPI slave interface

Register Overview Table

Table 271 Register Overview - ASCLIN (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN1_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN2_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN3_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN4_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN5_CLC	Clock Control Register	000 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN6_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN7_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN8_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN9_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN10_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN11_CLC	Clock Control Register	000 _H	See Family Spec
ASCLIN0_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN1_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN2_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN3_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN4_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN5_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN6_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN7_IOCR	Input and Output Control Register	004 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)
Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN8_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN9_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN10_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN11_IOCR	Input and Output Control Register	004 _H	See Family Spec
ASCLIN0_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN1_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN2_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN3_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN4_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN5_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN6_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN7_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN8_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN9_ID	Module Identification Register	008 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN10_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN11_ID	Module Identification Register	008 _H	See Family Spec
ASCLIN0_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN1_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN2_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN3_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN4_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN5_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN6_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN7_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN8_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN9_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN10_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec
ASCLIN11_TXFIFOCON	TX FIFO Configuration Register	00C _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN1_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN2_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN3_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN4_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN5_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN6_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN7_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN8_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN9_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN10_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN11_RXFIFOCON	RX FIFO Configuration Register	010 _H	See Family Spec
ASCLIN0_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN1_BITCON	Bit Configuration Register	014 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN3_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN4_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN5_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN6_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN7_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN8_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN9_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN10_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN11_BITCON	Bit Configuration Register	014 _H	See Family Spec
ASCLIN0_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN1_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN2_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN3_FRAMECON	Frame Control Register	018 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN5_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN6_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN7_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN8_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN9_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN10_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN11_FRAMECON	Frame Control Register	018 _H	See Family Spec
ASCLIN0_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN1_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN2_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN3_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN4_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN5_DATCON	Data Configuration Register	01C _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN6_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN7_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN8_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN9_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN10_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN11_DATCON	Data Configuration Register	01C _H	See Family Spec
ASCLIN0_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN1_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN2_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN3_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN4_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN5_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN6_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN7_BRG	Baud Rate Generation Register	020 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN8_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN9_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN10_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN11_BRG	Baud Rate Generation Register	020 _H	See Family Spec
ASCLIN0_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN1_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN2_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN3_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN4_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN5_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN6_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN7_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN8_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN9_BRD	Baud Rate Detection Register	024 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN10_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN11_BRD	Baud Rate Detection Register	024 _H	See Family Spec
ASCLIN0_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN1_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN2_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN3_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN4_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN5_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN6_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN7_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN8_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN9_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN10_LINCON	LIN Control Register	028 _H	See Family Spec
ASCLIN11_LINCON	LIN Control Register	028 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN1_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN2_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN3_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN4_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN5_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN6_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN7_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN8_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN9_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN10_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN11_LINBTIMER	LIN Break Timer Register	02C _H	See Family Spec
ASCLIN0_LINHBTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN1_LINHBTIMER	LIN Header Timer Register	030 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN3_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN4_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN5_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN6_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN7_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN8_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN9_LINHTIMER	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN10_LINHTIME R	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN11_LINHTIME R	LIN Header Timer Register	030 _H	See Family Spec
ASCLIN0_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN1_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN2_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN3_FLAGS	Flags Register	034 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN5_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN6_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN7_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN8_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN9_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN10_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN11_FLAGS	Flags Register	034 _H	See Family Spec
ASCLIN0_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN1_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN2_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN3_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN4_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN5_FLAGSSET	Flags Set Register	038 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN6_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN7_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN8_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN9_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN10_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN11_FLAGSSET	Flags Set Register	038 _H	See Family Spec
ASCLIN0_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN1_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN2_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN3_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN4_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN5_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN6_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN7_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN8_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN9_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN10_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN11_FLAGSCLEAR	Flags Clear Register	03C _H	See Family Spec
ASCLIN0_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN1_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN2_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN3_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN4_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN5_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN6_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN7_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN8_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN9_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN10_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN11_FLAGSENABLE	Flags Enable Register	040 _H	See Family Spec
ASCLIN0_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN1_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN2_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN3_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN4_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN5_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN6_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN7_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN8_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN9_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN10_TXDATA	Transmit Data Register	044 _H	See Family Spec
ASCLIN11_TXDATA	Transmit Data Register	044 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN1_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN2_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN3_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN4_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN5_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN6_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN7_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN8_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN9_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN10_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN11_RXDATA	Receive Data Register	048 _H	See Family Spec
ASCLIN0_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN1_CSR	Clock Selection Register	04C _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN3_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN4_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN5_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN6_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN7_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN8_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN9_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN10_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN11_CSR	Clock Selection Register	04C _H	See Family Spec
ASCLIN0_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN1_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN2_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN3_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)
Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN5_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN6_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN7_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN8_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN9_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN10_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN11_RXDATAD	Receive Data Debug Register	050 _H	See Family Spec
ASCLIN0_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN1_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN2_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN3_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN4_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN5_OCS	OCDS Control and Status	0E8 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN6_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN7_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN8_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN9_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN10_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN11_OCS	OCDS Control and Status	0E8 _H	See Family Spec
ASCLIN0_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN1_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN2_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN3_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN4_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN5_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN6_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN7_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN8_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN9_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN10_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN11_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	See Family Spec
ASCLIN0_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN1_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN2_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN3_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN4_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN5_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN6_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN7_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN8_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN9_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN10_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN11_KRST1	Kernel Reset Register 1	0F0 _H	See Family Spec
ASCLIN0_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN1_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN2_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN3_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN4_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN5_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN6_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN7_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN8_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN9_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN10_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec
ASCLIN11_KRST0	Kernel Reset Register 0	0F4 _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN1_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN2_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN3_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN4_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN5_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN6_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN7_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN8_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN9_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN10_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN11_ACCEN1	Access Enable Register 1	0F8 _H	See Family Spec
ASCLIN0_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN1_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec

Asynchronous Serial Interface (ASCLIN)

Table 271 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN3_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN4_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN5_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN6_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN7_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN8_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN9_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN10_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec
ASCLIN11_ACCEN0	Access Enable Register 0	0FC _H	See Family Spec

34.3 TC36x Specific Registers

No deviations from the Family Spec

34.4 Connectivity

Table 272 Connections of ASCLIN0

Interface Signals	connects		Description
ASCLIN0:ACTSA	from	P14.9:IN	Clear to send input
ASCLIN0:ACTSD	from	ASCLIN0:ARTS	Clear to send input

Asynchronous Serial Interface (ASCLIN)

Table 272 Connections of ASCLIN0 (cont'd)

Interface Signals	connects		Description
ASCLIN0:ARTS	to	P14.7:ALT(2)	Ready to send output
		ASCLIN0:ACTSD	
ASCLIN0:ARXA	from	P14.1:IN	Receive input
ASCLIN0:ARXB	from	P15.3:IN	Receive input
ASCLIN0:ARXD	from	P33.10:IN	Receive input
ASCLIN0:ASCLK	to	P14.0:ALT(6)	Shift clock output
		P15.2:ALT(6)	
ASCLIN0:ATX	to	IOM:MON2(12)	Transmit output
		IOM:REF2(12)	
		P14.0:ALT(2)	
		P14.1:ALT(2)	
		P15.2:ALT(2)	
		P15.3:ALT(2)	
		P33.9:ALT(6)	
ASCLIN0:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN0:TX_INT	to	INT:asclin0_TX_INT	ASCLIN Transmit Service Request
ASCLIN0:RX_INT	to	INT:asclin0_RX_INT	ASCLIN Receive Service Request
ASCLIN0:ERR_INT	to	INT:asclin0_ERR_INT	ASCLIN Error Service Request

Table 273 Connections of ASCLIN1

Interface Signals	connects		Description
ASCLIN1:ACTSA	from	P20.7:IN	Clear to send input
ASCLIN1:ACTSB	from	P32.4:IN	Clear to send input
ASCLIN1:ACTSD	from	ASCLIN1:ARTS	Clear to send input
ASCLIN1:ARTS	to	P20.6:ALT(2)	Ready to send output
		P23.1:ALT(2)	
		ASCLIN1:ACTSD	
ASCLIN1:ARXA	from	P15.1:IN	Receive input
ASCLIN1:ARXB	from	P15.5:IN	Receive input
ASCLIN1:ARXC	from	P20.9:IN	Receive input
ASCLIN1:ARXD	from	P14.8:IN	Receive input
ASCLIN1:ARXE	from	P11.10:IN	Receive input
ASCLIN1:ARXF	from	P33.13:IN	Receive input
ASCLIN1:ARXG	from	P02.3:IN	Receive input
ASCLIN1:ASCLK	to	P15.0:ALT(6)	Shift clock output
		P20.10:ALT(6)	
		P33.11:ALT(2)	
		P33.12:ALT(4)	

Asynchronous Serial Interface (ASCLIN)

Table 273 Connections of ASCLIN1 (cont'd)

Interface Signals	connects		Description
ASCLIN1:ASLSO	to	P14.3:ALT(4)	Slave select signal output
		P20.8:ALT(2)	
		P33.10:ALT(4)	
ASCLIN1:ATX	to	IOM:MON2(13)	Transmit output
		IOM:REF2(13)	
		P02.2:ALT(2)	
		P11.12:ALT(2)	
		P14.10:ALT(4)	
		P15.0:ALT(2)	
		P15.1:ALT(2)	
		P15.4:ALT(2)	
		P15.5:ALT(2)	
		P20.10:ALT(2)	
		P33.12:ALT(2)	
		P33.13:ALT(2)	
ASCLIN1:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN1:TX_INT	to	INT:asclin1_TX_INT	ASCLIN Transmit Service Request
ASCLIN1:RX_INT	to	INT:asclin1_RX_INT	ASCLIN Receive Service Request
ASCLIN1:ERR_INT	to	INT:asclin1_ERR_INT	ASCLIN Error Service Request

Table 274 Connections of ASCLIN2

Interface Signals	connects		Description
ASCLIN2:ACTSA	from	P10.7:IN	Clear to send input
ASCLIN2:ACTSB	from	P33.5:IN	Clear to send input
ASCLIN2:ACTSD	from	ASCLIN2:ARTS	Clear to send input
ASCLIN2:ARTS	to	P10.8:ALT(2)	Ready to send output
		P33.4:ALT(2)	
		ASCLIN2:ACTSD	
ASCLIN2:ARXA	from	P14.3:IN	Receive input
ASCLIN2:ARXB	from	P02.1:IN	Receive input
ASCLIN2:ARXD	from	P10.6:IN	Receive input
ASCLIN2:ARXE	from	P33.8:IN	Receive input
ASCLIN2:ARXG	from	P02.0:IN	Receive input
ASCLIN2:ASCLK	to	P02.4:ALT(2)	Shift clock output
		P10.6:ALT(2)	
		P14.2:ALT(6)	
		P33.7:ALT(2)	
		P33.9:ALT(4)	

Asynchronous Serial Interface (ASCLIN)

Table 274 Connections of ASCLIN2 (cont'd)

Interface Signals	connects		Description
ASCLIN2:ASLSO	to	P02.3:ALT(2)	Slave select signal output
		P10.5:ALT(6)	
		P33.6:ALT(2)	
ASCLIN2:ATX	to	IOM:MON2(14)	Transmit output
		IOM:REF2(14)	
		P02.0:ALT(2)	
		P10.5:ALT(2)	
		P14.2:ALT(2)	
		P14.3:ALT(2)	
		P33.8:ALT(2)	
		P33.9:ALT(2)	
ASCLIN2:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN2:TX_INT	to	INT:asclin2_TX_INT	ASCLIN Transmit Service Request
ASCLIN2:RX_INT	to	INT:asclin2_RX_INT	ASCLIN Receive Service Request
ASCLIN2:ERR_INT	to	INT:asclin2_ERR_INT	ASCLIN Error Service Request

Table 275 Connections of ASCLIN3

Interface Signals	connects		Description
ASCLIN3:ACTSA	from	P00.12:IN	Clear to send input
ASCLIN3:ACTSD	from	ASCLIN3:ARTS	Clear to send input
ASCLIN3:ARTS	to	P00.9:ALT(3)	Ready to send output
		ASCLIN3:ACTSD	
ASCLIN3:ARXA	from	P15.7:IN	Receive input
ASCLIN3:ARXB	from	P11.0:IN	Receive input
ASCLIN3:ARXC	from	P20.3:IN	Receive input
ASCLIN3:ARXD	from	P32.2:IN	Receive input
ASCLIN3:ARXE	from	P00.1:IN	Receive input
ASCLIN3:ARXF	from	P21.6:IN	Receive input
ASCLIN3:ARXGN	from	TC36x:P21.2	Differential Receive input (low active)
ASCLIN3:ARXGP	from	TC36x:P21.3	Differential Receive input (high active)

Asynchronous Serial Interface (ASCLIN)

Table 275 Connections of ASCLIN3 (cont'd)

Interface Signals	connects	Description	
ASCLIN3:ASCLK	to	P00.0:ALT(2)	Shift clock output
		P00.2:ALT(2)	
		P11.1:ALT(2)	
		P11.4:ALT(2)	
		P15.6:ALT(6)	
		P15.8:ALT(6)	
		P20.0:ALT(3)	
		P21.5:ALT(2)	
		P21.7:ALT(3)	
		P32.3:ALT(4)	
		P33.2:ALT(2)	
ASCLIN3:ASLSO	to	P00.3:ALT(2)	Slave select signal output
		P12.1:ALT(2)	
		P14.3:ALT(5)	
		P21.2:ALT(2)	
		P21.6:ALT(2)	
		P33.1:ALT(2)	
ASCLIN3:ATX	to	IOM:MON2(15)	Transmit output
		IOM:REF2(15)	
		P00.0:ALT(3)	
		P00.1:ALT(2)	
		P11.0:ALT(2)	
		P11.1:ALT(3)	
		P15.6:ALT(2)	
		P15.7:ALT(2)	
		P20.0:ALT(2)	
		P20.3:ALT(2)	
		P21.7:ALT(2)	
		P22.0:ALT(2)	
		P22.1:ALT(2)	
		P32.2:ALT(2)	
P32.3:ALT(2)			
ASCLIN3:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN3:TX_INT	to	INT:asclin3_TX_INT	ASCLIN Transmit Service Request
ASCLIN3:RX_INT	to	INT:asclin3_RX_INT	ASCLIN Receive Service Request
ASCLIN3:ERR_INT	to	INT:asclin3_ERR_INT	ASCLIN Error Service Request

Asynchronous Serial Interface (ASCLIN)

Table 276 Connections of ASCLIN4

Interface Signals	connects		Description
ASCLIN4:ACTSD	from	ASCLIN4:ARTS	Clear to send input
ASCLIN4:ARTS	to	ASCLIN4:ACTSD	Ready to send output
ASCLIN4:ARXA	from	P00.12:IN	Receive input
ASCLIN4:ASCLK	to	P00.10:ALT(2)	Shift clock output
ASCLIN4:ASLSO	to	P00.11:ALT(2)	Slave select signal output
ASCLIN4:ATX	to	P00.9:ALT(5)	Transmit output
ASCLIN4:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN4:TX_INT	to	INT:asclin4_TX_INT	ASCLIN Transmit Service Request
ASCLIN4:RX_INT	to	INT:asclin4_RX_INT	ASCLIN Receive Service Request
ASCLIN4:ERR_INT	to	INT:asclin4_ERR_INT	ASCLIN Error Service Request

Table 277 Connections of ASCLIN5

Interface Signals	connects		Description
ASCLIN5:ACTSD	from	ASCLIN5:ARTS	Clear to send input
ASCLIN5:ARTS	to	ASCLIN5:ACTSD	Ready to send output
ASCLIN5:ARXA	from	P00.6:IN	Receive input
ASCLIN5:ARXB	from	P33.4:IN	Receive input
ASCLIN5:ARXC	from	P22.3:IN	Receive input
ASCLIN5:ASCLK	to	P33.3:ALT(2)	Shift clock output
ASCLIN5:ASLSO	to	P14.8:ALT(2) P33.5:ALT(7)	Slave select signal output
ASCLIN5:ATX	to	P00.7:ALT(2) P22.2:ALT(2) P33.0:ALT(2)	Transmit output
ASCLIN5:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN5:TX_INT	to	INT:asclin5_TX_INT	ASCLIN Transmit Service Request
ASCLIN5:RX_INT	to	INT:asclin5_RX_INT	ASCLIN Receive Service Request
ASCLIN5:ERR_INT	to	INT:asclin5_ERR_INT	ASCLIN Error Service Request

Table 278 Connections of ASCLIN6

Interface Signals	connects		Description
ASCLIN6:ACTSD	from	ASCLIN6:ARTS	Clear to send input
ASCLIN6:ARTS	to	ASCLIN6:ACTSD	Ready to send output
ASCLIN6:ARXA	from	P23.3:IN	Receive input
ASCLIN6:ARXE	from	P22.0:IN	Receive input
ASCLIN6:ARXF	from	P23.1:IN	Receive input
ASCLIN6:ASCLK	to	P23.1:ALT(7)	Shift clock output

Asynchronous Serial Interface (ASCLIN)

Table 278 Connections of ASCLIN6 (cont'd)

Interface Signals	connects		Description
ASCLIN6:ASLSO	to	P23.4:ALT(2)	Slave select signal output
ASCLIN6:ATX	to	P22.0:ALT(7)	Transmit output
		P23.5:ALT(2)	
ASCLIN6:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN6:TX_INT	to	INT:asclin6_TX_INT	ASCLIN Transmit Service Request
ASCLIN6:RX_INT	to	INT:asclin6_RX_INT	ASCLIN Receive Service Request
ASCLIN6:ERR_INT	to	INT:asclin6_ERR_INT	ASCLIN Error Service Request

Table 279 Connections of ASCLIN7

Interface Signals	connects		Description
ASCLIN7:ACTSD	from	ASCLIN7:ARTS	Clear to send input
ASCLIN7:ARTS	to	ASCLIN7:ACTSD	Ready to send output
ASCLIN7:ARXC	from	P23.2:IN	Receive input
ASCLIN7:ARXE	from	P22.1:IN	Receive input
ASCLIN7:ASLSO	to	P14.8:ALT(3)	Slave select signal output
ASCLIN7:ATX	to	P22.1:ALT(7)	Transmit output
		P23.3:ALT(2)	
ASCLIN7:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN7:TX_INT	to	INT:asclin7_TX_INT	ASCLIN Transmit Service Request
ASCLIN7:RX_INT	to	INT:asclin7_RX_INT	ASCLIN Receive Service Request
ASCLIN7:ERR_INT	to	INT:asclin7_ERR_INT	ASCLIN Error Service Request

Table 280 Connections of ASCLIN8

Interface Signals	connects		Description
ASCLIN8:ACTSD	from	ASCLIN8:ARTS	Clear to send input
ASCLIN8:ARTS	to	ASCLIN8:ACTSD	Ready to send output
ASCLIN8:ARXC	from	P33.1:IN	Receive input
ASCLIN8:ARXD	from	P33.6:IN	Receive input
ASCLIN8:ASCLK	to	P02.8:ALT(3)	Shift clock output
ASCLIN8:ATX	to	P33.7:ALT(4)	Transmit output
ASCLIN8:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN8:TX_INT	to	INT:asclin8_TX_INT	ASCLIN Transmit Service Request
ASCLIN8:RX_INT	to	INT:asclin8_RX_INT	ASCLIN Receive Service Request
ASCLIN8:ERR_INT	to	INT:asclin8_ERR_INT	ASCLIN Error Service Request

Asynchronous Serial Interface (ASCLIN)

Table 281 Connections of ASCLIN9

Interface Signals	connects		Description
ASCLIN9:ACTSD	from	ASCLIN9:ARTS	Clear to send input
ASCLIN9:ARTS	to	ASCLIN9:ACTSD	Ready to send output
ASCLIN9:ARXC	from	P14.7:IN	Receive input
ASCLIN9:ARXD	from	P14.9:IN	Receive input
ASCLIN9:ARXE	from	P20.6:IN	Receive input
ASCLIN9:ARXF	from	P20.7:IN	Receive input
ASCLIN9:ATX	to	P14.7:ALT(4) P20.7:ALT(2)	Transmit output
ASCLIN9:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN9:TX_INT	to	INT:asclin9_TX_INT	ASCLIN Transmit Service Request
ASCLIN9:RX_INT	to	INT:asclin9_RX_INT	ASCLIN Receive Service Request
ASCLIN9:ERR_INT	to	INT:asclin9_ERR_INT	ASCLIN Error Service Request

Table 282 Connections of ASCLIN10

Interface Signals	connects		Description
ASCLIN10:ACTSD	from	ASCLIN10:ARTS	Clear to send input
ASCLIN10:ARTS	to	ASCLIN10:ACTSD	Ready to send output
ASCLIN10:ARXA	from	P00.4:IN	Receive input
ASCLIN10:ARXB	from	P00.8:IN	Receive input
ASCLIN10:ARXC	from	P13.0:IN	Receive input
ASCLIN10:ARXD	from	P13.1:IN	Receive input
ASCLIN10:ASCLK	to	P13.2:ALT(2)	Shift clock output
ASCLIN10:ASLSO	to	P13.3:ALT(2)	Slave select signal output
ASCLIN10:ATX	to	P00.8:ALT(3) P13.0:ALT(2)	Transmit output
ASCLIN10:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN10:TX_INT	to	INT:asclin10_TX_INT	ASCLIN Transmit Service Request
ASCLIN10:RX_INT	to	INT:asclin10_RX_INT	ASCLIN Receive Service Request
ASCLIN10:ERR_INT	to	INT:asclin10_ERR_INT	ASCLIN Error Service Request

Table 283 Connections of ASCLIN11

Interface Signals	connects		Description
ASCLIN11:ACTSD	from	ASCLIN11:ARTS	Clear to send input
ASCLIN11:ARTS	to	ASCLIN11:ACTSD	Ready to send output
ASCLIN11:ARXA	from	P10.0:IN	Receive input
ASCLIN11:ARXB	from	P10.4:IN	Receive input
ASCLIN11:ARXC	from	P21.0:IN	Receive input

Asynchronous Serial Interface (ASCLIN)

Table 283 Connections of ASCLIN11 (cont'd)

Interface Signals	connects		Description
ASCLIN11:ARXD	from	P21.1:IN	Receive input
ASCLIN11:ARXE	from	P21.2:IN	Receive input
ASCLIN11:ARXF	from	P21.5:IN	Receive input
ASCLIN11:ASCLK	to	P21.3:ALT(2)	Shift clock output
ASCLIN11:ASLSO	to	P21.4:ALT(2)	Slave select signal output
ASCLIN11:ATX	to	P10.0:ALT(2)	Transmit output
		P21.0:ALT(2)	
		P21.5:ALT(3)	
ASCLIN11:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN11:TX_INT	to	INT:asclin11_TX_INT	ASCLIN Transmit Service Request
ASCLIN11:RX_INT	to	INT:asclin11_RX_INT	ASCLIN Receive Service Request
ASCLIN11:ERR_INT	to	INT:asclin11_ERR_INT	ASCLIN Error Service Request

34.5 Revision History

Table 284 Revision History

Reference	Change to Previous Version	Comment
V3.2.6		
Page 2	Register tables updated.	
	No functional change in connectivity tables.	
V3.2.7		
-	No functional changes.	
V3.2.8		
-	No functional changes.	

Queued Synchronous Peripheral Interface (QSPI)**35 Queued Synchronous Peripheral Interface (QSPI)****35.1 TC36x Specific IP Configuration****Table 285 TC36x specific configuration of QSPI**

Parameter	QSPI0	QSPI1	QSPI2	QSPI3
QSPI module has HSIC				

Queued Synchronous Peripheral Interface (QSPI)

35.2 TC36x Specific Register Set

Table 286 Register Address Space - QSPI

Module	Base Address	End Address	Note
QSPI0	F0001C00 _H	F0001CFF _H	Register block QSPI0
QSPI1	F0001D00 _H	F0001DFF _H	Register block QSPI1
QSPI2	F0001E00 _H	F0001EFF _H	Register block QSPI2
QSPI3	F0001F00 _H	F0001FFF _H	Register block QSPI3

Register Overview Tables of QSPI

Table 287 Register Overview - QSPI0 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_CLC	Clock Control Register	000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_PISEL	Port Input Select Register	004 _H	U,SV	SV,P	Application Reset	10
QSPI0_ID	Module Identification Register	008 _H	U,SV	BE	Application Reset	See Family Spec
QSPI0_GLOBALCON	Global Configuration Register	010 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_GLOBALCON1	Global Configuration Register 1	014 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_BACON	Basic Configuration Register	018 _H	U,SV	BE	Application Reset	See Family Spec
QSPI0_ECONz (z=0-7)	Configuration Extension z	020 _H +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_STATUS	Status Register	040 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_STATUS1	Status Register 1	044 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_SSOC	Slave Select Output Control Register	048 _H	U,SV	SV,P	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)
Table 287 Register Overview - QSPI0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_FLAGSCLEAR	Flags Clear Register	054 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_XXLCON	Extra Large Data Configuration Register	058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_MIXENTRY	MIX_ENTRY Register	05C _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_BACONENTRY	BACON_ENTRY Register	060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064 _H +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_RXEXIT	RX_EXIT Register	090 _H	U,SV	BE	Application Reset	See Family Spec
QSPI0_RXEXITD	RX_EXIT Debug Register	094 _H	U,SV	BE	Application Reset	See Family Spec
QSPI0_MC	Move Counter Register	0A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_MCCON	Move Counter control Register	0A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_OCS	OCDS Control and Status	0E8 _H	U,SV	SV,P	Debug Reset	See Family Spec
QSPI0_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_KRST1	Kernel Reset Register 1	0F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_KRST0	Kernel Reset Register 0	0F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)

Table 287 Register Overview - QSPI0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_ACCEN1	Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
QSPI0_ACCEN0	Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	See Family Spec

Table 288 Register Overview - QSPI1 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI1_CLC	Clock Control Register	000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_PISEL	Port Input Select Register	004 _H	U,SV	SV,P	Application Reset	11
QSPI1_ID	Module Identification Register	008 _H	U,SV	BE	Application Reset	See Family Spec
QSPI1_GLOBALC ON	Global Configuration Register	010 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_GLOBALC ON1	Global Configuration Register 1	014 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_BACON	Basic Configuration Register	018 _H	U,SV	BE	Application Reset	See Family Spec
QSPI1_ECONz (z=0-7)	Configuration Extension z	020 _H +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_STATUS	Status Register	040 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_STATUS1	Status Register 1	044 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_SSOC	Slave Select Output Control Register	048 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_FLAGSCLEAR	Flags Clear Register	054 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)
Table 288 Register Overview - QSPI1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI1_XXLCON	Extra Large Data Configuration Register	058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_MIXENTRY	MIX_ENTRY Register	05C _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_BACONENTRY	BACON_ENTRY Register	060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064 _H +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_RXEXIT	RX_EXIT Register	090 _H	U,SV	BE	Application Reset	See Family Spec
QSPI1_RXEXITD	RX_EXIT Debug Register	094 _H	U,SV	BE	Application Reset	See Family Spec
QSPI1_MC	Move Counter Register	0A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_MCCON	Move Counter control Register	0A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_OCS	OCDS Control and Status	0E8 _H	U,SV	SV,P	Debug Reset	See Family Spec
QSPI1_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_KRST1	Kernel Reset Register 1	0F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_KRST0	Kernel Reset Register 0	0F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_ACCEN1	Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
QSPI1_ACCEN0	Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)
Table 289 Register Overview - QSPI2 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI2_CLC	Clock Control Register	000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_PISEL	Port Input Select Register	004 _H	U,SV	SV,P	Application Reset	12
QSPI2_ID	Module Identification Register	008 _H	U,SV	BE	Application Reset	See Family Spec
QSPI2_GLOBALCON	Global Configuration Register	010 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_GLOBALCON1	Global Configuration Register 1	014 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_BACON	Basic Configuration Register	018 _H	U,SV	BE	Application Reset	See Family Spec
QSPI2_ECONz (z=0-7)	Configuration Extension z	020 _H +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_STATUS	Status Register	040 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_STATUS1	Status Register 1	044 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_SSOC	Slave Select Output Control Register	048 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_FLAGSCLEAR	Flags Clear Register	054 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_XXLCON	Extra Large Data Configuration Register	058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MIXENTRY	MIX_ENTRY Register	05C _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_BACONENTRY	BACON_ENTRY Register	060 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)
Table 289 Register Overview - QSPI2 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI2_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064 _H +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_RXEXIT	RX_EXIT Register	090 _H	U,SV	BE	Application Reset	See Family Spec
QSPI2_RXEXITD	RX_EXIT Debug Register	094 _H	U,SV	BE	Application Reset	See Family Spec
QSPI2_MC	Move Counter Register	0A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MCCON	Move Counter control Register	0A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_OCS	OCDS Control and Status	0E8 _H	U,SV	SV,P	Debug Reset	See Family Spec
QSPI2_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_KRST1	Kernel Reset Register 1	0F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_KRST0	Kernel Reset Register 0	0F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_ACCEN1	Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
QSPI2_ACCEN0	Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	See Family Spec

Table 290 Register Overview - QSPI3 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI3_CLC	Clock Control Register	000 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_PISEL	Port Input Select Register	004 _H	U,SV	SV,P	Application Reset	13

Queued Synchronous Peripheral Interface (QSPI)
Table 290 Register Overview - QSPI3 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI3_ID	Module Identification Register	008 _H	U,SV	BE	Application Reset	See Family Spec
QSPI3_GLOBALCON	Global Configuration Register	010 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_GLOBALCON1	Global Configuration Register 1	014 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_BACON	Basic Configuration Register	018 _H	U,SV	BE	Application Reset	See Family Spec
QSPI3_ECONz (z=0-7)	Configuration Extension z	020 _H +z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_STATUS	Status Register	040 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_STATUS1	Status Register 1	044 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_SSOC	Slave Select Output Control Register	048 _H	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_FLAGSCLEAR	Flags Clear Register	054 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_XXLCON	Extra Large Data Configuration Register	058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MIXENTRY	MIX_ENTRY Register	05C _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_BACONENTRY	BACON_ENTRY Register	060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064 _H +x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_RXEXIT	RX_EXIT Register	090 _H	U,SV	BE	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)
Table 290 Register Overview - QSPI3 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI3_RXEXITD	RX_EXIT Debug Register	094 _H	U,SV	BE	Application Reset	See Family Spec
QSPI3_MC	Move Counter Register	0A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MCCON	Move Counter control Register	0A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_OCS	OCDS Control and Status	0E8 _H	U,SV	SV,P	Debug Reset	See Family Spec
QSPI3_KRSTCLR	Kernel Reset Status Clear Register	0EC _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_KRST1	Kernel Reset Register 1	0F0 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_KRST0	Kernel Reset Register 0	0F4 _H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_ACCEN1	Access Enable Register 1	0F8 _H	U,SV	SV,SE	Application Reset	See Family Spec
QSPI3_ACCEN0	Access Enable Register 0	0FC _H	U,SV	SV,SE	Application Reset	See Family Spec

Queued Synchronous Peripheral Interface (QSPI)

35.3 TC36x Specific Registers

35.3.1 Register block QSPI

Port Input Select Register

The PISEL register controls the input signal selection of the SSC module.

QSPI0_PISEL

Port Input Select Register

(004_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SLSIS		0	SCIS		0	SRIS		0	MRIS					
r	rw		r	rw		r	rw		r	rw					

Field	Bits	Type	Description
MRIS	2:0	rw	Master Mode Receive Input Select MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 _B P20.12_IN ,
SRIS	6:4	rw	Slave Mode Receive Input Select SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 _B P20.14_IN ,
SCIS	10:8	rw	Slave Mode Clock Input Select SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 _B P20.11_IN ,

Queued Synchronous Peripheral Interface (QSPI)

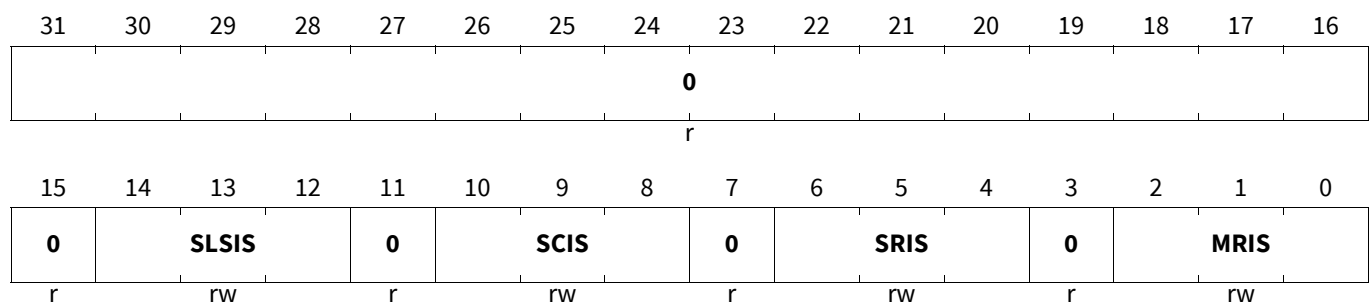
Field	Bits	Type	Description
SLSIS	14:12	rw	Slave Mode Slave Select Input Selection The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000 _B no input 001 _B P20.13_IN , 010 _B P20.9_IN ,
0	3, 7, 11, 31:15	r	Reserved Read as 0; should be written with 0.

QSPI1_PISEL

Port Input Select Register

(004_H)

Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
MRIS	2:0	rw	Master Mode Receive Input Select MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 _B P10.1_IN , 001 _B P11.3_IN ,
SRIS	6:4	rw	Slave Mode Receive Input Select SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000 _B P10.3_IN , 001 _B P11.9_IN , 010 _B P10.4_IN ,

Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
SCIS	10:8	rw	<p>Slave Mode Clock Input Select</p> <p>SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B P10.2_IN, 001_B P11.6_IN,</p>
SLSIS	14:12	rw	<p>Slave Mode Slave Select Input Selection</p> <p>The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B no input 001_B P11.10_IN,</p>
0	3, 7, 11, 31:15	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

QSPI2_PISEL

Port Input Select Register

(004_H)Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SLSIS		0	SCIS		0	SRIS		0	MRIS					
r	rw		r	rw		r	rw		r	rw					

Field	Bits	Type	Description
MRIS	2:0	rw	<p>Master Mode Receive Input Select</p> <p>MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B P15.4_IN, 001_B P15.7_IN, 010_B P21.3 P21.2, 100_B P15.2_IN, 101_B P14.10 P14.9,</p>

Queued Synchronous Peripheral Interface (QSPI)

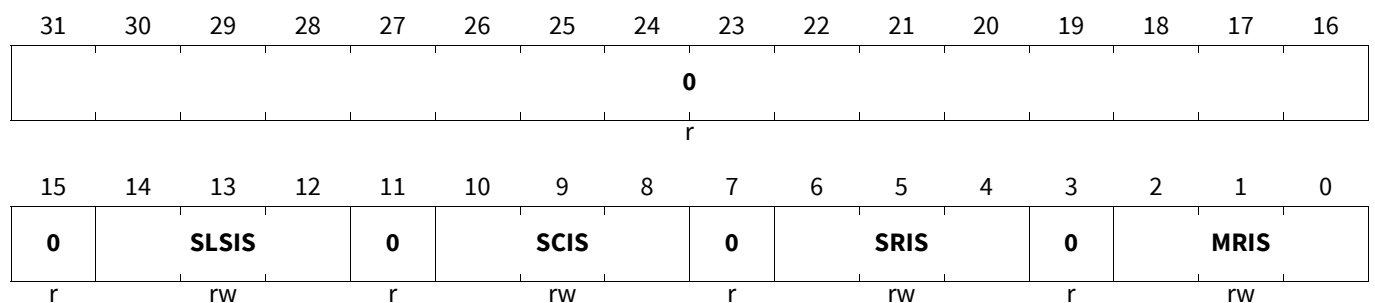
Field	Bits	Type	Description
SRIS	6:4	rw	<p>Slave Mode Receive Input Select SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B P15.5_IN, 001_B P15.6_IN,</p>
SCIS	10:8	rw	<p>Slave Mode Clock Input Select SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B P15.3_IN, 001_B P15.8_IN,</p>
SLSIS	14:12	rw	<p>Slave Mode Slave Select Input Selection The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000_B no input 001_B P15.2_IN, 010_B P15.1_IN,</p>
0	3, 7, 11, 31:15	r	<p>Reserved Read as 0; should be written with 0.</p>

QSPI3_PISEL

Port Input Select Register

(004_H)

Application Reset Value: 0000 0000_H



Queued Synchronous Peripheral Interface (QSPI)

Field	Bits	Type	Description
MRIS	2:0	rw	<p>Master Mode Receive Input Select</p> <p>MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B P02.5_IN, 001_B P10.7_IN, 011_B P22.1_IN,</p>
SRIS	6:4	rw	<p>Slave Mode Receive Input Select</p> <p>SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B P02.6_IN, 001_B P10.6_IN, 011_B P22.0_IN,</p>
SCIS	10:8	rw	<p>Slave Mode Clock Input Select</p> <p>SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B P02.7_IN, 001_B P10.8_IN, 011_B P22.3_IN,</p>
SLSIS	14:12	rw	<p>Slave Mode Slave Select Input Selection</p> <p>The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode.</p> <p>The following signal sources are available in this product (if supported by the package!)</p> <p>000_B no input 001_B P02.4_IN,</p>
0	3, 7, 11, 31:15	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

35.4 Connectivity

The tables below list all the connections of QSPI instances.

Queued Synchronous Peripheral Interface (QSPI)

Table 291 Connections of QSPI0

Interface Signals	connects		Description
QSPI0:MRST	to	IOM:MON2(0)	Slave SPI data output
		IOM:REF2(0)	
		P20.12:ALT(3)	
QSPI0:MRSTA	from	P20.12:IN	Master SPI data input
QSPI0:MTSR	to	P20.12:ALT(4)	Master SPI data output
		P20.14:ALT(3)	
QSPI0:MTSRA	from	P20.14:IN	Slave SPI data input
QSPI0:SCLK	to	P20.11:ALT(3)	Master SPI clock output
		P20.13:ALT(5)	
QSPI0:SCLKA	from	P20.11:IN	Slave SPI clock inputs
QSPI0:SLSIA	from	P20.13:IN	Slave select input
QSPI0:SLSIB	from	P20.9:IN	Slave select input
QSPI0:SLSO(0)	to	P20.8:ALT(3)	Master slave select output
QSPI0:SLSO(1)	to	P20.9:ALT(3)	Master slave select output
QSPI0:SLSO(2)	to	P20.13:ALT(3)	Master slave select output
QSPI0:SLSO(3)	to	P11.10:ALT(3)	Master slave select output
QSPI0:SLSO(4)	to	P11.11:ALT(3)	Master slave select output
QSPI0:SLSO(5)	to	P11.2:ALT(3)	Master slave select output
QSPI0:SLSO(6)	to	P20.10:ALT(3)	Master slave select output
QSPI0:SLSO(7)	to	P33.5:ALT(2)	Master slave select output
QSPI0:SLSO(8)	to	P20.6:ALT(3)	Master slave select output
QSPI0:SLSO(9)	to	P20.3:ALT(3)	Master slave select output
QSPI0:SLSO(13)	to	P15.0:ALT(3)	Master slave select output
QSPI0:TX_INT	to	INT:qspi0.TX_INT	QSPI Transmit Service Request
QSPI0:RX_INT	to	INT:qspi0.RX_INT	QSPI Receive Service Request
QSPI0:ERR_INT	to	INT:qspi0.ERR_INT	QSPI Error Service Request
QSPI0:PT_INT	to	INT:qspi0.PT_INT	QSPI Phase Transition Service Request
QSPI0:U_INT	to	INT:qspi0.U_INT	QSPI User Defined Service Request
QSPI0:HC_INT	to	INT:qspi0.HC_INT	QSPI High Speed Capture Service Request

Table 292 Connections of QSPI1

Interface Signals	connects		Description
QSPI1:MRST	to	IOM:MON2(1)	Slave SPI data output
		IOM:REF2(1)	
		P10.1:ALT(3)	
		P10.6:ALT(6)	
		P11.3:ALT(3)	

Queued Synchronous Peripheral Interface (QSPI)

Table 292 Connections of QSPI1 (cont'd)

Interface Signals	connects		Description
QSPI1:MRSTA	from	P10.1:IN	Master SPI data input
QSPI1:MRSTB	from	P11.3:IN	Master SPI data input
QSPI1:MTSR	to	P10.1:ALT(2)	Master SPI data output
		P10.3:ALT(3)	
		P10.4:ALT(4)	
		P11.9:ALT(3)	
QSPI1:MTSRA	from	P10.3:IN	Slave SPI data input
QSPI1:MTSRB	from	P11.9:IN	Slave SPI data input
QSPI1:MTSRC	from	P10.4:IN	Slave SPI data input
QSPI1:SCLK	to	P10.2:ALT(3)	Master SPI clock output
		P11.6:ALT(3)	
QSPI1:SCLKA	from	P10.2:IN	Slave SPI clock inputs
QSPI1:SCLKB	from	P11.6:IN	Slave SPI clock inputs
QSPI1:SLSIA	from	P11.10:IN	Slave select input
QSPI1:SLSO(0)	to	P20.8:ALT(4)	Master slave select output
QSPI1:SLSO(1)	to	P20.9:ALT(4)	Master slave select output
QSPI1:SLSO(2)	to	P20.13:ALT(4)	Master slave select output
QSPI1:SLSO(3)	to	P11.10:ALT(4)	Master slave select output
QSPI1:SLSO(4)	to	P11.11:ALT(4)	Master slave select output
QSPI1:SLSO(5)	to	P11.2:ALT(4)	Master slave select output
QSPI1:SLSO(6)	to	P33.10:ALT(2)	Master slave select output
QSPI1:SLSO(7)	to	P33.5:ALT(3)	Master slave select output
QSPI1:SLSO(8)	to	P10.4:ALT(3)	Master slave select output
QSPI1:SLSO(9)	to	P10.5:ALT(4)	Master slave select output
QSPI1:SLSO(10)	to	P10.0:ALT(3)	Master slave select output
QSPI1:TX_INT	to	INT:qspi1.TX_INT	QSPI Transmit Service Request
QSPI1:RX_INT	to	INT:qspi1.RX_INT	QSPI Receive Service Request
QSPI1:ERR_INT	to	INT:qspi1.ERR_INT	QSPI Error Service Request
QSPI1:PT_INT	to	INT:qspi1.PT_INT	QSPI Phase Transition Service Request
QSPI1:U_INT	to	INT:qspi1.U_INT	QSPI User Defined Service Request
QSPI1:HC_INT	to	INT:qspi1.HC_INT	QSPI High Speed Capture Service Request

Table 293 Connections of QSPI2

Interface Signals	connects		Description
QSPI2:MRST	to	IOM:MON2(2)	Slave SPI data output
		IOM:REF2(2)	
		P15.4:ALT(3)	
		P15.7:ALT(3)	

Queued Synchronous Peripheral Interface (QSPI)

Table 293 Connections of QSPI2 (cont'd)

Interface Signals	connects		Description
QSPI2:MRSTA	from	P15.4:IN	Master SPI data input
QSPI2:MRSTB	from	P15.7:IN	Master SPI data input
QSPI2:MRSTCN	from	TC36x:P21.2	Master SPI data input (LVDS N line)
QSPI2:MRSTCP	from	TC36x:P21.3	Master SPI data input (LVDS P line)
QSPI2:MRSTE	from	P15.2:IN	Master SPI data input
QSPI2:MRSTFN	from	TC36x:P14.9	Master SPI data input (LVDS N line)
QSPI2:MRSTFP	from	TC36x:P14.10	Master SPI data input (LVDS P line)
QSPI2:MTSR	to	P13.3:ALT(3)	Master SPI data output
		P15.5:ALT(3)	
		P15.6:ALT(3)	
QSPI2:MTSRA	from	P15.5:IN	Slave SPI data input
QSPI2:MTSRB	from	P15.6:IN	Slave SPI data input
QSPI2:MTSRN	to	P13.2:ALT(3)	Master SPI data output (LVDS N line)
QSPI2:SCLK	to	P13.1:ALT(3)	Master SPI clock output
		P15.3:ALT(3)	
		P15.6:ALT(5)	
		P15.8:ALT(3)	
		P33.1:ALT(3)	
QSPI2:SCLKA	from	P15.3:IN	Slave SPI clock inputs
QSPI2:SCLKB	from	P15.8:IN	Slave SPI clock inputs
QSPI2:SCLKN	to	P13.0:ALT(3)	Master SPI clock output (LVDS N line)
QSPI2:SLSIA	from	P15.2:IN	Slave select input
QSPI2:SLSIB	from	P15.1:IN	Slave select input
QSPI2:SLSO(0)	to	P15.2:ALT(3)	Master slave select output
QSPI2:SLSO(1)	to	P14.2:ALT(3)	Master slave select output
QSPI2:SLSO(2)	to	P14.6:ALT(3)	Master slave select output
QSPI2:SLSO(3)	to	P14.3:ALT(3)	Master slave select output
QSPI2:SLSO(4)	to	P14.7:ALT(3)	Master slave select output
QSPI2:SLSO(5)	to	P15.1:ALT(3)	Master slave select output
QSPI2:SLSO(6)	to	P33.13:ALT(4)	Master slave select output
QSPI2:SLSO(7)	to	P20.10:ALT(4)	Master slave select output
QSPI2:SLSO(8)	to	P20.6:ALT(4)	Master slave select output
QSPI2:SLSO(9)	to	P20.3:ALT(4)	Master slave select output
QSPI2:SLSO(10)	to	P33.2:ALT(3)	Master slave select output
QSPI2:SLSO(11)	to	P33.6:ALT(3)	Master slave select output
QSPI2:SLSO(12)	to	P33.4:ALT(3)	Master slave select output
QSPI2:TX_INT	to	INT:qspi2.TX_INT	QSPI Transmit Service Request
QSPI2:RX_INT	to	INT:qspi2.RX_INT	QSPI Receive Service Request

Queued Synchronous Peripheral Interface (QSPI)

Table 293 Connections of QSPI2 (cont'd)

Interface Signals	connects		Description
QSPI2:ERR_INT	to	INT:qspi2.ERR_INT	QSPI Error Service Request
QSPI2:PT_INT	to	INT:qspi2.PT_INT	QSPI Phase Transition Service Request
QSPI2:U_INT	to	INT:qspi2.U_INT	QSPI User Defined Service Request
QSPI2:HC_INT	to	INT:qspi2.HC_INT	QSPI High Speed Capture Service Request

Table 294 Connections of QSPI3

Interface Signals	connects		Description
QSPI3:MRST	to	IOM:MON2(3)	Slave SPI data output
		IOM:REF2(3)	
		P02.5:ALT(3)	
		P10.7:ALT(3)	
		P22.1:ALT(3)	
QSPI3:MRSTA	from	P02.5:IN	Master SPI data input
QSPI3:MRSTB	from	P10.7:IN	Master SPI data input
QSPI3:MRSTD	from	P22.1:IN	Master SPI data input
QSPI3:MTSR	to	P02.6:ALT(3)	Master SPI data output
		P10.6:ALT(3)	
		P22.0:ALT(3)	
QSPI3:MTSRA	from	P02.6:IN	Slave SPI data input
QSPI3:MTSRB	from	P10.6:IN	Slave SPI data input
QSPI3:MTSRD	from	P22.0:IN	Slave SPI data input
QSPI3:SCLK	to	P02.7:ALT(3)	Master SPI clock output
		P10.8:ALT(3)	
		P22.3:ALT(3)	
QSPI3:SCLKA	from	P02.7:IN	Slave SPI clock inputs
QSPI3:SCLKB	from	P10.8:IN	Slave SPI clock inputs
QSPI3:SCLKD	from	P22.3:IN	Slave SPI clock inputs
QSPI3:SLSIA	from	P02.4:IN	Slave select input
QSPI3:SLSO(0)	to	P02.4:ALT(3)	Master slave select output
QSPI3:SLSO(1)	to	P02.0:ALT(3)	Master slave select output
QSPI3:SLSO(2)	to	P02.1:ALT(3)	Master slave select output
QSPI3:SLSO(3)	to	P00.5:ALT(3)	Master slave select output
		P02.2:ALT(3)	
QSPI3:SLSO(4)	to	P00.2:ALT(6)	Master slave select output
		P02.3:ALT(3)	
QSPI3:SLSO(5)	to	P02.8:ALT(2)	Master slave select output
QSPI3:SLSO(6)	to	P00.8:ALT(2)	Master slave select output
QSPI3:SLSO(7)	to	P00.9:ALT(2)	Master slave select output

Queued Synchronous Peripheral Interface (QSPI)

Table 294 Connections of QSPI3 (cont'd)

Interface Signals	connects		Description
QSPI3:SLSO(8)	to	P10.5:ALT(3)	Master slave select output
QSPI3:SLSO(12)	to	P22.2:ALT(3)	Master slave select output
QSPI3:TX_INT	to	INT:qspi3.TX_INT	QSPI Transmit Service Request
QSPI3:RX_INT	to	INT:qspi3.RX_INT	QSPI Receive Service Request
QSPI3:ERR_INT	to	INT:qspi3.ERR_INT	QSPI Error Service Request
QSPI3:PT_INT	to	INT:qspi3.PT_INT	QSPI Phase Transition Service Request
QSPI3:U_INT	to	INT:qspi3.U_INT	QSPI User Defined Service Request
QSPI3:HC_INT	to	INT:qspi3.HC_INT	QSPI High Speed Capture Service Request

35.5 Revision History

Table 295 Revision History

Reference	Change to Previous Version	Comment
V3.0.20		
	No functional change.	

Micro Second Channel (MSC)

36 Micro Second Channel (MSC)

This chapter describes the Micro Second Channel (MSC) Module of the TC36x.

36.1 TC36x Specific IP Configuration

See features in family spec.

No product specific configuration for MSC

36.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

Table 296 Register Address Space - MSC

Module	Base Address	End Address	Note
MSC0	F0002600 _H	F00026FF _H	FPI slave interface

Register Overview Table

There are no product specific register for this module.

36.3 TC36x Specific Registers

There are no product specific register for this module.

36.4 Connectivity

The tables below list all the connections of MSC instances.

Table 297 Connections of MSC0

Interface Signals	connects		Description
MSC0:EMGSTOPMSC	from	SCU:scu_emgstop	Emergency stop signal from SCU
MSC0:EN(0)	to	P10.2:ALT(4)	Chip Select
		P10.3:ALT(4)	
		P10.4:ALT(5)	
		P11.11:ALT(5)	
		P14.10:ALT(3)	
		P15.5:ALT(5)	
MSC0:EN(1)	to	P10.1:ALT(4)	Chip Select
		P11.2:ALT(5)	
		P13.0:ALT(4)	
		P14.9:ALT(3)	
		P15.3:ALT(5)	
MSC0:FCLN	to	P13.0:ALT(5)	Shift-clock inverted part of the differential signal

Micro Second Channel (MSC)

Table 297 Connections of MSC0 (cont'd)

Interface Signals	connects		Description
MSC0:FCLP	to	SCU:E_REQ0(3)	Shift-clock direct part of the differential signal
		P11.6:ALT(5)	
		P13.1:ALT(5)	
		P13.2:ALT(4)	
MSC0:INJ0	from	P00.0:IN	Injection signal from port
MSC0:INJ1	from	P10.5:IN	Injection signal from port
MSC0:SDI(0)	from	P11.10:IN	Upstream asynchronous input signal
MSC0:SDI(1)	from	P10.2:IN	Upstream asynchronous input signal
MSC0:SDI(2)	from	P14.3:IN	Upstream asynchronous input signal
MSC0:SDI(3)	from	P11.3:IN	Upstream asynchronous input signal
MSC0:SON	to	P13.2:ALT(5)	Data output - inverted part of the differential signal
MSC0:SOP	to	P11.9:ALT(5)	Data output - direct part of the differential signal
		P13.3:ALT(5)	
MSC0:ALTINL(15:0)	from	GTM:MSC0.ALTINL(15:0)	GTM timer output vector - low part
MSC0:ALTINLEXT(15:0)	from	GTM:MSC0.ALTINLEXT(15:0)	GTM timer output vector - low extension part
MSC0:ALTINH(15:0)	from	GTM:MSC0.ALTINH(15:0)	GTM timer output vector - high part
MSC0:ALTINHEXT(15:0)	from	GTM:MSC0.ALTINHEXT(15:0)	GTM timer output vector - high extension part
MSC0:SR0_INT	to	INT:misc0.SR0_INT	MSC Service Request 0
MSC0:SR1_INT	to	INT:misc0.SR1_INT	MSC Service Request 1
MSC0:SR2_INT	to	INT:misc0.SR2_INT	MSC Service Request 2
MSC0:SR3_INT	to	INT:misc0.SR3_INT	MSC Service Request 3
MSC0:SR4_INT	to	INT:misc0.SR4_INT	MSC Service Request 4

36.5 Revision History

Table 298 Revision History

Reference	Change to Previous Version	Comment
V5.0.10		
Page 1	Connections table update, no functional change.	
Page 2	Clean up revision history.	

Single Edge Nibble Transmission (SENT)**37 Single Edge Nibble Transmission (SENT)**

This document describes the SENT Interface specific appendix for the product TC36x.

37.1 TC36x Specific IP Configuration

See features in family spec.

Table 299 TC36x specific configuration of SENT

Parameter	SENT
Number of SENT channels for this device	10

Single Edge Nibble Transmission (SENT)

37.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

Table 300 Register Address Space - SENT

Module	Base Address	End Address	Note
SENT	F0003000 _H	F0003AFF _H	FPI slave interface

Register Overview Table

There are no product specific register for this module.

37.3 TC36x Specific Registers

There are no product specific register for this module.

37.4 Connectivity

This section describes the connectivity of the SENT module.

37.4.1 Interrupt and DMA Controller Service Requests

The trigger outputs of the SENT module are connected via the Interrupt router. The request lines are connected as shown in [Connections of SENT](#).

37.4.2 Trigger Inputs

The module has 8 Sent Channels and the same number of trigger inputs but not more than $n+1 = 16$. They can be randomly chosen by programming IOCRx.ETS. The trigger inputs (TRIG[n:0]) of the SENT module are connected to the GTM as shown in [Connections of SENT](#).

37.4.3 Connections of SENT

The tables below list all the connections of SENT instances.

Table 301 Connections of SENT

Interface Signals	connects		Description
SENT:SENT0A	from	P40.0:IN	Receive input channel 0
SENT:SENT1A	from	P40.1:IN	Receive input channel 1
SENT:SENT2A	from	P40.2:IN	Receive input channel 2
SENT:SENT3A	from	P40.3:IN	Receive input channel 3
SENT:SENT4A	from	P40.4:IN	Receive input channel 4
SENT:SENT5A	from	P40.5:IN	Receive input channel 5
SENT:SENT6A	from	P40.6:IN	Receive input channel 6
SENT:SENT7A	from	P40.7:IN	Receive input channel 7
SENT:SENT8A	from	P40.8:IN	Receive input channel 8
SENT:SENT9A	from	P40.9:IN	Receive input channel 9

Single Edge Nibble Transmission (SENT)
Table 301 Connections of SENT (cont'd)

Interface Signals	connects		Description
SENT:SENT0B	from	P00.1:IN	Receive input channel 0
SENT:SENT1B	from	P00.2:IN	Receive input channel 1
SENT:SENT2B	from	P00.3:IN	Receive input channel 2
SENT:SENT3B	from	P00.4:IN	Receive input channel 3
SENT:SENT4B	from	P00.5:IN	Receive input channel 4
SENT:SENT5B	from	P00.6:IN	Receive input channel 5
SENT:SENT6B	from	P00.7:IN	Receive input channel 6
SENT:SENT7B	from	P00.8:IN	Receive input channel 7
SENT:SENT8B	from	P00.9:IN	Receive input channel 8
SENT:SENT9B	from	P00.10:IN	Receive input channel 9
SENT:SENT0C	from	P02.8:IN	Receive input channel 0
SENT:SENT1C	from	P02.7:IN	Receive input channel 1
SENT:SENT2C	from	P02.6:IN	Receive input channel 2
SENT:SENT3C	from	P02.5:IN	Receive input channel 3
SENT:SENT4C	from	P33.6:IN	Receive input channel 4
SENT:SENT5C	from	P33.5:IN	Receive input channel 5
SENT:SENT6C	from	P33.4:IN	Receive input channel 6
SENT:SENT7C	from	P33.3:IN	Receive input channel 7
SENT:SENT8C	from	P33.2:IN	Receive input channel 8
SENT:SENT9C	from	P33.1:IN	Receive input channel 9
SENT:SPC(0)	to	P00.1:ALT(6)	Transmit output
SENT:SPC(1)	to	P02.7:ALT(6)	Transmit output
SENT:SPC(2)	to	P00.3:ALT(6)	Transmit output
SENT:SPC(3)	to	P00.4:ALT(6)	Transmit output
SENT:SPC(4)	to	P00.5:ALT(6)	Transmit output
SENT:SPC(5)	to	P00.6:ALT(6)	Transmit output
SENT:SPC(6)	to	P00.7:ALT(6)	Transmit output
SENT:SPC(7)	to	P00.8:ALT(6)	Transmit output
SENT:SPC(8)	to	P00.9:ALT(6)	Transmit output
SENT:SPC(9)	to	P00.10:ALT(6)	Transmit output
SENT:TRIG(15:0)	from	GTM:SENT.TRIG(15:0)	GTM timer output vector
SENT:TRIGO(9:0)	to	INT:sent.TRIGO(9:0)	SENT TRIGO=m Service Request

Single Edge Nibble Transmission (SENT)**37.5 Revision History****Table 302 Revision History**

Reference	Change to Previous Version	Comment
V2.1.9		
	Initial version for TC36X.	
V2.1.10		
Page 1	Second sentence changed to internal audience only due to customer confusion. No functional change.	
Page 2	Minor notation update in connection table, no functional change.	

CAN Interface (MCMCAN)

38 CAN Interface (MCMCAN)

This section describes the MCMCAN Interface specific appendix for the product TC36x.

38.1 TC36x Specific IP Configuration

Table 303 TC36x specific configuration of CAN

Parameter	CAN0	CAN1
Node size in byte	1024	1024
Number of CAN Nodes	4	4
Number of TTCAN Nodes	1	
RAM size in byte	32768	16384
Maximum Number of Standard ID Filter Messages per node	128	128
Maximum Number of Extended ID Filter Messages per node	64	64
Maximum Number of RxFIFO structures per node	2	2
Maximum Number of Messages in a Rx buffer per node	64	64
Maximum Number of Tx Event Messages per node	32	32
Maximum Number of Tx Messages in a Tx Buffer per node	32	32
Maximum Number of Trigger Messages per node	64	

CAN Interface (MCMCAN)

38.2 TC36x Specific Register Set

Register Address Space Table

Table 304 Register Address Space - CAN

Module	Base Address	End Address	Note
CAN0	F020000 _H	F0208FFF _H	Bus Interface
CAN1	F0210000 _H	F0218FFF _H	Bus Interface

Register Overview Table

Table 305 Register Overview - CAN (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
CAN0_RAM	Embedded SRAM for messages (008000 _H Byte)	000000 _H	
CAN1_RAM	Embedded SRAM for messages (004000 _H Byte)	000000 _H	
CAN0_CLC	CAN Clock Control Register	008000 _H	See Family Spec
CAN1_CLC	CAN Clock Control Register	008000 _H	See Family Spec
CAN0_ID	Module Identification Register	008008 _H	See Family Spec
CAN1_ID	Module Identification Register	008008 _H	See Family Spec
CAN0_MCR	Module Control Register	008030 _H	See Family Spec
CAN1_MCR	Module Control Register	008030 _H	14
CAN0_BUFADR	Buffer receive address and transmit address	008034 _H	See Family Spec
CAN0_MECR	Measure Control Register	008040 _H	See Family Spec
CAN0_MESTAT	Measure Status Register	008044 _H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_ACCENCTR0	Access Enable Register Control 0	0080DC _H	See Family Spec
CAN1_ACCENCTR0	Access Enable Register Control 0	0080DC _H	See Family Spec
CAN0_OCS	OCDS Control and Status	0080E8 _H	See Family Spec
CAN1_OCS	OCDS Control and Status	0080E8 _H	See Family Spec
CAN0_KRSTCLR	Kernel Reset Status Clear Register	0080EC _H	See Family Spec
CAN1_KRSTCLR	Kernel Reset Status Clear Register	0080EC _H	See Family Spec
CAN0_KRST1	Kernel Reset Register 1	0080F0 _H	See Family Spec
CAN1_KRST1	Kernel Reset Register 1	0080F0 _H	See Family Spec
CAN0_KRST0	Kernel Reset Register 0	0080F4 _H	See Family Spec
CAN1_KRST0	Kernel Reset Register 0	0080F4 _H	See Family Spec
CAN0_ACCEN0	Access Enable Register 0	0080FC _H	See Family Spec
CAN1_ACCEN0	Access Enable Register 0	0080FC _H	See Family Spec
CAN0_ACCENNODEi0 (i=0-3)	Access Enable Register CAN Node i 0	008100 _H +i*400 H	See Family Spec
CAN1_ACCENNODEi0 (i=0-3)	Access Enable Register CAN Node i 0	008100 _H +i*400 H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_STARTADRi (i=0-3)	Start Address Node i	008108 _H +i*400 H	See Family Spec
CAN1_STARTADRi (i=0-3)	Start Address Node i	008108 _H +i*400 H	See Family Spec
CAN0_ENDADRi (i=0-3)	End Address Node i	00810C _H +i*40 0 _H	See Family Spec
CAN1_ENDADRi (i=0-3)	End Address Node i	00810C _H +i*40 0 _H	See Family Spec
CAN0_ISREGi (i=0-3)	Interrupt Signalling Register i	008110 _H +i*400 H	See Family Spec
CAN1_ISREGi (i=0-3)	Interrupt Signalling Register i	008110 _H +i*400 H	See Family Spec
CAN0_GRINT1i (i=0-3)	Interrupt routing for Groups 1 i	008114 _H +i*400 H	See Family Spec
CAN1_GRINT1i (i=0-3)	Interrupt routing for Groups 1 i	008114 _H +i*400 H	See Family Spec
CAN0_GRINT2i (i=0-3)	Interrupt routing for Groups 2 i	008118 _H +i*400 H	See Family Spec
CAN1_GRINT2i (i=0-3)	Interrupt routing for Groups 2 i	008118 _H +i*400 H	See Family Spec
CAN0_NTCCRi (i=0-3)	Node i Timer Clock Control Register	008120 _H +i*400 H	See Family Spec
CAN1_NTCCRi (i=0-3)	Node i Timer Clock Control Register	008120 _H +i*400 H	See Family Spec
CAN0_NTATTRi (i=0-3)	Node i Timer A Transmit Trigger Register	008124 _H +i*400 H	See Family Spec
CAN1_NTATTRi (i=0-3)	Node i Timer A Transmit Trigger Register	008124 _H +i*400 H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_NTBTRi (i=0-3)	Node i Timer B Transmit Trigger Register	008128 _H +i*400 H	See Family Spec
CAN1_NTBTRi (i=0-3)	Node i Timer B Transmit Trigger Register	008128 _H +i*400 H	See Family Spec
CAN0_NTCTTRi (i=0-3)	Node i Timer C Transmit Trigger Register	00812C _H +i*40 0 _H	See Family Spec
CAN1_NTCTTRi (i=0-3)	Node i Timer C Transmit Trigger Register	00812C _H +i*40 0 _H	See Family Spec
CAN0_NTRTRi (i=0-3)	Node i Timer Receive Timeout Register	008130 _H +i*400 H	See Family Spec
CAN1_NTRTRi (i=0-3)	Node i Timer Receive Timeout Register	008130 _H +i*400 H	See Family Spec
CAN0_NPCRi (i=0-3)	Node i Port Control Register	008140 _H +i*400 H	See Family Spec
CAN1_NPCRi (i=0-3)	Node i Port Control Register	008140 _H +i*400 H	See Family Spec
CAN0_TTCRi (i=0)	Time Trigger Control Register	0081F0 _H	See Family Spec
CAN0_CRELi (i=0-3)	Core Release Register i	008200 _H +i*400 H	See Family Spec
CAN1_CRELi (i=0-3)	Core Release Register i	008200 _H +i*400 H	See Family Spec
CAN0_ENDNi (i=0-3)	Endian Register i	008204 _H +i*400 H	See Family Spec
CAN1_ENDNi (i=0-3)	Endian Register i	008204 _H +i*400 H	See Family Spec
CAN0_DBTPi (i=0-3)	Data Bit Timing & Prescaler Register i	00820C _H +i*40 0 _H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN1_DBTPi (i=0-3)	Data Bit Timing & Prescaler Register i	00820C _H +i*40 0 _H	See Family Spec
CAN0_TESTi (i=0-3)	Test Register i	008210 _H +i*400	See Family Spec
CAN1_TESTi (i=0-3)	Test Register i	008210 _H +i*400	See Family Spec
CAN0_RWDi (i=0-3)	RAM Watchdog i	008214 _H +i*400	See Family Spec
CAN1_RWDi (i=0-3)	RAM Watchdog i	008214 _H +i*400	See Family Spec
CAN0_CCCRi (i=0-3)	CC Control Register i	008218 _H +i*400	See Family Spec
CAN1_CCCRi (i=0-3)	CC Control Register i	008218 _H +i*400	See Family Spec
CAN0_NBTPi (i=0-3)	Nominal Bit Timing & Prescaler Register i	00821C _H +i*40 0 _H	See Family Spec
CAN1_NBTPi (i=0-3)	Nominal Bit Timing & Prescaler Register i	00821C _H +i*40 0 _H	See Family Spec
CAN0_TSCCi (i=0-3)	Timestamp Counter Configuration i	008220 _H +i*400	See Family Spec
CAN1_TSCCi (i=0-3)	Timestamp Counter Configuration i	008220 _H +i*400	See Family Spec
CAN0_TSCVi (i=0-3)	Timestamp Counter Value i	008224 _H +i*400	See Family Spec
CAN1_TSCVi (i=0-3)	Timestamp Counter Value i	008224 _H +i*400	See Family Spec
CAN0_TOCCi (i=0-3)	Timeout Counter Configuration i	008228 _H +i*400	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN1_TOCCi (i=0-3)	Timeout Counter Configuration i	008228 _H +i*40 H	See Family Spec
CAN0_TOCVi (i=0-3)	Timeout Counter Value i	00822C _H +i*40 0 _H	See Family Spec
CAN1_TOCVi (i=0-3)	Timeout Counter Value i	00822C _H +i*40 0 _H	See Family Spec
CAN0_ECRi (i=0-3)	Error Counter Register i	008240 _H +i*40 H	See Family Spec
CAN1_ECRi (i=0-3)	Error Counter Register i	008240 _H +i*40 H	See Family Spec
CAN0_PSRi (i=0-3)	Protocol Status Register i	008244 _H +i*40 H	See Family Spec
CAN1_PSRi (i=0-3)	Protocol Status Register i	008244 _H +i*40 H	See Family Spec
CAN0_TDCRi (i=0-3)	Transmitter Delay Compensation Register i	008248 _H +i*40 H	See Family Spec
CAN1_TDCRi (i=0-3)	Transmitter Delay Compensation Register i	008248 _H +i*40 H	See Family Spec
CAN0_IRi (i=0-3)	Interrupt Register i	008250 _H +i*40 H	See Family Spec
CAN1_IRi (i=0-3)	Interrupt Register i	008250 _H +i*40 H	See Family Spec
CAN0_IEi (i=0-3)	Interrupt Enable i	008254 _H +i*40 H	See Family Spec
CAN1_IEi (i=0-3)	Interrupt Enable i	008254 _H +i*40 H	See Family Spec
CAN0_GFCi (i=0-3)	Global Filter Configuration i	008280 _H +i*40 H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN1_GFCi (i=0-3)	Global Filter Configuration i	008280 _H +i*400 H	See Family Spec
CAN0_SIDFCi (i=0-3)	Standard ID Filter Configuration i	008284 _H +i*400 H	See Family Spec
CAN1_SIDFCi (i=0-3)	Standard ID Filter Configuration i	008284 _H +i*400 H	See Family Spec
CAN0_XIDFCi (i=0-3)	Extended ID Filter Configuration i	008288 _H +i*400 H	See Family Spec
CAN1_XIDFCi (i=0-3)	Extended ID Filter Configuration i	008288 _H +i*400 H	See Family Spec
CAN0_XIDAMi (i=0-3)	Extended ID AND Mask i	008290 _H +i*400 H	See Family Spec
CAN1_XIDAMi (i=0-3)	Extended ID AND Mask i	008290 _H +i*400 H	See Family Spec
CAN0_HPMSi (i=0-3)	High Priority Message Status i	008294 _H +i*400 H	See Family Spec
CAN1_HPMSi (i=0-3)	High Priority Message Status i	008294 _H +i*400 H	See Family Spec
CAN0_NDAT1i (i=0-3)	New Data 1 i	008298 _H +i*400 H	See Family Spec
CAN1_NDAT1i (i=0-3)	New Data 1 i	008298 _H +i*400 H	See Family Spec
CAN0_NDAT2i (i=0-3)	New Data 2 i	00829C _H +i*40 0 _H	See Family Spec
CAN1_NDAT2i (i=0-3)	New Data 2 i	00829C _H +i*40 0 _H	See Family Spec
CAN0_RXF0Ci (i=0-3)	Rx FIFO 0 Configuration i	0082A0 _H +i*40 0 _H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN1_RXF0Ci (i=0-3)	Rx FIFO 0 Configuration i	0082A0 _H +i*40 0 _H	See Family Spec
CAN0_RXF0Si (i=0-3)	Rx FIFO 0 Status i	0082A4 _H +i*40 0 _H	See Family Spec
CAN1_RXF0Si (i=0-3)	Rx FIFO 0 Status i	0082A4 _H +i*40 0 _H	See Family Spec
CAN0_RXF0Ai (i=0-3)	Rx FIFO 0 Acknowledge i	0082A8 _H +i*40 0 _H	See Family Spec
CAN1_RXF0Ai (i=0-3)	Rx FIFO 0 Acknowledge i	0082A8 _H +i*40 0 _H	See Family Spec
CAN0_RXBCi (i=0-3)	Rx Buffer Configuration i	0082AC _H +i*40 0 _H	See Family Spec
CAN1_RXBCi (i=0-3)	Rx Buffer Configuration i	0082AC _H +i*40 0 _H	See Family Spec
CAN0_RXF1Ci (i=0-3)	Rx FIFO 1 Configuration i	0082B0 _H +i*40 0 _H	See Family Spec
CAN1_RXF1Ci (i=0-3)	Rx FIFO 1 Configuration i	0082B0 _H +i*40 0 _H	See Family Spec
CAN0_RXF1Si (i=0-3)	Rx FIFO 1 Status i	0082B4 _H +i*40 0 _H	See Family Spec
CAN1_RXF1Si (i=0-3)	Rx FIFO 1 Status i	0082B4 _H +i*40 0 _H	See Family Spec
CAN0_RXF1Ai (i=0-3)	Rx FIFO 1 Acknowledge i	0082B8 _H +i*40 0 _H	See Family Spec
CAN1_RXF1Ai (i=0-3)	Rx FIFO 1 Acknowledge i	0082B8 _H +i*40 0 _H	See Family Spec
CAN0_RXESCi (i=0-3)	Rx Buffer/FIFO Element Size Configuration i	0082BC _H +i*40 0 _H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN1_RXESCI (i=0-3)	Rx Buffer/FIFO Element Size Configuration i	0082BC _H +i*40 0 _H	See Family Spec
CAN0_TXBCI (i=0-3)	Tx Buffer Configuration i	0082C0 _H +i*40 0 _H	See Family Spec
CAN1_TXBCI (i=0-3)	Tx Buffer Configuration i	0082C0 _H +i*40 0 _H	See Family Spec
CAN0_TXFQSI (i=0-3)	Tx FIFO/Queue Status i	0082C4 _H +i*40 0 _H	See Family Spec
CAN1_TXFQSI (i=0-3)	Tx FIFO/Queue Status i	0082C4 _H +i*40 0 _H	See Family Spec
CAN0_TXESCI (i=0-3)	Tx Buffer Element Size Configuration i	0082C8 _H +i*40 0 _H	See Family Spec
CAN1_TXESCI (i=0-3)	Tx Buffer Element Size Configuration i	0082C8 _H +i*40 0 _H	See Family Spec
CAN0_TXBRPI (i=0-3)	Tx Buffer Request Pending i	0082CC _H +i*40 0 _H	See Family Spec
CAN1_TXBRPI (i=0-3)	Tx Buffer Request Pending i	0082CC _H +i*40 0 _H	See Family Spec
CAN0_TXBARI (i=0-3)	Tx Buffer Add Request i	0082D0 _H +i*40 0 _H	See Family Spec
CAN1_TXBARI (i=0-3)	Tx Buffer Add Request i	0082D0 _H +i*40 0 _H	See Family Spec
CAN0_TXBCRI (i=0-3)	Tx Buffer Cancellation Request i	0082D4 _H +i*40 0 _H	See Family Spec
CAN1_TXBCRI (i=0-3)	Tx Buffer Cancellation Request i	0082D4 _H +i*40 0 _H	See Family Spec
CAN0_TXBTOI (i=0-3)	Tx Buffer Transmission Occurred i	0082D8 _H +i*40 0 _H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN1_TXBTOi (i=0-3)	Tx Buffer Transmission Occurred i	0082D8 _H +i*40 0 _H	See Family Spec
CAN0_TXBCFi (i=0-3)	Tx Buffer Cancellation Finished i	0082DC _H +i*40 0 _H	See Family Spec
CAN1_TXBCFi (i=0-3)	Tx Buffer Cancellation Finished i	0082DC _H +i*40 0 _H	See Family Spec
CAN0_TXBTIEi (i=0-3)	Tx Buffer Transmission Interrupt Enable i	0082E0 _H +i*40 0 _H	See Family Spec
CAN1_TXBTIEi (i=0-3)	Tx Buffer Transmission Interrupt Enable i	0082E0 _H +i*40 0 _H	See Family Spec
CAN0_TXBCIEi (i=0-3)	Tx Buffer Cancellation Finished Interrupt Enable i	0082E4 _H +i*40 0 _H	See Family Spec
CAN1_TXBCIEi (i=0-3)	Tx Buffer Cancellation Finished Interrupt Enable i	0082E4 _H +i*40 0 _H	See Family Spec
CAN0_TXEFCi (i=0-3)	Tx Event FIFO Configuration i	0082F0 _H +i*400 H	See Family Spec
CAN1_TXEFCi (i=0-3)	Tx Event FIFO Configuration i	0082F0 _H +i*400 H	See Family Spec
CAN0_TXEFSi (i=0-3)	Tx Event FIFO Status i	0082F4 _H +i*400 H	See Family Spec
CAN1_TXEFSi (i=0-3)	Tx Event FIFO Status i	0082F4 _H +i*400 H	See Family Spec
CAN0_TXEFAi (i=0-3)	Tx Event FIFO Acknowledge i	0082F8 _H +i*400 H	See Family Spec
CAN1_TXEFAi (i=0-3)	Tx Event FIFO Acknowledge i	0082F8 _H +i*400 H	See Family Spec
CAN0_TTTMCi (i=0)	TT Trigger Memory Configuration i	008300 _H	See Family Spec

CAN Interface (MCMCAN)

Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_TTRMCi (i=0)	TT Reference Message Configuration i	008304 _H	See Family Spec
CAN0_TTOCFi (i=0)	TT Operation Configuration i	008308 _H	See Family Spec
CAN0_TTMLMi (i=0)	TT Matrix Limits i	00830C _H	See Family Spec
CAN0_TURCFi (i=0)	TUR Configuration i	008310 _H	See Family Spec
CAN0_TTOCNI (i=0)	TT Operation Control i	008314 _H	See Family Spec
CAN0_TTGTPi (i=0)	TT Global Time Preset i	008318 _H	See Family Spec
CAN0_TTTMKi (i=0)	TT Time Mark i	00831C _H	See Family Spec
CAN0_TTIRi (i=0)	TT Interrupt Register i	008320 _H	See Family Spec
CAN0_TTIEi (i=0)	TT Interrupt Enable i	008324 _H	See Family Spec
CAN0_TTOSTi (i=0)	TT Operation Status i	00832C _H	See Family Spec
CAN0_TURNAi (i=0)	TUR Numerator Actual i	008330 _H	See Family Spec
CAN0_TTLGTi (i=0)	TT Local & Global Time i	008334 _H	See Family Spec
CAN0_TTCTCi (i=0)	TT Cycle Time & Count i	008338 _H	See Family Spec

CAN Interface (MCMCAN)**Table 305 Register Overview - CAN (ascending Offset Address) (cont'd)**

Short Name	Long Name	Offset Address	Page Number
CAN0_TTCPTi (i=0)	TT Capture Time i	00833C _H	See Family Spec
CAN0_TTCSMi (i=0)	TT Cycle Sync Mark i	008340 _H	See Family Spec

CAN Interface (MCMCAN)

38.3 TC36x Specific Registers

38.3.1 Bus Interface

Module Control Register

The Module Control Register MCR contains basic settings that determine the operation of the MCMCAN module. The write access to the lowest byte of the MCR register becomes only valid, if and only if, MCR.CCCE and MCR.CI are already set during write access. To switch the clocks on or off, the bits of MCR.CCCE and MCR.CI have to be reset afterwards. Before this sequence hasn't taken place, no write access to the corresponding nodes, can be done.

Note: If the baud rate logic is supplied from an unstable clock source, or no clock at all, the CAN functionality is not guaranteed.

To be able to change the clock settings the following programming sequence needs to be met:

```
uwTemp = CANn_MCR.U;
uwTemp |= (0xC0000000 | CLKSELx);
CANn_MCR.U = uwTemp;
uwTemp &= ~0xC0000000;
CANn_MCR.U = uwTemp;
```

The clock settings for CAN nodes becomes active.

To be able to start the RAM initialization, the following programming sequence need to be met:

```
CANn_MCR |= 0xC0000000;
Wait until CANn_MCR.RBUSY is 0b
Set CANn_MCR.RINIT to 0b
Set CANn_MCR.RINIT to 1b
Dummy read CANn_MCR
Wait until CANn_MCR.RBUSY is 0b
Set CANn_MCR.RINIT to 0b
CANn_MCR &= ~0xC0000000;
RAM initialization is finished
```

CAN1_MCR

Module Control Register

(008030_H)

Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CCCE	CI	RINIT	RBUSY	0				0							
rw	rw	rw	rh	r				r							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								CLKSEL3	CLKSEL2	CLKSEL1	CLKSELO				
r								rw	rw	rw	rw				

CAN Interface (MCMCAN)

Field	Bits	Type	Description
CLKSEL0	1:0	rw	Clock Select 0 This bitfield is MCR.CI and MCR.CCCE protected. 00 _B No clock supplied 01 _B The asynchronous clock source is switched on 10 _B The synchronous clock source is switched on 11 _B Both clock sources are switched on
CLKSEL1	3:2	rw	Clock Select 1 This bitfield is MCR.CI and MCR.CCCE protected. 00 _B No clock supplied 01 _B The asynchronous clock source is switched on 10 _B The synchronous clock source is switched on 11 _B Both clock sources are switched on
CLKSEL2	5:4	rw	Clock Select 2 This bitfield is MCR.CI and MCR.CCCE protected. 00 _B No clock supplied 01 _B The asynchronous clock source is switched on 10 _B The synchronous clock source is switched on 11 _B Both clock sources are switched on
CLKSEL3	7:6	rw	Clock Select 3 This bitfield is MCR.CI and MCR.CCCE protected. 00 _B No clock supplied 01 _B The asynchronous clock source is switched on 10 _B The synchronous clock source is switched on 11 _B Both clock sources are switched on
RBUSY	28	rh	RAM BUSY This bit shows that the RAM Initialization is running. This bit is set back to 0b by hardware when the RAM initialization is completed.
RINIT	29	rw	RAM Init This bit is MCR.CI and MCR.CCCE protected. This bit starts the initialization of the RAM block to all 0x0. The RAM initialization is started only when this bit is changed from 0b to 1b and also RBUSY is 0b.
CI	30	rw	Change Init Needs to be set to enable and disable clocks. 0 _B Change Init disabled 1 _B Change Init enabled (takes effect with CCCE:=1)
CCCE	31	rw	Clock and RAM Change Enable Needs to be set to enable and disable the clocks. 0 _B Clock and RAM Change disabled 1 _B Clock and RAM Change enabled (takes effect with CI:=1)
0	23:8, 27:24	r	Reserved Shall read 0; shall be written with 0.

38.4 Connectivity

CAN Interface (MCMCAN)

Table 306 Connections of CAN0

Interface Signals	connects		Description
CAN0:DSTDBG	from	DMU:SCU_ENTERED_DE ST_DBG	Destructive Debug entered
CAN0:DXSCLK	to	TCU:dxs_clk	DXS Clock, DAP module clock
CAN0:ECTT(1)	from	P02.4:IN	External CAN time trigger input
CAN0:ECTT(2)	from	P02.5:IN	External CAN time trigger input
CAN0:ECTT(4:3)	from	SCU:E_IOUT(3:2)	External CAN time trigger input
CAN0:ECTT(5)	from	ERAY0:TINT0	External CAN time trigger input
CAN0:ECTT(6)	from	ERAY0:TINT1	External CAN time trigger input
CAN0:INT(5:0)	to	HSM:EXT_INT(18:13)	CAN interrupt request
CAN0:INT(12)	to	GTM:TIM0_IN1(13)	CAN interrupt request
		GTM:TIM1_IN1(13)	
		GTM:TIM2_IN1(13)	
		CCU61:CC61IND	
CAN0:INT(13)	to	GTM:TIM0_IN2(13)	CAN interrupt request
		GTM:TIM1_IN2(13)	
		GTM:TIM2_IN2(13)	
CAN0:INT(14)	to	GTM:TIM0_IN3(13)	CAN interrupt request
		GTM:TIM1_IN3(13)	
		GTM:TIM2_IN3(13)	
CAN0:INT(15)	to	GTM:TIM0_IN4(13)	CAN interrupt request
		GTM:TIM1_IN4(13)	
		GTM:TIM2_IN4(13)	
		CCU61:T13HRE	
CAN0:STM0_SR0_INT	from	STM0:SR0_INT	System Timer Service Request 0
CAN0:STM0_SR1_INT	from	STM0:SR1_INT	System Timer Service Request 1
CAN0:STM1_SR0_INT	from	STM1:SR0_INT	System Timer Service Request 0
CAN0:STM1_SR1_INT	from	STM1:SR1_INT	System Timer Service Request 1
CAN0:TTCPT_TRIG(4)	from	SCU:E_IOUT(4)	Capture time trigger input
CAN0:TRIG(3:0)	from	GTM:CAN0.TRIG(3:0)	GTM timer output vector
CAN0:INT(15:0)	to	INT:mcmcan0.INT(15:0)	CAN Service Request

Table 307 Connections of CAN00

Interface Signals	connects		Description
CAN00:RXDA	from	P02.1:IN	CAN receive input node 0
CAN00:RXDB	from	P20.7:IN	CAN receive input node 0
CAN00:RXDC	from	P12.0:IN	CAN receive input node 0
CAN00:RXDD	from	P33.12:IN	CAN receive input node 0

CAN Interface (MCMCAN)

Table 307 Connections of CAN00 (cont'd)

Interface Signals	connects		Description
CAN00:RXDE	from	P33.7:IN	CAN receive input node 0
CAN00:TXD	to	IOM:MON2(5)	CAN transmit output node 0
		IOM:REF2(5)	
		P02.0:ALT(5)	
		P12.1:ALT(5)	
		P20.8:ALT(5)	
		P33.8:ALT(5)	
		P33.13:ALT(5)	

Table 308 Connections of CAN01

Interface Signals	connects		Description
CAN01:RXDA	from	P15.3:IN	CAN receive input node 1
CAN01:RXDB	from	P14.1:IN	CAN receive input node 1
CAN01:RXDD	from	P33.10:IN	CAN receive input node 1
CAN01:TXD	to	IOM:MON2(6)	CAN transmit output node 1
		IOM:REF2(6)	
		P14.0:ALT(5)	
		P15.2:ALT(5)	
		P33.9:ALT(5)	

Table 309 Connections of CAN1

Interface Signals	connects		Description
CAN1:DSTDBG	from	DMU:SCU_ENTERED_DE ST_DBG	Destructive Debug entered
CAN1:STM0_SR0_INT	from	STM0:SR0_INT	System Timer Service Request 0
CAN1:STM0_SR1_INT	from	STM0:SR1_INT	System Timer Service Request 1
CAN1:STM1_SR0_INT	from	STM1:SR0_INT	System Timer Service Request 0
CAN1:STM1_SR1_INT	from	STM1:SR1_INT	System Timer Service Request 1
CAN1:TRIG(3:0)	from	GTM:CAN1.TRIG(3:0)	GTM timer output vector
CAN1:INT(15:0)	to	INT:mcmcan1.INT(15:0)	CAN Service Request

Table 310 Connections of CAN02

Interface Signals	connects		Description
CAN02:RXDA	from	P15.1:IN	CAN receive input node 2
CAN02:RXDB	from	P02.3:IN	CAN receive input node 2
CAN02:RXDD	from	P14.8:IN	CAN receive input node 2
CAN02:RXDE	from	P10.2:IN	CAN receive input node 2

CAN Interface (MCMCAN)

Table 310 Connections of CAN02 (cont'd)

Interface Signals	connects		Description
CAN02:TXD	to	IOM:MON2(7)	CAN transmit output node 2
		IOM:REF2(7)	
		P02.2:ALT(5)	
		P10.3:ALT(6)	
		P14.10:ALT(5)	
		P15.0:ALT(5)	

Table 311 Connections of CAN03

Interface Signals	connects		Description
CAN03:RXDA	from	P00.3:IN	CAN receive input node 3
CAN03:RXDB	from	P32.2:IN	CAN receive input node 3
CAN03:RXDC	from	P20.0:IN	CAN receive input node 3
CAN03:RXDD	from	P11.10:IN	CAN receive input node 3
CAN03:RXDE	from	P20.9:IN	CAN receive input node 3
CAN03:TXD	to	IOM:MON2(8)	CAN transmit output node 3
		IOM:REF2(8)	
		P00.2:ALT(5)	
		P11.12:ALT(5)	
		P20.3:ALT(5)	
		P20.10:ALT(5)	
		P32.3:ALT(5)	

Table 312 Connections of CAN10

Interface Signals	connects		Description
CAN10:RXDA	from	P00.1:IN	CAN receive input node 0
CAN10:RXDB	from	P14.7:IN	CAN receive input node 0
CAN10:RXDC	from	P23.0:IN	CAN receive input node 0
CAN10:RXDD	from	P13.1:IN	CAN receive input node 0
CAN10:TXD	to	P00.0:ALT(5)	CAN transmit output node 0
		P13.0:ALT(7)	
		P14.9:ALT(4)	
		P23.1:ALT(5)	

Table 313 Connections of CAN11

Interface Signals	connects		Description
CAN11:RXDA	from	P02.4:IN	CAN receive input node 1
CAN11:RXDB	from	P00.5:IN	CAN receive input node 1
CAN11:RXDD	from	P11.7:IN	CAN receive input node 1

CAN Interface (MCMCAN)

Table 313 Connections of CAN11 (cont'd)

Interface Signals	connects		Description
CAN11:TXD	to	P00.4:ALT(3)	CAN transmit output node 1
		P02.5:ALT(2)	
		P11.0:ALT(5)	

Table 314 Connections of CAN12

Interface Signals	connects		Description
CAN12:RXDA	from	P20.6:IN	CAN receive input node 2
CAN12:RXDB	from	P10.8:IN	CAN receive input node 2
CAN12:RXDC	from	P23.3:IN	CAN receive input node 2
CAN12:RXDD	from	P11.8:IN	CAN receive input node 2
CAN12:TXD	to	P10.7:ALT(6)	CAN transmit output node 2
		P11.1:ALT(5)	
		P20.7:ALT(5)	
		P23.2:ALT(5)	

Table 315 Connections of CAN13

Interface Signals	connects		Description
CAN13:RXDA	from	P14.7:IN	CAN receive input node 3
CAN13:RXDB	from	P33.5:IN	CAN receive input node 3
CAN13:RXDD	from	P11.13:IN	CAN receive input node 3
CAN13:TXD	to	P11.4:ALT(5)	CAN transmit output node 3
		P14.6:ALT(4)	
		P33.4:ALT(7)	

Note: For the connectivity of the MCMCAN module to the STM module, please refer to the User Manual, chapter MCMCAN User Interface under CAN Transmit Trigger Inputs section.

38.5 Revision History

Table 316 Revision History

Reference	Change to Previous Version	Comment
V1.19.8		
Page 1	Update of “specific configuration of CAN” table.	
Page 14	CAN_MCR register bit field “reserved” fixed.	
V1.19.9		
–	No changes in the TC36x appendix.	
V1.19.10		
Page 19	Added note at the end of connections tables.	
V1.19.11		

CAN Interface (MCMCAN)**Table 316 Revision History** (cont'd)

Reference	Change to Previous Version	Comment
–	No functional changes.	
V1.19.12		
Page 1	Update of “specific configuration of CAN” table.	
V1.19.13		
Page 14	Updated information on bit implementation in A-step.	

FlexRay™ Protocol Controller (E-Ray)

39 FlexRay™ Protocol Controller (E-Ray)

Text with reference to family spec.

39.1 TC36x Specific IP Configuration

No product specific configuration for ERAY

FlexRay™ Protocol Controller (E-Ray)

39.2 TC36x Specific Register Set

Register Address Space Table

Table 317 Register Address Space - ERAY

Module	Base Address	End Address	Note
ERAY0	F001C000 _H	F001CFFF _H	FPI slave interface

Register Overview Table

Table 318 Register Overview - ERAY (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
ERAY0_CLC	Clock Control Register	0000 _H	See Family Spec
ERAY0_CUST1	Busy and Input Buffer Control Register	0004 _H	See Family Spec
ERAY0_ID	Module Identification Register	0008 _H	See Family Spec
ERAY0_CUST3	Customer Interface Timeout Counter Register	000C _H	See Family Spec
ERAY0_TEST1	Test Register 1	0010 _H	See Family Spec
ERAY0_TEST2	Test Register 2	0014 _H	See Family Spec
ERAY0_LCK	Lock Register	001C _H	See Family Spec
ERAY0_EIR	Error Service Request Select Register	0020 _H	See Family Spec
ERAY0_SIR	Status Service Request Register	0024 _H	See Family Spec
ERAY0_EILS	Error Service Request Line Select	0028 _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_SILS	Status Service Request Line Select	002C _H	See Family Spec
ERAY0_EIES	Error Service Request Enable Set	0030 _H	See Family Spec
ERAY0_EIER	Error Service Request Enable Reset	0034 _H	See Family Spec
ERAY0_SIES	Status Service Request Enable Set	0038 _H	See Family Spec
ERAY0_SIER	Status Service Request Enable Reset	003C _H	See Family Spec
ERAY0_ILE	Service Request Line Enable	0040 _H	See Family Spec
ERAY0_T0C	Timer 0 Configuration	0044 _H	See Family Spec
ERAY0_T1C	Timer 1 Configuration	0048 _H	See Family Spec
ERAY0_STPW1	Stop Watch Register 1	004C _H	See Family Spec
ERAY0_STPW2	Stop Watch Register 2	0050 _H	See Family Spec
ERAY0_SUCC1	SUC Configuration Register 1	0080 _H	See Family Spec
ERAY0_SUCC2	SUC Configuration Register 2	0084 _H	See Family Spec
ERAY0_SUCC3	SUC Configuration Register 3	0088 _H	See Family Spec
ERAY0_NEMC	NEM Configuration Register	008C _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_PRTC1	PRT Configuration Register 1	0090 _H	See Family Spec
ERAY0_PRTC2	PRT Configuration Register 2	0094 _H	See Family Spec
ERAY0_MHDC	MHD Configuration Register	0098 _H	See Family Spec
ERAY0_GTUC01	GTU Configuration Register 1	00A0 _H	See Family Spec
ERAY0_GTUC02	GTU Configuration Register 2	00A4 _H	See Family Spec
ERAY0_GTUC03	GTU Configuration Register 3	00A8 _H	See Family Spec
ERAY0_GTUC04	GTU Configuration Register 4	00AC _H	See Family Spec
ERAY0_GTUC05	GTU Configuration Register 5	00B0 _H	See Family Spec
ERAY0_GTUC06	GTU Configuration Register 6	00B4 _H	See Family Spec
ERAY0_GTUC07	GTU Configuration Register 7	00B8 _H	See Family Spec
ERAY0_GTUC08	GTU Configuration Register 8	00BC _H	See Family Spec
ERAY0_GTUC09	GTU Configuration Register 9	00C0 _H	See Family Spec
ERAY0_GTUC10	GTU Configuration Register 10	00C4 _H	See Family Spec
ERAY0_GTUC11	GTU Configuration Register 11	00C8 _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_CCSV	Communication Controller Status Vector	0100 _H	See Family Spec
ERAY0_CCEV	Communication Controller Error Vector	0104 _H	See Family Spec
ERAY0_SCV	Slot Counter Value	0110 _H	See Family Spec
ERAY0_MTCCV	Macrotick and Cycle Counter Value	0114 _H	See Family Spec
ERAY0_RCV	Rate Correction Value	0118 _H	See Family Spec
ERAY0_OCV	Offset Correction Value	011C _H	See Family Spec
ERAY0_SFS	SYNC Frame Status	0120 _H	See Family Spec
ERAY0_SWNIT	Symbol Window and Network Idle Time Status	0124 _H	See Family Spec
ERAY0_ACS	Aggregated Channel Status	0128 _H	See Family Spec
ERAY0_ESIDn (n=01-15)	Even Sync ID Symbol Window n	0130 _H +(n-1)*4	See Family Spec
ERAY0_OSIDn (n=01-15)	Odd Sync ID Symbol Window n	0170 _H +(n-1)*4	See Family Spec
ERAY0_NMVx (x=1-3)	Network Management Vector x	01B0 _H +(x-1)*4	See Family Spec
ERAY0_MRC	Message RAM Configuration	0300 _H	See Family Spec
ERAY0_FRF	FIFO Rejection Filter	0304 _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_FRFM	FIFO Rejection Filter Mask	0308 _H	See Family Spec
ERAY0_FCL	FIFO Critical Level	030C _H	See Family Spec
ERAY0_MHDS	Message Handler Status	0310 _H	See Family Spec
ERAY0_LDTS	Last Dynamic Transmit Slot	0314 _H	See Family Spec
ERAY0_FSR	FIFO Status Register	0318 _H	See Family Spec
ERAY0_MHDF	Message Handler Constraints Flags	031C _H	See Family Spec
ERAY0_TXRQ1	Transmission Request Register 1	0320 _H	See Family Spec
ERAY0_TXRQ2	Transmission Request Register 2	0324 _H	See Family Spec
ERAY0_TXRQ3	Transmission Request Register 3	0328 _H	See Family Spec
ERAY0_TXRQ4	Transmission Request Register 4	032C _H	See Family Spec
ERAY0_NDAT1	New Data Register 1	0330 _H	See Family Spec
ERAY0_NDAT2	New Data Register 2	0334 _H	See Family Spec
ERAY0_NDAT3	New Data Register 3	0338 _H	See Family Spec
ERAY0_NDAT4	New Data Register 4	033C _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_MBSC1	Message Buffer Status Changed 1	0340 _H	See Family Spec
ERAY0_MBSC2	Message Buffer Status Changed 2	0344 _H	See Family Spec
ERAY0_MBSC3	Message Buffer Status Changed 3	0348 _H	See Family Spec
ERAY0_MBSC4	Message Buffer Status Changed 4	034C _H	See Family Spec
ERAY0_NDIC1	New Data Interrupt Control 1	03A8 _H	See Family Spec
ERAY0_NDIC2	New Data Interrupt Control 2	03AC _H	See Family Spec
ERAY0_NDIC3	New Data Interrupt Control 3	03B0 _H	See Family Spec
ERAY0_NDIC4	New Data Interrupt Control 4	03B4 _H	See Family Spec
ERAY0_MSIC1	Message Buffer Status Changed Interrupt Control 1	03B8 _H	See Family Spec
ERAY0_MSIC2	Message Buffer Status Changed Interrupt Control 2	03BC _H	See Family Spec
ERAY0_MSIC3	Message Buffer Status Changed Interrupt Control 3	03C0 _H	See Family Spec
ERAY0_MSIC4	Message Buffer Status Changed Interrupt Control 4	03C4 _H	See Family Spec
ERAY0_CREL	Core Release Register	03F0 _H	See Family Spec
ERAY0_ENDN	Endian Register	03F4 _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_WRDSn (n=01-64)	Write Data Section n	0400 _H +(n-1)*4	See Family Spec
ERAY0_WRHS1	Write Header Section 1	0500 _H	See Family Spec
ERAY0_WRHS2	Write Header Section 2	0504 _H	See Family Spec
ERAY0_WRHS3	Write Header Section 3	0508 _H	See Family Spec
ERAY0_IBCM	Input Buffer Command Mask	0510 _H	See Family Spec
ERAY0_IBCR	Input Buffer Command Request	0514 _H	See Family Spec
ERAY0_RDDSn (n=01-64)	Read Data Section n	0600 _H +(n-1)*4	See Family Spec
ERAY0_RDHS1	Read Header Section 1	0700 _H	See Family Spec
ERAY0_RDHS2	Read Header Section 2	0704 _H	See Family Spec
ERAY0_RDHS3	Read Header Section 3	0708 _H	See Family Spec
ERAY0_MBS	Message Buffer Status	070C _H	See Family Spec
ERAY0_OBCM	Output Buffer Command Mask	0710 _H	See Family Spec
ERAY0_OBCR	Output Buffer Command Request	0714 _H	See Family Spec
ERAY0_OTSS	OCDS Trigger Set Select	0870 _H	See Family Spec

FlexRay™ Protocol Controller (E-Ray)

Table 318 Register Overview - ERAY (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ERAY0_OCS	OCDS Control and Status	08E8 _H	See Family Spec
ERAY0_KRSTCLR	Kernel Reset Status Clear Register	08EC _H	See Family Spec
ERAY0_KRST1	Kernel Reset Register 1	08F0 _H	See Family Spec
ERAY0_KRST0	Kernel Reset Register 0	08F4 _H	See Family Spec
ERAY0_ACCEN0	Access Enable Register 0	08FC _H	See Family Spec

39.3 TC36x Specific Registers

No deviations from the Family Spec

39.4 Connectivity**Table 319 Connections of ERAY0**

Interface Signals	connects		Description
ERAY0:MT	to	CCU:eray_mt GTM:TIM0_IN7(13) GTM:TIM1_IN7(13) GTM:TIM2_IN7(13) SCU:E_REQ2(3)	Macrotick-clock from CC (synchronous to fpi clock)
ERAY0:RXDA0	from	P14.8:IN	Receive Channel A0
ERAY0:RXDA1	from	P11.9:IN	Receive Channel A1
ERAY0:RXDA2	from	P02.1:IN	Receive Channel A2
ERAY0:RXDA3	from	P14.1:IN	Receive Channel A3
ERAY0:RXDB0	from	P14.7:IN	Receive Channel B0
ERAY0:RXDB1	from	P11.10:IN	Receive Channel B1
ERAY0:RXDB2	from	P02.3:IN	Receive Channel B2
ERAY0:RXDB3	from	P14.1:IN	Receive Channel B3
ERAY0:STPWT(3:0)	from	SCU:E_PDOUT(3:0)	StoP Watch Trigger signal
ERAY0:TINT0	to	CAN0:ECTT(5)	Timer Interrupt 0 (high-active)
ERAY0:TINT1	to	CAN0:ECTT(6)	Timer Interrupt 1 (high-active)

FlexRay™ Protocol Controller (E-Ray)

Table 319 Connections of ERAY0 (cont'd)

Interface Signals	connects		Description
ERAY0:TXDA	to	P02.0:ALT(6)	Transmit Channel A
		P11.3:ALT(4)	
		P14.0:ALT(3)	
		P14.10:ALT(6)	
ERAY0:TXDB	to	P02.2:ALT(6)	Transmit Channel B
		P11.12:ALT(4)	
		P14.0:ALT(4)	
		P14.5:ALT(6)	
ERAY0:TXENA	to	P02.4:ALT(6)	Transmit Enable Channel A
		P11.6:ALT(4)	
		P14.9:ALT(6)	
ERAY0:TXENB	to	P02.5:ALT(6)	Transmit Enable Channel B
		P11.6:ALT(2)	
		P11.11:ALT(6)	
		P14.6:ALT(6)	
		P14.9:ALT(5)	
ERAY0:sleep_n	from	SCU:scu_syst_sleep_n	turn-off request from processor
ERAY0:INT0_INT	to	INT:eray0.INT0_INT	E-RAY Service Request 0
ERAY0:INT1_INT	to	INT:eray0.INT1_INT	E-RAY Service Request 1
ERAY0:TINT0_INT	to	INT:eray0.TINT0_INT	E-RAY Timer Interrupt 0 Service Request
ERAY0:TINT1_INT	to	INT:eray0.TINT1_INT	E-RAY Timer Interrupt 1 Service Request
ERAY0:NDAT0_INT	to	INT:eray0.NDAT0_INT	E-RAY New Data 0 Service Request
ERAY0:NDAT1_INT	to	INT:eray0.NDAT1_INT	E-RAY New Data 1 Service Request
ERAY0:MBSC0_INT	to	INT:eray0.MBSC0_INT	E-RAY Message Buffer Status Changed 0 Service Request
ERAY0:MBSC1_INT	to	INT:eray0.MBSC1_INT	E-RAY Message Buffer Status Changed 1 Service Request
ERAY0:OBUSY	to	INT:eray0.OBUSY	E-RAY Output Buffer Busy Service Request
ERAY0:IBUSY_INT	to	INT:eray0.IBUSY_INT	E-RAY Input Buffer Busy Service Request

39.5 Revision History

Table 320 Revision History

Reference	Change to Previous Version	Comment
V3.2.9		
-	Initial version for TC36x	
V3.2.10		
-	No functional change.	

FlexRay™ Protocol Controller (E-Ray)**Table 320 Revision History** (cont'd)

Reference	Change to Previous Version	Comment
V3.2.11		
–	No functional change.	

Peripheral Sensor Interface (PSI5)

40 Peripheral Sensor Interface (PSI5)

This chapter describes the Peripheral Sensor Interface (short PSI5) Module of the TC36x.

40.1 TC36x Specific IP Configuration

See features in family spec.

Table 321 TC36x specific configuration of PSI5

Parameter	PSI5
Number of PSI5 channels for this device	2

40.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

Table 322 Register Address Space - PSI5

Module	Base Address	End Address	Note
PSI5	F0005000 _H	F0005AFF _H	FPI slave interface

Register Overview Tables of PSI5

Table 323 Register Overview - PSI5 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_CLC	Clock Control Register	000 _H	SV,U	SV,E,P	Application Reset	See Family Spec
	Reserved (004 _H Byte)	004 _H	BE	BE		
PSI5_ID	Module Identification Register	008 _H	SV,U	BE	Application Reset	See Family Spec
PSI5_FDR	PSI5 Fractional Divider Register	00C _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_FDRL	Fractional Divider Register for Lower Bit Rate	010 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_FDRH	Fractional Divider Register for Higher Bit Rate	014 _H	SV,U	SV,E,P	Application Reset	See Family Spec

Peripheral Sensor Interface (PSI5)

Table 323 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_FDRT	Fractional Divider Register for Time Stamp	018 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_TSRA	Module Time Stamp Register A	01C _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_TSRB	Time Stamp Register B	020 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_TSRC	Module Time Stamp Register C	024 _H	SV,U	SV,E,P	Application Reset	See Family Spec
	Reserved (004 _H Byte)	028 _H	BE	BE		
PSI5_GCR	Global Control Register	02C _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_IOCRAx (x=0-1)	Input and Output Control Register x	030 _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RCRAx (x=0-1)	Receiver Control Register A x	034 _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RCRBx (x=0-1)	Receiver Control Register B x	038 _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RCRCx (x=0-1)	Receiver Control Register C x	03C _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_WDTxw (w=0-6;x=0-1)	Watch Dog Timer Register xw	040 _H +x* 90 _H +w*4	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_RSRx (x=0-1)	Receive Status Register x	05C _H +x* 90 _H	SV,U	BE	Application Reset	See Family Spec
PSI5_SDSxz (x=0-1;z=0-5)	Serial Data and Status Register xz	060 _H +x* 90 _H +z*4	SV,U	BE	Application Reset	See Family Spec
PSI5_SPTSCx (x=0-1)	Start of Pulse Time Stamp Capture Register x	078 _H +x* 90 _H	SV,U	BE	Application Reset	See Family Spec

Peripheral Sensor Interface (PSI5)

Table 323 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_SFTSCx (x=0-1)	Start of Frame Time Stamp Capture Register x	07C _H +x* 90 _H	SV,U	BE	Application Reset	See Family Spec
PSI5_RDRLx (x=0-1)	Receive Data Register Low x	080 _H +x* 90 _H	SV,U	BE	Application Reset	See Family Spec
PSI5_RDRHx (x=0-1)	Receive Data Register High x	084 _H +x* 90 _H	SV,U	BE	Application Reset	See Family Spec
PSI5_PGCx (x=0-1)	Pulse Generation Control Register x	088 _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_CTVx (x=0-1)	Channel Trigger Value Register x	08C _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_SCRx (x=0-1)	Send Control Register x	090 _H +x* 90 _H	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_SDRLx (x=0-1)	Send Data Register Low x	094 _H +x* 90 _H	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SDRHx (x=0-1)	Send Data Register High x	098 _H +x* 90 _H	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SSRLx (x=0-1)	Send Shift Register Low x	09C _H +x* 90 _H	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SSRHx (x=0-1)	Send Shift Register High x	0A0 _H +x* 90 _H	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SORLx (x=0-1)	Send Output Register Low x	0A4 _H +x* 90 _H	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_SORHx (x=0-1)	Send Output Register High x	0A8 _H +x* 90 _H	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_INTOV	Interrupt Overview Register	2F8 _H	SV,U	BE	Application Reset	See Family Spec
PSI5_INPx (x=0-1)	Interrupt Node Pointer Register x	2FC _H +x* 4	SV,U	SV,E,P	Application Reset	See Family Spec

Peripheral Sensor Interface (PSI5)

Table 323 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_INTSTATAx (x=0-1)	Interrupt Status Register A x	310 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_INTSTATBx (x=0-1)	Interrupt Status Register B x	324 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_INTSETAx (x=0-1)	Interrupt Set Register A x	338 _H +x* 4	nBE	SV,E,P	Application Reset	See Family Spec
PSI5_INTSETBx (x=0-1)	Interrupt Set Register B x	34C _H +x* 4	nBE	SV,E,P	Application Reset	See Family Spec
PSI5_INTCLRAX (x=0-1)	Interrupt Clear Register A x	360 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_INTCLRBx (x=0-1)	Interrupt Clear Register A x	374 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_INTENAx (x=0-1)	Interrupt Enable Register A x	388 _H +x* 4	SV,U	SV,E,P	Application Reset	See Family Spec
PSI5_INTENBx (x=0-1)	Interrupt Enable Register B x	39C _H +x* 4	SV,U	SV,E,P	Application Reset	See Family Spec
	Reserved (01C _H Byte)	3B0 _H	BE	BE		
PSI5_OCS	OCDS Control and Status	3CC _H	U,SV	SV,P	Debug Reset	See Family Spec
PSI5_ACCEN0	Access Enable Register 0	3D0 _H	U,SV	SV,SE	Application Reset	See Family Spec
PSI5_ACCEN1	Access Enable Register 1	3D4 _H	U,SV	SV,SE	Application Reset	See Family Spec
PSI5_KRST0	Kernel Reset Register 0	3D8 _H	U,SV	SV,P,E	Application Reset	See Family Spec
PSI5_KRST1	Kernel Reset Register 1	3DC _H	U,SV	SV,P,E	Application Reset	See Family Spec

Peripheral Sensor Interface (PSI5)

Table 323 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_KRSTCLR	Kernel Reset Status Clear Register	3E0 _H	U,SV	SV,P,E	Application Reset	See Family Spec
PSI5_RFCx (x=0-1)	Receive FIFO Control Register x	3E4 _H +x* 4	SV,U	SV,U,P	Application Reset	See Family Spec
PSI5_RDFx (x=0-1)	Receive Data FIFO x	3F8 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RSIOVx (x=0-1)	RSI Overview Register x	40C _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RMIOVx (x=0-1)	RMI Overview Register x	420 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_NBIOVx (x=0-1)	NBI Overview Register x	434 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_TEIOVx (x=0-1)	TEI Overview Register x	448 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_CRCIOVx (x=0-1)	CRCI Overview Register x	45C _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RDIOVx (x=0-1)	RDI Overview Register x	470 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_NFIOVx (x=0-1)	NFI Overview Register x	484 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_MEIOVx (x=0-1)	MEI Overview Register x	498 _H +x* 4	SV,U	BE	Application Reset	See Family Spec
PSI5_RSISEx (x=0-1)	RSI Overview Set Register x	4AC _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RMISEx (x=0-1)	RMI Overview Set Register x	4C0 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NBISEx (x=0-1)	NBI Overview Set Register x	4D4 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec

Peripheral Sensor Interface (PSI5)

Table 323 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_TEISETx (x=0-1)	TEI Overview Set Register x	4E8 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_CRCISETx (x=0-1)	CRCI Overview Set Register x	4FC _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RDISETx (x=0-1)	RDI Overview Set Register x	510 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NFISETx (x=0-1)	NFI Overview Set Register x	524 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_MEISETx (x=0-1)	MEI Overview Set Register x	538 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RSICLRx (x=0-1)	RSI Overview Clear Register x	54C _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RMICLRx (x=0-1)	RMI Overview Clear Register x	560 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NBICLRx (x=0-1)	NBI Overview Clear Register x	574 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_TEICLRx (x=0-1)	TEI Overview Clear Register x	588 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_CRCICLRx (x=0-1)	CRCI Overview Clear Register x	59C _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_RDICLRx (x=0-1)	RDI Overview Clear Register x	5B0 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_NFICLRx (x=0-1)	NFI Overview Clear Register x	5C4 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
PSI5_MEICLRx (x=0-1)	MEI Overview Clear Register x	5D8 _H +x* 4	nBE	SV,U,P	Application Reset	See Family Spec
	Reserved (014 _H Byte)	5EC _H	BE	BE		

Peripheral Sensor Interface (PSI5)

Table 323 Register Overview - PSI5 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PSI5_RDMLxy (x=0-3;y=0-31)	Receive Data Memory Low xy	600 _H +x* 100 _H +y* 8	SV,U	BE	Application Reset	See Family Spec
PSI5_RDMHxy (x=0-3;y=0-31)	Receive Data Memory High xy	604 _H +x* 100 _H +y* 8	SV,U	BE	Application Reset	See Family Spec
	Reserved (100 _H Byte)	A00 _H	BE	BE		

40.3 TC36x Specific Registers

There are no product specific register for this module.

40.4 Connectivity

The tables below list all the connections of PSI5 instances.

Table 324 Connections of PSI5

Interface Signals	connects		Description
PSI5:RX0A	from	P00.1:IN	RXD inputs (receive data) channel 0
PSI5:RX1A	from	P00.3:IN	RXD inputs (receive data) channel 1
PSI5:RX0B	from	P02.3:IN	RXD inputs (receive data) channel 0
PSI5:RX1B	from	P02.5:IN	RXD inputs (receive data) channel 1
PSI5:RX0C	from	P33.1:IN	RXD inputs (receive data) channel 0
PSI5:RX1C	from	P33.3:IN	RXD inputs (receive data) channel 1
PSI5:TX(0)	to	IOM:REF1(14)	TXD outputs (send data)
		P00.2:ALT(4)	
		P02.2:ALT(4)	
		P33.2:ALT(4)	
PSI5:TX(1:0)	to	IOM:MON1(15:14)	TXD outputs (send data)
PSI5:TX(1)	to	P00.4:ALT(4)	TXD outputs (send data)
		P02.6:ALT(4)	
		P33.4:ALT(4)	
PSI5:TRIG(5:0)	from	GTM:PSI5.TRIG(5:0)	GTM timer output vector - synchronized
PSI5:TRIGO(7:0)	to	INT:psi5.TRIGO(7:0)	PSI5 Service Request

40.5 Revision History

Table 325 Revision History

Reference	Change to Previous Version	Comment
V1.17.11		
	Register Overview table added.	

Peripheral Sensor Interface (PSI5)**Table 325 Revision History**

Reference	Change to Previous Version	Comment
Page 7	No functional changes. Formal changes in Connectivity tables.	
	Revision History entries up to V1.17.10 removed.	
V1.17.12		
Page 1	Second sentence changed to internal audience only due to customer confusion. No functional change.	

Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)

41 Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)

This chapter describes the Peripheral Sensor Interface with Serial PHY Connection (short PSI5-S) Module of the TC36x.

41.1 TC36x Specific IP Configuration

See features in family spec.

Table 326 TC36x specific configuration of PSI5S

Parameter	PSI5S
Number of channels for this device	8

41.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

Table 327 Register Address Space - PSI5S

Module	Base Address	End Address	Note
PSI5S	F0007000 _H	F0007FFF _H	FPI slave interface

Register Overview Table

There are no product specific register for this module.

41.3 TC36x Specific Registers

There are no product specific register for this module.

41.4 Connectivity

The tables below list all the connections of PSI5-S instances.

Table 328 Connections of PSI5S

Interface Signals	connects		Description
PSI5S:CLK	to	P02.4:ALT(4)	PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
		P33.10:ALT(5)	
PSI5S:RXA	from	P00.3:IN	RX data input
PSI5S:RXB	from	P02.5:IN	RX data input
PSI5S:RXC	from	P33.5:IN	RX data input
PSI5S:TX	to	P00.4:ALT(2)	TX data output
		P02.6:ALT(2)	
		P33.6:ALT(7)	

Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)
Table 328 Connections of PSI5S (cont'd)

Interface Signals	connects		Description
PSI5S:TRIG(7:0)	from	GTM:PSI5S.TRIG(7:0)	GTM timer output vector
PSI5S:TRIGO(7:0)	to	INT:psi5s.TRIGO(7:0)	PSI5-S Service Request

41.5 Revision History**Table 329 Revision History**

Reference	Change to Previous Version	Comment
V1.12.10		
Page 1	Connections table update, signal "PSI5S:CLK" added.	
Page 2	Clean up revision history.	

Gigabit Ethernet MAC (GETH)

42 Gigabit Ethernet MAC (GETH)

This document describes the GETH Interface specific appendix for the product TC36x.

42.1 TC36x Specific IP Configuration

No product specific configuration for GETH

42.2 TC36x Specific Register Set

Register Address Space Table

The address space for the module registers is defined in [Register Address Space Table](#).

Table 330 Register Address Space - GETH

Module	Base Address	End Address	Note
GETH	F001D000 _H	F001F0FF _H	FPI bus interface

Register Overview Table

Table 331 Register Overview - GETH (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_CONFIGURATION	MAC Configuration Register	0000 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_EXT_CONFIGURATION	MAC Extended Configuration Register	0004 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PACKET_FILTER	MAC Packet Filter Register	0008 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_WATCHDOG_TIMEOUT	MAC Watchdog Timeout Register	000C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_TAG_CTRL	MAC VLAN Tag Control Register	0050 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_TAG_DATA	MAC VLAN Tag Data Register	0054 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_TAG_FILTER_i (i=0-7)	MAC VLAN Tag Filter i Register	0054 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_VLAN_HASH_TABLE	MAC VLAN Hash Table Register	0058 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_INCL	MAC VLAN Tag Inclusion or Replacement Register	0060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_INCL_Q_i (i=0-3)	MAC VLAN Tag Inclusion or Replacement Register per Queue	0060 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INNER_VLAN_INCL_i (i=0-3)	MAC Inner VLAN Tag Inclusion or Replacement Register	0064 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_QUEUE_0_TX_FLOW_CTRL	MAC Queue 0 TX Flow Control Register	0070 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_FLOW_CTRL	MAC Receive Flow Control Register	0090 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_QUEUE_CTRL_4	MAC Receive Queue Control 4 register	0094 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_QUEUE_CTRL_0	MAC Receive Queue Control 0 Register	00A0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_QUEUE_CTRL_1	MAC Receive Queue Control 1 Register	00A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_QUEUE_CTRL_2	MAC Receive Queue Control 2 Register	00A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INTERRUPT_STATUS	MAC Interrupt Status Register	00B0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INTERRUPT_ENABLE	MAC Interrupt Enable Register	00B4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_TX_STATUS	MAC Receive Transmit Status Register	00B8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PMT_CONTROL_STATUS	MAC PMT Control and Status Register	00C0 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_RWK_PACKET_FILTER	MAC Wake-up Packet Filter Register	00C4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_COMMAND_0	MAC Wake-up Filter Command 0 Register	00C4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_OFFSET_0	MAC Wake-up Filter Offset 0 Register	00C4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_CRC_i (i=0-1)	MAC Wake-up Filter CRC i Register	00C4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_BYTE_MASK_i (i=0-3)	MAC Wake-up i Filter Byte Mask register	00C4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_CONTROL_STATUS	MAC LPI Control and Status Register	00D0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_TIMERS_CONTROL	MAC LPI Timers Control Register	00D4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_ENTRY_TIMER	MAC LPI Entry Timer Register	00D8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_1US_TIC_COUNTER	MAC One Microsecond Tic Counter Register	00DC _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PHY_INTERFACE_CONTROL_STATUS	MAC PHY Interface Control and Status Register	00F8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VERSION	MAC Version Register	0110 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_DEBUG	MAC Debug Register	0114 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE0	MAC Hardware Feature Register 0	011C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE1	MAC Hardware Feature Register 1	0120 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_HW_FEATURE2	MAC Hardware Feature Register 2	0124 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE3	MAC Hardware Feature Register 3	0128 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_MDI_O_ADDRESS	MAC MDIO Address Register	0200 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_MDI_O_DATA	MAC MDIO Data Register	0204 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_CSR_SW_CTRL	MAC CSR Software Controls Register	0230 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_EXT_CFG1	MAC Extended Configuration Register 1	0238 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADD_RESS0_HIGH	MAC Address 0 High Register	0300 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADD_RESS0_LOW	MAC Address 0 Low Register	0304 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADD_RESSi_HIGH (i=1-31)	MAC Address i High Register	0308 _H +(i-1)*8	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADD_RESSi_LOW (i=1-31)	MAC Address i Low Register	030C _H +(i-1)*8	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_CONTROL	MMC Control Register	0700 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_RX_INTERRUPT	MMC Receive Interrupts Register	0704 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_TX_INTERRUPT	MMC Transmit Interrupts Register	0708 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_RX_INTERRUPT_MAS K	MMC Receive Interrupts Mask Register	070C _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MMC_TX_INTERRUPT_MASK	MMC Transmit Interrupts Mask Register	0710 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OCTET_COUNT_GOOD_BAD	Good And Bad Transmitted Octet Count Register	0714 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PACKET_COUNT_GOOD_BAD	Good And Bad Transmitted Packets Count Register	0718 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_BROADCAST_PACKETS_GOOD	Good Transmitted Broadcast Packets Count Register	071C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTICAST_PACKETS_GOOD	Good Transmitted Multicast Packets Count Register	0720 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_64OCTETS_PACKETS_GOOD_BAD	Good And Bad 64 Octets Packets Transmitted Count Register	0724 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_65TO127OCTETS_PACKETS_GOOD_BAD	Good And Bad 65to127 Octets Packets Transmitted Count Register	0728 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_128TO255OCTETS_PACKETS_GOOD_BAD	Good And Bad 128to255 Octets Packets Transmitted Count Register	072C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_256TO511OCTETS_PACKETS_GOOD_BAD	Good And Bad 256to511 Octets Packets Transmitted Count Register	0730 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_512TO1023OCTETS_PACKETS_GOOD_BAD	Good And Bad 512to1023 Octets Packets Transmitted Count Register	0734 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_1024TO_MAXOCTETS_PACKETS_GOOD_BAD	Good And Bad 1024toMax Octets Packets Transmitted Count Register	0738 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_UNICAST_PACKETS_GOOD_BAD	Good Transmitted Unicast Packets Count Register	073C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTICAST_PACKETS_GOOD_BAD	Good And Bad Transmitted Multicast Packets Count Register	0740 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_TX_BROADCAST_PACKETS_GOOD_BAD	Good And Bad Transmitted Broadcast Packets Count Register	0744 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_UNDERFLOW_ERROR_PACKETS	Transmitted Underflow Error Packets Count Register	0748 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_SINGLE_COLLISION_GOOD_PACKETS	Good Transmitted Single Collision Count Register	074C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTIPLE_COLLISION_GOOD_PACKETS	Transmitted Multiple Collision Count Register	0750 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_DEFERRED_PACKETS	Transmitted Deferred Packets Count Register	0754 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LATE_COLLISION_PACKETS	Transmitted Late Collision Packets Count Register	0758 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_EXCESSIVE_COLLISION_PACKETS	Transmitted Excessive Collision Packets Count Register	075C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_CARRIER_ERROR_PACKETS	Transmitted Carrier Error Packets Count Register	0760 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OCTET_COUNT_GOOD	Good Transmitted Octet Count Register	0764 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PACKET_COUNT_GOOD	Good Transmitted Packet Count Register	0768 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_EXCESSIVE_DEFERRAL_ERROR	Transmitted Excessive Deferral Error Count Register	076C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PAUSE_PACKETS	Transmitted Pause Packets Count Register	0770 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_VLAN_PACKETS_GOOD	Good Transmitted VLAN Packets Count Register	0774 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OSIZE_PACKETS_GOOD	Good Transmitted Osize Packets Count Register	0778 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RX_PACKETS_COUNT_GOOD_BAD	Good And Bad Received Packets Count Register	0780 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OCTET_COUNT_GOOD_BAD	Good And Bad Received Octet Count Register	0784 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OCTET_COUNT_GOOD	Good Received Octet Count Register	0788 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_BROADCAST_PACKETS_GOOD	Good Received Broadcast Packets Count Register	078C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_MULTICAST_PACKETS_GOOD	Good Received Multicast Packets Count Register	0790 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_CRC_ERROR_PACKETS	Received CRC Error Packets Count Register	0794 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_ALIGNMENT_ERROR_PACKETS	Received Alignment Error Count Register	0798 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_RUNTIME_ERROR_PACKETS	Received Runtime Error Count Register	079C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_JABBER_ERROR_PACKETS	Received Jabber Error Count Register	07A0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_UNDERSIZE_PACKETS_GOOD	Good Received Undersized Packets Count Register	07A4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OVERSIZED_PACKETS_GOOD	Good Received Oversized Packets Count Register	07A8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_64OCTETS_PACKETS_GOOD_BAD	Good And Bad 64 Octets Packets Received Count Register	07AC _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_65TO127OCTETS_PACKETS_GOOD_BAD	Good And Bad 65to127 Octets Packets Received Count Register	07B0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_128TO255OCTETS_PACKETS_GOOD_BAD	Good And Bad 128to255 Octets Packets Received Count Register	07B4 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RX_256TO511OCTETS_PACKETS_GOOD_BAD	Good And Bad 256to511 Octets Packets Received Count Register	07B8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_512TO1023OCTETS_PACKETS_GOOD_BAD	Good And Bad 512to1023 Octets Packets Received Count Register	07BC _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	Good And Bad 1024toMax Octets Packets Received Count Register	07C0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_UNICAST_PACKETS_GOOD	Good Received Unicast Packets Count Register	07C4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LENGTH_ERROR_PACKETS	Received Length Error Packets Count Register	07C8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OUT_OF_RANGE_TYPE_PACKETS	Received Out Of Range Type Count Register	07CC _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_PAUSE_PACKETS	Received Pause Packets Count Register	07D0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_FIFO_OVERFLOW_PACKETS	Received FIFO Overflow Count Register	07D4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_VLAN_PACKETS_GOOD_BAD	Good And Bad Received VLAN Packets Count Register	07D8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_WATCHDOG_ERROR_PACKETS	Received Watchdog Error Count Register	07DC _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_RECEIVE_ERROR_PACKETS	Received Receive Error Count Register	07E0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_CONTROL_PACKETS_GOOD	Good Received Control Packets Count Register	07E4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LPI_USECONDS_CNTR	Transmitted LPI Microseconds Count Register	07EC _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_TX_LPI_TRAN_CNTR	Transmitted LPI Transition Count Register	07F0 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LPI_USEC_CNTR	Received Microseconds LPI Count Register	07F4 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LPI_TRANS_RAN_CNTR	Received LPI Transition Count Register	07F8 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_IPC_RX_INTERRUPT_MASK	MMC IPC Receive Interrupts Mask Register	0800 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_IPC_RX_INTERRUPT	MMC IPC Receive Interrupts Register	0808 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_GOOD_PACKETS	Good Received RxIPv4 Packets Count Register	0810 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_HEADER_ERROR_PACKETS	Received IPv4 Header Error Packets Count Register	0814 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_NO_PAYLOAD_PACKETS	Received IPv4 No Payload Packets Count Register	0818 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_FRAGMENTED_PACKETS	Received IPv4 Fragmented Packets Count Register	081C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS	Received IPv4 UDP Checksum Disabled Packets Count Register	0820 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_GOOD_PACKETS	Good Received RxIPv6 Packets Count Register	0824 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_HEADER_ERROR_PACKETS	Received IPv6 Header Error Packets Count Register	0828 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_NO_PAYLOAD_PACKETS	Received IPv6 No Payload Packets Count Register	082C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_GOOD_PACKETS	Good Received UDP Packets Count Register	0830 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RXUDP_ERROR_PACKETS	Received UDP Error Packets Count Register	0834 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_GOOD_PACKETS	Good Received TCP Packets Count Register	0838 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_ERROR_PACKETS	Received TCP Error Packets Count Register	083C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_GOOD_PACKETS	Good Received ICMP Packets Count Register	0840 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_ERROR_PACKETS	Received ICMP Error Packets Count Register	0844 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_GOOD_OCTETS	Good Received IPV4 Octets Count Register	0850 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_HEADER_ERROR_OCTETS	Received IPV4 Header Error Octets Count Register	0854 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_NO_PAYLOAD_OCTETS	Received IPV4 No Payload Octets Count Register	0858 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_FRAGMENTED_OCTETS	Received IPV4 Fragmented Octets Count Register	085C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	Received IPV4 UDP Checksum Disabled Octets Count Register	0860 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_GOOD_OCTETS	Good Received IPV6 Octets Count Register	0864 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_HEADER_ERROR_OCTETS	Received IPV6 Header Error Octets Count Register	0868 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_NO_PAYLOAD_OCTETS	Received IPV6 No Payload Octets Count Register	086C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_GOOD_OCTETS	Good Received UDP Octets Count Register	0870 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RXUDP_ER RROR_OCTETS	Received UDP Error Octets Count Register	0874 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_G OOD_OCTETS	Good Received TCP Octets Count Register	0878 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_ER ROR_OCTETS	Received TCP Error Octets Count Register	087C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_G OOD_OCTETS	Good Received ICMP Octets Count Register	0880 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_ER RROR_OCTETS	Received ICMP Error Octets Count Register	0884 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_CONTRO L	MAC Timestamp Control Register	0B00 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SUB _SECOND_INCRE MENT	MAC Sub-Second Increment Register	0B04 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYST EM_TIME_SECON DS	MAC System Time Seconds Register	0B08 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYST EM_TIME_NANO SECONDS	MAC System Time Nanoseconds Register	0B0C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYST EM_TIME_SECON DS_UPDATE	MAC System Time Seconds Update Register	0B10 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYST EM_TIME_NANO SECONDS_UPDA TE	MAC System Time Nanoseconds Update Register	0B14 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_ADDEND	MAC Timestamp Addend Register	0B18 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYST EM_TIME_HIGHE R_WORD_SECON DS	MAC System Time Higher Word Seconds Register	0B1C _H	U,SV	U,SV,P	Application Reset	See Family Spec

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Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_TIME STAMP_STATUS	MAC Timestamp Status Register	0B20 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TX_T IMESTAMP_STAT US_NANOSECON DS	MAC Transmit Timestamp Nanoseconds Status Register	0B30 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TX_T IMESTAMP_STAT US_SECONDS	MAC Transmit Timestamp Seconds Status Register	0B34 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_INGRESS _ASYM_CORR	MAC Timestamp Ingress Asymmetry Correction Register	0B50 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_EGRESS_ ASYM_CORR	MAC Timestamp Egress Asymmetry Correction Register	0B54 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_INGRESS _CORR_NANOSE COND	MAC Timestamp Ingress Correction Nanoseconds Register	0B58 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_EGRESS_ CORR_NANOSEC OND	MAC Timestamp Egress Correction Nanoseconds Register	0B5C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_INGRESS _CORR_SUBNAN OSEC	MAC Timestamp Ingress Correction Subnanoseconds Register	0B60 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIME STAMP_EGRESS_ CORR_SUBNANO SEC	MAC Timestamp Egress Correction Subnanoseconds Register	0B64 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS _CONTROL	MAC PPS Control Register	0B70 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS 0_TARGET_TIME _SECONDS	MAC PPS 0 Target Time Seconds Register	0B80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS 0_TARGET_TIME _NANOSECONDS	MAC PPS 0 Target Time Nanoseconds Register	0B84 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_PPS0_INTERVAL	MAC PPS 0 Interval Register	0B88 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS0_WIDTH	MAC PPS 0 Width Register	0B8C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_OPERATION_MODE	MTL Operation Mode Register	0C00 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_INTERRUPT_STATUS	MTL Interrupt Status Register	0C20 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_DMA_MAP0	MTL Receive Queue and DMA Channel Mapping 0 Register	0C30 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_OPERATION_MODE	MTL Queue 0 Transmit Operation Mode Register	0D00 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_UNDERFLOW	MTL Queue 0 Transmit Underflow Counter Register	0D04 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_DEBUG	MTL Queue 0 Transmit Debug Register	0D08 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_ETS_STATUS	MTL Queue 0 Transmit Status Register	0D14 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_QUANTUM_WEIGHT	MTL Queue 0 Transmit Quantum or Weights Register	0D18 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_Q0_INTERRUPT_CONTROL_STATUS	MTL Queue 0 Interrupt Control Status Register	0D2C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ0_OPERATION_MODE	MTL Queue 0 Receive Operation Mode Register	0D30 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT	MTL Queue 0 Receive Missed Packet and Overflow Counter Register	0D34 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ0_DEBUG	MTL Queue 0 Receive Debug Register	0D38 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MTL_RXQ0_CONTROL	MTL Queue 0 Receive Control Register	0D3C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_OPERATION_MODE (i=1-3)	MTL Queue i Transmit Operation Mode Register	0D40 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_UNDERFLOW (i=1-3)	MTL Queue i Transmit Underflow Counter Register	0D44 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_DEBUG (i=1-3)	MTL Queue i Transmit Debug Register	0D48 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_ETS_CONTROL (i=1-3)	MTL Queue i Transmit ETS Control Register	0D50 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_ETS_STATUS (i=1-3)	MTL Queue i Transmit ETS Status Register	0D54 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_QUANTUM_WEIGHT (i=1-3)	MTL Queue i Transmit Quantum or Weights Register	0D58 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_SENDSLOPECREDIT (i=1-3)	MTL Queue i Transmit SendSlopeCredit Register	0D5C _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_HICREDIT (i=1-3)	MTL Queue i Transmit HiCredit Register	0D60 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_LOCREDIT (i=1-3)	MTL Queue i Transmit LoCredit Register	0D64 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_Qi_INTERRUPT_CONTROL_STATUS (i=1-3)	MTL Queue i Interrupt Status Register	0D6C _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_OPERATION_MODE (i=1-3)	MTL Queue i Receive Operation Mode Register	0D70 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MTL_RXQi_MISSED_PACKET_OVERFLOW_COUNTER (i=1-3)	MTL Queue i Receive Missed Packet and Overflow Counter Register	0D74 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_DEBUG (i=1-3)	MTL Queue i Receive Debug Register	0D78 _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_CONTROL (i=1-3)	MTL Queue i Receive Control Register	0D7C _H +(i-1)*40 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_MODE	DMA Bus Mode Register	1000 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_SYS_BUS_MODE	DMA System Bus Mode Register	1004 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_INTERRUPT_STATUS	DMA Interrupt Status Register	1008 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_DEBUG_STATUS0	DMA Debug Status 0 Register	100C _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_DEBUG_STATUS1	DMA Debug Status 1 Register	1010 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_Channel_i_CONTROL (i=0-3)	DMA Channel i Control Register	1100 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_Channel_i_TX_CONTROL (i=0-3)	DMA Channel i Transmit Control Register	1104 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_Channel_i_RX_CONTROL (i=0-3)	DMA Channel i Receive Control Register	1108 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_Channel_i_TXDESC_LIST_ADDRESS (i=0-3)	DMA Channel i Transmit Descriptor List Address Register	1114 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_Channel_i_RXDESC_LIST_ADDRESS (i=0-3)	DMA Channel i Receive Descriptor List Address Register	111C _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_DMA_CHi_TXDESC_TAIL_POINTER (i=0-3)	DMA Channel i Transmit Descriptor Tail Pointer Register	1120 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_TAIL_POINTER (i=0-3)	DMA Channel i Recieve Descriptor Tail Pointer Register	1128 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TXDESC_RING_LENGTH (i=0-3)	DMA Channel i Transmit Descriptor Ring Length Register	112C _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_RING_LENGTH (i=0-3)	DMA Channel i Recieve Descriptor Ring Length Register	1130 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_INTERRUPT_ENABLE (i=0-3)	DMA Channel i Interrupt Enable Register	1134 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RX_INTERRUPT_WATCHDOG_TIMER (i=0-3)	DMA Channel i Recieve Interrupt Watchdog Timer Register	1138 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_SLOT_FUNCTION_CONTROL_STATUS (i=0-3)	DMA Channel i Slot Function Control and Status Register	113C _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APPLICATION_TRANSMIT_DESCRIPTOR (i=0-3)	DMA Channel i Current Application Transmit Descriptor Register	1144 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APPLICATION_RECEIVE_DESCRIPTOR (i=0-3)	DMA Channel i Current Application Receive Descriptor Register	114C _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APPLICATION_TRANSMIT_BUFFER_ADDRESS (i=0-3)	DMA Channel i Current Application Transmit Buffer Address Register	1154 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec

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Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_DMA_CHi_CURRENT_APP_RXBUFFER (i=0-3)	DMA Channel i Current Application Receive Buffer Address Register	115C _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_STATUS (i=0-3)	DMA Channel i Status Register	1160 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_MISS_FRAME_COUNT (i=0-3)	DMA Channel i Missed Frames Count Register	1164 _H +i*80 _H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_CLC	Clock Control Register	2000 _H	SV,U	SV,E,P	Application Reset	See Family Spec
GETH_ID	Module Identification Register	2004 _H	SV,U	BE	Application Reset	See Family Spec
GETH_GPCTL	General Purpose Control Register	2008 _H	SV,U	SV,P	Application Reset	See Family Spec
GETH_ACCEN0	Access Enable Register 0	200C _H	U,SV	SV,SE	Application Reset	See Family Spec
GETH_ACCEN1	Access Enable Register 1	2010 _H	U,SV	SV,SE	Application Reset	See Family Spec
GETH_KRST0	Kernel Reset Register 0	2014 _H	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_KRST1	Kernel Reset Register 1	2018 _H	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_KRSTCLR	Kernel Reset Status Clear Register	201C _H	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_ACCEN0Dx (x=0-3)	Access Enable Register 0 for DMAx	2020 _H +x*8	U,SV	SV,SE	Application Reset	See Family Spec

Gigabit Ethernet MAC (GETH)

Table 331 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_ACCEN1Dx (x=0-3)	Access Enable Register 1 for DMAx	2024 _H +x*8	U,SV	SV,SE	Application Reset	See Family Spec
GETH_SKEWCTL	Skew Control Register	2040 _H	SV,U	SV,P	Application Reset	See Family Spec

42.3 TC36x Specific Registers

No deviations from the Family Spec

42.4 Connectivity

If for one product no signal is connected to an alternate input, it is connected to GND internally at module entity level. This allows to leave some signals unconnected in the application (i.e. RXER, CRS, COL) and save pins and external connection to GND. The tables below list all the connections of the instances.

Table 332 Connections of GETH

Interface Signals	connects		Description
GETH:COLA	from	P11.15:IN	Collision MII
GETH:CRSA	from	P11.14:IN	Carrier Sense MII
GETH:CRSB	from	P11.11:IN	Carrier Sense MII
GETH:CRSDVA	from	P11.11:IN	Carrier Sense / Data Valid combi-signal for RMII
GETH:CRSDVB	from	P11.14:IN	Carrier Sense / Data Valid combi-signal for RMII
GETH:GREFCLK	from	TC36x:P11.5	Gigabit Reference Clock input for RGMII (125 MHz high precision)
GETH:MDC	to	P02.8:ALT(6)	MDIO clock
		P12.0:ALT(6)	
		P21.2:ALT(5)	
GETH:MDIO	to	P00.0:HWOUT(0)	MDIO Output
		P12.1:HWOUT(0)	
		P21.3:HWOUT(0)	
GETH:MDIOA	from	P00.0:IN	MDIO Input
GETH:MDIOC	from	P12.1:IN	MDIO Input
GETH:MDIOD	from	P21.3:IN	MDIO Input
GETH:PPS	to	P14.4:ALT(6)	Pulse Per Second
GETH:RCTLA	from	P11.11:IN	Receive Control for RGMII
GETH:REFCLKA	from	P11.12:IN	Reference Clock input for RMII (50 MHz)
GETH:RXCLKA	from	P11.12:IN	Receive Clock MII and RGMII

Gigabit Ethernet MAC (GETH)

Table 332 Connections of GETH (cont'd)

Interface Signals	connects		Description
GETH:RXCLKB	from	P11.4:IN	Receive Clock MII and RGMII
GETH:RXCLKC	from	P12.0:IN	Receive Clock MII and RGMII
GETH:RXD0A	from	P11.10:IN	Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
GETH:RXD1A	from	P11.9:IN	Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
GETH:RXD2A	from	P11.8:IN	Receive Data 2 MII and RGMII (RGMII can use RXD2A only)
GETH:RXD3A	from	P11.7:IN	Receive Data 3 MII and RGMII (RGMII can use RXD3A only)
GETH:RXDVA	from	P11.11:IN	Receive Data Valid MII
GETH:RXDVB	from	P11.14:IN	Receive Data Valid MII
GETH:RXERA	from	P11.13:IN	Receive Error MII
GETH:RXERB	from	P21.7:IN	Receive Error MII
GETH:RXERC	from	P10.0:IN	Receive Error MII
GETH:TRIGO(9:0)	to	INT:eth.TRIGO(9:0)	Ethernet Service Request
GETH:TCTL	to	TC36x:P11.6	Transmit Control for RGMII
GETH:TXCLK	to	TC36x:P11.4	Transmit Clock Output for MII and RGMII
GETH:TXCLKA	from	P11.5:IN	Transmit Clock Input for MII
GETH:TXCLKB	from	P11.12:IN	Transmit Clock Input for MII
GETH:TXD(0)	to	TC36x:P11.3	Transmit Data
GETH:TXD(1)	to	TC36x:P11.2	Transmit Data
GETH:TXD(2)	to	TC36x:P11.1	Transmit Data
GETH:TXD(3)	to	TC36x:P11.0	Transmit Data
GETH:TXEN	to	TC36x:P11.6	Transmit Enable MII and RMII
GETH:TXER	to	P11.4:ALT(6)	Transmit Error MII

42.5 DMA Burst Lengths Limitations by the System

Not all burst lengths of the IP are supported by the system.

The GETH kernel IP supports various burst length of 1 up to 32 beats as defined in DMA_CHi_TX_CONTROL.TxPBL and GETH_DMA_CHi_RX_CONTROL.RxPBL. They can be multiplied by 8 by setting DMA_CH(#i)_Control.PBLx8.

Other than specified in the IP only the following burst lengths are supported by the system: SINGLE, INCR4, INCR8. Note that DMA_CH(#i)_Control.PBLx8 must not be set with PBL values higher than 1.

42.6 Buffer and Descriptor Alignment

The GETH is implemented as a 32 bit peripheral. Nevertheless it is connected to 64 bit wide bus (SRI). To make full use of the possible performance of SRI and its bridges, the data buffers and the descriptors need to be aligned to 64 bit addresses.

Gigabit Ethernet MAC (GETH)

42.7 Embedded FIFOs

The GETH uses two embedded FIFOs. The TX FIFO has a size of 4 kByte, the RX FIFO has a size of 8 kByte.

42.8 Master TAG ID

The module has 4 DMA Channels that share one master interface connecting them to the SRI bus. In order to distinguish the 4 DMAs from each other in the system, the master tag ID will dynamically be changed depending on the currently active DMA. [Table 333](#) details which ID is presented for each DMA.

Table 333 Master TAG IDs for the Gigabit Ethernet MAC

DMA	Master TAG ID
DMA0	0x28 _H
DMA1	0x29 _H
DMA2	0x2A _H
DMA3	0x2B _H

42.9 Interrupt Service Requests

The module has 10 Service Request Nodes connecting it to the interrupt system. The interrupt request lines are connected to the interrupt controller as shown in [Table 334](#).

Table 334 Service Request Lines of Ethernet MAC

IR SRC	GETH IP signal	GETH IP function	Description
SRC_GETH0	GETH_TRIGO0	GETH_INTR	DMA functions (sbd_intr_o), this internal line is connected via OR gate to GETH.SR0 wake up on LAN (pmt_intr_o), this internal line is connected via OR gate to GETH.SR0 wake up on EEE - LPI (lpi_intr_o), this internal line is connected via OR gate to GETH.SR0
SRC_GETH1	GETH_TRIGO1	GETH_PPS	Pulse Per Second signal from Precision Time Protocol (ptp_pps_o)
SRC_GETH2	GETH_TRIGO2	GETH_TX_DMA0	TX interrupt from DMA 0 (sbd_perch_tx_intr_o[0])
SRC_GETH3	GETH_TRIGO3	GETH_TX_DMA1	TX interrupt from DMA 1(sbd_perch_tx_intr_o[1])
SRC_GETH4	GETH_TRIGO4	GETH_TX_DMA2	TX interrupt from DMA 2(sbd_perch_tx_intr_o[2])
SRC_GETH5	GETH_TRIGO4	GETH_TX_DMA3	TX interrupt from DMA 3(sbd_perch_tx_intr_o[3])
SRC_GETH6	GETH_TRIGO6	GETH_RX_DMA0	RX interrupt from DMA 0 (sbd_perch_rx_intr_o[0])
SRC_GETH7	GETH_TRIGO7	GETH_RX_DMA1	RX interrupt from DMA 1(sbd_perch_rx_intr_o[1])
SRC_GETH8	GETH_TRIGO8	GETH_RX_DMA2	RX interrupt from DMA 2(sbd_perch_rx_intr_o[2])
SRC_GETH9	GETH_TRIGO9	GETH_RX_DMA3	RX interrupt from DMA 3(sbd_perch_rx_intr_o[3])

42.10 Clocks

The module has multiple clock inputs and outputs connecting it to the system. They are connected to the system as shown in [Table 335](#).

If the application wants to use the IP in RGMII mode the application has to execute the following steps:

Gigabit Ethernet MAC (GETH)

- Prior to the application reset the application must switch on f_{GETH} (by configuring CCUCON5.GETHDIV)
- Attach an external 125 MHz clock to input GREFCLK
- Activate the application reset
- Wait for 10 μ s

Table 335 Clock Lines of Ethernet MAC

Clock Line	Connected to	Description
hclk_i / f_{AHB}	f_{GETH}	AHB master interface clock
clk_csr_i / f_{CSR}	f_{SPB}	AHB slave interface clock
clk_tx_i	GETH_TXCLK (port pin)	MII transmit clock Input from PHY (10/100 MBit/s) The external PHY or oscillator provides this transmission clock. TXD[3:0] is synchronous to this clock. This is 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_gref_i	GETH_GREFCLK (port pin)	RGMII transmit clock Reference Input from PHY (1000 MBit/s). The external PHY or oscillator provides this clock as reference. TXD[3:0] is not necessarily synchronous to this clock! This is always 125 MHz in 1000/100/10 MBit/s mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_tx_o	GETH_TXCLK (port pin)	RGMII transmission clock Output to PHY (1000 MBit/s) . TXD[3:0] is synchronous (DDR) to this 125 MHz clock to the PHY. If RGMII is downgraded to 100 MBit/s it is divided internally to 25 MHz and for 10 MBit/s to 2.5 MHz. In each case it is generated from clk_gref_i by respective division. This division is controlled automatically by evaluation of mac_speed_o[1:0] and phy_intf_sel_i[2:0]. TXCLK has the same on chip delay and output pad delay as the TXD signals and TCTL unless clock skew is selected in SKEW.
clk_rx_i	GETH_RXCLK (port pin)	Receive clock from Phy. The external PHY provides this receive clock for RGMII, GMII, MII, and RMII interfaces. This clock is 125 MHz in 1 Gbps mode, 25 MHz in 100 Mbps mode, 2.5 MHz in 10 Mbps mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_rmii_i	ETH_REFCLK (port pin)	50-MHz clock used by the RMII from PHY. In 100 MBit/s Mode, it is divided internally to 25 MHz and provided to the internal MII interface. If RMII is downgraded to 10 MBit/s it is divided internally to 2,5 MHz. This division is controlled automatically by evaluation of mac_speed_o[1:0] and phy_intf_sel_i[2:0]. Needs a clock input during SW reset (GETH_BUS_MODE.SWR).
clk_ptp_ref_i	f_{GETH}	Reference Clock for the Time Stamp Update Logic

Gigabit Ethernet MAC (GETH)
42.11 Revision History**Table 336 Revision History**

Reference	Change to Previous Version	Comment
V1.3.10		
Page 22	Previous versions removed from revision history.	-
Page 18	Connections table changed (no functional changes).	-
V1.3.11		
-	No functional change.	-
V1.3.12		
Page 21	f_{SRI} changed to f_{GETH} as connection of clk_ptp_ref_i.	
Page 18	Updated connection of MII and RGMII in Connectivity .	
V1.3.13		
-	No functional changes.	-
V1.3.14		
-	No functional changes.	-
V1.3.15		
-	No functional changes.	-

43 External Bus Unit (EBU)

This device doesn't contain an EBU module.

44 SD- and eMMC Interface (SDMMC)

This device doesn't contain an SDMMC module.

45 Hardware Security Module (HSM)

The HSM is a separate processor subsystem dedicated for security tasks. It is connected as master and slave to the SPB bus.

For security reasons this module is described in a separate documentation. Please contact your Infineon representative for further information.

Input Output Monitor (IOM)

46 Input Output Monitor (IOM)

This document describes the IOM specific appendix for the product TC36x.

46.1 TC36x Specific IP Configuration

Table 337 TC36x specific configuration of IOM

Parameter	IOM
Number of FPC channels	16
Number of GTM inputs	8
Number of LAM	16
Number of ECM	1

46.2 TC36x Specific Register Set

Register Address Space Table

Table 338 Register Address Space - IOM

Module	Base Address	End Address	Note
IOM	F0035000 _H	F00351FF _H	FPI slave interface

Register Overview Table

There are no product specific register for this module.

46.3 TC36x Specific Registers

There are no product specific register for this module.

46.4 Connectivity

This section describes the connectivity of the IOMmodule.

Table 339 Connections of IOM

Interface Signals	connects		Description
IOM:GTM(7:0)	from	GTM:TOUT(29:22)	GTM-provided inputs to EXOR combiner
IOM:MON1(0)	from	CCU60:CC62	Monitor input 1
IOM:MON1(1)	from	CCU60:CC61	Monitor input 1
IOM:MON0(12:0)	from	GTM:TOUT(34:22)	Monitor input 0
IOM:MON1(2)	from	CCU60:CC60	Monitor input 1
IOM:MON1(3)	from	CCU60:COU60	Monitor input 1
IOM:MON1(4)	from	CCU60:COU61	Monitor input 1
IOM:MON0(15:13)	from	GTM:TOUT(70:68)	Monitor input 0
IOM:MON1(5)	from	CCU60:COU62	Monitor input 1

Input Output Monitor (IOM)
Table 339 Connections of IOM (cont'd)

Interface Signals	connects		Description
IOM:MON1(6)	from	CCU60:COUT63	Monitor input 1
IOM:MON1(7)	from	CCU61:COUT63	Monitor input 1
IOM:MON1(8)	from	CCU61:CC60	Monitor input 1
IOM:MON1(9)	from	CCU61:CC61	Monitor input 1
IOM:MON2(0)	from	QSPI0:MRST	Monitor input 2
IOM:MON2(1)	from	QSPI1:MRST	Monitor input 2
IOM:MON2(2)	from	QSPI2:MRST	Monitor input 2
IOM:MON2(3)	from	QSPI3:MRST	Monitor input 2
IOM:MON2(5)	from	CAN00:TXD	Monitor input 2
IOM:MON2(6)	from	CAN01:TXD	Monitor input 2
IOM:MON2(7)	from	CAN02:TXD	Monitor input 2
IOM:MON2(8)	from	CAN03:TXD	Monitor input 2
IOM:MON1(10)	from	CCU61:CC62	Monitor input 1
IOM:MON1(11)	from	CCU61:COUT60	Monitor input 1
IOM:MON1(12)	from	CCU61:COUT61	Monitor input 1
IOM:MON1(13)	from	CCU61:COUT62	Monitor input 1
IOM:MON1(15:14)	from	PSI5:TX(1:0)	Monitor input 1
IOM:MON2(11:9)	from	GTM:TOUT(106:104)	Monitor input 2
IOM:MON2(12)	from	ASCLIN0:ATX ASCLIN0:ATXP	Monitor input 2
IOM:MON2(13)	from	ASCLIN1:ATX ASCLIN1:ATXP	Monitor input 2
IOM:MON2(14)	from	ASCLIN2:ATX ASCLIN2:ATXP	Monitor input 2
IOM:MON2(15)	from	ASCLIN3:ATX ASCLIN3:ATXP	Monitor input 2
IOM:PIN(0)	from	P33.0:IN	GPIO pad input to FPC
IOM:PIN(1)	from	P33.1:IN	GPIO pad input to FPC
IOM:PIN(2)	from	P33.2:IN	GPIO pad input to FPC
IOM:PIN(3)	from	P33.3:IN	GPIO pad input to FPC
IOM:PIN(4)	from	P33.4:IN	GPIO pad input to FPC
IOM:PIN(5)	from	P33.5:IN	GPIO pad input to FPC
IOM:PIN(6)	from	P33.6:IN	GPIO pad input to FPC
IOM:PIN(7)	from	P33.7:IN	GPIO pad input to FPC
IOM:PIN(8)	from	P33.8:IN	GPIO pad input to FPC
IOM:PIN(9)	from	P33.9:IN	GPIO pad input to FPC
IOM:PIN(10)	from	P33.10:IN	GPIO pad input to FPC
IOM:PIN(11)	from	P33.11:IN	GPIO pad input to FPC
IOM:PIN(12)	from	P33.12:IN	GPIO pad input to FPC

Input Output Monitor (IOM)
Table 339 Connections of IOM (cont'd)

Interface Signals	connects	Description
IOM:PIN(13)	from P20.12:IN	GPIO pad input to FPC
IOM:PIN(14)	from P20.13:IN	GPIO pad input to FPC
IOM:PIN(15)	from P20.14:IN	GPIO pad input to FPC
IOM:REF1(0)	from CCU60:COOUT63	Reference input 1
IOM:REF1(1)	from CCU60:COOUT62	Reference input 1
IOM:REF1(2)	from CCU60:COOUT61	Reference input 1
IOM:REF1(3)	from CCU60:COOUT60	Reference input 1
IOM:REF1(4)	from CCU60:CC62	Reference input 1
IOM:REF0(15:0)	from GTM:TOUT(15:0)	Reference input 0
IOM:REF1(5)	from CCU60:CC61	Reference input 1
IOM:REF1(6)	from CCU60:CC60	Reference input 1
IOM:REF1(7)	from CCU61:COOUT63	Reference input 1
IOM:REF1(8)	from CCU61:COOUT62	Reference input 1
IOM:REF1(9)	from CCU61:COOUT61	Reference input 1
IOM:REF2(0)	from QSPI0:MRST	Reference input 2
IOM:REF2(1)	from QSPI1:MRST	Reference input 2
IOM:REF2(2)	from QSPI2:MRST	Reference input 2
IOM:REF2(3)	from QSPI3:MRST	Reference input 2
IOM:REF2(5)	from CAN00:TXD	Reference input 2
IOM:REF2(6)	from CAN01:TXD	Reference input 2
IOM:REF2(7)	from CAN02:TXD	Reference input 2
IOM:REF2(8)	from CAN03:TXD	Reference input 2
IOM:REF1(10)	from CCU61:COOUT60	Reference input 1
IOM:REF1(11)	from CCU61:CC62	Reference input 1
IOM:REF1(12)	from CCU61:CC61	Reference input 1
IOM:REF1(13)	from CCU61:CC60	Reference input 1
IOM:REF1(14)	from PSI5:TX(0)	Reference input 1
IOM:REF2(11:9)	from GTM:TOUT(109:107)	Reference input 2
IOM:REF2(12)	from ASCLIN0:ATX ASCLIN0:ATXP	Reference input 2
IOM:REF2(13)	from ASCLIN1:ATX ASCLIN1:ATXP	Reference input 2
IOM:REF2(14)	from ASCLIN2:ATX ASCLIN2:ATXP	Reference input 2
IOM:REF2(15)	from ASCLIN3:ATX ASCLIN3:ATXP	Reference input 2

Input Output Monitor (IOM)**46.5 Revision History****Table 340 Revision History**

Reference	Change to Previous Version	Comment
V2.1.15		
-	No changes.	

47 8-Bit Standby Controller (SCR)

The description of the SCR for all devices is covered by the family specification.

Revision history

Document version	Date of release	Description of changes
V2.0.0	2021-02	<ul style="list-style-type: none"> Version comparison table updated. For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.6.0	2020-08	<ul style="list-style-type: none"> Version comparison table updated. For further changes see respective revision history of each chapter. The version comparison table below gives an overview. Removed device TC3Ax from set of documentation.
V1.5.0	2020-04	<ul style="list-style-type: none"> Version comparison table updated. For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.4.0	2019-12	<ul style="list-style-type: none"> Added TC3Ax appendix as target specification. Version comparison table updated. For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.3.0	2019-09	<ul style="list-style-type: none"> Added additional device TC3Ax to AURIX™ TC3xx set of documentation. Version comparison table updated. For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.2.0	2019-04	<ul style="list-style-type: none"> Added additional device TC3Ex to AURIX™ TC3xx set of documentation. Version comparison table updated. For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.1.0	2019-01	<ul style="list-style-type: none"> Power Management System for Low-End (PMSLE) added. TC33x and TC33xEXT added. Changes in connectivity tables. Version comparison table new. Detailed Revision History contained in each chapter.
V1.0.0	2018-08	<ul style="list-style-type: none"> First revision of the User's Manual. Detailed OCDS information not contained. Available under NDA. Detailed Revision History contained in each chapter.

Version comparison table for AURIX™ TC36x appendix

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
Introduction	V1.0.0	V1.0.0	No
MEMMAP	V0.1.20	V0.1.21	Yes, see chapter revision history
FW	V1.1.0.1.17	V1.1.0.1.18	No functional changes
SRI Fabric	V1.1.16	V1.1.17	No functional changes

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
• SBCU, EBCU	V1.2.8	V1.2.9	No functional changes
CPU	V1.1.20	V1.1.21	No functional changes
NVM Subsystem	V2.0.7	V2.0.7	No
• DMU	V2.0.11	V2.0.12	No functional changes
• NVM	V2.0.6	V2.0.6	No
LMU	n/a	n/a	–
DAM	n/a	n/a	–
SCU	V2.1.26	V2.1.27	No functional changes
CCU	see SCU	see SCU	–
PMS	V2.2.33	V2.2.34	No functional changes
PMSLE	n/a	n/a	–
MTU	V7.4.12	V7.4.13	Yes, see chapter revision history
PORTS	V1.8.21	V1.8.21	No
SMU	V4.0.22	V4.0.23	Yes, see chapter revision history
INT	V1.2.11	V1.2.11	No
FCE	V4.2.9	V4.2.9	No
DMA	V0.1.18	V0.1.18	No
SPU	n/a	n/a	–
SPU2	n/a	n/a	–
BITMGR	n/a	n/a	–
SPULCKSTP	n/a	n/a	–
EMEM	n/a	n/a	–
RIF	n/a	n/a	–
HSPDM	n/a	n/a	–
CIF	n/a	n/a	–
STM	V9.2.4	V9.2.4	No
GTM	V2.2.23	V2.2.24	Yes, see chapter revision history
CCU6	V3.0.0	V3.0.0	No
GPT12	V3.0.2	V3.0.2	No
CONVCTRL	V3.0.1	V3.0.1	No
EVADC	V3.0.4	V3.0.5	No functional changes
EDSADC	V3.0.5	V3.0.6	No functional changes
I2C	V2.3.6	V2.3.6	No
HSSL	V3.0.18	V3.0.19	No functional changes
• HSCT	V2.3.15	V2.3.15	No
ASCLIN	V3.2.8	V3.2.8	No
QSPI	V3.0.20	V3.0.20	No
MSC	V5.0.10	V5.0.10	No

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
SENT	V2.1.10	V2.1.10	No
MCMCAN	V1.19.13	V1.19.13	No
E-Ray	V3.2.10	V3.2.11	No functional changes
PSI5	V1.17.12	V1.17.12	No
PSI5-S	V1.12.10	V1.12.10	No
GETH	V1.3.14	V1.3.15	No functional changes
EBU	n/a	n/a	–
SDMMC	n/a	n/a	–
HSM	n/a	n/a	–
IOM	V2.1.15	V2.1.15	No
SCR	n/a	n/a	–

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