International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1140

Continuous dc Current Ratings of International Rectifier's Large Semiconductor Packages

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Section 1: Classic Current Rating for Power Semiconductors

There is a trend within the discrete power component industry of late to increase the dc current rating for low on-resistance devices to levels that historically have not been seen. This trend has accelerated as power transistor manufacturers introduce higher current / lower voltage designs. Mature JEDEC package designs, originally intended decades ago for dc currents on the order of 10’s of Amperes are now emerging as capable of 100’s of Amps. Is this due to some significant improvement in package materials / design or is this all smoke and mirrors? The answer is a little of both.

The current carrying capability of any package ultimately depends on three factors: temperature, temperature, and temperature. And as with real-estate, this one single factor depends on location, location, location. The temperatures of interest here are actually at three distinct sites on a package. The most important of these locations is the junction. For continuous current rating, on-resistance of the device determines the junction temperature through I^2R Joule heating. The on-resistance of Silicon dice now range below the 1 milliohm benchmark. Less resistance means more current and less heat due to conductive losses. This improvement could mean a reduction in paralleled-device count. Component costs, assembly costs, heat sinking costs and improved PCB utilization may be realized if a device can carry more current than earlier generations. Junction temperature has historically been the basis for setting the current limit, as was covered in a previous IR Application Note, AN-949.[1] However, with the migration toward lower on-resistance Silicon design and technologies, two other locations on a package must be considered.

The other two locations on a device undergoing high current flow, critical for temperature constraint, are the internal wire bonds and the contact point between the package leads and the substrate, often a printed circuit board. Ignore these temperatures and you may jeopardize the long term reliability in an application.

IR defines what can be called the “ultimate current” for power packages on discrete products. This ultimate current represents the largest current any given package can withstand under the most forgiving of setups for heat management. The bench setup used in measuring the ultimate current at International Rectifier is full immersion of parts in a nucleated-boiling inert fluid. Nucleated boiling can be a very effective means of removing heat from hot objects. There are, in fact, more aggressive (exotic) heat removal methodologies[2] but the approach adopted here is more than adequate to showcase the ability of new Silicon platforms. The key word in this approach is showcase. To actually utilize our parts in an application that targeted currents at the level of the ultimate current would likely be costly and impractical. Nucleated boiling is an expensive and tricky proposition. Our intent with this concept, however, is to state an upper limit for current capability of a package, offer up practical limits, and then provide a

methodology for users to assess their own maximum current. Geometries, copper traces, and heat management are the primary ingredients in the fight to reduce costs and improve efficiencies in power electronics, but attention to thermal management is crucial.

Section 2: Current Rating-Junction Temperature

The classic equation used for setting the maximum current rating for a device is limited by the maximum junction temperature, T_J max, with the perfect situation of the heat sink held to 25ºC. The Rated Id (continuous) for a power MOSFET would therefore be:

$$I_{D\max} = \sqrt{\frac{T_{J\max} - T_C}{R_{DS(on)} R_{\theta(JC)}}} \quad \text{Eqn 1.}$$

where $R_{DS(on)}$ is the limiting value of the on-resistance at rated $T_{J\,max}$, T_C is the case temperature set at 25 ºC, $R_{\theta JC}$ is the maximum value of thermal resistance between the top of die (junction) and the backside, middle of the heat sink. This approach to setting the I_{Dmax} has been around as long as power MOSFETs. It represents an early example of “specsmanship” amongst power MOS manufacturers. Very few users are willing to employ chilled water-cooled heat sinks to achieve this max current, which is what would be needed to maintain a case temperature at 25 ºC. Also, few users would also be willing to run the junction temperatures at $T_{J\,max}$. A more practical approach for the designer to generate their own, guard-banded I_{Dmax} (call it I_{Dgb})for a given application, utilizing a typical finned, air cooled heat sink with a thermal resistance of $R_{\theta ha}$ is:

$$I_{Dgb} = \sqrt{\frac{T_{Jgb} - T_A}{R_{DS(on)}\left(R_{\theta(JC)} + R_{\theta(CS)} + R_{\theta(hs)}\right)}} \quad \text{Eqn 2.}$$

where T_{Jgb} is a guard banded maximum junction temperature (50% to 75% T_J max) and $R_{\theta(CS)}$ is the case-to-sink thermal resistance.

Section 3: Current Rating-Wire Bond Temperature

Some International Rectifier power MOSFETs in TO-220 packages have 30% of the on-resistance coming from wire bond resistance. This percentage is poised to increase as resistances drop for new Silicon designs. If these devices are pushed to their limit for power dissipation via conductive losses in the die, then a new method for heat management must account for heat dissipation in the wires and leads. Multiple sources of power dissipation complicate a hitherto simple package.

When heat is generated by Aluminum source wire bonds inside of a package, that heat can flow in three directions: axially through the two wire ends, and radially out through the epoxy. If heat does not exit efficiently, then the

temperature could build up in the wire. At the upper limit, when the wire temperature reaches the melting point of Aluminum (660 ºC), current will cease flowing and you will have a non-functional part.

Epoxy mold compound, used in our legacy packages, extends the maximum current and power that wires can carry by conducting heat radially from the wire to the ambient, beyond what wire bonds experience when surrounded by air. This effect is reflected in the fusing current capability. Figure 1 is IR data from1996 on fusing current for three packages, comparing air vs. epoxy surrounding the wires of various diameters.

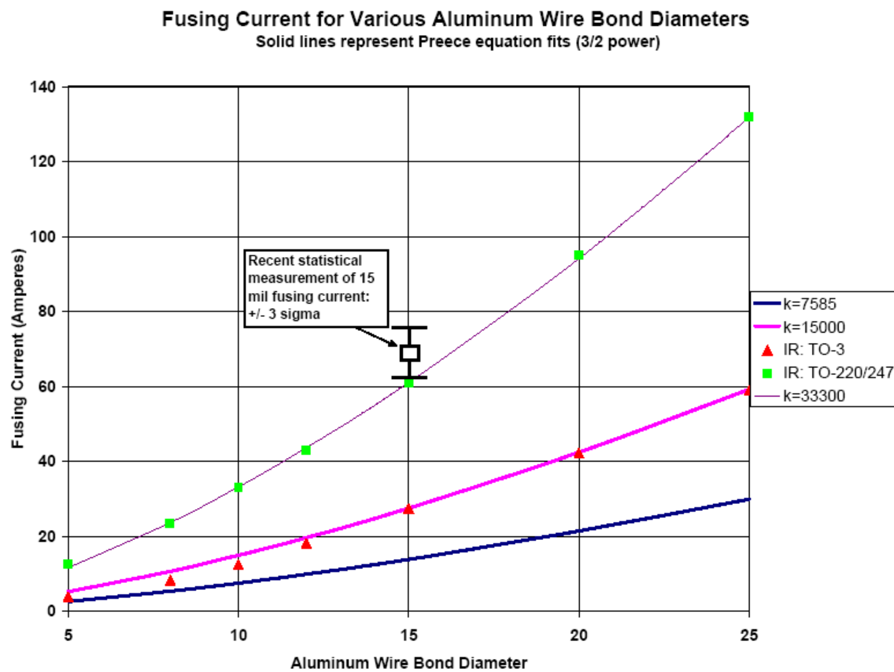

Figure 1: Fusing currents for Aluminum wires in air and in epoxy.

The lower two solid curves represent the historic 3/2 power law[3] [$I_f = k \times D^{3/2}$] for fusing current with two widely quoted k-constants for Aluminum. The magenta curve in the middle closely matches our TO-3 hermetic package fusing current capability (red triangles). However, when the same wire bonds are embedded in epoxy mold compound, the fusing current constant more than doubles (green squares). The single data point in the center with statistical limits is from a recent experiment, confirming time invariance of fusing current.

Reliability studies at International Rectifier from the same study cited in figure 1 revealed another important effect—if the mold compound, in contact with the wire bonds, remains above the glass transition of the epoxy due to wire bond heating, then time and temperature will degrade the chemical bonds of the epoxy compound, at this interface. These changes will do two things. First, the thermal

resistance of the epoxy, which determines the radial heat flow away from the wire, will degrade. Second, this chemical process could leave the nominally robust epoxy matrix porous and prone to the ingression of moisture and ionic contaminants into the package. Neither of theses changes would be good.

For these reasons, International Rectifier began rating packages to guarantee that no wire bond would exceed the glass transition of the mold compound. For example, a TO-220 package with an IRF3205 die, which has three 0.38 mm (15 mils) diameter source wire bonds, could carry 120 Amperes (40Ampere per wire) but an overriding limit of 75 Amperes was conservatively set for the overall package limit.

Section 4: Current Rating-Lead Contact Temperature

No matter how good a semiconductor package is for thermal capability, it must still be attached to the outside world. Conductors making contact to package leads, carrying high levels of current, can generate heating at the solder joint. The quantity and composition can affect the solder joint temperature, T_b. Metal conductors are often isolated from other conductors with organic based insulators and these insulators will have their own temperature limitations. Heat generated by a conductor must not soften the supporting insulator if that material is important for mechanical support of the conductors. This softening is typically correlated to the glass transition temperature (T_G) of the organic material. For FR-4 board material, this ranges between 110 ºC and 130 ºC. However, some board materials can go above 220 ºC. In any application, the lowest-rated-temperature material at the lead/board interface will constrain the peak temperature.

The original National Bureau of Standards set guidelines (IPC-2221 / MIL-STD-275) for current flow in FR-4 Printed Circuit Boards in 1956. Those numbers (10-15 A/mm^2, internal layers de-rating up to 50% and via holes at 5-10 A/via)[4] were based upon 1 ounce copper on trace with one ounce copper on the back side of a PCB. These upper limits were to accommodate the T_G for the FR-4. The power electronics industry today has learned to add higher copper content to aggressive current applications as a means of keeping the temperature down or increasing the current density. A higher copper content, consisting of multiple and/or thicker copper layers, pulls more heat away from the leads of a device. As will be demonstrated in the next section, this heat removal reduces temperature at the point of contact for high current conductors.

Other innovations, such as insulator metal substrate (IMS), have pushed many of these temperature constraints back onto the semiconductor package. These circuit boards pull the power away from the conductive traces so efficiently that power dissipation within the package again becomes the limitation.

Section 5: Influence of Mounting Methodology

The basis for setting the original package current ratings at International Rectifier were highly conservative: wires were soldered to the tips of the drain and source leads with a case not heat sunk. Few users would apply our part in their socket this way but those that did would certainly be guaranteed reliable performance. The analysis also relied upon infrared camera temperature measurements of exposed wire bonds. Etching open epoxy mold compound from around the source wires allowed IR temperature measurements but this method may have adversely skewed the observed temperatures (cf., figure 1).

A refined attempt at characterization of wire bond *in situ* temperature was recently completed. Wire temperature measurements used a fine thermocouple probe, inserted down into small hole in the mold compound and spring-loaded against the wire bond. The probe consisted of two 3-mil diameter thermocouple wires. The hole was then back filled with silicone compound, so as to exclude air from the wire surface. The thermal resistivity of this probe/silicone structure was equivalent to that of the displaced epoxy mold compound. The setup with the fine thermocouple is shown in figure 2.

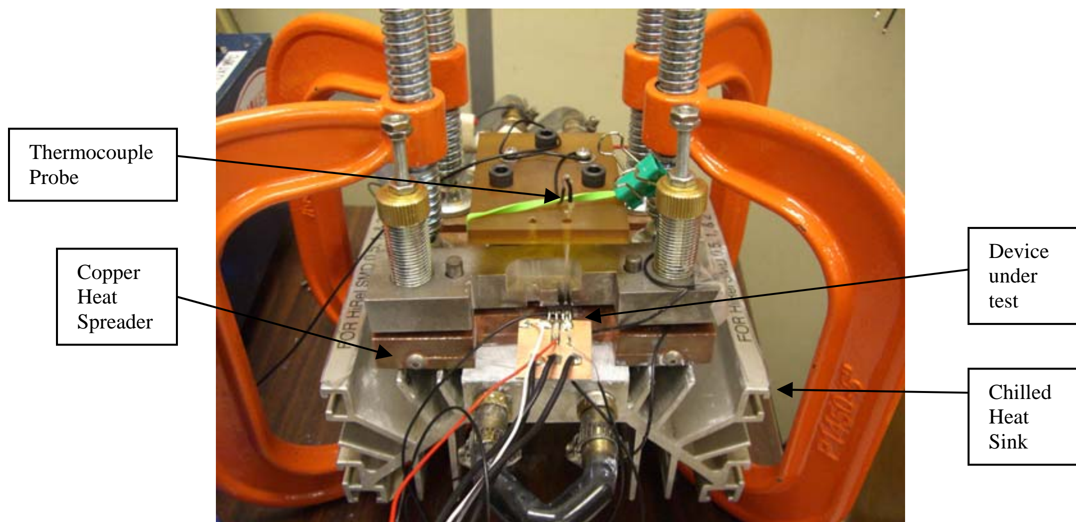

Figure 2: Experimental setup for wire bond temperature measurement

A single 15 mil diameter Aluminum wire bond was used to connect to a 2 milliohm die inside of a D2Pak package. Current conduction into the device was achieved with two methods of contact. Either heavy gauge wires were soldered to the leads of a package or the leads were soldered into vias of a double sided FR-4 PCB (as shown above) with 2 oz copper.

The temperature profile characterization, as seen in figure 3 below, indicated that the hottest temperature along the wire bond in this study was at the lead, not on the wire bond itself.

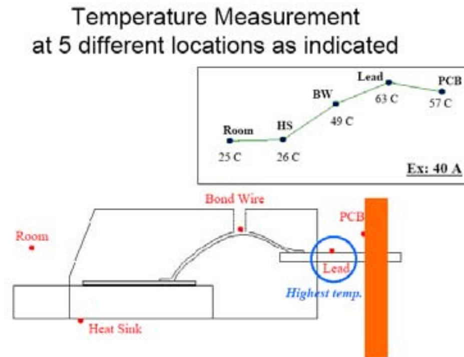

Figure 3: Typical temperature profile of wire bond

The observed temperature profile suggests that for both the PCB thru-hole mount and the surface mount configurations, the primary source of heat is the Joule heating of the lead, wire and copper trace. Heat is flowing both into the pcb and down to the die from the lead. The thermal resistance of the lead-to-air is on the order of 10 ºC/W. In contrast, the thermal resistance of the bond wire from the lead to the die is 300 ºC/W. Thus, the heat generated at the PCB goes mainly from the PCB to air, with a very little power actually flowing into the device through the wire. For this geometry, then, the wire bond or even multiple wire bonds will have little influence upon the temperature of the FR-4 board mounting. Most of the heat produced in the leads will need to be removed from the leads and the PCB directly to the environment.

Section 6: Current Rating Factors-Four Studies

The maximum dc current flowing into a package, in a given application, is dependant upon the temperatures at three locations (see figure 4) on a component. How is a user to determine beforehand how much current the package can handle? The most critical temperature, T_J, the junction temperature, is the best defined if the user understands their thermal stack, as specified in equation 2. The least well defined temperature, resulting from the contact resistance from the component to the circuit board, T_b, is entirely up to and defined by the user. This temperature can be affected by solder composition and quantity. The third temperature, located at the lead at the package, T_L, can be determined for each package and is presented in the following section for TO-220, TO-247, D^2Pak, and TO-262 packages. The temperature at this location has been found to independent of the junction temperature. Instead, it is dependent upon the I_d flowing into the package and the ambient temperature around the lead. This conclusion seems counterintuitive at first blush but the data from the following four recent studies supports this contention.

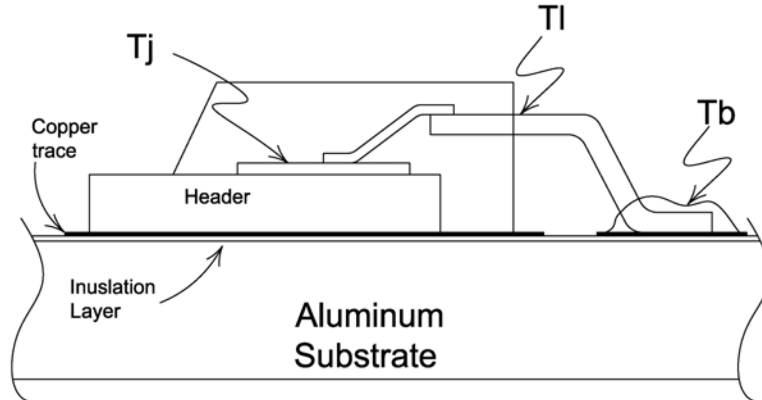

Figure 4: Cross-sectional view of D^2Pak mounted on IMS substrate.

Study 1: ID vs Temperature: Air / Nucleated boiling

IRFS3006PbFs were solder-mounted to IMS Aluminum substrates. Two sets of measurements were made on these devices to obtain the T_L v. I_D: in still air and in a nucleated boiling inert liquid. The junction temperatures were monitored by recording the V_{DS} as a function of I_D and then correlating the increase in on-resistance (V_{DS}/I_D) with an increase in T_J [5]. The lead temperatures were monitored with an 8 channel USB thermocouple monitor utilizing type T, fine wire thermocouples soldered onto the leads next to the epoxy bodies. The T_L vs. I_D^2 and T_J vs. I_D^2 results are presented in figures 5 and 6.

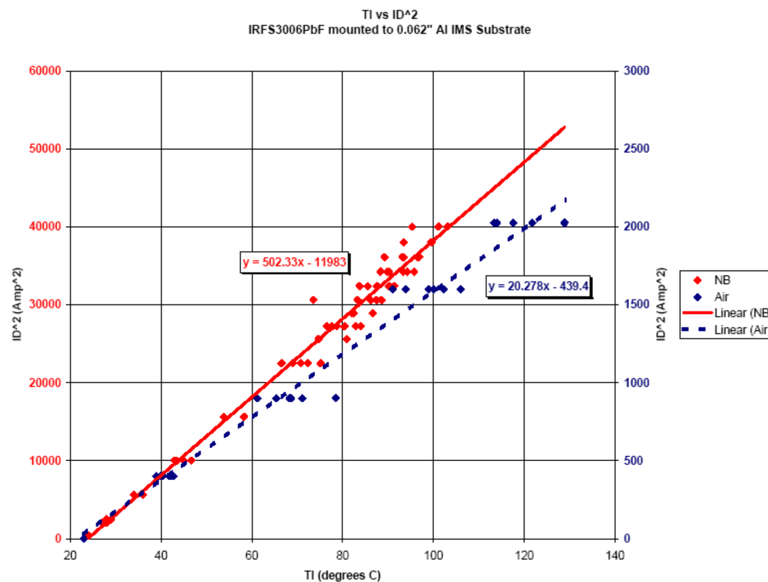

Figure 5: T_L vs I_D^2 for IRFS3006PbF devices mounted to IMS substrates.

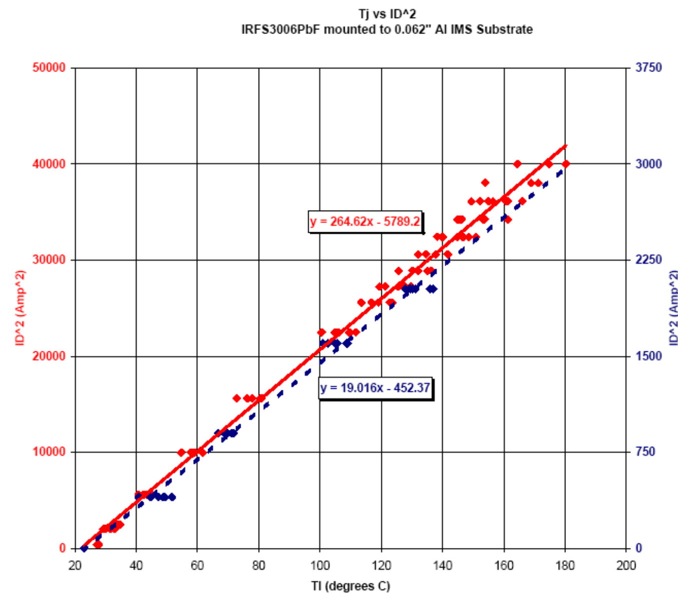

Figure 6: T_J vs I_D^2 for IRFS3006PbF devices mounted to IMS substrates.

The plots are temperature vs. I_D^2 along with linear LSFs. Note that the different scales, on the left and right, differ by over an order of magnitude. The linearity of the data suggests that the temperatures are the results of Joule heating ($I^2 \times R_{DSON} \times Rth$). The blue data (still air) reaches fairly high temperatures with relatively low currents (right hand scale in blue) as opposed to the red data (IMS immersed in a 23ºC bath of inert liquid, heat removal provided by nucleated boiling).

The linearity of the data sets in figure 5 could be explained by two mechanisms. First, lead temperatures could have simply followed the junction temperatures, which are expected to be linear. The junction temperatures in figure 6 might be expected to have elevated the temperature of one end of the wire bonds and therefore caused the lead temperature to follow along. The second possibility is that the lead temperatures followed a Joule heating curve because the heat generated in the wire bond and lead were dissipated directly to the ambient. To evaluate this latter possibility, we make a comparison between the data with high T_J against data with no T_J in the next section.

Study 2: ID vs Temperature: Die / No Die

We now compare two sets of independent data. The first set is the IRFS3006PbF D2Pak -7 pin data set (red) from figure 5. The second data set was from the earlier study for wire bond fusing current study, which utilized a TO-247 package with the same wire bond configuration as the 3006 but with no die. The leads of the TO-247s were soldered to heavy gauge wires and immersed in the same nucleated boiling liquid as used in the nucleated boiling setup for the

3006 devices from study 1. Prior to the onset of wire fusing, lead temperatures under nucleated boiling conditions were captured. The T_L vs I_D^2 data is presented figure 7 below.

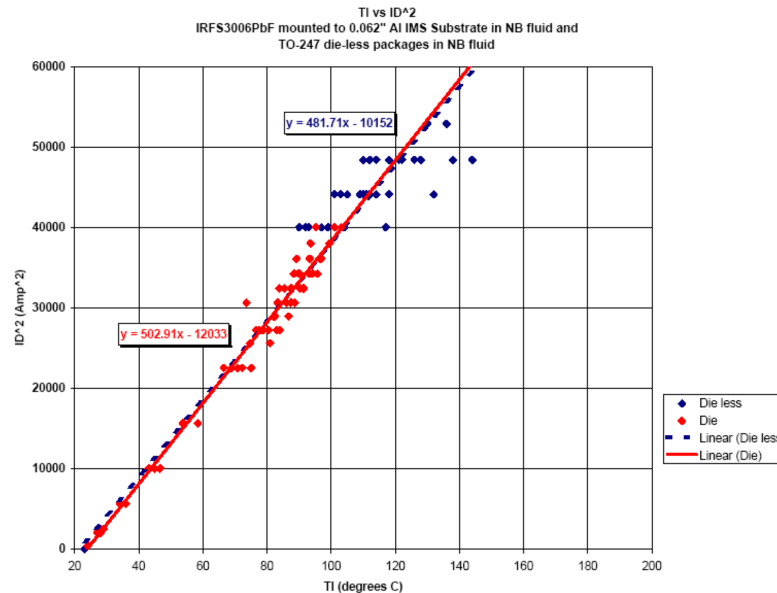

Figure 7: T_L vs I_D^2 for IRFS3006PbF devices mounted to IMS substrates(red data) compared to a die-less TO-247 packages, both in an inert nucleated boiling liquid (blue data).

Both sets of data refer just to the left hand vertical scale. What we observe is that the data sets are co-located on the same least square fit line. The main difference between the two sets of data in figure 7 is that the wire bond inside the package contacts a hot die (red data points) versus contacting a cool copper header (blue data points).

The only power dissipated within the TO-247 die-less package in figure 7 was generated by the wire bond (~0.25 mOhms) and lead resistances. The power dissipation of the 3006 is due primarily to the die (~1.0 mOhms) was from 40 to 50 Watts at the junction. The temperature at the back of either header does not go much above 80ºC because the copper is held close to the boiling point of the fluid. The end of the bond wires inside the package with the die, however, would be 20ºC hotter due to the power dissipation at die. The conclusion, therefore, is that the rise in lead temperature, T_L, is the result of lead heat removal into the environment surrounding the lead and not related to the junction temperature of the die. This conclusion is a very powerful statement! If a user knows the I_D^2 vs. T_L relationship for a given application environment, then they can establish a maximum current for that socket based on an upper limit of temperature, such as T_G of the mold compound or T_{max} of the PCB and then treat the junction temperature independently.

Does this interpretation make sense from a device physics perspective? Direct measurement of embedded wire bonds and junction temperatures is a difficult task. A good numerical finite element analysis may offer some support. Failing that, one can look at the situation from a “first principles”, qualitative viewpoint. Heat generated within the wire bond produces its highest temperature at the midpoint. Heat will flow axially toward the die and toward the lead, as well as radially outward. The theoretical thermal resistance of a 15 mil Aluminum wire, 7mm in length is about 300 ºC/W. Even with four such wire bonds in parallel (one of the “real” package improvements), the total thermal resistance of 75 ºC/W. If the die temperature is elevated, then heat flowing from the die to the lead along this wire will be greatly inhibited by this high resistance. The lead temperature will not modulate very much in response to the heat flowing along the wire from the die to the lead. However, heat generated within the bond wire near the lead end will flow outward to the lead through a shorter length of wire and hence and might contribute to the lead temperature. In all likelihood, the primary source of high lead temperature will be the heat generated at the lead solder joint itself, as we observed in section 5.

Study 3: ID vs Temperature: IMS / PCB in air

Another comparison can be made is to examine the contribution of the lead thermal resistance to ambient air for two different mounting configurations. In figure 8, we compare the I_D vs lead temperature for two mounting substrates.

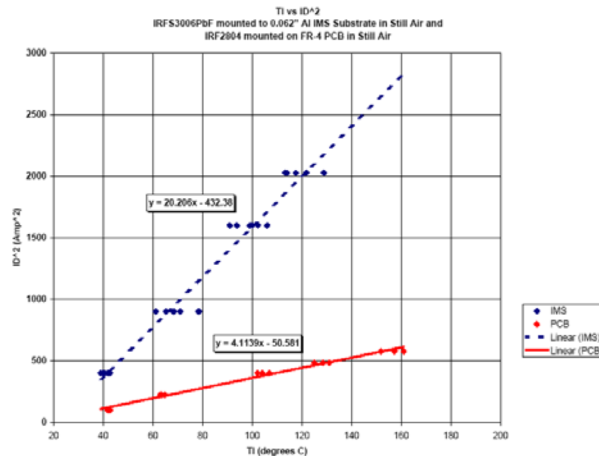

Figure 8: T_L vs I_D^2 for IRFS3006PbF devices mounted to IMS substrates compared to an IRF2804S mounted to an FR-4 PCB in still air.

The source lead on the 3006 is heat sunk to the Aluminum IMS substrate while the lead on the 2804 is essentially isolated with a very small Copper layer for heat spreading. The PCB trace used for the 2804S was narrow enough to have possibly generated significant amounts of heat to the lead. There is some difference between the source pins of the 3-pin 2804 and the 7 pin 3006 but the total lead area for each package would not be expected to account for the 400%

better heat dissipation that is apparent in figure 8. The conclusion is that most of the high current advantage of the IMS configuration is the heat removal from the lead into the metal substrate.

Study 4: T_G Speed Limit Revisited (Aged vs. Non-Aged)

The push for lead-free components in our industry has necessitated changes in packages for most manufacturers. A change in mold compound for the D^2Pak packages, to accommodate the higher solder reflow temperatures, has now introduced a different concern. The new epoxy for these packages has a glass transition temperature below the T_J max of the data sheet. These products have been shown to be robust at Pb-free solder reflow temperatures and have qualified to all AEC Q-101 test regimens and other internal reliability tests. The concern is whether the thermal conductivity of these new mold compounds will change with time if they are exposed to temperatures above their T_G. Figure 9 represents parts with the low T_G compound that have been exposed to 1000 hours at T_a = 175 ºC, followed by a current stress to assess the I_D v T_L. The results suggest that the thermal conductivity of the new compound does not degrade with exposure to temperatures exceeding T_G, to seemingly contradict the original observations from the 90’s. The data may actually suggest that the aged parts have a lower thermal resistance than virgin devices.

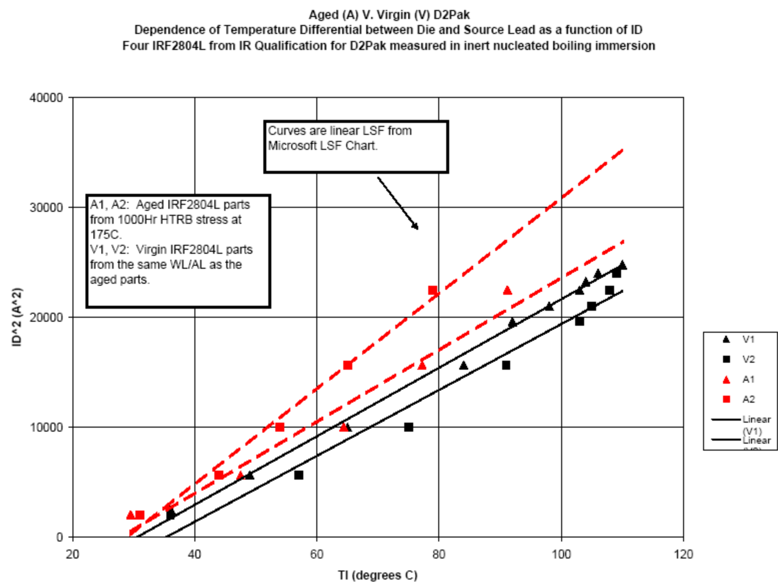

Figure 9: Study comparing two D2Pak FETs aged for 1,000 hours at 175ºC oven vs. two non-aged parts from the same lot. The objective was to look for a higher lead temperature on the aged parts, as a function of I_D^2. Leads on the aged parts (red data) demonstrate a lower temperature relative the leads of the virgin devices (blue data), for the same current level. All packages were mounted in identical configurations.

The study above did not quantify any change in the epoxy thermal conductivity but it does seem contrary to the earlier work on a different class of mold compounds, as 1000 hours of exposure at a temperature which was 40ºC hotter than the T_G should have given a significant difference. The possible improvement in thermal conductivity may indicate that the mold compound is densifying around the wire at this temperature and actually improving the radial thermal heat flow. The original limitation of T_G on package current rating is likely due to the higher T_G materials and the exposure to temperature over +200ºC. Junction temperature, therefore, will remain the upper limit for package capability as well.

Section 7: "Ultimate" Current Assessment

With data sheets showing up in the marketplace presenting extraordinary levels of rated current, the question arose as to what should be the ultimate current rating for an International Rectifier package. An investigation at IR set about the task of determining how much current is too much. The approach was to assemble several groups of parts, *sans* die, and with various wire bond configurations. Then, assess how much current it would take to damage the packages.

In this evaluation, the die-free devices were soldered to heavy gage wires and placed in an inert bath. A DC current was applied to the drain and source leads for 3 minute periods, with 5 Amp step increases in current for each time period, until the device broke down. The recorded current failure points were considered the last successful 3 minute period. The heat generated along the leads was carried away through nucleated boiling with a boiling point of 80ºC. In addition to stressing standard packages, some parts were intentionally damaged prior to epoxy mold compound application. This damage consisted of cutting one of the wire bonds, nicking one of the heels of a wire, and nicking all of the heels of the wires. The intent was to determine if such defects could be screened at final test with high levels of tester current.

Results of the Ultimate Current Evaluation

The statistically guard-banded results of the evaluation are presented in table 1. For the TO-220 and TO-247, the 20 mil diameter wire bond clearly affords the greatest ultimate current capability. It was also clear that a missed bond in any of the configurations could greatly reduce the ultimate current capability. The good news is that this potential defect is detectable at a high-current final test by causing a concurrent increase in Rdson well beyond the nominal distribution of the assembly lot. Based upon this study, a statistically based upper limit for the ultimate current rating for all of the legacy packages is being established for newer high current parts.

Package	Wire Bond Diam	No. of Bonds-matrl.	"Ultimate" Current
TO-220AB	15 mil	4 Al	160 A
TO-247	15 mil	4 Al	160 A
TO-262/3	15 mil	4 Al	160 A
TO-220AB	20 mil	3 Al	195 A
TO-247	20 mil	3 Al	195 A
TO-262/3	20 mil	3 Al	195 A
TO-262/3	20 mil	4 Al	240 A

Table 1: Ultimate current ratings for packages with different wire bonding configurations. With no attention to lead thermal management, the recommended current for all of the packages above is 75A.

Ultimate Current Limits and Derating

So, what good is the concept of an ultimate current limit? Few users are going to immerse parts in a nucleated boiling fluid to utilize the efficient heat removal from the leads of a package in an application. This is not a recommended solution to controlling the junction- and lead-temperature in a socket. The ultimate current does place a ceiling on the amount of current that can safely be forced into a device under the best-of-all-possible-worlds scenario. This large value, in conjunction with nominal levels determined from a conservative thermal management perspective, will give the user the perspective on how high a current that they can operate and how sensitive this performance parameter is in every manufacturer's data sheet to the actual application conditions.

In one sense, the ultimate package current limit is another example of industry specsmanship. There is, however, one redeeming benefit to this concept. New products that will be released in the future which have exceptionally low on-resistance will stand out based upon the new ultimate current limit. Many designers use the I_D max as a method of comparing one manufacturer to another, in terms of current handling capability. In this sense, this parameter will give the user the ability to compare different parts based upon this key value and not penalize those advanced products, with their potential for higher efficiency and lower operating temperatures, by rating their current lower because of package constraints. If a device's maximum junction temperature is reached with a current that is less than the packages ultimate current capability, then the current rating in the data sheet will be set via the classic method (eqn 1). If the Silicon die has exceptional capability for conduction, such that its T_J max is not exceeded at the classic current rating of the package, then its data sheet will carry the high "Ultimate Current" value on its banner characteristics, along with a reference to this application note.

Section 8: What current Can I Expect to Get From a Power MOSFET?

The heritage fleet of power MOSFET products has been rated via the classic method as described by equation 1. Those ratings fall on a very conservative engineering side. Newer, advanced products like the expanding suite of IR Trench products will begin carrying the new ultimate current limits, if appropriate. So how is the customer to determine how much of the current can he safely run in their application if the ultimate current is not achievable?

The answer depends very much upon how the device is used and how the environment for the application will affect the heat flow from the power device. The lead temperature will primarily vary with the square of the current. That thermal resistance will need to be evaluated for the mounting method used if the device is to be aggressively pushed for drain current.

The following procedure gives the user a direct, step by step method for determining the maximum current that they can force into an IR FET in their application:

1. Determine the maximum lead temperature for the application. As mentioned previously, this maximum lead or bond temperature is usually constrained to the glass transition temperature of the PCB material. Your board manufacturer is the best source for this recommendation. The maximum temperature for the lead will default to T_J max for the particular data sheet, if the board material is rated higher than T_J max of the device.
2. Board design to maximize current in an application. Consider alternative circuit board materials and weigh the use of more copper layers, thinner insulator layers, and thicker copper layers if more current is desired. These all are methods of lowering surface temperatures or increasing current capability on board traces. Adam[6] provides some insights into various ways of maximizing current capability of a PCB.
3. Measure the lead temperature of a mounted device in the lab. To do this, you will need to:
   a. Build some evaluation samples. The best way to power on the device on an actual circuit board is to isolate the gate trace and drive it with +15 Volt dc supply, relative to the source on an n-channel device. Solder heavy wires to the source and the drain traces near but not too close to the device or the wires could thermally interfere with the measurement. It might be helpful to have removed other components from that area of the circuit board, as they could pull current away from the FET being evaluated.
   b. Attach thermocouple wires. Solder thermocouple wires to the source lead, very close to the circuit board trace where it solders to the source lead (T_b) and on the lead, close to the epoxy body (T_L). Select or fabricate the thermocouple from fine wire so as to minimize its ability to pull heat away from the leads. T-type thermocouple wire will provide the highest resolution in the

range of temperatures. Thermocouples are tricky. I will be necessary to ensure that the first contact point between the two wires is enveloped with solder at the lead. Otherwise this point will become the temperature reference and if it is in air, it will report a lower T_L value. Non-contact methods should also work for measuring T_L, provided the lead is “blackened” to improve emissivity, the focus is set to a small area on the lead, and the system is calibrated.

c. Apply dc current. If the application uses forced air, then activate this cooling in a worst case condition (lowest CFM, worst geometry). Bias the gate circuit with dc voltage to turn on the FET. Then, apply current into the drain with a variable output power supply configured for constant current. The supply must be capable of reaching the target current for the application.

d. Measure T_L and T_b vs current. Take several measurements over different currents. Record the current and the temperature of the lead and solder attach point. Allow the system to sit for at least 3 minutes at each current level. If the soldered-on thermocouple falls off, then that is a good indication that there is too much current. If you have another connection to the drain, then a recording of the drain-source voltage should be made. Calculate the change in Rdson and correlate with the TJ based on the data sheet, as pointed out in reference 5. You can use the copper half of the T-type thermocouple which is connected to the source lead as the source Kelvin reference point for this Vds reading.

e. Plot the data. Plot out the data points, as shown for an exercise in figure 10 (a replication of figure 5), with a spreadsheet, plotting the square of the current vs. the T_L readings (we found that the T_b was roughly the same as T_L in this application). In this example, we have selected the IRFS3006PbF on the IMS substrate with air cooling. The blue dashed line is the least square fit to our lab data but represents the median response. Using a software package, like TableCurve 2D®, we can calculate a LSF representing the [median – 99.99%], shown as the magenta solid line. Our IMS manufacturer indicated that the insulation on the IMS was only rated for 150ºC. Taking this temperature as our limit to the lead temperature (the package epoxy is rated to 175 ºC), we draw in the green vertical arrow. We then draw the red horizontal arrow from the intersection of the green arrow and the magenta line to indicate our statistical limit for the I_D^2, which reads about 2000. This places the current limit for this application at 45 Amperes, the square root of 2000. This I_D is well below the rating for this part, 270A, but the high current rating in the data sheet is based on the Silicon limit. From Table 1, the ultimate current for this part is 290A. Clearly, any effort to reduce the Joule heating of the source lead will go a long way toward safely running this device at a current higher than 45A.

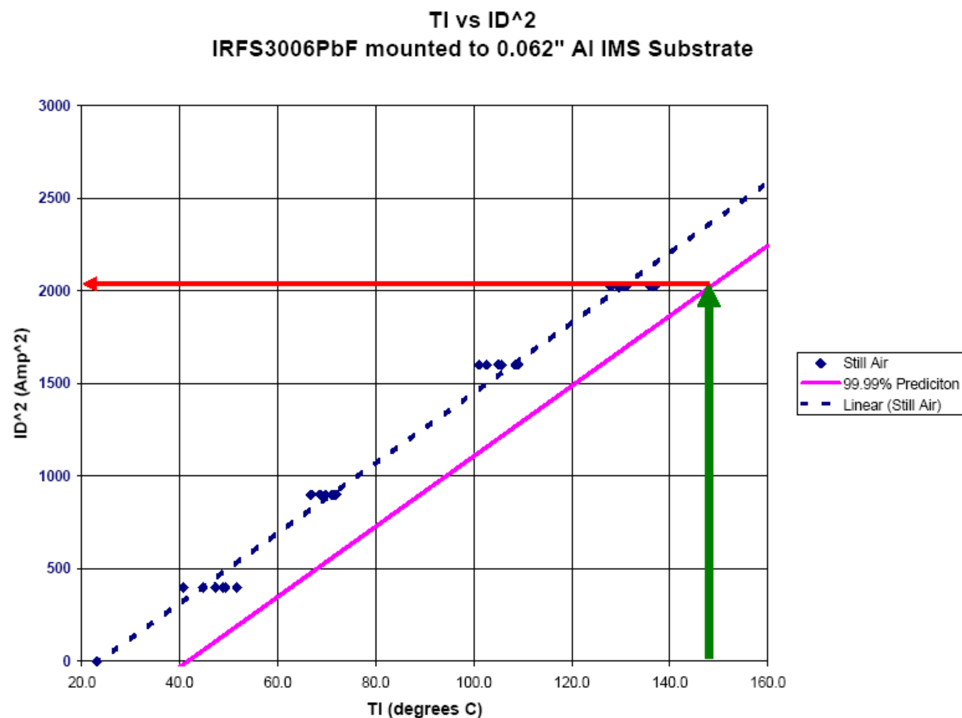

Figure 10 Example of Max I_D calculation for socket.

Summary

The maximum amount of continuous dc current that you can force into a FET supplied by any manufacturer is rarely the publicized I_D max on the banner headlines for a components specifications, particularly for low voltage, high current devices. The primary constraint upon the amount of current is the temperature of the source contact on a printed circuit board. The user must know what temperature constraints are present for their choice of PCB. Specific details that affect the package capability and the socket capability are outlined. Some typical samples of specific packages and mounting configurations are presented. The ultimate determination of the thermal resistance of the source lead-to-ambient requires direct measurement of a given mounting configuration. A method for performing this *in situ* assessment is presented.

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[1] Application Note 949, "Current Rating of Power Semiconductors", available at http://www.irf.com/technical-info/appnotes/an-949.pdf.
[2] Iversen, A.H., Whitaker, S., "Uniform temperature, ultrahigh flux heat sinks using curved surfacesubcoooled nucleate boiling," 5th IEEE SEMI-THERM Symposium, 1989, Feb 1989, pp. 88-92.
[3] C.f. various Engineering manuals, originally derived by Sir W. H. Preece, "On the heating effects of electric currents," *Proc. Royal Society*, vol. 36, pp. 464, 1884.
[4] Adam, J., "New Correlations Between Electrical Current and Temperature Rise in PCB Traces," 20th IEEE SEMI-THERM Symposium, 2004, Mar 2004, pp. 292-299.
[5] IRFS3006PbF data sheet, figure 4, "Normalized ON-Resistance vs. Temperature," p.3.