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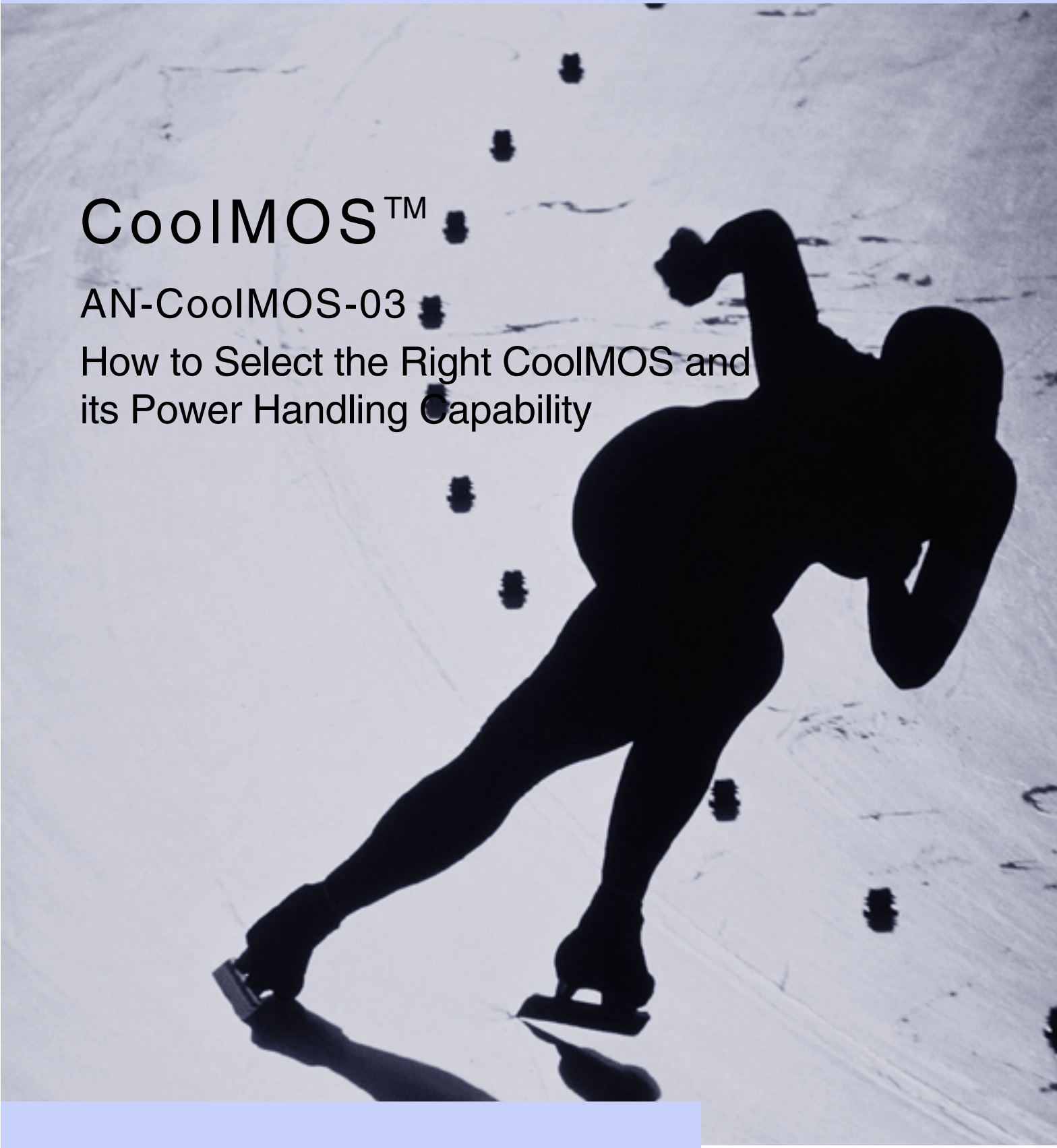

CoolMOS™

AN-CoolIMOS-03

How to Select the Right CoolMOS and its Power Handling Capability

Power Management & Supply

Infineon technologies

Never stop thinking.

How to Select the Right CoolMOS™ and its Power Handling Capability

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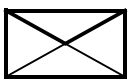

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1 Abstract

This application note is focusing on the selection of the high voltage MOSFET for Switched Mode Power Supply (SMPS). It shows a mathematical way to select the MOSFET with the intention to accelerate the design cycle of a SMPS.

Iteration process is introduced to evaluate as well the maximum allowable power dissipation as the conduction and switching power losses of the MOSFET. Maximum peak pulse current for discontinuous and continuous conduction mode converters has been calculated. To simplify the first iteration, charts of the output power handling capability versed the switching frequency have been shown.

2 Introduction

In the last couple of years the design cycle duration of SMPS in electronic applications becomes more and more important. Many applications need well controlled voltage containing features like low power dissipation for standby mode and a high efficiency during normal mode. These features make great demands on the power supply itself which can be satisfied by SMPS, like it is done actually for instance in most PC, charger or TV-set. Due to this wide range of applications the requirements for the SMPS cover a extensive array of features.

Some applications require one output voltage of the SMPS, others need more than one, some SMPS have a higher output voltage than the input voltage, others vice versa. One of the most important parameter for the selection of SMPS is the output power. To have a solution for each of the different applications, different topologies have been developed to achieve an optimum cost/performance ratio.

Figure 1 shows the most popular topologies for different output power classes.

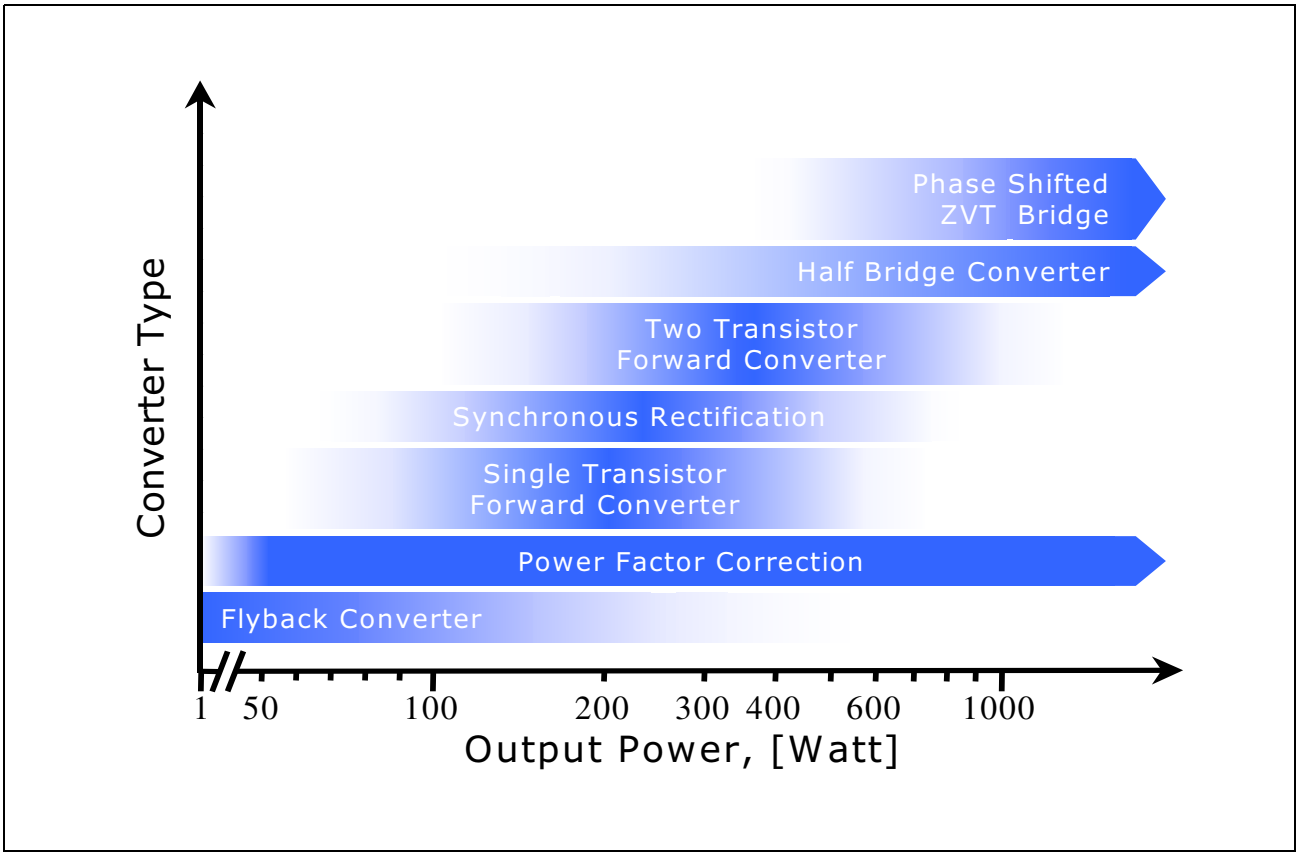


Figure 1 SMPS-Topologies Versed Output Power

The topologies mentioned in **Figure 1** can be operated in continuous conduction mode and in discontinuous conduction mode. The main difference between these both families are the shape of the current. Discontinuous conduction mode has a triangular shaped current, whereas for the continuous conduction mode a trapezoid shaped current is typical.

These topologies lead to different requirements for the MOSFETs, like

- packages
- drain-source voltage rating
- drain current rating
- on state resistance.

3 Selecting the Package

The selection of the MOSFET package mainly depends on following parameters.

Power dissipation/ cooling	Power losses of the MOSFET has a great impact on selection of the package. SMD packages can be used for lower power dissipation: DPAK for approximately 0.5 W (depending on pad size) D2PAK for approximately 1 W (depending on pad size) The through hole packages like TO-220 and especially TO-247 with attached heat sink and forced cooling can dissipate much more power.
Creepage distance	The creepage distance between legs of the package should correspond to the voltage requirements in the given application field.
Space/volume	The size of the package can be also influence by the available space/volume/height in a given case of SMPS/lamp ballast. For examples, notebook adapters use I2Pak in order to reduce the height of the device.
Cost	Smaller packages are usually less expensive, than the bigger ones. Also SMD mounting technology can be more cost-effective during the manufacturing process. Fully isolated package helps to reduce the cost of heat sink assembly by skipping the manufacturing step of putting the isolation pad between package and heat sink.

4 How to Choose the Voltage Rating of the MOSFET?

The avalanche breakdown voltage of CoolMOS is slightly higher than it's voltage rating due to typical safety margin. The voltage rating is defined at room temperature. Breakdown voltage of CoolMOS has strong positive temperature coefficient as it can be seen in **Figure 2**.

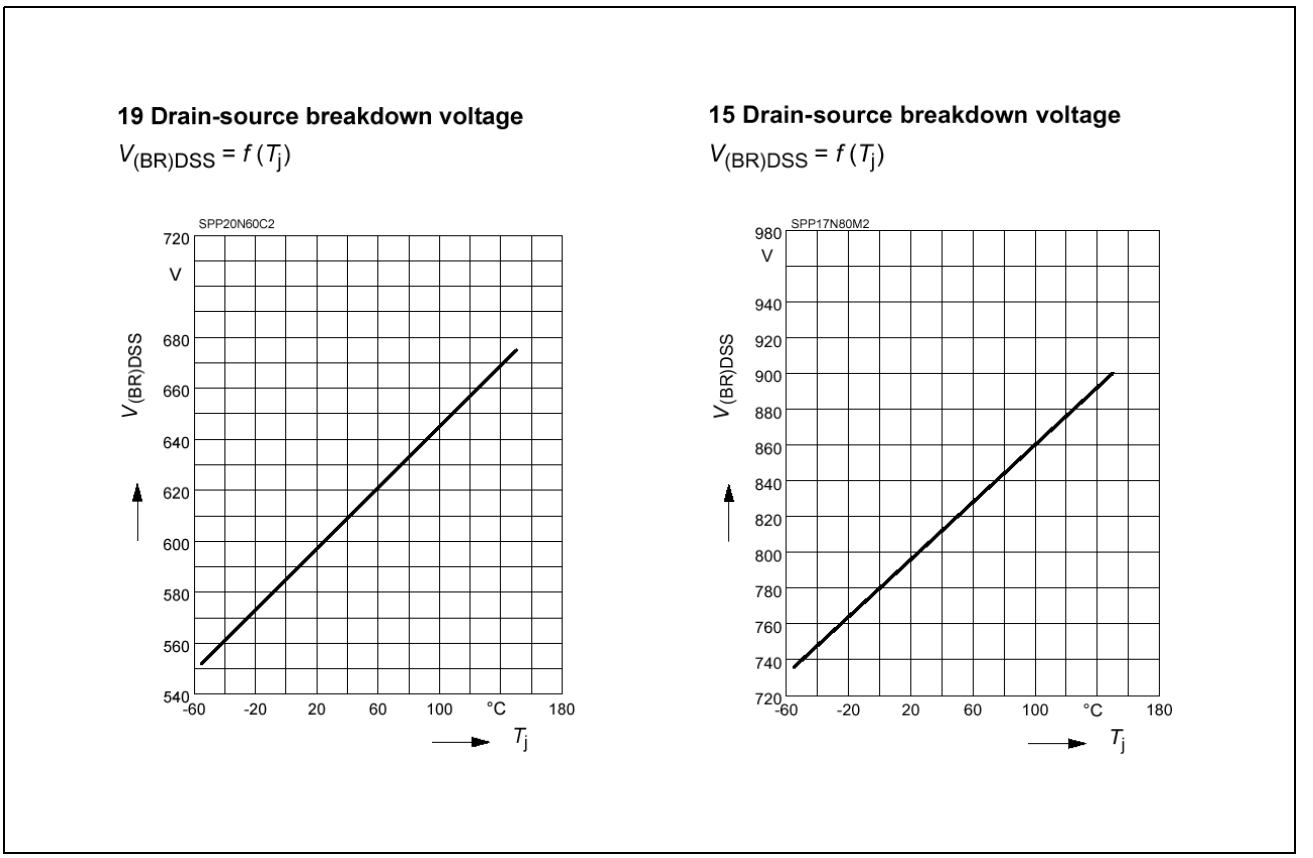


Figure 2 Dependence of the Breakdown Voltage on the Junction Temperature of 600 V CoolMOS and 800 V CoolMOS

Breakdown voltage at typical operation temperature of 100 - 120°C is approx. 7% higher than rated voltage.

Reliability tests are done at rated voltage, especially the HTRB (High Temperature Reversed Bias). These test results are used as input information for calculation of acceleration factors in different reliability models. In order to achieve high forecasted reliability the maximum operating voltage should be lower than the one used in HTRB.

Another criteria for selecting the voltage rating of the MOSFET are the overvoltage spikes. During turn off transient the voltage on the drain can reach much higher values as in steady state due to parasitic inductances in the circuit.

All these criteria should be considered during the selection of the MOSFET voltage rating. The maxi-mum steady state voltage during turn off should not exceed 70 to 90% of the rated voltage. These derating values has been achieved by the years of experience.

5 How to Select the Operating Junction Temperature?

Similar reliability rules can be applied for the selection of operating junction temperature of the MOSFET. The operating junction temperature should not exceed the maximum value specified in the datasheet. Pushing the operating temperature to the maximum is not reasonable. The majority of reliability test are done at maximum junction temperature, especially the HTRB (High Temperature Reversed Bias) and HTGS (High Temperature Gate Source). These test results are used as input information for calculation of acceleration factors in different reliability models. In order to achieve high forecasted reliability the maximum operating temperature should be lower than the maximum one. For example, reducing the junction temperature by 30°C will improve the MTBF (Mean Time Between Failure) of the CoolMOS by an order of magnitude.

On the other hand, the on-state resistance of the MOSFET increases with the junction temperature. It leads to increase in conduction power losses.

For these reasons the derating factors of 70-90% of the maximum junction temperature are recommended.

6 How to Choose the Current Rating of the MOSFET?

In the majority of SMPS applications the MOSFET is not being stressed up to it's maximum current rating due to poor cooling conditions. Designer prefers to take an advantage of low on-state resistance of the MOSFET in order to reduce the power losses. Usually MOSFETs with selected low $R_{ds(on)}$ have higher current rating then needed in the application. Nevertheless, it is useful to check the Safe Operating Area of the selected MOSFET.

On the other hand, gate-source voltage should be high enough to completely turn on the MOSFET. The transistor should be able to carry the maximum pulse current in converter under all conditions. Especially during start up or short circuit on the output of SMPS the supply voltage for the control IC can fall close to under voltage lockout limit. Some modern control IC have the under voltage lock out of approximately 7 V. The gate-source voltage of MOSFET can be less than 5 V, if we consider the voltage drops on the output stage of the control IC and on the current sense resistor in source path of transistor. MOSFET should be able to carry the required current without increase of drain-source voltage at given gate-source voltage. The transfer characteristic from the datasheet can be used in order to prove it **Figure 3**. If the MOSFET does not meet the requirements, another transistor with higher current rating should be selected.

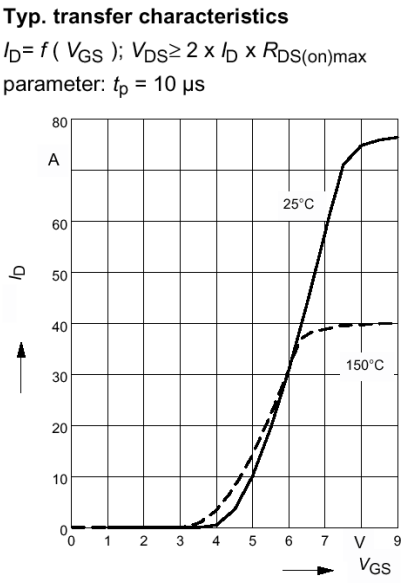


Figure 3 Transfer Characteristic

7 How to Choose the Right $R_{ds(on)}$)?

The most complicated selection is to choose the correct on state resistance of the device. The limit for the on state resistance is the maximum allowable power dissipation of the application and the maximum junction temperature of the MOSFET.

The power losses of the MOSFET can be divided into the conduction losses and the switching losses. The conduction losses are easy to calculate due to a constant on state resistance of the MOSFET and a well defined drain current.

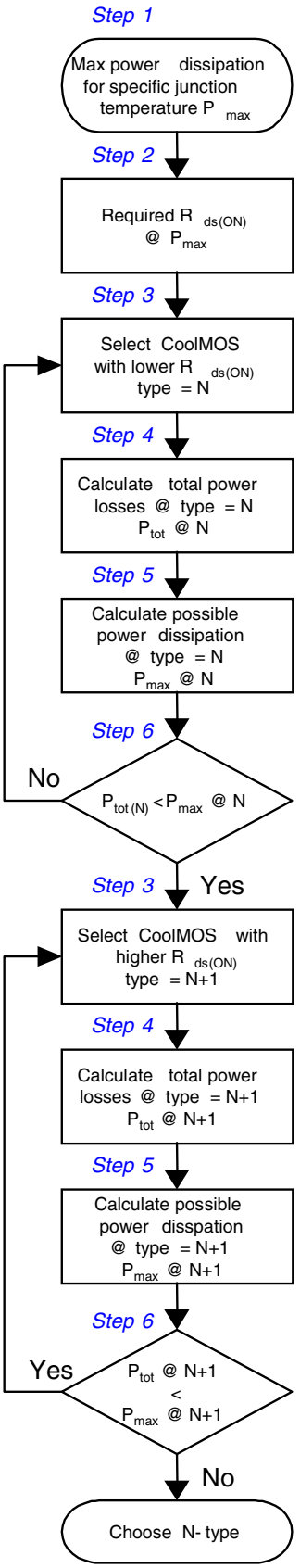
Problems occur by calculating the switching losses of the MOSFET. These losses strongly depend on parasitic parameters of the circuit. This application note is based on measurements of the switching energy versed the drain current in a test setup, which means, that it is not one to one transferable to other applications due to different parasitics. Test setup of SMPS is still necessary for the designer, but with this application note it is possible to save iterations for the design process.

The intention of this application note is to relieve the development of a SMPS by selecting an optimum MOSFET fulfilling the requirements of the application. To achieve this the maximum allowable power dissipation of the application with consideration of heat sink, topology etc. is compared with power losses of the MOSFET itself.

Designing the SMPS is a complicated process that requires many iterations. One thing the designer knows for sure is the output power of the SMPS. In most case the choice of topology is also done. It is usually based on the output power and the output voltage level.

Next step might be to fix the switching frequency. This is the point where the problem starts. Let us assume that the switching frequency is fixed to some value, which corresponds to other design criteria like EMI noise or magnetic losses, but is not related to the power losses in the MOSFET.

We will also assume, that the space for heat sink is known. That means we can estimate the thermal resistance of the heat sink R_{thCA}.



Step 1: Calculate the maximum power dissipation for a specific junction temperature

First step would be to calculate how much power losses can be allowed for the defined heat sink and specific junction temperature.

Step 2: Calculate the required $R_{ds(ON)}$ satisfying the maximum power losses from Step 1

At this point we already know the value of the maximum allowable power dissipation. We also know the topology and the drain current waveform. By using the drain current waveform we can calculate the value of $R_{ds(ON)}$, that will satisfy the maximum power losses. For the first iteration we will use only conduction power losses because we do not know the MOSFET type yet. The switching losses depend strongly on the particular MOSFET type. For this reason we will skip the switching losses for the first iteration, but we will check it in the following steps.

Step 3: Select the CoolMOS type with $R_{ds(ON)}$ defined in Step 2

In this step we will select the CoolMOS transistor type, that has the required on state resistance calculated in Step 2. Please note to use not a room temperature value, but a value at a higher junction tem-perature specific for particular design (usually between 110°C and 120°C). It should be double of a room temperature value.

Step 4: Calculate the total power losses for the selected Cool-MOS type in Step 3

Now we have enough information to calculate the total power losses for the selected CoolMOS transistor under particular operating conditions. As we now know the exact transistor type, we are able to calculate the switching power losses for a given switching frequency.

Step 5: Recalculate the maximum power dissipation for a selected CoolMOS type

With the available junction to case thermal resistance of the selected CoolMOS device it is possible to make the calculation of maximum allowable power dissipation more precisely. This step can help to skip one of the iteration what will be explained in Step 6.

Step 6: Compare the total power losses calculated in Step 4 for the selected CoolMOS type with maximum allowable power dissipation from Step 5

At this point it is necessary to compare the total power losses calculated in Step 4 with the maximum allowable power dissipation resulting from the defined junction temperature and heat sink (Step 5).

If the total power losses from Step 4 are lower than the maximum allowable power dissipation (Step 1), then the selected CoolMOS type meets the requirements. We did find the right type.

As a further optimization it could be possible to check if the next CoolMOS type with higher $R_{ds(ON)}$ will do the same job. Repeat Steps 4, 5 and 6 with this new selection.

In case of total power losses from Step 4 are higher than the maxi-mum allowable power dissipation (Step 1), select the next type from the CoolMOS family with lower on state resistance and repeat the Steps 4, 5 and 6. Another possibility would be to adjust the heat sink.

The right type is found, when the next CoolMOS with higher $R_{ds(ON)}$ does not meet the requirements.

Step 1 Calculate the maximum power dissipation for a specific junction temperature

First step would be to calculate how much power losses can be allowed for the defined heat sink and specific junction temperature.

8 How to Calculate the Maximum Power Losses for a Specific Junction Temperature?

This section explains how to calculate the maximum allowable power dissipation in the CoolMOS for a specific junction temperature using the datasheet parameters.

Input information:

$T_{J(max)}$ - maximum junction temperature

T_A - ambient temperature

R_{thJC} - assumed thermal resistance junction to case for the specific device

R_{thCA} - thermal resistance case to ambient

Solution:

The actual junction temperature:

$$T_J = \left[P_{max} \cdot \left(R_{thJC} + R_{thCA}\right)\right] + T_A \qquad [1]$$

then the maximum allowable power dissipation:

$$P_{tot} = \frac{T_{J(max)} - T_A}{R_{thJC} + R_{thCA}} \qquad [2]$$

Example for Step 1:

We assume that the thermal resistance of the heat sink is

R_{thCA} = 40 K/W.

Actually we have to consider the thermal resistance junction to case of the MOSFET also, but we did not select the MOSFET type yet. Let us assume some value for the thermal resistance of MOSFET just for the first iteration. Let us say it will be the value of second smallest CoolMOS device with a thermal resistance of 5 K/W:

R_{thJC} = 5 K/W.

The maximum allowed junction temperature in our case will be very conservative value:

T_J = 110°C.

The ambient temperature is:

T_A = 70°C

Now using the equation 2 we can calculate the maximum allowable power dissipation in our case:

$$P_{max} = \frac{T_J - T_A}{R_{thJC} + R_{thCA}} = \frac{110\ °C - 70\ °C}{5\frac{K}{W} + 40\frac{K}{W}} = 0.889\ W$$

Step 2 Calculate the required $R_{ds(ON)}$ satisfying the maximum power losses from Step 1

At this point we already know the value of the maximum allowable power dissipation. We also know the topology and the drain current waveform. Using the drain current waveform we can calculate the value of $R_{ds(on)}$, that will satisfy the maximum power losses. For the first iteration we will use only conduction power losses because we did not know the MOSFET type yet. The switching losses depend strongly on the particular MOSFET type. For this reason we will skip the switching losses for the first iteration, but we will check it in the following steps.

9 How to Calculate the Power Losses?

This section demonstrates how to calculate the power losses in the CoolMOS from the actual circuit using the datasheet parameters.

10 Conduction Losses

Input information:

D - duty cycle

t_{on} - turn on time

f - switching frequency

$V_{in(dc)}$ - input DC voltage

$R_{ds(ON)}$ - drain to source on-state resistance

Solution:

Conduction energy losses can be obtained by

$$E_{cond} = \int_0^{t_{on}} v_{ds}(t) \cdot i_d(t)\, dt = \int_0^{t_{on}} R_{ds(ON)} \cdot i_d(t)^2\, dt \qquad [3]$$

where, $v_{ds}(t)$ is the on-state voltage drop and $i_d(t)$ is the drain current waveform after turn on. Then conduction power losses:

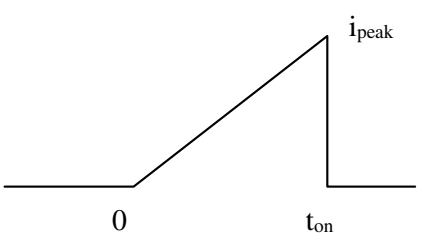
$$P_{cond} = E_{cond} \cdot f \qquad [4]$$

The turn on resistance of a MOSFET depends on its junction temperature. The on-state resistance at defined junction temperature can be calculated as:

$$R_{ds(ON)}(T_J) = R_{ds(ON)}(25\ °C) \cdot \left(1 + \frac{\alpha}{100}\right)^{T_J - 25\ °C}$$

The temperature factor a is for all CoolMOS transistors 0.8.

10.1 Discontinuous Conduction Mode Converter

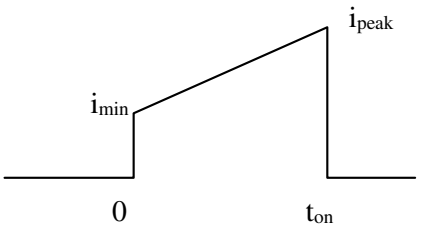
The drain current waveform:	Mathematical expression:
	$i_d = i_{peak} \cdot \frac{t}{t_{on}}$

$$E_{cond} = \int_0^{t_{on}} v_{ds}(t) \cdot i_d(t)\, dt = \int_0^{t_{on}} R_{ds(ON)} \cdot i_d(t)^2\, dt = \frac{1}{3} \cdot R_{ds(ON)} \cdot i_{peak}^2 \cdot t_{on} \qquad [5]$$

$$P_{cond} = E_{cond} \cdot f = \frac{1}{3} \cdot R_{ds(ON)} \cdot i_{peak}^2 \cdot D \qquad [6]$$

10.2 Continuous Conduction Mode Converter

The drain current waveform:



Mathematical expression:

$$i_d = i_{\min} + \frac{i_{peak} - i_{\min}}{t_{on}} \cdot t$$

In order to simplify the equations we will assume, that:

$$i_{min} = K_{min} \cdot i_{peak}$$

This means that the minimum drain current is a fixed percentage of the peak drain current.

$$E_{cond} = \int_0^{t_{on}} R_{ds(ON)} \cdot i_d(t)^2 \, dt = \frac{1}{3} \cdot \left(i_{min}^2 + i_{peak} \cdot i_{min} + i_{peak}^2 \right) \cdot R_{ds(ON)} \cdot t_{on} \quad [7]$$

$$P_{cond} = E_{cond} \cdot f = \frac{1}{3} \cdot R_{ds(ON)} \cdot D \cdot \left(i_{min}^2 + i_{peak} \cdot i_{min} + i_{peak}^2 \right) \quad [8]$$

Example for Step 2 (discontinuous conduction mode converter):

We can find how to calculate the $R_{ds(ON)}$ using equation 6:

$$R_{ds(ON)} = \frac{3 \cdot P_{cond}}{i_{peak}^2 \cdot D}$$

In our design we will use the following operating parameters:

i_{peak} = 2.4 A (peak drain current),

D = 0.21 (duty cycle).

From the example for **Step 1** we have

P_{max} = 0.889 W.

Now we can calculate the required on state resistance at T_J = 110°C:

$$R_{ds(ON)} = \frac{3 \cdot P_{cond}}{i_{peak}^2 \cdot D} = \frac{3 \cdot 0.889\ W}{(2.4\ A)^2 \cdot 0.21} = 2.205\ \Omega$$

As we can see the required on state resistance of CoolMOS for satisfying the maximum power dissipation is slightly above 2 Ω.

For a selection of required CoolMOS we need the on state resistance at a junction temperature of 25°C.

$$R_{ds(ON)}(25\ °C) = \frac{R_{ds(on)}(T_J)}{\left(1+\frac{\alpha}{100}\right)^{T_J - 25\ °C}} = \frac{2.205\ \Omega}{\left(1+\frac{0.8}{100}\right)^{110\ °C - 25\ °C}} = 1.12\ \Omega$$

For later calculations we will make the simplification, that on state resistance at 25°C is half of the resistance at junction temperature.

Using this information we can select a type from the CoolMOS family.

Step 3 Select the CoolMOS type with $R_{ds(on)}$ defined in Step 2

In this step we will select the CoolMOS transistor type, that has the required on state resistance calculated in **Step 2**. Please note to use not a room temperature value, but the value at a higher junction temperature specific for particular design (usually between 110°C and 120°C). It is approximately double of a room temperature value. This selection based only on conduction losses. The switching losses were not considered in this first iteration.

Example for Step 3 (discontinuous conduction mode converter):

From our previous calculation the required on state resistance is

$R_{ds(on)}$ =1.12 Ω

at T_J = 25°C.

Let us take a look on the CoolMOS product family.

	SOT-223	TO-252 (D-PAK)	TO-251 (I-PAK)	TO-220 SMD (D²-PAK)	TO-220	TO-220 FullPAK	TO-262 I²-PAK	TO-247
6.0 Ω 0.8 A	SPN01N60S5	SPD01N60S5	SPU01N60S5					
3.0 Ω 1.9 A	SPN02N60C3[1] SPN02N60S5	SPD02N60C3 SPD02N60S5	SPU02N60C3[1] SPU02N60S5	SPB02N60C3 SPB02N60S5	SPP02N60C3 SPP02N60S5			
1.4 Ω 3.2 A	SPN03N60C3[1] SPN03N60S5	SPD03N60C3 SPD03N60S5	SPU03N60C3[1] SPU03N60S5	SPB03N60C3 SPB03N60S5	SPP03N60C3 SPP03N60S5			
0.95 Ω 4.5 A	SPN04N60C3[1] SPN04N60C2 SPN04N60S5 Best-in-Class	SPD04N60C3 SPD04N60C2 SPD04N60S5	SPU04N60C3[1] SPU04N60C2 SPU04N60S5	SPB04N60C3 SPB04N60C2 SPB04N60S5	SPP04N60C3 SPP04N60C2 SPP04N60S5	SPA04N60C3 SPA04N60C2		
0.6 Ω 7.3 A		SPD07N60C3 SPD07N60C2 SPD07N60S5 Best-in-Class	SPU07N60C3[1] SPU07N60C2 SPU07N60S5 Best-in-Class	SPB07N60C3 SPB07N60C2 SPB07N60S5	SPP07N60C3 SPP07N60C2 SPP07N60S5	SPA07N60C3 SPA07N60C2	SPI07N60C3 SPI07N60S5	
0.38 Ω 11 A				SPB11N60C3 SPB11N60C2 SPB11N60S5	SPP11N60C3 SPP11N60C2 SPP11N60S5	SPA11N60C3 SPA11N60C2	SPI11N60C3 SPI11N60S5	
0.19 Ω 20 A				SPB20N60C3 SPB20N60C2 SPB20N60S5 Best-in-Class	SPP20N60C3 SPP20N60C2 SPP20N60S5 Best-in-Class	SPA20N60C3 SPA20N60C2 Best-in-Class		
0.07 Ω 47 A								Best-in-Class

[1]available on request, [2]available in Q2 2002

Figure 4 600 V Product Family

The SPP04N60C3 seems to be a good choice.

Step 4 Calculate the total power losses for the selected CoolMOS type in Step 3

Now we have enough information to calculate the total power losses for the selected CoolMOS transistor under particular operating conditions. As we now know the exact transistor type, we are able to calculate the switching power losses for a given switching frequency.

11 Switching Losses

Input information:

f - switching frequency

$V_{ds(on)}$ - DC voltage between drain and source before the start of the turn-on transition

$V_{ds(off)}$ - DC voltage between drain and source after the end of the turn-off transition

R_{gate} - gate resistor

E_{on} - energy losses during turn-on transition

E_{off} - energy losses during turn-off transition

$R_{gate(test)}$ - gate resistance during measurement of E_{on} and E_{off}

$V_{ds(test)}$ - drain to source voltage during measurement of E_{on} and E_{off}

Solution:

Switching energy losses occur due to simultaneous presence of significant drain-source voltage and drain current during each transient from turn off state into turn on state and vice versa.

Turn on switching energy losses can be obtained by

$$E_{on} = \int_{0}^{t_{d(on)} + t_r} v_{ds}(t) \cdot i_d(t)\, dt \qquad [9]$$

Turn off switching energy losses is expressed as

$$E_{off} = \int_{0}^{t_{d(off)} + t_f} v_{ds}(t) \cdot i_d(t)\, dt \qquad [10]$$

Total switching power losses are:

$$P_{sw} = (E_{on} + E_{off}) \cdot f \qquad [11]$$

Next charts will demonstrate the parameters, which influence the switching behavior of MOSFET and correspondingly the values of switching energy losses. The information shown is based on the investigations of a usual boost converter driven in the double pulse measurement mode. Please note that the turn on transient strongly depends on the used commutated diode and not on the MOSFET itself in case of non-triangle current waveforms. The power losses are given mostly by the characteristics of the commutated diode.

Both E_{on} and E_{off} strongly depend on the value of drain current **Figure 5**. E_{on} losses are dominated by the used commutated diode, not by MOSFET. We should take the power losses value at the corresponding drain current value in particular case. The curve can be interpolated with a second order polynome in order to simplify the calculations.

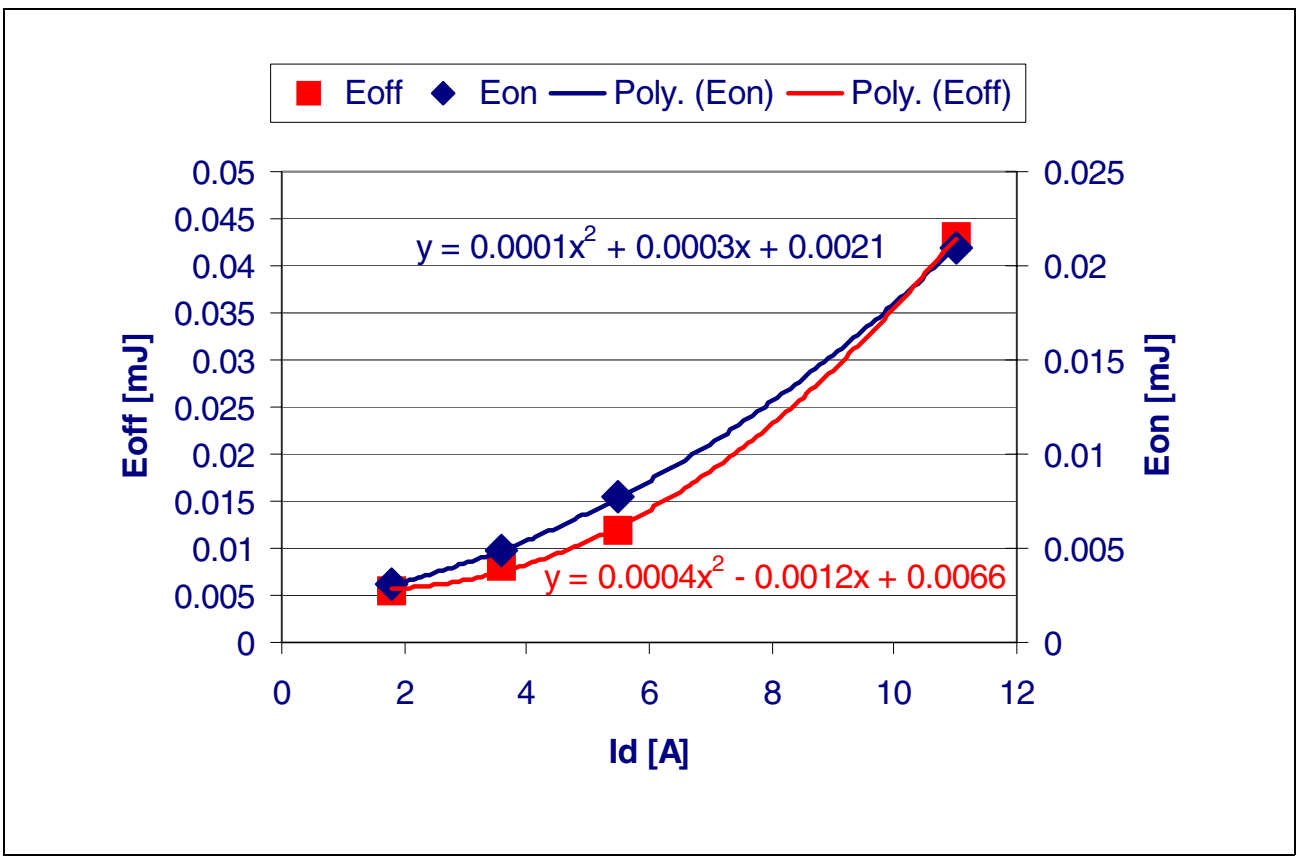


Figure 5 Switching Energy Losses vs. Drain Current (SPP11N60C3, SDP06S60, R_{gate} = 6.8 Ω, V_{ds} = 380 V, T_J = 125°C)

This information can be found in CoolMOS datasheets. It can be easily implemented directly into calculation.

$$E_{on}(i_d) = E_{on}(i_d) \quad [12]$$

$$E_{off}(i_d) = E_{off}(i_d) \quad [13]$$

Figure 6 demonstrates the switching energy losses versed external gate resistor. The recharging speed of CoolMOS capacitance can be controlled by R_{gate}. It influences the switching time, and correspondingly the switching losses. The curves are almost linear.

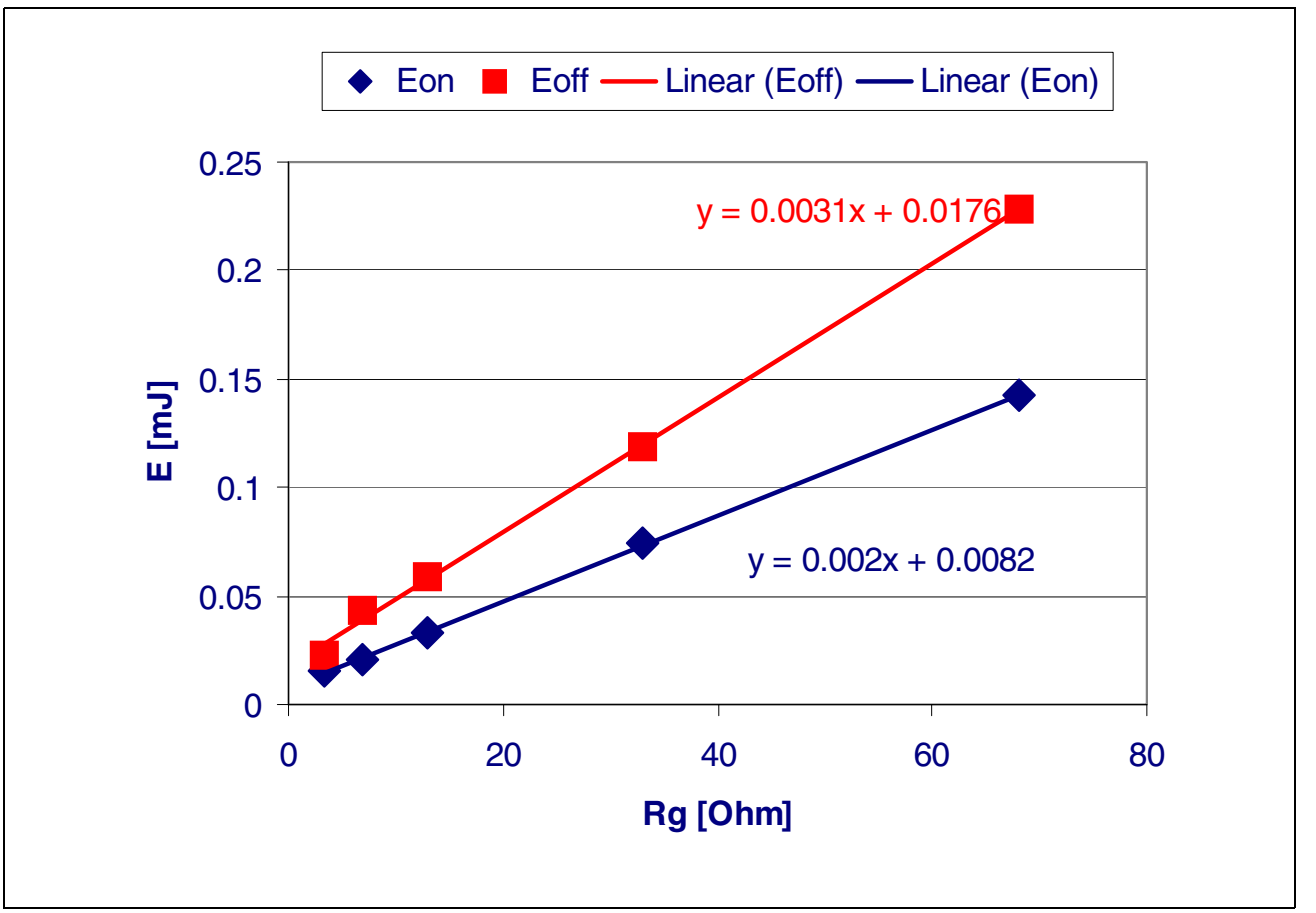


Figure 6 Switching Energy Losses vs. Gate Resistor (SPP11N60C3, SDP06S60, I_d = 11 A, V_{ds} = 380 V, T_J = 125°C)

The CoolMOS datasheet includes this chart. If your particular design does have another gate resistor as given in the datasheet you should implement a corrective factor into the equations of switching losses as following:

$$E_{on}(i_d, R_{gate}) = E_{on}(i_d) \cdot \frac{E_{on}(R_{gate})}{E_{on}(R_{gate(test)})} = E_{on}(i_d) \cdot CF_{on}(R_{gate}) \quad [14]$$

$$E_{off}(i_d, R_{gate}) = E_{off}(i_d) \cdot \frac{E_{off}(R_{gate})}{E_{off}(R_{gate(test)})} = E_{off}(i_d) \cdot CF_{off}(R_{gate}) \quad [15]$$

We include corrective factors to maintain the clarity for following calculations.

$$CF_{on}(R_{gate}) = \frac{E_{on}(R_{gate})}{E_{on}(R_{gate(test)})} \quad [16]$$

$$CF_{off}(R_{gate}) = \frac{E_{off}(R_{gate})}{E_{off}(R_{gate(test)})} \quad [17]$$

The drain to source voltage across the CoolMOS also has an effect on switching behavior. The dependence of switching losses on the drain-source voltage is almost linear **Figure 7**.

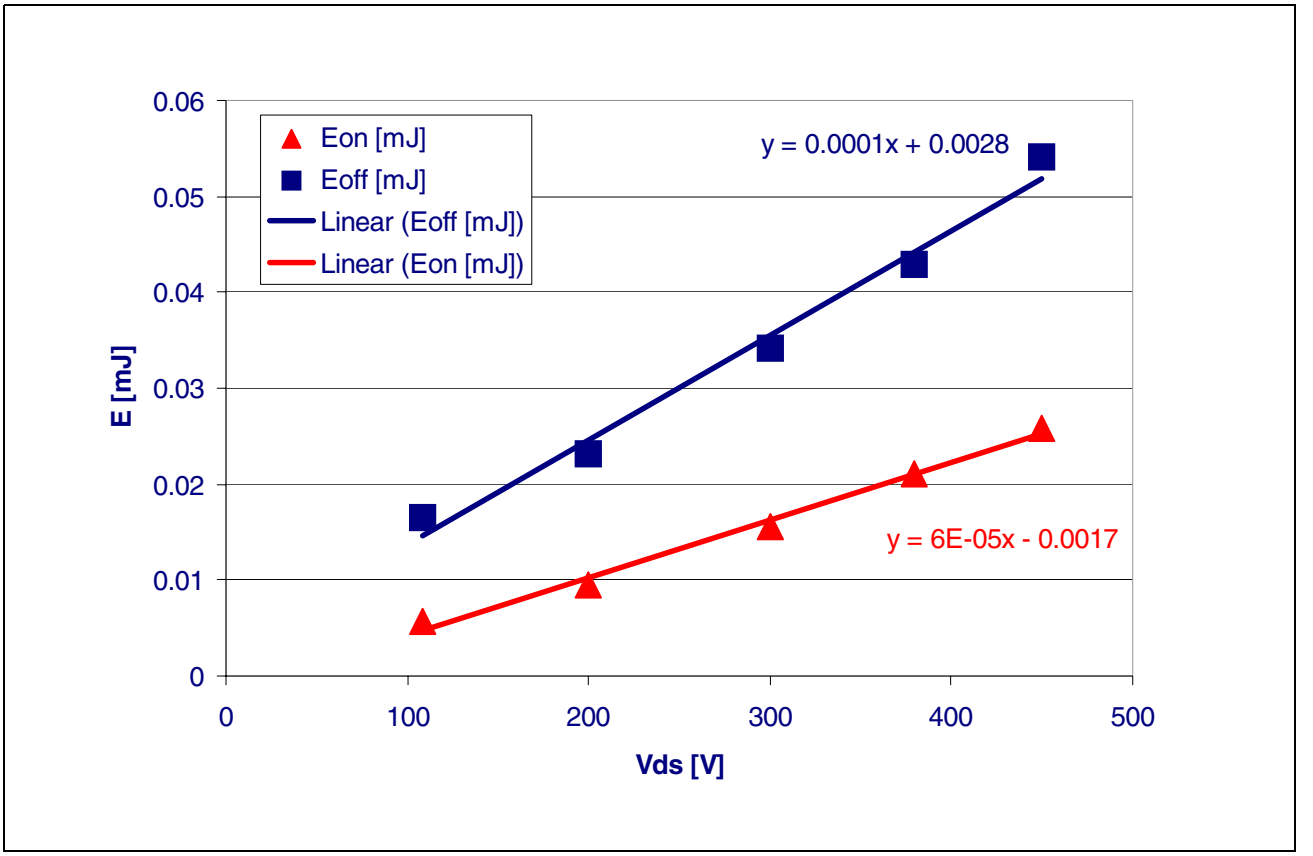


Figure 7 Switching Energy Losses vs. Drain-Source Voltage (SPP11N60C3, SDP06S60, I_d = 11 A, R_{gate} = 6.8 Ω, T_J = 125°C)

This information is not included in the datasheet due to the linearity of this dependence. We are still able to calculate the corrective factor for the switching losses, if the particular design's voltage differs from the datasheet parameters:

$$E_{on}(i_d, V_{ds(on)}) = E_{on}(i_d) \cdot \frac{E_{on}(V_{ds(on)})}{E_{on}(V_{ds(test)})} = E_{on}(i_d) \cdot \frac{6 \cdot 10^{-5} \cdot \frac{mJ}{V} \cdot V_{ds(on)} - 1.7 \cdot 10^{-3} mJ}{0.021\,mJ} = E_{on}(i_d) \cdot CF_{on}(V_{DS}(on)) \quad [18]$$

$$E_{off}(i_d, V_{ds(off)}) = E_{off}(i_d) \cdot \frac{E_{off}(V_{ds(off)})}{E_{off}(V_{ds(test)})} = E_{off}(i_d) \cdot \frac{10^{-4} \cdot \frac{mJ}{V} \cdot V_{ds(off)} + 2.8 \cdot 10^{-3}}{0.043\,mJ} = E_{off}(i_d) \cdot CF_{off}(V_{DS}(off)) \quad [19]$$

We include corrective factors to maintain the clarity for following calculations.

$$CF_{on}\left(V_{DS}(on)\right) = \frac{E_{on}\left(V_{ds(on)}\right)}{E_{on}\left(V_{ds(test)}\right)} = \frac{6\cdot 10^{-5}\cdot\frac{mJ}{V}\cdot V_{ds(on)} - 1.7\cdot 10^{-3}mJ}{0.021\,mJ} \quad [20]$$

$$CF_{off}\left(V_{DS}(off)\right) = \frac{E_{off}\left(V_{ds(off)}\right)}{E_{off}\left(V_{ds(test)}\right)} = \frac{10^{-4}\cdot\frac{mJ}{V}\cdot V_{ds(off)} + 2.8\cdot 10^{-3}}{0.043\,mJ} \quad [21]$$

Summarizing the switching energy depends on the peak current, the drain to source voltage and the gate resistance. To calculate the switching energy, the charts of the datasheet are the basis plus the correction factors for gate resistance and drain to source voltage.

$$E_{on}\left(i_d, V_{ds(on)}, R_g\right) = E_{on}\left(i_d\right)\cdot\frac{E_{on}\left(V_{ds(on)}\right)}{E_{on}\left(V_{ds(test)}\right)}\cdot\frac{E_{on}\left(R_{gate}\right)}{E_{on}\left(R_{gate(test)}\right)} = E_{on}\left(i_d\right)\cdot CF_{on}\left(V_{DS}(on)\right)\cdot CF_{on}\left(R_{gate}\right) \quad [22]$$

$$E_{off}\left(i_d, V_{ds(off)}, R_{gate}\right) = E_{off}\left(i_d\right)\cdot\frac{E_{off}\left(V_{ds(off)}\right)}{E_{off}\left(V_{ds(test)}\right)}\cdot\frac{E_{off}\left(R_{gate}\right)}{E_{off}\left(R_{gate(test)}\right)} = E_{off}\left(i_d\right)\cdot CF_{off}\left(V_{DS}(off)\right)\cdot CF_{off}\left(R_{gate}\right) \quad [23]$$

As it can be seen in **Figure 8**, the dependence of turn off energy losses on the gate-source voltage is negligibly low. Turn on behavior is dominated by the commutated diode, not by the CoolMOS. We will skip both dependencies in order to simplify the analysis.

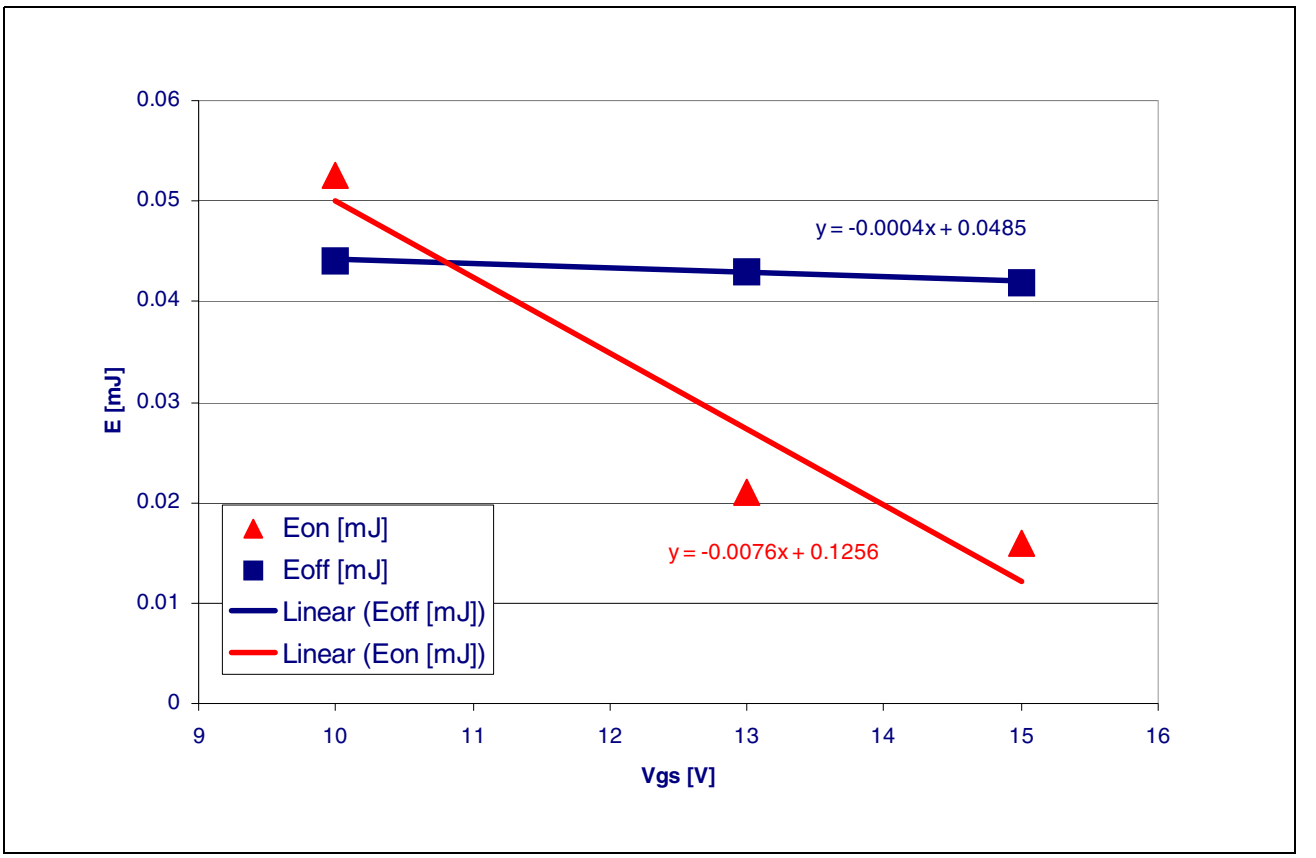
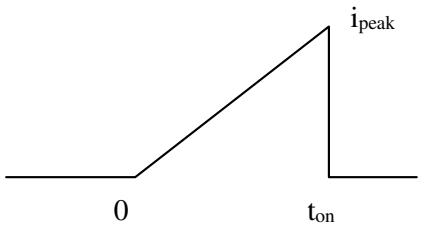


Figure 8 Switching Energy Losses vs. Gate-Source Voltage ($SPP11N60C3$, $SDP06S60$, I_d = 11 A, R_{gate} = 6.8 Ω, V_{ds} = 380 V, T_J = 125°C)

11.1 Discontinuous Conduction Mode Converter

The drain current waveform:	Mathematical expression:
	$i_d = i_{peak} \cdot \frac{t}{t_{on}}$

Turn-on energy losses is negligible:

$$E_{on} = 0 \quad [24]$$

Turn-off energy losses

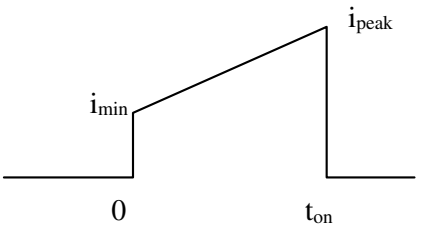
$$E_{off}\left(i_{peak}, V_{ds(off)}, R_g\right) = E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right) \quad [25]$$

Since the switching energy is proportional to V_{ds} and R_g, the result is scaled by the ratio of the actual circuit voltage and gate resistance to the test voltage and the test gate resistance in the datasheet.

Total switching power losses:

$$P_{sw} = \left(E_{on} + E_{off}\right) \cdot f = E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right) \cdot f \quad [26]$$

11.2 Continuous and Discontinuous Conduction Mode Converter

The drain current waveform:	Mathematical expression:
	$i_d = i_{\min} + \cdot \frac{i_{peak} - i_{\min}}{t_{on}} \cdot t$ In order to simplify the equations we will assume, that: $i_{min} = K_{min} \cdot i_{peak}$ This means that the minimum drain current is a fixed percentage of the peak drain current.

Turn-on energy losses:

$$E_{on}\left(i_{min}, V_{ds(on)}, R_g\right) = E_{on}\left(i_{min}\right) \cdot CF_{on}\left(V_{DS}(on)\right) \cdot CF_{on}\left(R_{gate}\right) \quad [27]$$

Since the switching energy is proportional to voltage, the result is scaled by the ratio of the actual circuit voltage to the test voltage in the datasheet.

Turn-off energy losses:

$$E_{off}\left(i_{peak}, V_{ds(off)}, R_{gate}\right) = E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right) \quad [28]$$

Since the switching energy is proportional to voltage, the result is scaled by the ratio of the actual circuit voltage to the test voltage in the datasheet.

Total switching power losses:

$$P_{sw} = \left(E_{on} + E_{off}\right) \cdot f = \begin{bmatrix} \left(E_{on}\left(i_{min}\right) \cdot CF_{on}\left(V_{DS}(on)\right) \cdot CF_{on}\left(R_{gate}\right)\right) \ \ldots \\ + \left(E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right)\right) \end{bmatrix} \cdot f \quad [29]$$

12 Total Power Losses

Total power losses for periodical signal can be calculated as the sum of conduction losses and switching losses:

$$P_{tot} = P_{cond} + P_{sw} \quad [30]$$

12.1 Discontinuous Conduction Mode Converter

$$P_{tot} = \frac{1}{3} \cdot R_{ds(ON)} \cdot {i_{peak}}^2 \cdot D + E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right) \cdot f \quad [31]$$

12.2 Continuos Current Mode Converter

$$P_{tot} = \frac{1}{3} \cdot R_{ds(ON)} \cdot D \cdot \left({i_{min}}^2 + i_{peak} \cdot i_{min} + {i_{peak}}^2\right) \ldots + \left[\left(E_{on}\left(i_{min}\right) \cdot CF_{on}\left(V_{DS}(on)\right) \cdot CF_{on}\left(R_{gate}\right)\right) + E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right)\right] \cdot f \quad [32]$$

Example for Step 4 (discontinuous conduction mode converter):

Our discontinuous conduction mode converter has following operating conditions:

i_{peak} = 2.4 A (peak drain current),

D = 0.21 (duty cycle),

f = 60 kHz (switching frequency),

R_{gate} = 12 Ω (gate resistance)

$V_{ds(on)}$ = 380 V (DC voltage between drain and source before the start of the turn-on transition, the bulk capacitor voltage),

$V_{ds(off)}$ = 480 V (DC voltage between drain and source after the end of the turn-off transition, the bulk capacitor voltage plus the flyback voltage).

The selected CoolMOS SPP04N60C3 in **Step 3** has approximately 1.9 Ω on state resistance at junction temperature of 110°C: $R_{ds(ON)}$ = 1.9 Ω. The turn off energy losses are E_{off} (i_{peak}) = 6 µJ at i_{peak} = 2.4 A and R_{gate} = 18 Ω, this information can be found in the datasheet of CoolMOS.

Due to the dependence of switching energy to drain source voltage and gate resistance, this energy must be calculated for the particular conditions of SMPS. With the charts given in **Figure 6** and **Figure 7** this calculation can be easily made. The results of this calculation are valid for an 11 A device but to calculate the switching losses for our example you have to use the ratio between the energies of SMPS and the energies determined in the test circuit. This ratio is the same for all CoolMOS devices.

$$CF_{off}\left(V_{ds}(off)\right) = \frac{10^{-4} \cdot \frac{mJ}{V} \cdot V_{ds(off)} + 2.8 \cdot 10^{-3}}{0.043\,mJ} = \frac{10^{-4} \cdot \frac{mJ}{V} \cdot 480\,V + 2.8 \cdot 10^{-3}}{0.043\,mJ} = 1.181$$

$$CF_{off}\left(R_{gate}\right) = \frac{E_{off}\left(R_{gate}\right)}{E_{off}\left(R_{gate(test)}\right)} = \frac{E_{off}\left(12\,\Omega\right)}{E_{off}\left(18\,\Omega\right)} = \frac{4.9uJ}{6.7uJ} = 0.731$$

Using this information we can calculate the total power losses:

$$P_{tot} = \frac{1}{3} \cdot 1.9\Omega \cdot (2.4A)^2 \cdot 0.21 + 6uJ \cdot 1.181 \cdot 0.731 \cdot 60 \cdot kHz = 1.077W$$

Now we know the total power losses of SPP04N60C3 in this particular design.

Step 5 Recalculate the maximum power dissipation for a selected CoolMOS type

With the available junction to case thermal resistance of selected CoolMOS device it is possible to make the calculation of maximum allowable power dissipation more precisely. This step can help to skip one of the iterations what will be explained in **Step 6**.

Example for Step 5:

The thermal resistance of the heat sink including the isolation material remains the same R_{thCA} = 40 K/W.

The thermal resistance junction to case of the SPP04N60C3 is:

R_{thJC} = 2.5 K/W.

The maximum allowed junction temperature in our case is:

T_J = 110°C.

The ambient temperature is:

T_A = 70°C

Now using the **Equation [2]** we can calculate the maximum allowable power dissipation in our case more precise:

$$P_{max} = \frac{T_J - T_A}{R_{thJC} + R_{thCA}} = \frac{110\ °C - 70\ °C}{2.5\frac{K}{W} + 40\frac{K}{W}} = 0.941\ W$$

As we can see the maximum allowable power dissipation for SPP04N60C3 is 0.941 W.

Step 6 Compare the total power losses calculated in Step 4 for a selected CoolMOS type with maximum allowable power dissipation from Step 5

At this point it is necessary to compare the total power losses calculated in step 4 with the maxi-mum allowable power dissipation resulting from the defined junction temperature and heat sink (**Step 5**).

If the total power losses from step 4 are lower than the maximum allowable power dissipation (**Step 1**), then the selected CoolMOS type meets the requirements. We did find the right type. As a further optimization it could be possible to check if the next CoolMOS type with higher $R_{ds(ON)}$ will do the same job. Repeat **Step 4**, **Step 5** and **Step 6** with this new selection.

In case of total power losses from **Step 4** are higher than the maximum allowable power dissipation (**Step 1**), select the next type from the CoolMOS family with lower on state resistance and repeat the **Step 4**, **Step 5** and **Step 6**. Another possibility would be to adjust the heat sink.

The right type is found, when the next CoolMOS with higher $R_{ds(ON)}$ does not meet the requirements.

Example for Step 6 (discontinuous conduction mode converter):

As we calculated in **Step 4** the SPP04N60C3 has total power losses of 1.077 W in this particular design. The maximum allowable power dissipation from **Step 5** is 0.941 W. This means the SPP04N60C3 does not meet the requirements of this particular design. Now we have two possibilities -selecting the next CoolMOS with lower on state resistance or adjusting the heat sink.

Example for CoolMOS type with lower $R_{ds(ON)}$ (discontinuous conduction mode converter):

Let us first select the next CoolMOS with lower $R_{ds(ON)}$ and repeat the **Step 4**, **Step 5** and **Step 6**.

Step 3 (second iteration):

We choose SPP07N60C3.

Step 4 (second iteration):

Our discontinuous conduction mode converter has following operating conditions:

i_{peak} = 2.4 A (peak drain current)

D = 0.21 (duty cycle)

f = 60 kHz (switching frequency)

R_{gate}=12 Ω (gate resistance)

$V_{ds(on)}$ = 380 V (DC voltage between drain and source before the start of the turn-on transition, the bulk capacitor voltage)

$V_{ds(off)}$ = 480 V (DC voltage between drain and source after the end of the turn-off transition, the bulk capacitor voltage plus the flyback voltage)

The CoolMOS SPP07N60C3 selected in **Step 3** has approximately 1.2 Ω on state resistance at junction temperature of 110°C: $R_{ds(ON)}$ = 1.2 Ω. The turn off energy losses is E_{off} (i_{peak}) = 7 µJ at i_{peak} = 2.4 A and R_{gate} = 12 Ω, this information can be found in the datasheet of CoolMOS.

The dependency of switching energy versed drain source voltage and gate resistance must be calculated with the formulas **[17]** and **[21]** for both correction factors. The correction factor for the gate resistance is 1, due to the condition of same used R_{gate} for the test and for this particular SMPS.

Using all this information we can calculate the total power losses:

$$P_{tot} = \frac{1}{3} \cdot 1.2\Omega \cdot (2.4A)^2 \cdot 0.21 + 7uJ \cdot 1.181 \cdot 60kHz = 0.98W$$

Step 5 (second iteration):

The thermal resistance of the heat sink including the isolation material remains the same R_{thCA} = 40 K/W.

The thermal resistance junction to case of the SPP07N60C3 is:

R_{thJC} = 1.5 K/W.

The maximum allowed junction temperature in our case is:

T_J = 110°C.

The ambient temperature is:

T_A = 70°C

Now using the **Equation [2]** we can calculate the maximum allowable power dissipation in this case more precise:

$$P_{max} = \frac{T_J - T_A}{R_{thJC} + R_{thCA}} = \frac{110\,°C - 70\,°C}{1.5\,\frac{K}{W} + 40\,\frac{K}{W}} = 0.964\ W$$

Step 6 (second iteration):

As we can see, the total power losses from **Step 4** are higher than the maximum allowable power dissipation (**Step 5**). The SPP07N60C3 is still not the right choice.

Let us now try another possibility. We will keep the SPP07N60C3, but we will slightly improve the thermal resistance of our heat sink by 3 K/W. Now we can calculate the maximum allowable power dissipation for this new heat sink (**Step 5**).

Step 5 (third iteration):

The thermal resistance of the heat sink including the isolation material is

R_{thCA} = 37 K/W.

All other parameters will remain the same.

$$P_{max} = \frac{T_J - T_A}{R_{thJC} + R_{thCA}} = \frac{110\ °C - 70\ °C}{1.5\ \frac{K}{W} + 37\ \frac{K}{W}} = 1.039\ W$$

Step 6 (third iteration):

Let us compare the total power losses from **Step 4** (second iteration) and the maximum allowable power dissipation calculated in **Step 5** (third iteration). At this point we did achieve an optimum between selected CoolMOS type and adjusted heat sink. The selection of MOSFET is done.

13 Calculation of Peak Pulse Current

As shown in the previous section, the selection of the right MOSFET type is a complicated approach, which requires many iterations. In order to reduce the number of iterations, it is useful to select the optimal CoolMOS type for the first iteration. This section shows how to calculate the peak pulse current for the particular CoolMOS type and presents useful charts for preselection.

Combining the **Equation [2]** and **[25]**, the information about the peak pulse current can be obtained.

13.1 Discontinuous Conduction Mode Converter

From the condition that the total power losses should be lower than the maximum allowable power dissipation:

$$P_{tot} \le P_{max} \qquad [33]$$

and correspondingly:

$$\frac{1}{3} \cdot R_{ds(ON)} \cdot i_{peak}^2 \cdot D + E_{off}\left(i_{peak}\right) \cdot CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right) \cdot f \le \frac{T_J - T_A}{R_{thJC} + R_{thCA}} \qquad [34]$$

The relation between peak current and switching frequency can be expressed as:

$$f \le \frac{\frac{T_J - T_A}{R_{thJC} + R_{thCA}} - \frac{1}{3} \cdot R_{ds(ON)} \cdot {i_{peak}}^2 \cdot D}{CF_{off}\left(V_{DS}(off)\right) \cdot CF_{off}\left(R_{gate}\right) \cdot E_{off}\left(i_{peak}\right)} \quad [35]$$

Now let us calculate what peak current can be handled by each particular CoolMOS C3 type, depending on the switching frequency. Due to the complexity of the equations and dependencies we will use the numeric solution. Next figure shows the peak drain current in a discontinuous conduction mode converter with following operating conditions:

D = 0.21	duty cycle
$V_{dc(in)}$ = 380 V	bulk capacitor voltage
V_r = 100 V	reflected voltage
T_J = 110°C	junction - temperature
T_A = 70°C	ambient - temperature
η = 0.8	efficiency

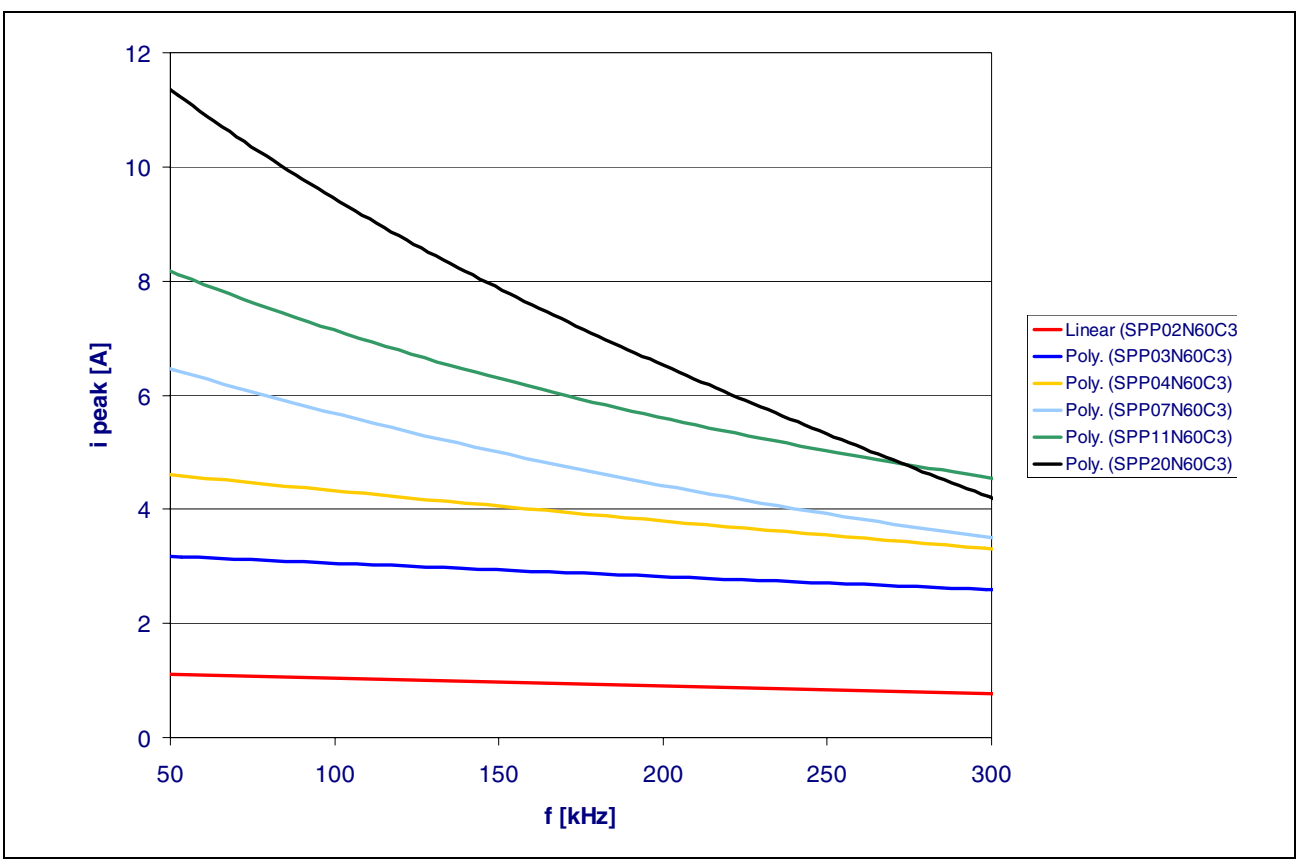


Figure 9 Peak Current Handling Capability in Discontinuous Conduction Mode Converter (external heat sink thermal resistance is 10 K/W)

13.2 Continuous Conduction Mode Converter

From the condition that the total power losses should be lower than the maximum allowable power dissipation

$$P_{tot} \leq P_{max} \quad [36]$$

and correspondingly:

$$\frac{1}{3}\cdot R_{ds(ON)}\cdot D\cdot\left(i_{min}^{\ 2} + i_{peak}\cdot i_{min} + i_{peak}^{\ 2}\right) \ldots + \left(E_{on}\left(i_{min}\right)\cdot CF_{on}\left(V_{DS}(on)\right)\cdot CF_{on}\left(R_{gate}\right) + E_{off}\left(i_{peak}\right)\cdot CF_{off}\left(V_{DS}(off)\right)\cdot CF_{off}\left(R_{gate}\right)\right)\cdot f \leq \frac{T_J - T_A}{R_{thJC} + R_{thCA}} \quad [37]$$

$$f \leq \frac{\left[\frac{T_J - T_A}{R_{thJC} + R_{thCA}} - \frac{1}{3}\cdot R_{ds(ON)}\cdot D\cdot\left(i_{min}^{\ 2} + i_{peak}\cdot i_{min} + i_{peak}^{\ 2}\right)\right]}{E_{on}\left(i_{min}\right)\cdot CF_{on}\left(V_{DS}(on)\right)\cdot CF_{on}\left(R_{gate}\right) + E_{off}\left(i_{peak}\right)\cdot CF_{on}\left(V_{DS}(on)\right)\cdot CF_{on}\left(R_{gate}\right)} \quad [38]$$

$$K_{min} = \frac{i_{min}}{i_{peak}} \quad [39]$$

Now let us calculate what peak current can be handled by each particular CoolMOS C3 type depending on the switching frequency.

Due to the complexity of the equations and dependencies the numeric solution has being used. Next figure shows the peak drain current in a continuous conduction mode converter with following operating conditions:

D = 0.45	duty cycle
$V_{dc(in)}$ = 380 V	bulk capacitor voltage
T_J = 110°C	junction - temperature
T_A = 70°C	ambient - temperature
η = 0.8	efficiency
K_{min} = 0.72	factor I_{min}, I_{max}

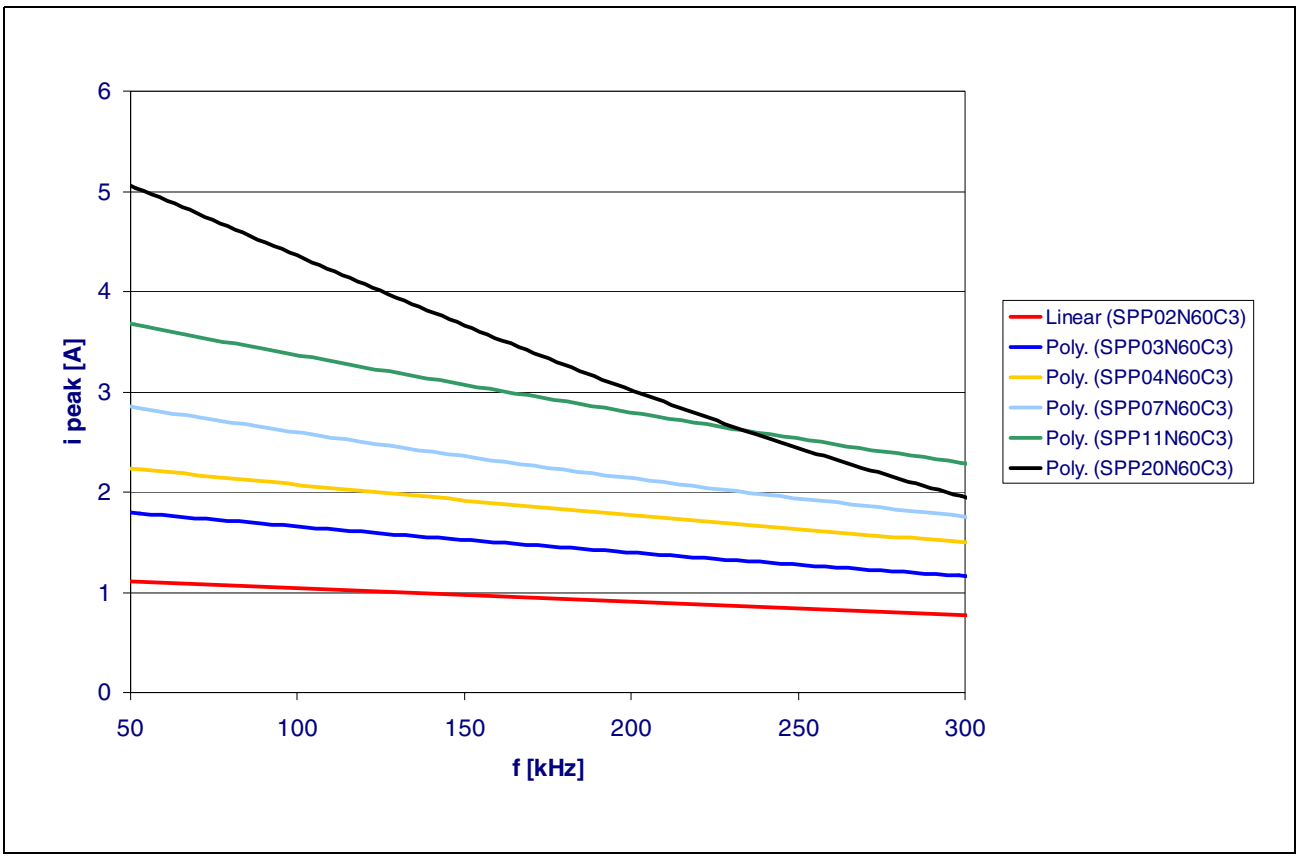


Figure 10 Peak Current Handling Capability in Continuous Conduction Mode Converter (external heat sink thermal resistance is 10 K/W)

14 Maximum Output Power Capability

14.1 Discontinuous Conduction Mode Converter

To make a first selection, which CoolMOS is best for a particular application, it is more interesting to know the output power capability for each device. But that is not a problem at all, with the formulas given in the above section because of a linear relation between the primary peak current and the output power.

Maximum output power:

$$P_{out} = \eta \cdot P_{in} = \eta \cdot V_{in(DC)} \cdot I_{in(DC)} = \eta \cdot V_{in(DC)} \cdot \frac{1}{2} \cdot i_{peak} \quad [40]$$

where η is efficiency of power converter.

Now let us calculate what output power can be handled by each particular CoolMOS C3 type, depending on the switching frequency. Due to the complexity of the equations and

dependencies we will use the numeric solution. Next figure shows the output power in a discontinuous conduction mode converter with following operating conditions:

D = 0.21	duty cycle
$V_{dc(in)}$ = 380 V	bulk capacitor voltage
V_r = 100 V	reflected voltage
T_J = 110°C	junction - temperature
T_A = 70°C	ambient - temperature
η = 0.8	efficiency

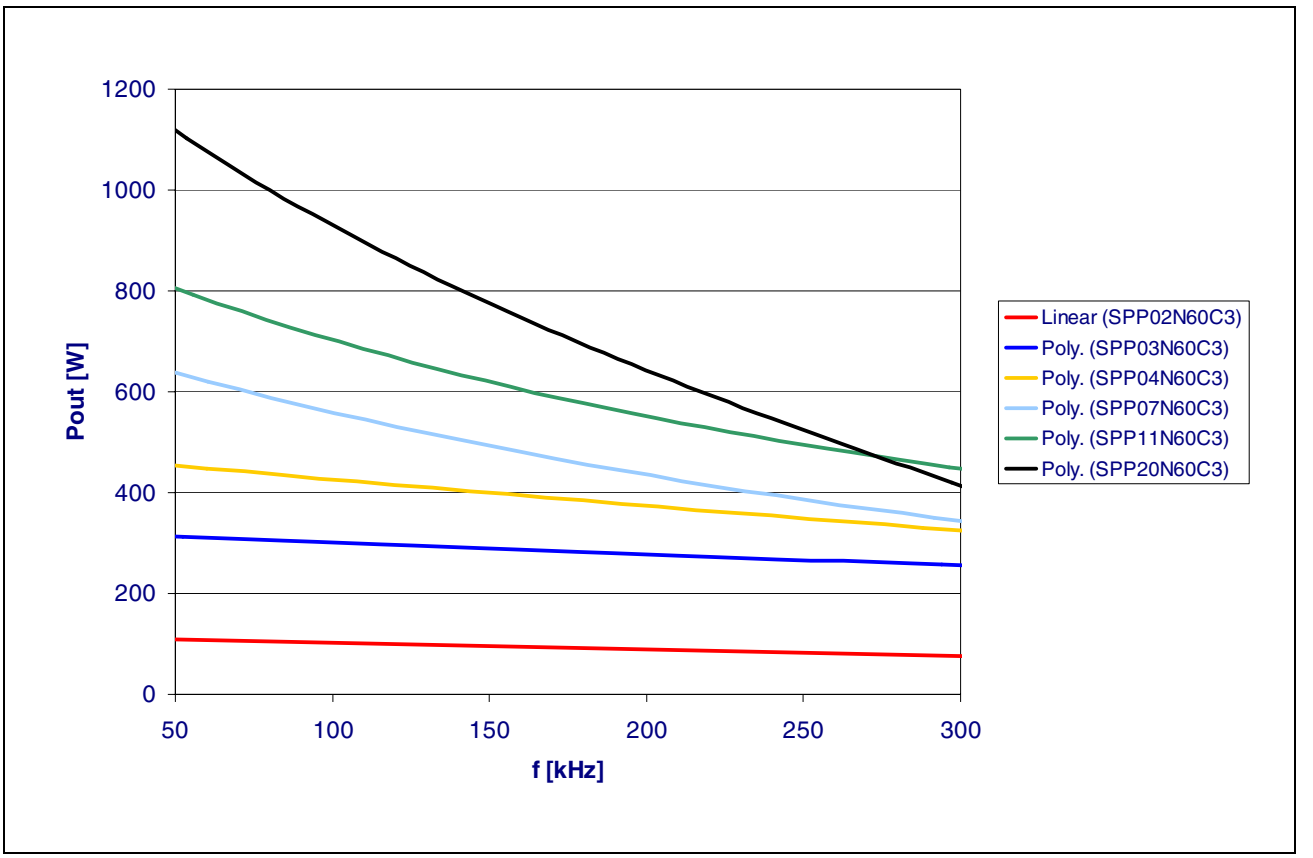


Figure 11 Power Handling Capability in Discontinuous Conduction Mode Converter (external heat sink thermal resistance is 10 K/W)

14.2 Continuous Conduction Mode Converter

For a continuous conduction mode converter exists also a linear relation between the primary peak current and the output power of the SMPS. We can also use the formulas for the peak pulse current for continuous conduction mode converter, and multiply them with a linear transformation factor in order to achieve a diagram, where the ratio between the power handling capability and the frequency are shown.

Maximum output power:

$$P_{out} = \eta \cdot P_{in} = \eta \cdot V_{in(DC)} \cdot I_{in(DC)} = \eta \cdot V_{in(DC)} \cdot \frac{1}{2} \cdot \left(i_{min} + i_{peak} \right) \cdot D \quad [41]$$

where η is efficiency of power converter.

Now let us calculate what output power can be handled by each particular CoolMOS C3 type depending on the switching frequency. Due to the complexity of the equations and dependencies we will use the numeric solution. Next figure shows the output power in a continuous conduction mode converter with following operating conditions:

D = 0.45	duty cycle
$V_{dc(in)}$ = 380 V	bulk capacitor voltage
T_J = 110°C	junction - temperature
T_A = 70°C	ambient - temperature
η = 0.8	efficiency
K_{minn} = 0.72	factor I_{min}, I_{max}

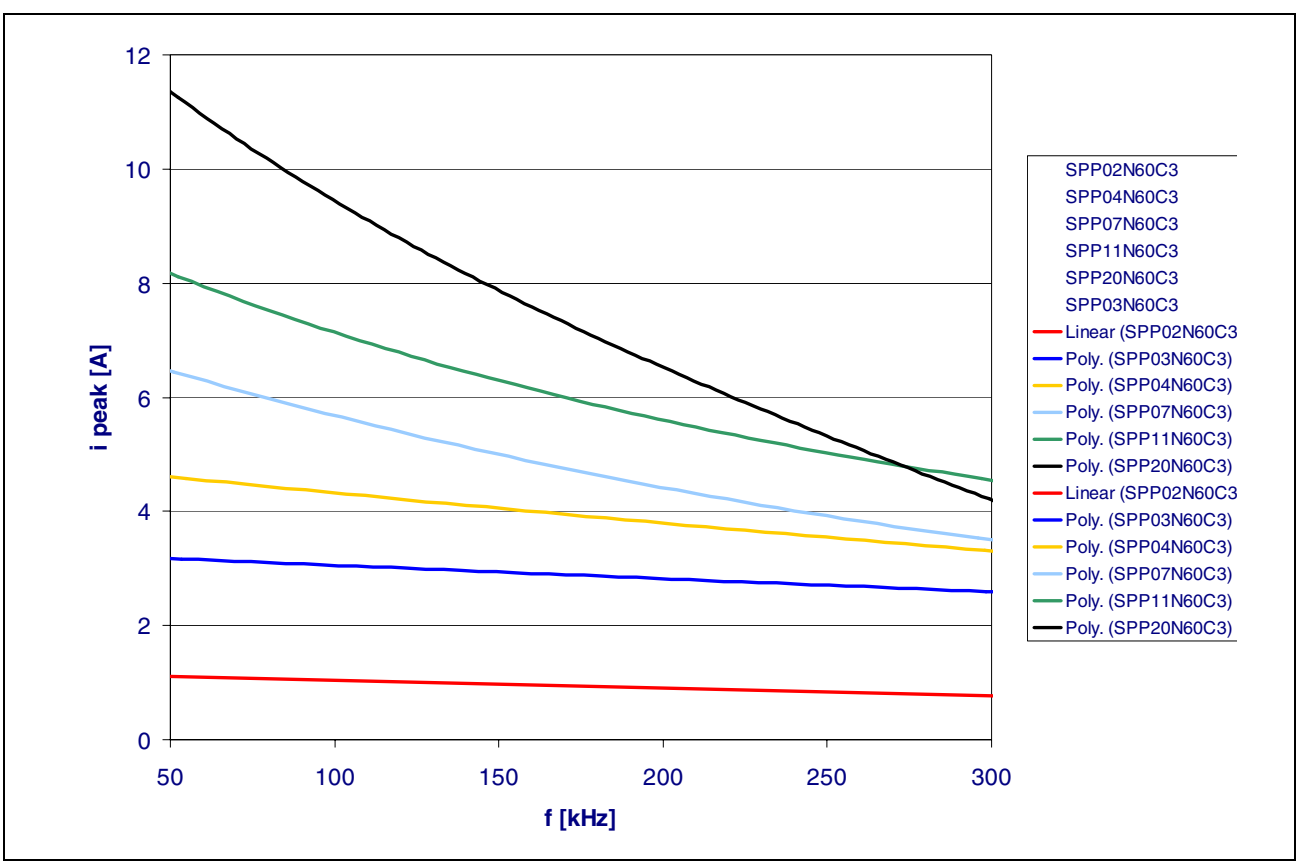


Figure 12 Power Handling Capability in Continuous Conduction Mode Converter (external heat sink thermal resistance is 10 K/W)

15 Conclusion

Due to different MOSFET technologies from several semiconductor manufacturers and significant differences in the way the datasheet is done selecting the right MOSFET for the particular design becomes a complicated task. This application note shows a way to design in the CoolMOS in continuous and discontinuous conduction mode converters.

The introduced iteration approach is based on the calculation of the power losses in the transistor itself. The power losses could be divided into two main parts, the conduction losses and the switching losses. Conduction losses depend on the on state resistance and are simple to calculate. Whereas the switching losses can be influenced by a lot of parameters like nonlinear output drain-source capacitance, total gate resistance, parasitic inductances and capacitances of the circuit layout. These are difficult to handle. Calculation of the switching losses mentioned in this application note are based on measured values.

The cooling condition of the system and the heat sink design limits the maximum allowable power dissipation of the MOSFET in an SMPS. Based on this limitation and on the calculated power losses it is possible to select an optimal transistor type.

Drain current versus the switching frequency charts, as well as output power versus the switching frequency charts can be used as a pre-selection of the MOSFET type for discontinuous and continuous conduction mode converters. It is possible to skip some initial iterations using these charts.

The described approach helps to reduce the number of experimental iterations and thus reduce the design cycle time.

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