The new OptiMOS™ 5 150 V

Optimized parameters and advantages in the application

About this document

Scope and purpose

The new OptiMOS™ 5 150 V shows several improvements. As a result of deep investigations before starting the development process significant MOSFET parameters are now optimized.
These 5 main parameters and the impact in the application are shown in this application note

Intended audience

Power supply design engineers

Table of contents

About this document . . . 1

Table of contents . . . 1

1 Introduction . . . 2

2 ON resistance $R_{DS(on)}$ . . . 3

3 Figures-of-Merit (gate) . . . 5

3.1 Figure of FOM_g and FOM_{gd} . . . 5

3.2 Figure-of-Merit output charge FOM_{oss} . . . 5

4 Gate threshold voltage V_{GSth} . . . 6

5 Reverse recovery charge Q_{rr} . . . 7

6 Summary . . . 9

Trademarks . . . 10

Please read the Important Notice and Warnings at the end of this document

1 Introduction

In general, before developing a new silicon technology, it is important to clarify which MOSFET properties might be changed, or improved, to provide significant added value to the customer. A great challenge in this process is the variety of possible applications which have to be considered individually. The best-known and most frequently applied method is chip shrinking. This is an attempt to fit the important component parameters onto a smaller silicon area and thus reduce the manufacturing costs. In the past, new silicon technologies were optimized particularly in terms of the following parameters:

1) ON resistance $R_{DS(on)}$. This determines the losses during the ON time

2) Figures-of-Merit (FOM_g and FOM_{gd}). These parameters are instrumental in describing the driving losses

3) Figure-of-Merit output charge FOM_{OSS}. This is a significant part of the switching losses

4) Threshold voltage $V_{(GS)th}$. It describes at which gate-source voltage the MOSFET starts to conduct

The experiences from the last MOSFET generations and the evaluations of the target applications were considered during the development of the new OptiMOS™ 5 150 V. In addition, their requirements were integrated into the development with a high priority. A fifth component parameter was identified as particularly important here:

5) The so-called reverse-recovery charge Q_{rr}

This parameter does more than just describe the important property of the body diode of the power MOSFET. In many applications, a high reverse recovery charge Q_{rr} leads to EMC problems, increased stress on the components and, if no suitable countermeasures are taken, potentially even to problems with the thermal management. The conventional remedy is to reduce the switching speed by increasing the external gate resistor, but this usually results in a significant increase in the switching losses. This would require a more complex and therefore more expensive thermal management. It might even reduce the lifespan of the entire assembly.

The following chapters describe the improvements and benefits of the new technology. The last chapter focuses on the "Q_{rr}" in detail.

2 ON resistance $R_{DS(on)}$

A direct comparison between the OptiMOS^{TM} 3 and the new OptiMOS^{TM} 5 in terms of the product of the ON resistance and the (active) chip area ($R_{DS(on)}$*A) shows a significant improvement, i.e. the resulting $R_{DS(on)}$ is up to 25 percent lower with the same chip area (Fig. 1)

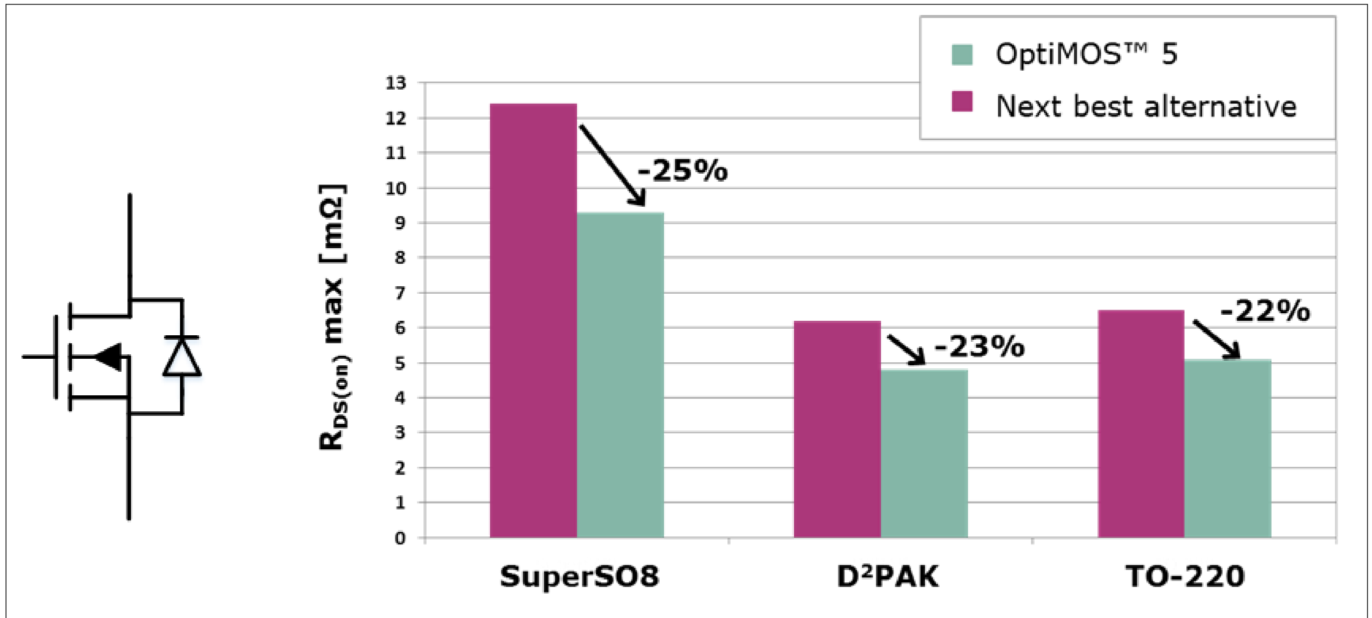


Figure 1 **$R_{DS(on)}$ reduction with OptiMOS^{TM} 5 150 V**

Benefits in the application are:

1) Considering the same package, the ON losses can be reduced by up to 25 percent compared to the next best alternative

2) Depending on the application, it is now possible to use a smaller package (e.g. SuperSO8 instead of a D^{2}PAK)

3) Where appropriate, it is possible to eliminate a through-hole device (THD), such as the TO-220; instead SMD packages such as the D^{2}PAK or even SuperSO8 can be used

4) MOSFETs often have to be connected in parallel to reduce the resulting drain-source ON resistance. The OptiMOS^{TM} 5 150 V makes it possible to either reduce the amount of paralleled MOSFETs or entirely avoid the parallel connection. The OptiMOS^{TM} 5 150 V, therefore, may result in less required space and a better cost position

5) Compared to its predecessor OptiMOS^{TM} 3, the OptiMOS^{TM} 5 has a smaller chip, with its corresponding cost benefits, while the $R_{DS(on)}$ is unchanged

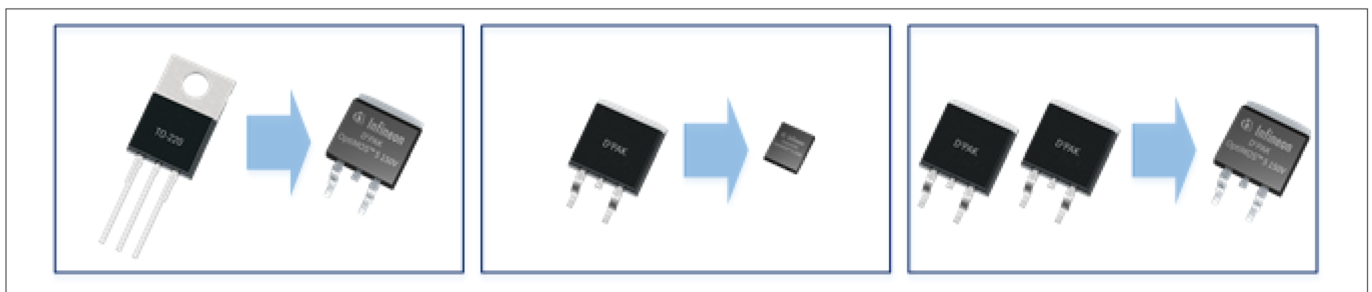


Figure 2 **Package optimization with OptiMOS^{TM} 5 150 V**

Another possibility for optimizing the circuit occurs in cases where a full-bridge rectification with 75 V, or 80 V, MOSFETs on the secondary side of the power supply is required due to the ON losses (Fig. 2). The greatest

disadvantage of this full-bridge rectification (the use of high-side or half-bridge drivers) can now be avoided. The low $R_{DS(on)}$ of the OptiMOS^{TM} 5 150 V enables a simple and less expensive solution that exclusively uses low-side switches and the correspondingly less expensive drivers.

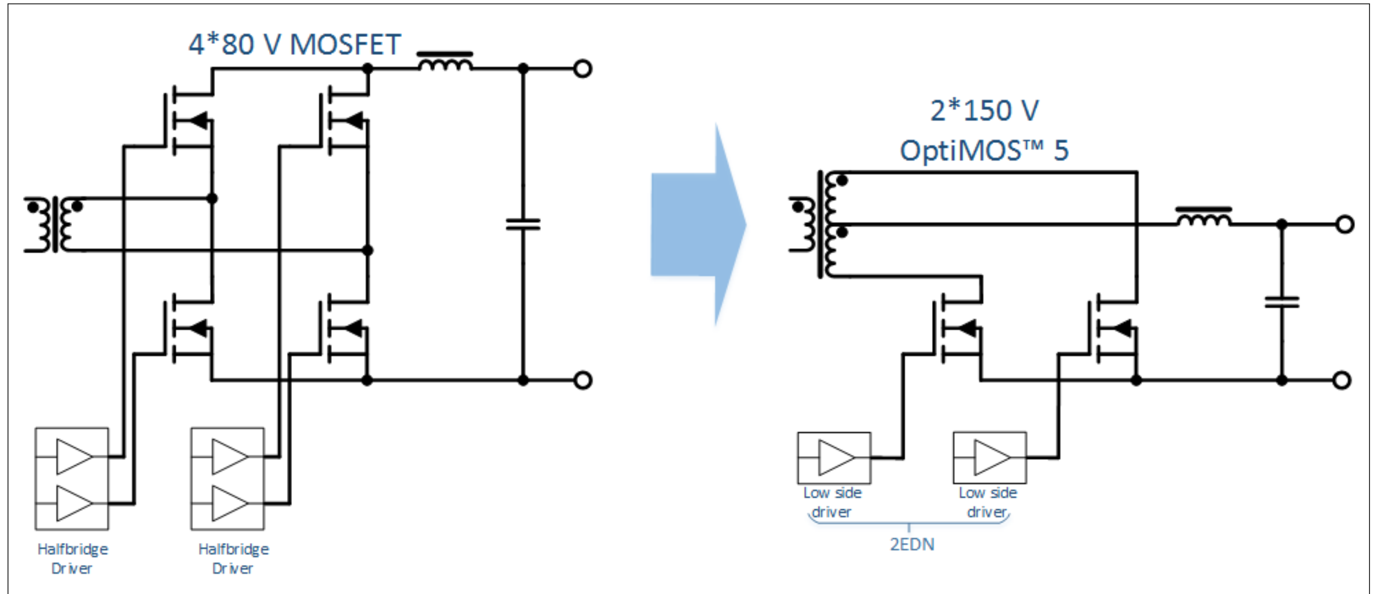


Figure 3 Reduced complexity and number of parts with OptiMOS^{TM} 5 150 V

3 Figures-of-Merit (gate)

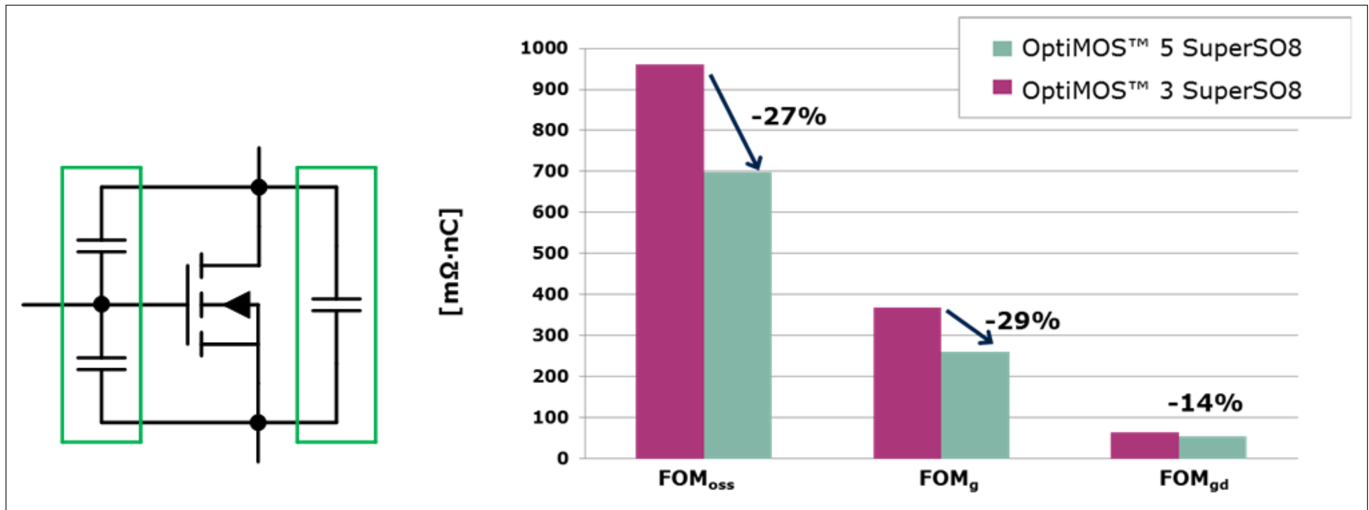


Figure 4 Reduced Figure-of-Merit output charge FOM_{OSS}, gate total charge FOM_g and gate drain charge FOM_{gd}

3.1 Figure of FOM_g and FOM_{gd}

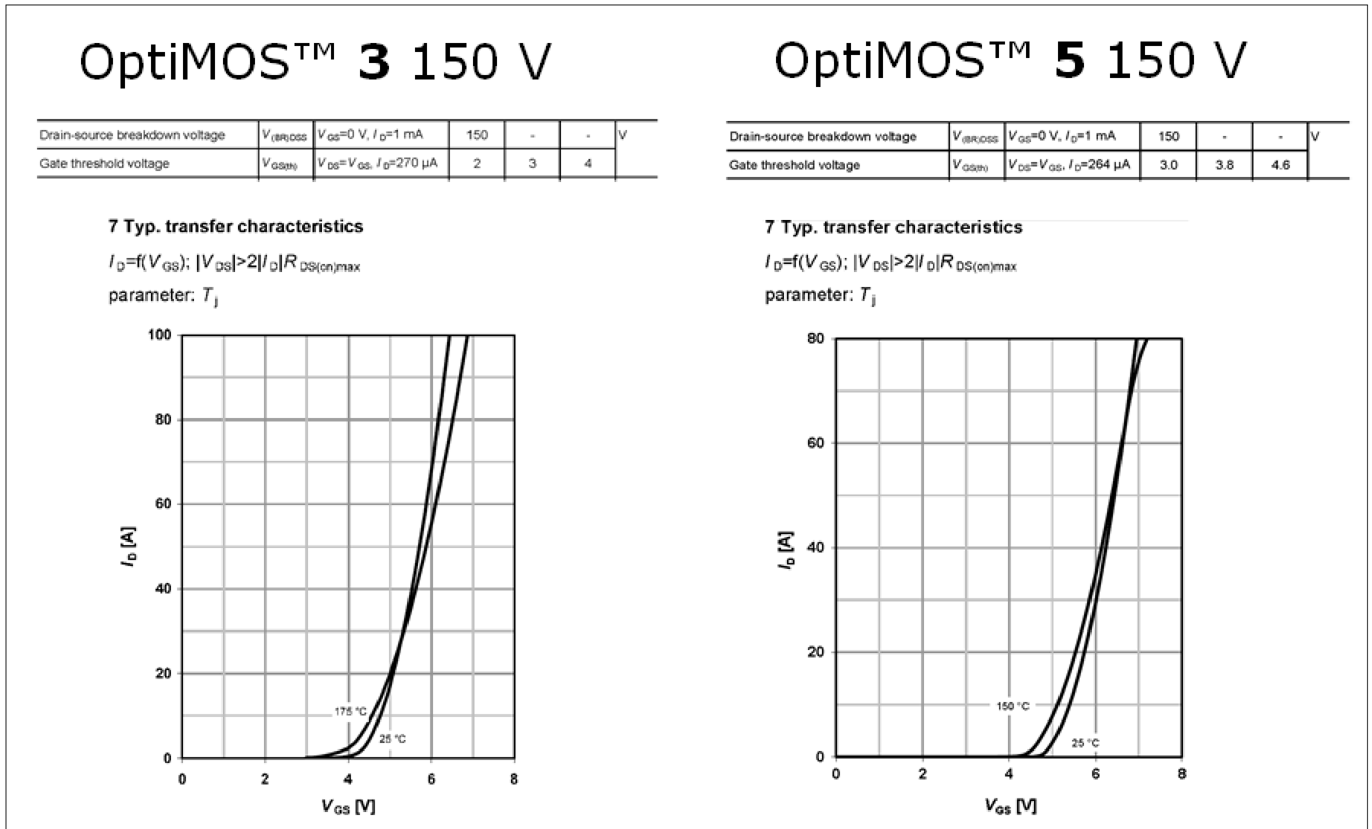
One option for increasing the efficiency level of a power supply is the reduction of the switching times. For the same driver circuit, a lower gate charge results in faster switching with correspondingly lower switching losses. At higher switching frequencies, the energy required to drive the MOSFET is no longer negligible. After all, the driver circuit not only has to supply it but also convert it into heat. With the OptiMOS™ 5 150 V, the driver is less impacted by the resulting lower temperature, which also reduces the probability of failure for the entire assembly.

3.2 Figure-of-Merit output charge FOM_{oss}

The MOSFET output capacitance is charged in every switching cycle. The stored energy in it generally cannot be used and creates a significant portion of the switching losses. If an OptiMOS™ 3 is now replaced by an OptiMOS™ 5 with the same $R_{DS(on)}$, precisely these losses are reduced. This can lead to a higher efficiency and a reduction of the load on the components with the resulting positive effects on the failure probability.

4 Gate threshold voltage V_{GSth}

The gate threshold voltage specifies when a defined drain-source current should flow. For logic-level MOSFETs, this value is usually between about 1 V and 2 V and for normal-level MOSFETs generally between 2 V and 4 V. The lower this value, the higher is the danger of an unwanted induced turn-on of the MOSFET with increased losses or even a destruction of the MOSFET. To reduce this risk, the threshold voltage was set significantly higher in the OptiMOS™ 5 150 V. The guaranteed minimum value, for example in the IPB044N15N5 (D^2PAK with 4.4 mΩ), is now at 3 V with a maximum value of 4.6 V.



OptiMOS™ 3 150 V

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	150	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=270 µA	2	3	4	

OptiMOS™ 5 150 V

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	150	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=264 µA	3.0	3.8	4.6	

Figure 5 Gate threshold voltages and transfer characteristics IPB065N15N3 G (left) and IPB044N15N5

5 Reverse recovery charge Q_{rr}

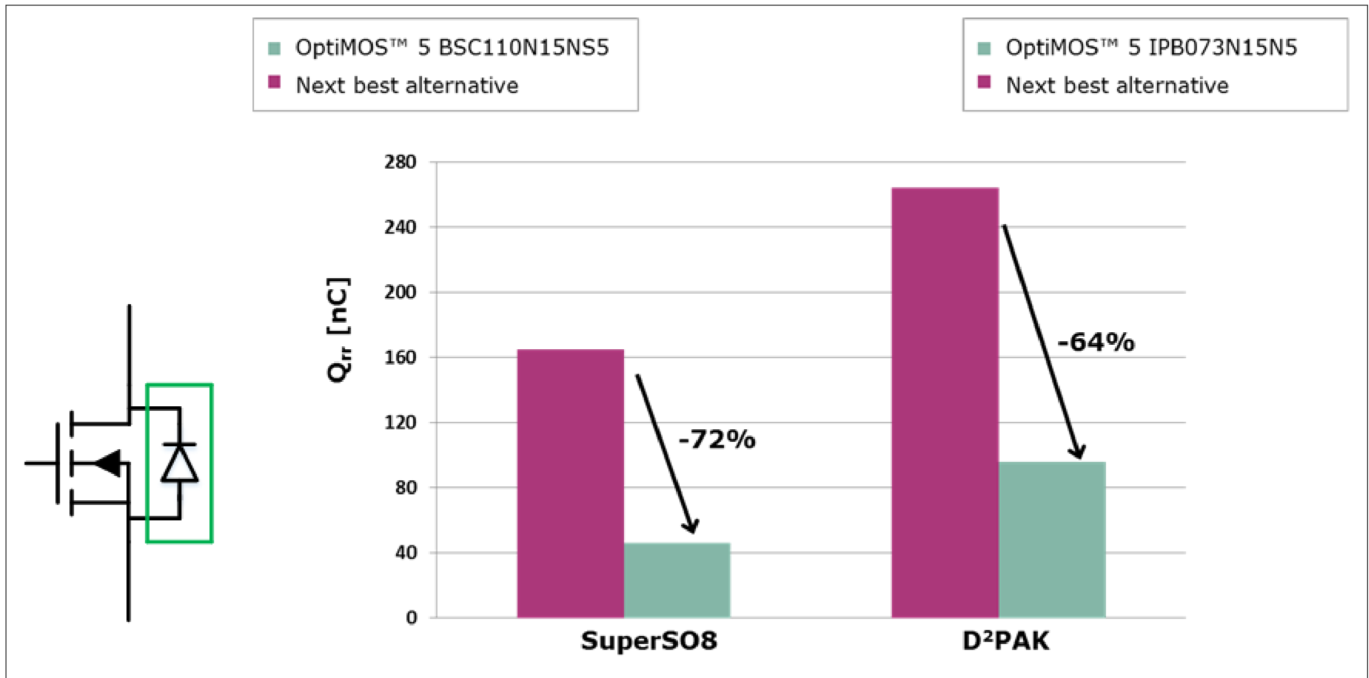


Figure 6 Reduced reverse recovery charge Q_{rr}

If the $R_{DS(on)}$ losses can still be calculated easily, the switching losses deserve closer consideration. They can be calculated by means of the voltage/current product. The current and voltage curve are easy to determine and when the switching frequency is included it is possible to specify the switching losses. In theory, these switching losses can be reduced when the switching times are shortened by reducing the gate resistor. This is not always possible in practice because other factors prohibit it. In applications with commutation of the body diode, the so-called reverse recovery charge Q_{rr} also has to be eliminated along with the operating current. This does not concern only SMPS topologies; in low voltage drives applications, it is usually necessary to block a (conducting) body diode as well.

This is most easily seen during the free-wheeling phase of a synchronous buck converter.

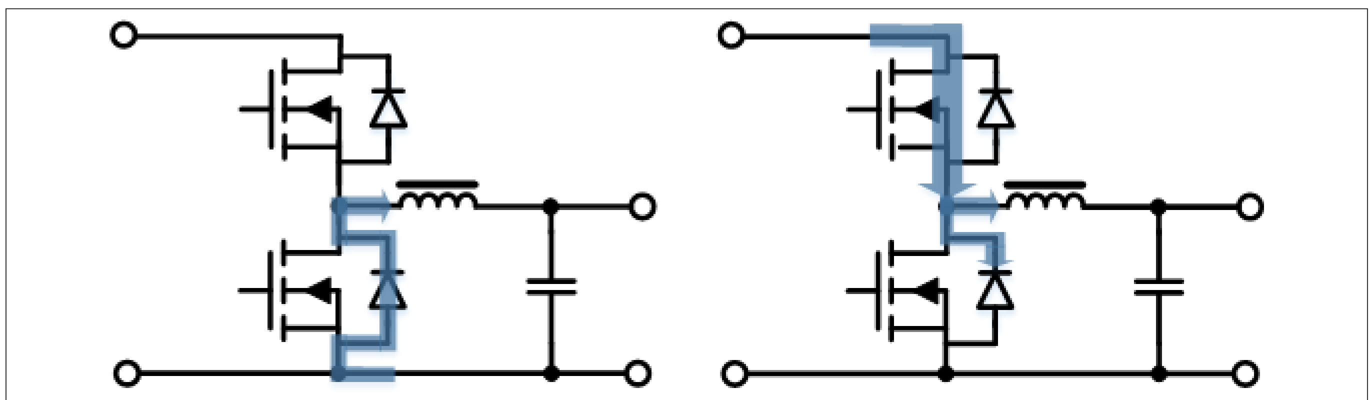


Figure 7 Reduced stress to the semiconductors due to the optimized reverse recovery charge Q_{rr}

First the current flows in the low-side MOSFET in the direction of the diode. Then the MOSFET is switched ON, which bypasses the body diode; the losses are therefore initially purely $R_{DS(on)}$ losses. Shortly before the high-side MOSFET is turned on, the channel of the low-side MOSFETs has to be turned off, even if usually for much less than a microsecond. During that time (left side in Fig. 7), the freewheeling current is diverted entirely to the body diode of the low-side MOSFET. If the high-side MOSFET is now switched on (right side in Fig. 7), it not only

has to take over the load current but also block the diode and depletes the reverse recovery charge Q_{rr}. The operating current is increased by the reverse recovery of the body diode, which in cases of higher switching speeds can even have significantly higher peak than the actual load current. This does not just result in a higher stress on the switching high-side MOSFET but potentially also in EMC problems due to the steep slopes.

The conventional practice now is to increase the external gate resistor of the MOSFET and thus reduce the switching speed. However, this results in increased switching losses in the MOSFET with the corresponding effects on the thermal management and the reliability of the assembly. The same problem can also be found in other applications wherever a conducting body diode is commutated. This includes, for example, synchronous rectifiers and motor inverters. In the OptiMOS™ 5 150 V, this reverse recovery charge has been significantly reduced. In practice, this means that with the same $R_{DS(on)}$, the external gate resistor can be much smaller compared to that used with the OptiMOS™ 3 150 V. The direct and visible result of this measure is a reduction of the switching losses.

6 Summary

The OptiMOS^{TM} 5 150 V has been significantly improved in comparison to its predecessor, the OptiMOS^{TM} 3. Not only was the $R_{DS(on)}$ substantially reduced, but also the parameters Figures-of-Merit FOM_g, FOM_{gd} and FOM_{oss}, which are instrumental for the switching speed, were optimized.

The behavior of the body diode was substantially improved by the drastically reduced reverse recovery charge Q_{rr}, with the corresponding positive effects on the EMC behavior and the efficiency. The OptiMOS^{TM} 5 150 V can thus lead to a reduction in development time and costs. In addition, the OptiMOS^{TM} 5 150 V enables easier thermal management with reduced stress on the components.

Trademarks of Infineon Technologies AG

µHVIC™, µIPM™, µPFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolDP™, CoolGaN™, COOLiR™, CoolMOS™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDrivIR™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOS™, ORIGA™, PowIRaudio™, PowIRStage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOC™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™.

Trademarks Update 2015-12-22

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2016-10-11

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2016 Infineon Technologies AG

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-hpb1474546701148

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury