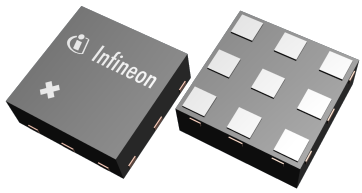
BGA10M1MN9

Mid-Band Low Noise Amplifier with Gain Steps and MIPI Control

Features

- Operating frequencies: 1.8 - 2.2 GHz
- Insertion power gain: 20.6 dB
- Low noise figure: 0.85 dB
- Low current consumption: 6.2 mA
- Support of 1.2 V and 1.8 V V_{DD}/V_{IO}
- Integrated DC block capacitors at input and output
- MIPI RFFE 3.0



1.1 x 1.1 mm^2

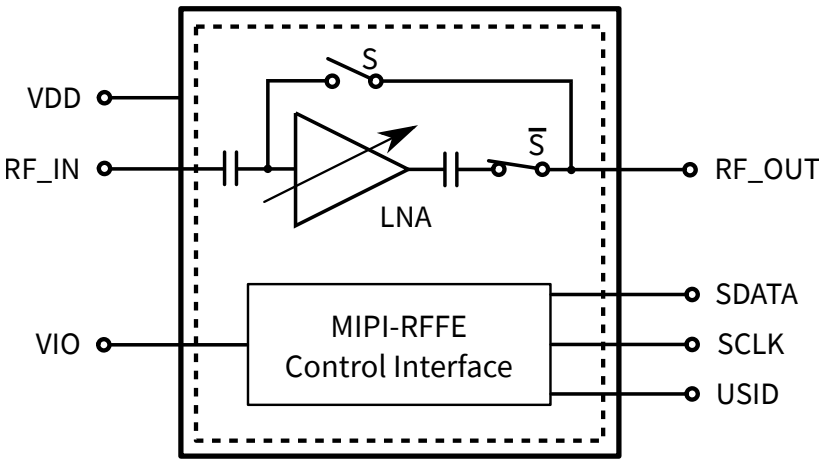
Potential Applications

The BGA10M1MN9 is designed for 4G and 5G applications covering 3GPP Bands between 1.8 and 2.2 GHz (e.g. B1 and B3). As a result of high gain and an ultra-low Noise Figure performance of the LNA frontend losses can be compensated and the data rate can be significantly improved. The MIPI interface provides a comprehensive control over multiple gain modes and bias modes to increase the overall system dynamic range.

Product Validation

Fully qualified according to JEDEC for Industrial Applications.

Block Diagram



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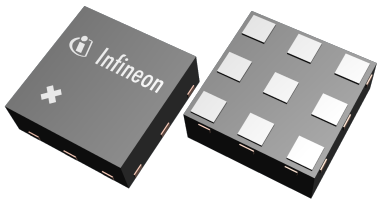
1 Features



- Frequency range from 1.8 to 2.2 GHz
- Power gain: 20.6 dB
- Low noise figure: 0.85 dB
- Low current consumption: 6.2 mA
- Gain mode support for MediaTek, LSI and Qualcomm platforms
- MIPI RFFE 3.0
- RF output internally matched to 50 Ω
- Support of 1.2 V and 1.8 V V_{DD}/V_{IO}
- Software programmable MIPI RFFE USID
- 4 USIDs supported
- Small form factor 1.1 mm x 1.1 mm
- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

2 Product Description

The BGA10M1MN9 is a low noise amplifier for LTE and 5G which covers a wide frequency range from 1.8 GHz to 2.2 GHz. The LNA provides up to 20.6 dB gain and 0.85 dB noise figure at a current consumption of 6.2 mA in the application configuration described in Chapter 7. Multiple gain modes allow adjustment of gain and linearity to increase the system dynamic range and to accommodate to changing interference scenarios. The BGA10M1MN9 supports ultra-low bypass current of 2 µA and 1.2 V operating voltage to reduce power consumption. It operates from 1.1 V to 2.0 V supply voltage over temperature. The compact 9 pin TSNP-9 package with the dimension of 1.1 x 1.1 mm^2 helps to save space on the PCB.

Product Name	Marking	Package
BGA10M1MN9	E	TSNP-9-2 / TSNP-9-6

3 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage VDD	V_{DD}	-0.5	–	2.2	V	[1]
Voltage at RF_IN	V_{RF_IN}	0	–	V_{DD}	V	
Voltage at RF_OUT	V_{RF_OUT}	0	–	0	V	–
Current into pin VDD	I_{DD}	–	–	9.2	mA	–
RF input power	P_{IN}	–	–	25	dBm	CW signal, VSWR 10:1, tested at device level, V_{DD} typ., 25 °C, for 30 s and all modes[2]
Total power dissipation	P_{tot}	–	–	20	mW	
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-30	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
ESD robustness, HBM	V_{ESD_HBM}	-2000	–	2000	V	[3]
ESD robustness, CDM	V_{ESD_CDM}	-1000	–	1000	V	[4]
RFFE Supply Voltage	V_{IO}	-0.5	–	2.2	V	–
RFFE Supply Voltage Levels	V_{SCLK}, V_{SDATA}, V_{USID}	-0.7	–	V_{IO} + 0.7 (max. 2.2)	V	–

[1] All voltages refer to GND-Nodes unless otherwise noted
[2] RF input power higher than +10 dBm exceeding operating range
[3] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[4] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

4 DC Characteristics

Table 3: DC Characteristics at T_A = 25 °C

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	1.1	1.2	2.0	V	–
Supply Current[2]	I_{DD}	4.7	6.2	7.7	mA	Bias 5, for G10 and G9 mode
		3.4	4.4	5.4	mA	Bias 3, for G8 and G7 mode
		2.6	3.6	4.6	mA	Bias 2, for G6 and G3A mode
		2.0	2.8	3.6	mA	Bias 1, for G5 mode
		1.3	1.9	2.5	mA	Bias 0, for G4 mode
		–	2	3	µA	Bypass mode (all bias)
RFFE supply voltage range 1	V_{IO}	1.1	1.2	1.3	V	–
RFFE supply voltage range 2	V_{IO}	1.65	1.8	1.95	V	–
RFFE supply current	I_{VIO}	–	2	5	µA	Idle State
RFFE input high voltage[3]	V_{IH}	0.7 * V_{IO}	–	V_{IO}	V	Logical "1"
RFFE input low voltage[3]	V_{IL}	0	–	0.3 * V_{IO}	V	Logical "0"
RFFE output high voltage[4]	V_{OH}	0.8 * V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[4]	V_{OL}	0	–	0.2 * V_{IO}	V	–
RFFE control input capacitance	C_{SCLK_IN}, C_{SDATA_IN}	–	–	2	pF	–
RFFE control load capacitance	C_{SDATA_L}	–	–	80	pF	–
RFFE SCLK write frequency	f_{SCLK_W}	0.032	–	52	MHz	–
RFFE SCLK read frequency	f_{SCLK_R}	0.032	–	26	MHz	–

[1] Based on the application described in Chapter 7
[2] V_{DD} = 1.2 V
[3] SCLK, SDATA and USID
[4] SDATA

5 RF Characteristics

Table 4: RF Characteristics in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, f = 1.8 – 2.2 GHz, bias settings according to Table 3

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain f = 2100 MHz	$\|S_{21}\|^2$	19.1	20.6	22.1	dB	G10
		16.1	17.6	19.1	dB	G9
		12.8	14.3	15.8	dB	G8
		9.9	11.4	12.9	dB	G7
		6.9	8.4	9.9	dB	G6
		4.6	6.1	7.6	dB	G5
		-1.7	-0.2	1.3	dB	G4
		-4.1	-2.6	-1.1	dB	G3A (Active bypass)
		-3.7	-2.7	-1.7	dB	G3 (Passive bypass)
		-6.9	-5.9	-4.9	dB	G2
		-12.8	-11.8	-10.8	dB	G1

Continued on next page

RF Characteristics

Table 4: RF Characteristics – Continued from previous page

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Noise Figure f = 2100 MHz	NF	–	0.85	1.4	dB	G10
		–	0.9	1.5	dB	G9
		–	1.0	1.6	dB	G8
		–	1.1	1.7	dB	G7
		–	1.35	2.0	dB	G6
		–	4.7	5.3	dB	G5
		–	5.3	5.9	dB	G4
		–	9.6	10.2	dB	G3A (Active bypass)
		–	2.7	3.7	dB	G3 (Passive bypass)
		–	5.9	6.9	dB	G2
		–	11.8	12.8	dB	G1
Input Return Loss[1] f = 2100 MHz	RL_{in}	4	6	–	dB	G10
		4	6	–	dB	G9
		6	8	–	dB	G8
		5	7	–	dB	G7
		6	8	–	dB	G6
		6	8	–	dB	G5
		5	7	–	dB	G4
		6	8	–	dB	G3A (Active bypass)
		7	10	–	dB	G3 (Passive bypass)
		10	18	–	dB	G2
		7	10	–	dB	G1
Output Return Loss f = 2100 MHz	RL_{out}	10	19	–	dB	G10
		10	19	–	dB	G9
		10	21	–	dB	G8
		10	19	–	dB	G7
		9	12	–	dB	G6
		10	22	–	dB	G5
		9	12	–	dB	G4
		9	12	–	dB	G3A (Active bypass)
		7	9	–	dB	G3 (Passive bypass)
		7	10	–	dB	G2
		10	18	–	dB	G1

Continued on next page

[1] Can be tuned by using additional external matching components

RF Characteristics

Table 4: RF Characteristics – Continued from previous page

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse Isolation f = 2100 MHz	$1/\lvert S_{12}\rvert^2$	37	42	–	dB	G10
		38	43	–	dB	G9
		31	36	–	dB	G8
		33	38	–	dB	G7
		35	40	–	dB	G6
		31	36	–	dB	G5
		35	40	–	dB	G4
		35	40	–	dB	G3A (Active bypass)
		1.7	2.7	–	dB	G3 (Passive bypass)
		4.9	5.9	–	dB	G2
		10.8	11.8	–	dB	G1
Inband input 1dB-compression point f = 2100 MHz	IP_{1dB}	-24	-20	–	dBm	G10
		-23	-19	–	dBm	G9
		-18	-14	–	dBm	G8
		-18	-14	–	dBm	G7
		-17	-13	–	dBm	G6
		-10	-6	–	dBm	G5
		-8	-4	–	dBm	G4
		-7	-3	–	dBm	G3A (Active bypass)
		+2	+6	–	dBm	G3 (Passive bypass)
		0	+4	–	dBm	G2
		+2	+6	–	dBm	G1
Inband input 3rd-order intercept point[1]	$IIP3$	-12	-7	–	dBm	G10, P_{IN} = -40 dBm for each tone
		-12	-7	–	dBm	G9, P_{IN} = -40 dBm for each tone
		-6	-1	–	dBm	G8, P_{IN} = -32 dBm for each tone
		-6	-1	–	dBm	G7, P_{IN} = -32 dBm for each tone
		-7	-2	–	dBm	G6, P_{IN} = -30 dBm for each tone
		-1	+4	–	dBm	G5, P_{IN} = -25 dBm for each tone
		-4	+1	–	dBm	G4, P_{IN} = -25 dBm for each tone
		+2	+7	–	dBm	G3A, P_{IN} = -14 dBm for each tone
		+17	+22	–	dBm	G3, P_{IN} = -20 dBm for each tone
		+14	+19	–	dBm	G2, P_{IN} = -9 dBm for each tone
		+15	+20	–	dBm	G1, P_{IN} = -5 dBm for each tone
Phase discontinuity between all Gain Mode combinations f = 2100 MHz		-5	–	5	°	Part to part variation after compensation in Base Band with constant value
Stability	k	> 1	–	–	–	f = 1 MHz - 10 GHz

[1] f_1 = 2100 MHz, $f_2 = f_1$ + 2 MHz

6 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the ’MIPI Alliance Specification for RF Front-End Control Interface version 3.0 - 1 December 2019’ as well as the ’Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)’.

Table 5: MIPI features

Feature	Supported	Comment
MIPI 3.0 Features		
Extended Trigger support	Yes	Include EXT_TRIG_A set (register 0x2D + 0x2E necessary) and EXT_TRIG_B set (register 0x2F + 0x30 necessary).
Timed Triggers	Yes	Include counter registers (register 0x38 - 0x3F for EXT_TRIG_A set necessary and 0x31 - 0x37 for EXT_TRIG_B set necessary).
Mappable Triggers	Yes	Additional MTRIG_SET_x required in UDR register range.
Standard Reach RFFE Bus Length	Yes	RFFE Bus Length of up to 15 cm (standard)
Longer Reach RFFE Bus Length Feature	Yes	Longer Reach allows for longer RFFE bus lengths. This requires a limitation to the Standard Frequency Range of RFFE plus additional timing requirements for all devices on the bus
Programmable driver strength	Yes	Allows to program MIPI device Bus driver strength (relevant vor Read Back messages) up to 80pF via BUS_LD-Register (0x2B) Default value: 50 pF
Register 0 write command sequence	Yes	Shortened Write Sequence for Register 0 - Caution: only 7 LSBs in Reg 0 can be addressed
Register read and write command sequence	Yes	Standard Register Read/Write procedure addressing standard register space of 0x00 - 0x1F
Extended register read and write command sequence	Yes	Register Read/Write procedure addressing extended register space of 0x00 - 0xFF
Extended Register Write Long Command Sequence	No	Register Read/Write procedure addressing extended register space of 0x0000 - 0xFFFF
Masked write command sequence	Yes	Allow only certain bits in a register to be updated during a write command. Relevant Registers marked "MW" in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	SCLK range 32 kHz - 26 MHz for read and write commands
Support for extended frequency range operations for SCLK	Yes	SCLK range 26 MHz - 52 MHz for write commands
sRead (synchronous Read) Full Speed or half speed up to 26 MHz	Yes	Relaxed Slave Setup Time requirements as Master samples Data on rising edge of SCLK signal
"Regular" Read Full Speed or half speed up to 13 MHz	Yes	Stricter Slave Setup Time requirements as Master samples Data on falling edge of SCLK signal

Table 5: MIPI features (continued)

Feature	Supported	Comment
"Regular" Read Full Speed or half speed up to 26 MHz (MIPI RFFE 1.10 feature)	No	Full-Speed "regular" (falling edge sampling) Read operations are no longer specified for use in the Standard Frequency Range in MIPI RFFE3.0, and are intended to be replaced by Full-Speed sRead operations in the Standard Frequency Range. Half-Speed Data Response accesses for Read operations in the Standard Frequency Range remain supported. Read operations are not supported for use in the Extended Frequency Range. In the Ext FR only Half-Speed Data Response (HSDR) accesses using sReads are valid for Slaves (or non-BOMs) driving SDATA on the bus.
Product ID + extended product ID register	Yes	PRODUCT_ID (address 0x1D) and EXT_PRODUCT_ID (address 0x20) Registers
Extended Manufacturer ID	Yes	According to MIPI2.1 specification
Revision ID register	Yes	This Register contains the Device Revision (address 0x21)
Programmable GSID (Group Slave Identifier)	Yes	GROUP_SID Register (at address 0x22). Only in case RFFE 1.1 backwards compatibilty is supported: GROUP_SID0 Bitfield access at address 0x1B (copy of GROUP_SID0)
Programmable USID (Unique Slave Identifier)	Yes	Device can be also explicitly addressed via combination of (old) USID, Manufacturer ID, and (extended) product ID to reprogram USID via (extended) Register Write sequence (see MIPI RFFE Spec v3.0 Chapter 6.2.2)
Trigger functionality	Yes	3 "standard" Triggers via PM_TRIG[5:0] consisting of 3 Mask- and 3 Trigger Bits
Trigger Handling in Secondary Mode: Ignore Triggers	Yes	When Device is and stays in Secondary Mode, Triggers are IGNORED (NOTE: Triggers in combination with a mode change are not ignored)
Extended Triggers and Trigger Masks	Yes	Additional eight Triggers and the associated Trigger Masks (registers at addresses 0x2D and 0x2E)
Broadcast/GSID write to PM TRIG register	Yes	The above mentioned Trigger Register (and extended trigger register) can be accessed via Broadcast/GSID writes to trigger several MIPI devices snychronously. NOTE: Trigger Mask bits are nor changed wih Broadcast/GSID writes
Reset	Yes	Reset is possible via VIO, PM TRIG or register SW_RST (0x23). NOTE: SW_RST only resets User Defined Registers, it does not reset the values of any reserved registers

Table 5: MIPI features (continued)

Feature	Supported	Comment
Status/Error sum register	Yes	ERR_SUM Register (address 0x24). Only in case RFFE 1.1 backwards compatibilty is supported: RFFE_STATUS Register access at address 0x1A (copy of ERR_SUM)
USID_Sel pin	Yes	External pin for changing USID (values: see programing section), 1 USID pin addressable by customer

Table 6: User Defined Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	ENABLE_CTRL	0	ENABLE	0: LNA Disable 1: LNA Enable OR'ed with Enable bit (Bit7 in register 1)	0	No	mTrig set C	R/W MW
0x01	MODE_CTRL	7	ENABLE	0: LNA Disable 1: LNA Enable OR'ed with Enable bit (Bit0 in register 0)	00000000	No	mTrig set A	R/W MW
		6:3	GAIN_CTRL	LNA Gain control				
		2:0	LNA_BIAS	LNA Bias control				
0x10	MTRIG_1	7:4	reserved		0001	No	N/A	R/W
		3:0	MTRIG_SET_A	Mappable Trigger Set A	0000			
0x11	MTRIG_2	7:4	reserved		0000	No	N/A	R/W
		3:0	MTRIG_SET_C	Mappable Trigger Set C	1111			

Table 7: Register mapping

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation mode	1	Yes	N/A	R/W MW
				1: Secondary Mode (triggers are ignored)				
		6	PWR_MODE(0), State Bit Vector	0: No action	0			
				1: Powered Reset (STARTUP to active state)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	01100111	No	N/A	R
0x1E	MANUFACT._ID	7:0	MANUFACTURER_ID	Manufacturer ID. This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. See http://mid.mipi.org.	00011010	No	N/A	R

Table 7: Register mapping (continued)

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x1F	MAN_USID	7:6	MANUFACTURER_ID[11:10]	These bits are read-only. However, for reprogramming the USID, a write command sequence is performed on this register, even though the write does not change its value. See http://mid.mipi.org.	00	No	N/A	R
		5:4	MANUFACTURER_ID[9:8]	These bits are read-only. However, for reprogramming the USID, a write command sequence is performed on this register, even though the write does not change its value. See http://mid.mipi.org.	01			
		3:0	USID[3:0]	These bits store the USID of the device. Performing a write to this register using the described programming sequences will re-program the USID.	See Tab. 9	No	N/A	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	N/A	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision.	0011	No	N/A	R
		3:0	SUB_REVISION	Chip sub revision.	0000			
0x22	GS_ID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	N/A	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	N/A	R/W
		6:0	reserved	Reserved for future use	0000000			
0x24	ERR_SUM	7	reserved	Reserved for future use	0	No	N/A	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

Table 7: Register mapping (continued)

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x2B	BUS_LD	7:3	reserved	Reserved for future use	00000	No	N/A	R/W
		2:0	BUS_LD[2:0]	Programs the drive strength of the SDATA driver in feedback modes. 0x0: 10pF 0x1: 20pF 0x2: 30pF 0x3: 40pF 0x4: 50pF 0x5: 60pF 0x6: 80pF 0x7: 80pF	100			
0x2C	TEST_PATT	7:0	TEST_PATT[7:0]	A read to this register will trigger the slave to transmit a fixed test pattern of 0xD2.	11010010	No	N/A	R
0x2D	EXT_TRIGGER _MASK_A	7	EXT_TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_A are masked. Data is held in shadow registers until the EXT_TRIGGER_A bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_A are not masked. Data writes go directly to the active registers.	0	No	N/A	R/W MW
		6	EXT_TRIGGER_MASK_9		0			
		5	EXT_TRIGGER_MASK_8		0			
		4	EXT_TRIGGER_MASK_7		0			
		3	EXT_TRIGGER_MASK_6		0			
		2	EXT_TRIGGER_MASK_5		0			
		1	EXT_TRIGGER_MASK_4		0			
		0	EXT_TRIGGER_MASK_3		0			
0x2E	EXT_TRIGGER_A	7	EXT_TRIGGER_10	Extended Trigger A. This bit has no effect if EXTENDED_TRIGGER_MASK_A is 1. When the part is in secondary mode and a trigger request is sent in the same command sequence that still keeps the part in secondary mode, the trigger request is ignored. This applies to Triggers only, not to Trigger Masks. When the part is in normal mode and sent to secondary mode, or when the part is in secondary mode and sent to normal mode, trigger requests in the same command sequence are NOT ignored.	0	Yes	N/A	R/W MW
		6	EXT_TRIGGER_9		0			
		5	EXT_TRIGGER_8		0			
		4	EXT_TRIGGER_7		0			
		3	EXT_TRIGGER_6		0			
		2	EXT_TRIGGER_5		0			
		1	EXT_TRIGGER_4		0			
		0	EXT_TRIGGER_3		0			
0x2F	EXT_TRIGGER_B	7	reserved	Extended Trigger B. This bit has no effect if EXTENDED_TRIGGER_MASK_B is 1. When the part is in secondary mode and a trigger request is sent in the same command sequence that still keeps the part in secondary mode, the trigger request is ignored. This applies to Triggers only, not to Trigger Masks. When the part is in normal mode and sent to secondary mode, or when the part is in secondary mode and sent to normal mode, trigger requests in the same command sequence are NOT ignored.	0	Yes	N/A	R/W MW
		6	EXT_TRIGGER_17		0			
		5	EXT_TRIGGER_16		0			
		4	EXT_TRIGGER_15		0			
		3	EXT_TRIGGER_14		0			
		2	EXT_TRIGGER_13		0			
		1	EXT_TRIGGER_12		0			
		0	EXT_TRIGGER_11		0			

Table 7: Register mapping (continued)

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x30	EXT_TRIGGER_MASK_B	7	reserved	0: Data writes to registers tied to EXT_TRIGGER_B are masked. Data is held in shadow registers until the EXT_TRIGGER_B bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_B are not masked. Data writes go directly to the active registers.	0	No	N/A	R/W MW
		6	EXT_TRIGGER_MASK_17		0			
		5	EXT_TRIGGER_MASK_16		0			
		4	EXT_TRIGGER_MASK_15		0			
		3	EXT_TRIGGER_MASK_14		0			
		2	EXT_TRIGGER_MASK_13		0			
		1	EXT_TRIGGER_MASK_12		0			
		0	EXT_TRIGGER_MASK_11		0			
0x31	EXT_TRIG_B_CNT_11	7:0	EXT_TRIG_B_CNT_11	Counter register most significant byte is R/W accessible via EXT_TRIG_A/B_CNT_X [7:0]. The actual programmable counting range of the counter is then 2, 4, ... 510 SCLK cycles.	00000000	Yes	N/A	R/W
0x32	EXT_TRIG_B_CNT_12	7:0	EXT_TRIG_B_CNT_12		00000000	Yes	N/A	R/W
0x33	EXT_TRIG_B_CNT_13	7:0	EXT_TRIG_B_CNT_13		00000000	Yes	N/A	R/W
0x34	EXT_TRIG_B_CNT_14	7:0	EXT_TRIG_B_CNT_14		00000000	Yes	N/A	R/W
0x35	EXT_TRIG_B_CNT_15	7:0	EXT_TRIG_B_CNT_15		00000000	Yes	N/A	R/W
0x36	EXT_TRIG_B_CNT_16	7:0	EXT_TRIG_B_CNT_16		00000000	Yes	N/A	R/W
0x37	EXT_TRIG_B_CNT_17	7:0	EXT_TRIG_B_CNT_17		00000000	Yes	N/A	R/W
0x38	EXT_TRIG_A_CNT_3	7:0	EXT_TRIG_A_CNT_3		00000000	Yes	N/A	R/W
0x39	EXT_TRIG_A_CNT_4	7:0	EXT_TRIG_A_CNT_4		00000000	Yes	N/A	R/W
0x3A	EXT_TRIG_A_CNT_5	7:0	EXT_TRIG_A_CNT_5		00000000	Yes	N/A	R/W
0x3B	EXT_TRIG_A_CNT_6	7:0	EXT_TRIG_A_CNT_6		00000000	Yes	N/A	R/W
0x3C	EXT_TRIG_A_CNT_7	7:0	EXT_TRIG_A_CNT_7		00000000	Yes	N/A	R/W
0x3D	EXT_TRIG_A_CNT_8	7:0	EXT_TRIG_A_CNT_8		00000000	Yes	N/A	R/W
0x3E	EXT_TRIG_A_CNT_9	7:0	EXT_TRIG_A_CNT_9		00000000	Yes	N/A	R/W
0x3F	EXT_TRIG_A_CNT_10	7:0	EXT_TRIG_A_CNT_10		00000000	Yes	N/A	R/W

Table 8: Timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VIO Rise Time	$T_{VIOrise}$	50[1]	–	450	µs	
VIO Supply Reset Timing	$T_{VIO-RST}$	10	–	–	µs	
Reset Delay Time	T_{SIGOL}	0.12	–	–	µs	
LNA turn on time [2]	t_{PUP}	–	–	1	µs	
LNA turn off time [3]	t_{POFF}	–	–	1	µs	
LNA gain settling time[4]	t_{GST}	–	–	1	µs	

[1]VIO rise time down to 10 µs is supported as long as first programming starts 50 µs after VIO rise
[2]50% last SCLK falling edge to within 0.5 dB gain error of steady state gain
[3]50% last SCLK falling edge to less than -20 dB S21
[4]Gain switching between any of 2 gains gears to be with 0.5 dB gain error of steady state gain (start 50% last SCLK falling edge)

Table 9: USID States

USID pin	SDATA/SCLK	USID
0	Nominal	0b1000
1	Nominal	0b1001
0	Swap	0b1010
1	Swap	0b1011

Table 10: Gain Modes of Operation

	Register	ENABLE_CTRL (0x00)	MODE_CTRL (0x01)							
	Bitfield	ENABLE	ENABLE	GAIN_CTRL				BIAS_CTRL[1]			
State	Mode	D0	D7	D6	D5	D4	D3	D2	D1	D0	Comment
1	OFF	0	0	x	x	x	x	x	x	0	
2	Gain G10 (21 dB)	x	1	1	0	1	0	1	0	1	Bias 5
3		1	x								
4	Gain G9 (18 dB)	x	1	1	0	0	1	1	0	1	Bias 5
5		1	x								
6	Gain G8 (15 dB)	x	1	1	0	0	0	0	1	1	Bias 3
7		1	x								
8	Gain G7 (12 dB)	x	1	0	1	1	1	0	1	1	Bias 3
9		1	x								
10	Gain G6 (9 dB)	x	1	0	1	1	0	0	1	0	Bias 2
11		1	x								
12	Gain G5 (6 dB)	x	1	0	1	0	1	0	0	1	Bias 1
13		1	x								
14	Gain G4 (0 dB)	x	1	0	1	0	0	0	0	0	Bias 0
15		1	x								
16	Gain G3A (-3 dB)	x	1	1	0	1	1	0	1	0	Bias 2
17		1	x								
18	Gain G3 (-3 dB)	x	1	0	0	1	1	0	0	0	Bias settings don't care, use Bias 0
19		1	x								
20	Gain G2 (-6 dB)	x	1	0	0	1	0	0	0	0	Bias settings don't care, use Bias 0
21		1	x								
22	Gain G1 (-12 dB)	x	1	0	0	0	1	0	0	0	Bias settings don't care, use Bias 0
23		1	x								

[1]Recommended bias setting, bias can be changed according to table 11

Table 11: Bias control table

		BIAS_CTRL bits		
State	Mode	D2	D1	D0
1	Bias 0 (1.9 mA)	0	0	0
2	Bias 1 (2.8 mA)	0	0	1
3	Bias 2 (3.6 mA)	0	1	0
4	Bias 3 (4.4 mA)	0	1	1
5	Bias 4 (5.3 mA)	1	0	0
6	Bias 5 (6.2 mA)	1	0	1
7	Bias 6 (6.9 mA)	1	1	0
8	Bias 7 (7.7 mA)	1	1	1

7 Application Information

Pin Configuration and Function

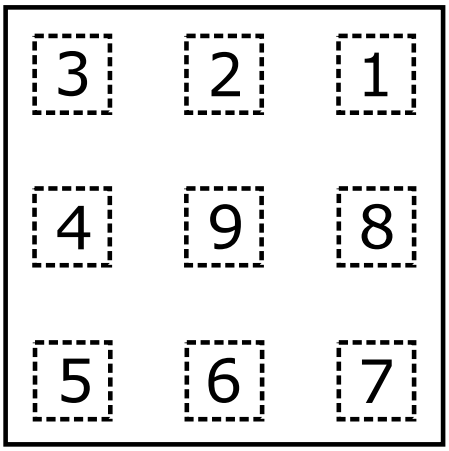


Figure 1: BGA10M1MN9 Pin Configuration (top view)

Table 12: Pin Definition and Function

Pin No.	Name	Function
1	RF_OUT	LNA output
2	GND	Ground
3	RF_IN	LNA input
4	USID	USID select pin
5	VIO	MIPI RFFE supply
6	SCLK	MIPI RFFE clock
7	SDATA	MIPI RFFE data
8	VDD	Power supply
9	GND	Ground

Application Board Configuration

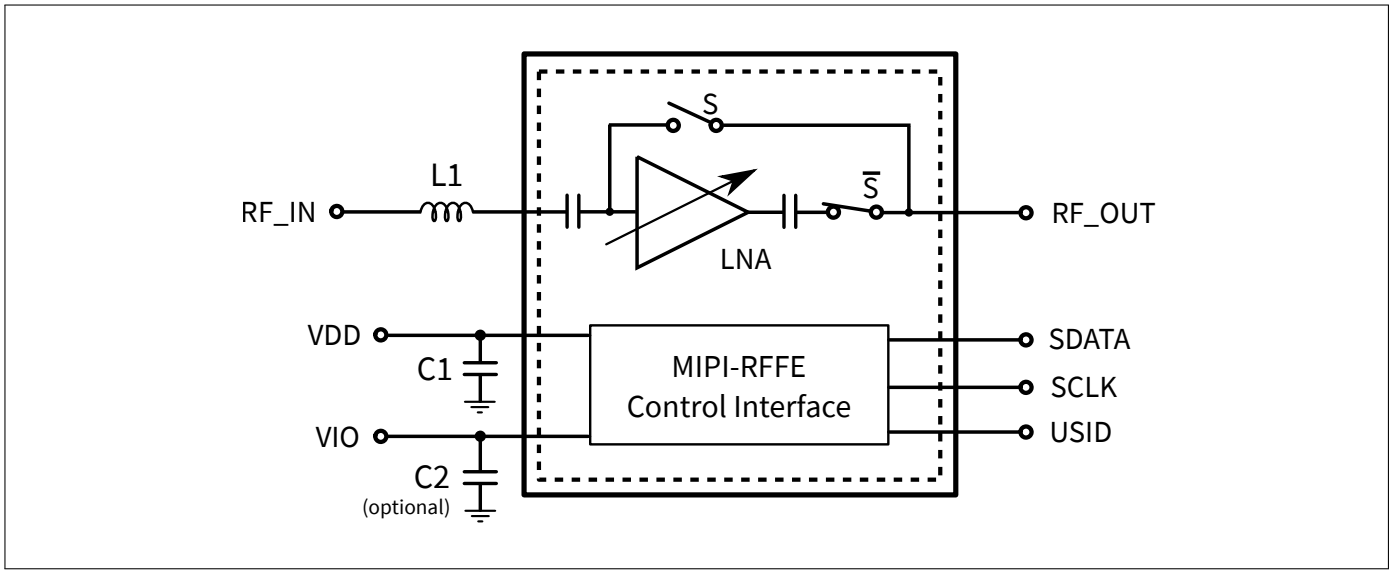


Figure 2: BGA10M1MN9 Application Schematic

Table 13: Bill of Materials Table

Name	Value	Package	Manufacturer	Function
C1	10 nF	0201	Various	RF bypass[1]
C2 (optional)	10 nF	0201	Various	RF bypass[1]
L1	6.8 nH	0201	muRata LQP HQ type	Input matching
N1	BGA10M1MN9	TSNP-9-2 / TSNP-9-6	Infineon	Multi gain mode LNA

[1] RF bypass recommended to mitigate power supply noise

8 Package Information

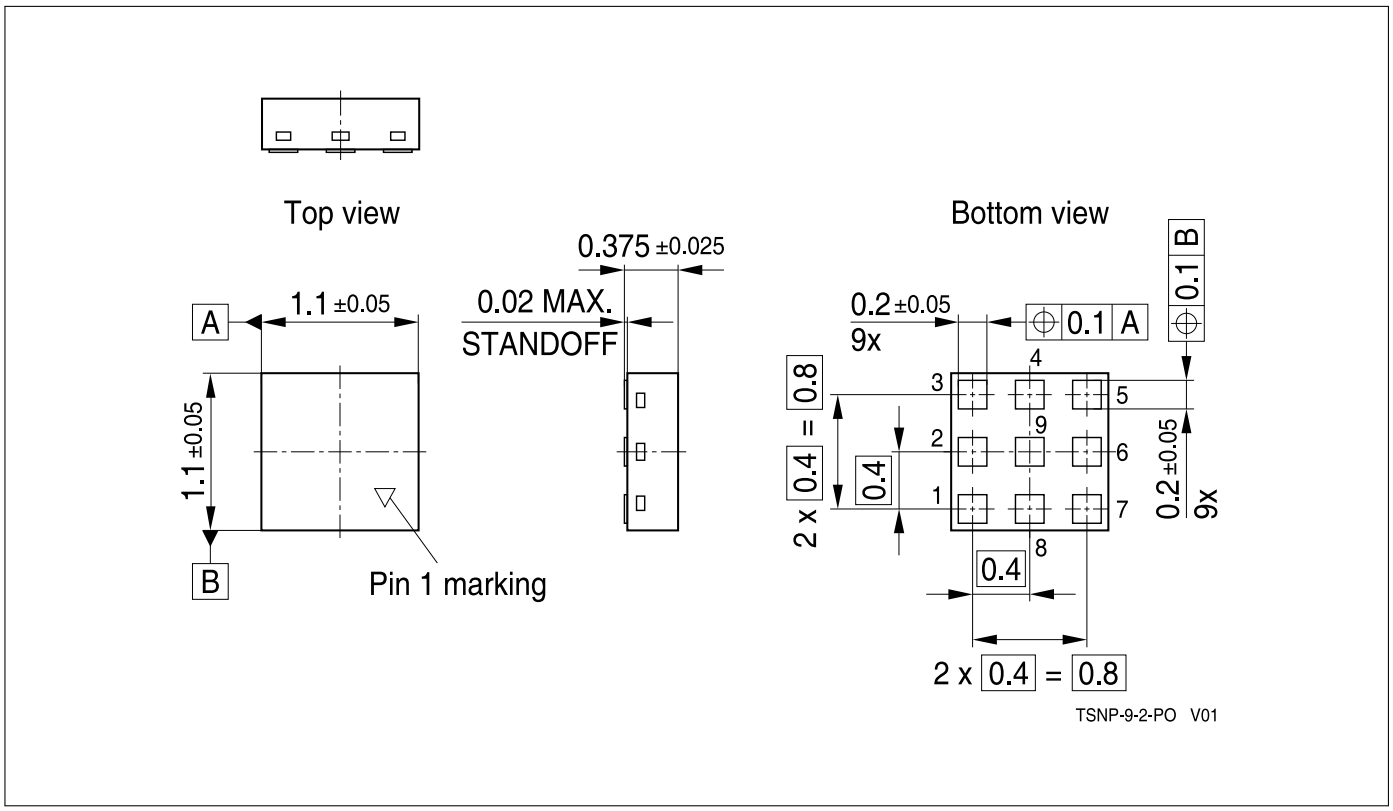


Figure 3: TSNP-9-2 Package Outline (top, side and bottom views)

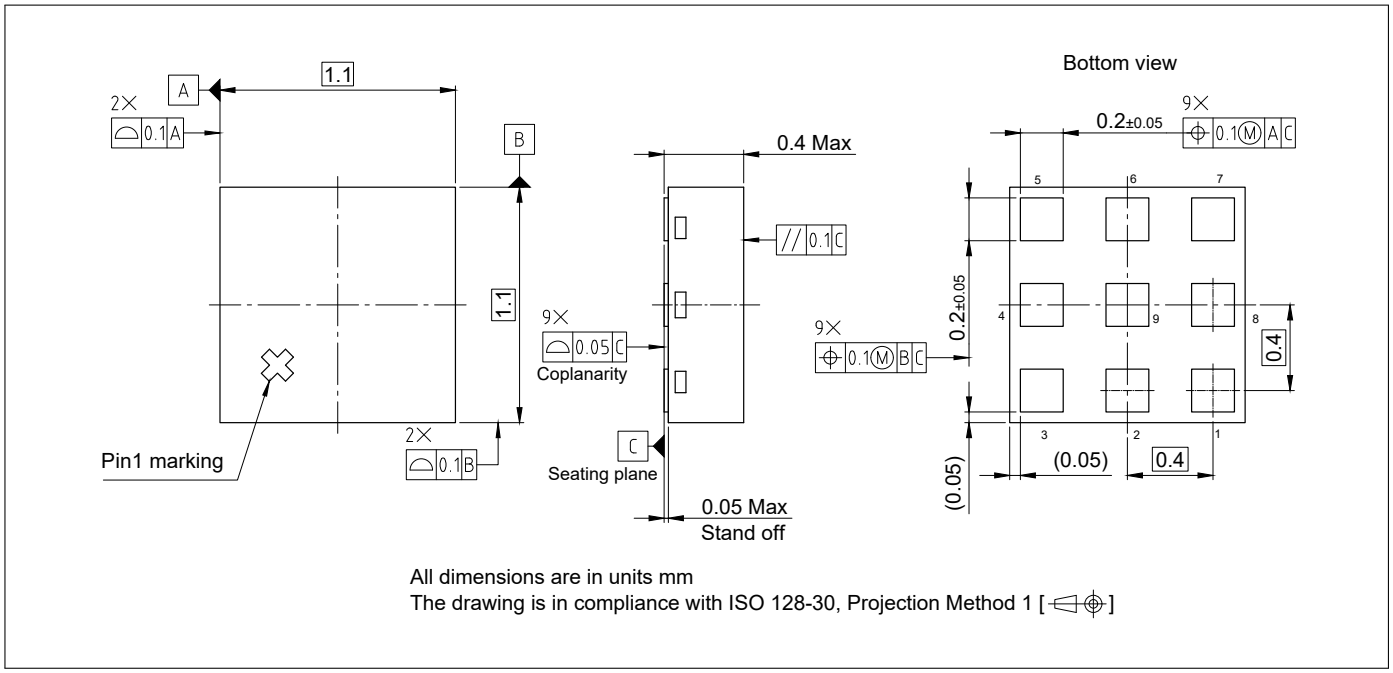


Figure 4: TSNP-9-6 Package Outline (top, side and bottom views)

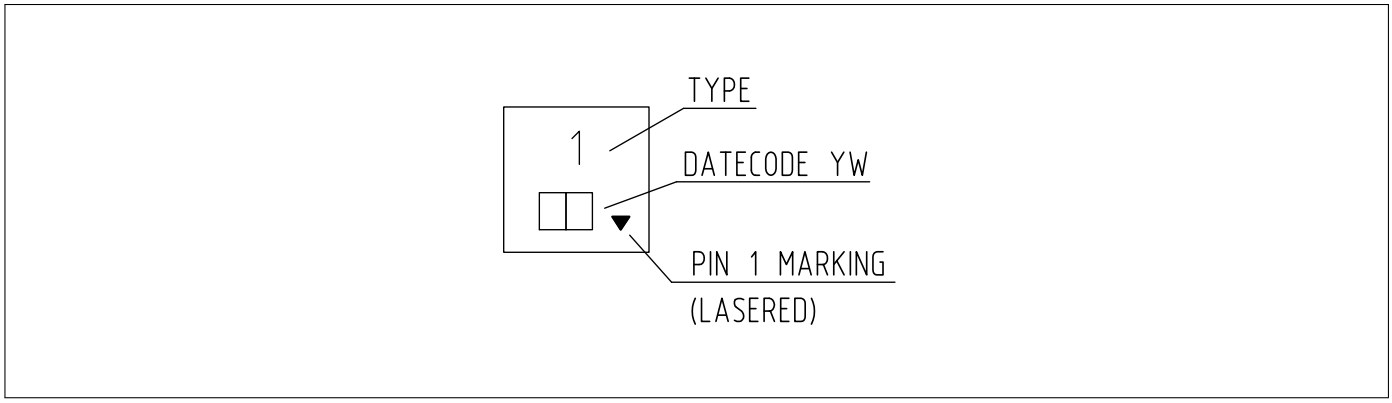


Figure 5: TSNP-9-2 Marking Specification (top view)

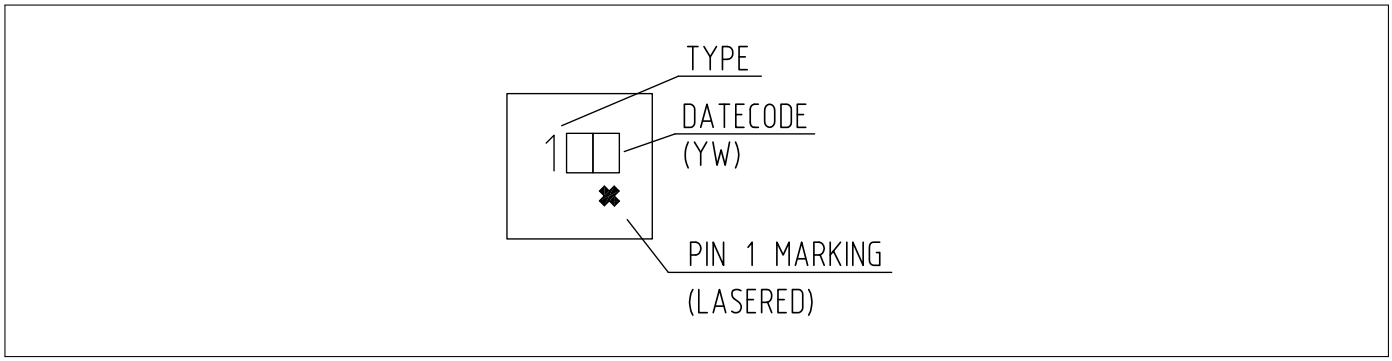


Figure 6: TSNP-9-6 Marking Specification (top view)

Table 14: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 15: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

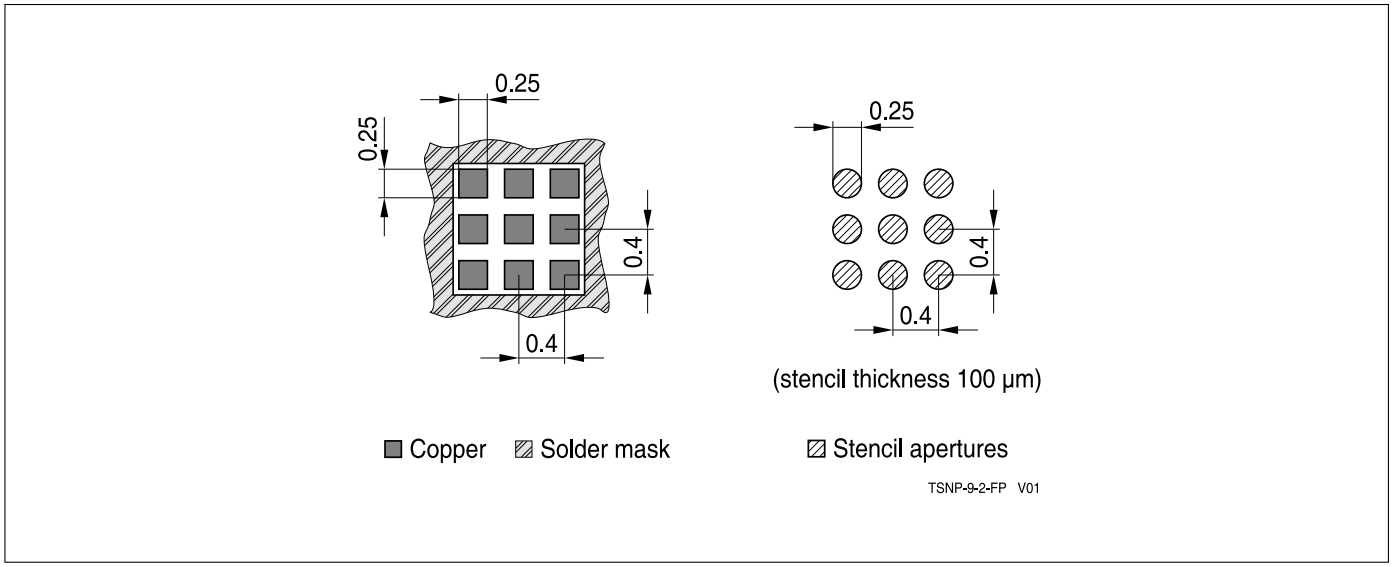


Figure 7: TSNP-9-2 Footprint Recommendation

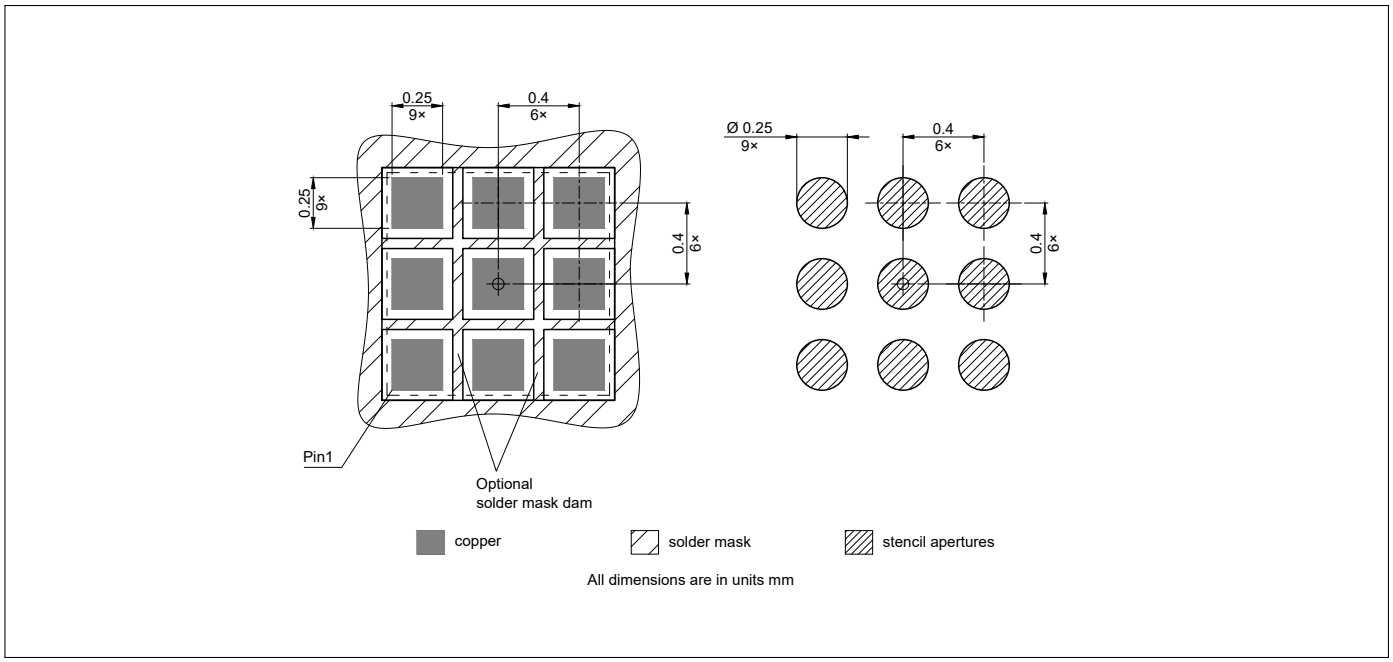


Figure 8: TSNP-9-6 Footprint Recommendation

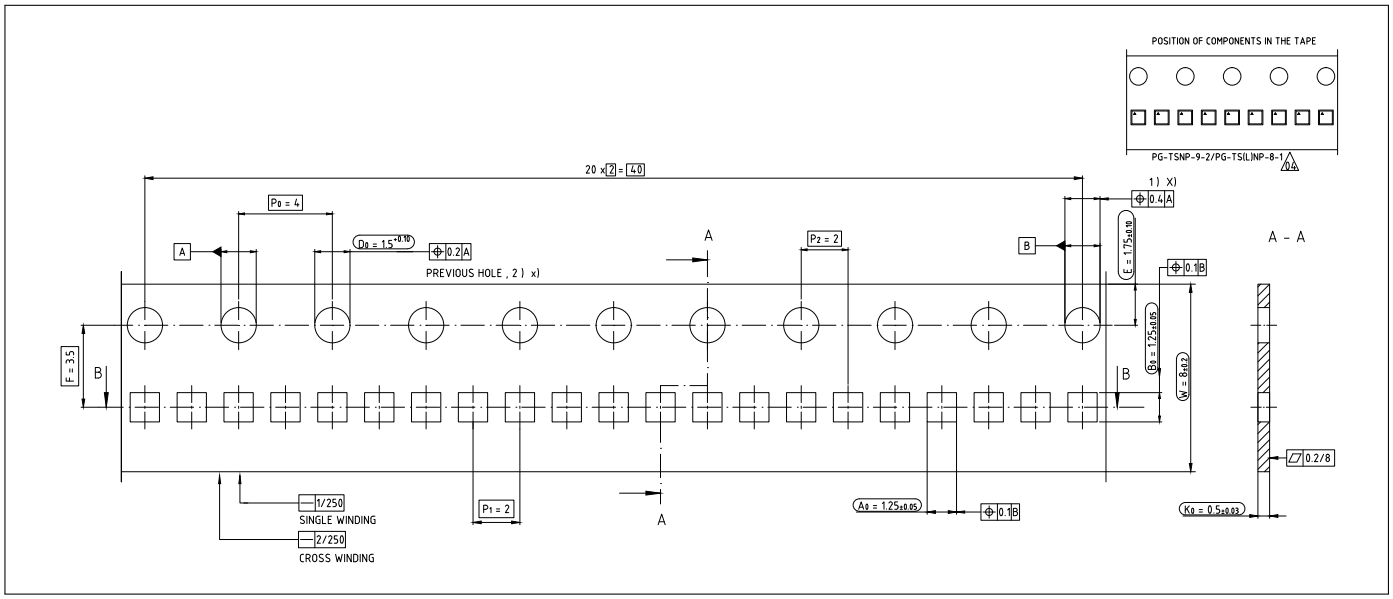


Figure 9: TSNP-9-2 Carrier Tape

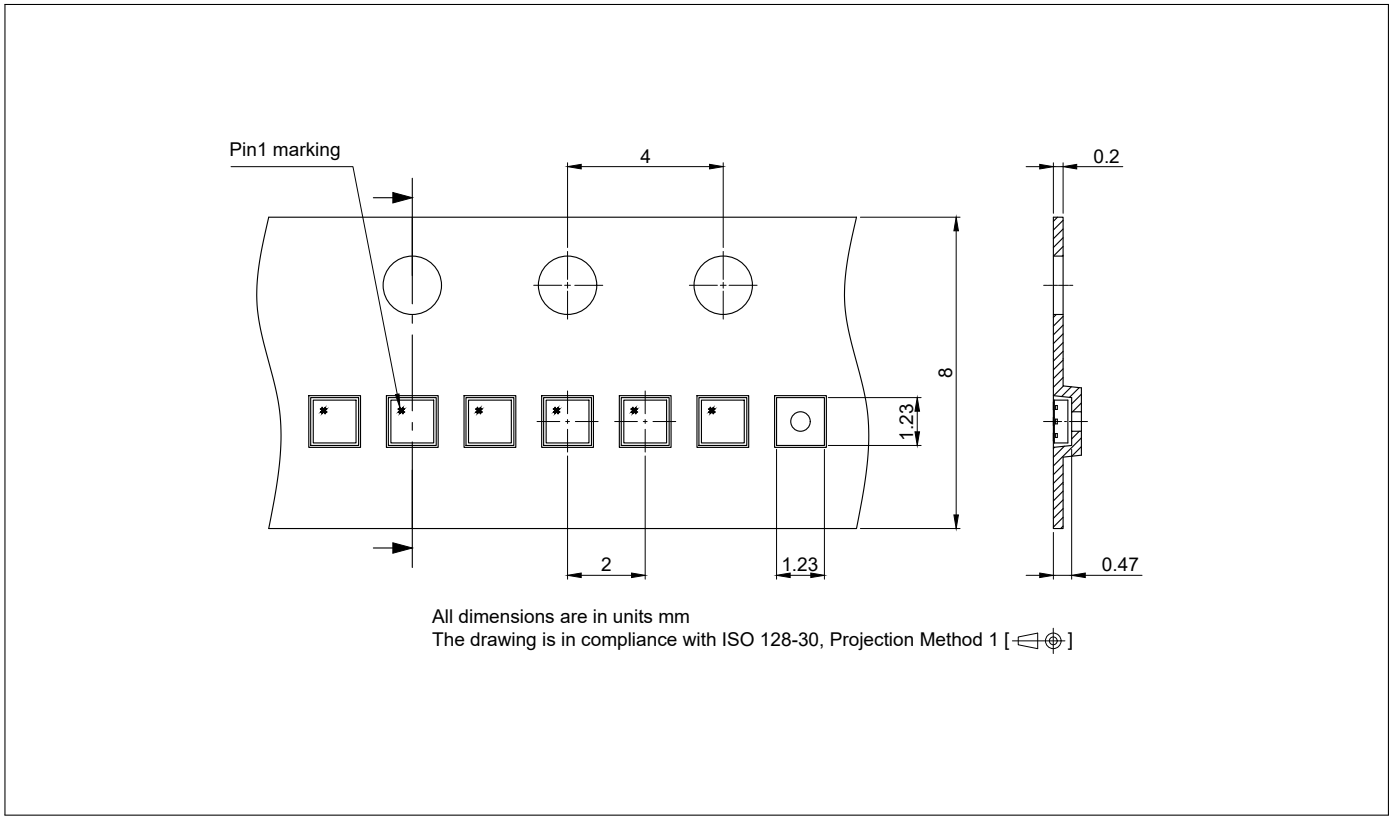


Figure 10: TSNP-9-6 Carrier Tape

Revision History	
Preliminary, v1.0, 2022-10-17	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.0, 2023-09-11	
Title page	Block diagram updated
3	Values for max. RF input power and total power dissipation added
4-6	RF parameters updated, min/max-values added
16	Bias control table updated
18	Application circuit updated

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