BGSA14M2N10

Ultra small antenna tuning SP4T

Features

- Ultra low R_{ON} resistance of 0.85 Ω in ON state
- Low C_{OFF} capacitance of 160 fF in OFF state
- High RF operating peak voltage handling of 45 V in OFF state
- MIPI RFFE 2.1 control interface
- Extremely low current consumption of 22 µA
- 4 default USID addresses via external USID_SEL pin
- Small form factor 0.95 mm x 1.3 mm (MSL1, 260 °C per JEDEC J-STD-020)

RoHS
Halogen-Free
Lead-Free
Green

Potential applications

- Impedance, antenna and inductance tuning, tunable filters

Product validation

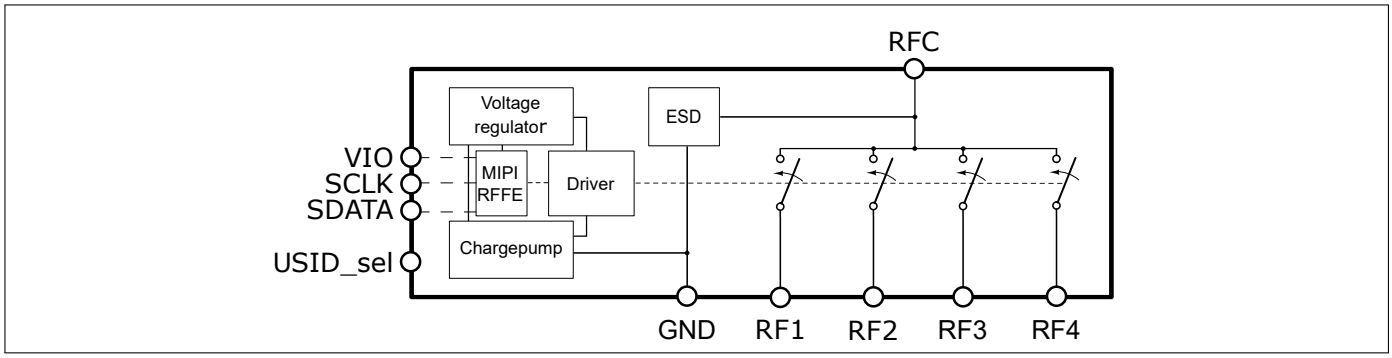
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The BGSA14M2N10 is a very small single-pole four throws (SP4T) antenna tuning switch optimized for RF applications up to 7.125 GHz. Its MIPI RFFE digital control interface allows easy implementation and best flexibility when operated in cellular mobile RF front-end designs.

The BGSA14M2N10 includes 4 low R_{on} ports making it ideal for high Q tuning applications. Thanks to its high RF voltage ruggedness, it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses.

Block diagram



Type	Marking	Package	Ordering information
BGSA14M2N10	M2	TSNP-10-9	BGSA 14M2N10 E6329
		TSNP-10-10	BGSA 14M2N10 E6329

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1 Maximum ratings

Table 1: Maximum ratings table at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	7.125	GHz	[1]
RFFE Supply voltage [2]	V_{IO}	-0.3	–	2.2	V	Only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF peak voltage	V_{RF_max}	–	–	50	V	Short term peaks (1 µs in 0.1% duty cycle), exceeding typical linearity, R_{ON} and C_{OFF} parameters, in isolation mode, test condition schematic in Fig. 2
ESD robustness, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD robustness, HBM [4]	$V_{ESD_{HBM}}$	-2	–	+2	kV	
Junction temperature	T_j	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	–	55	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
RFFE Control Voltage Levels	V_{SCLK}, V_{SDATA}, V_{USID_SEL}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{IO}. A high RF ripple at the V_{IO} can exceed the maximum ratings by $V_{IO} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R=1.5 kΩ, C=100 pF).

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

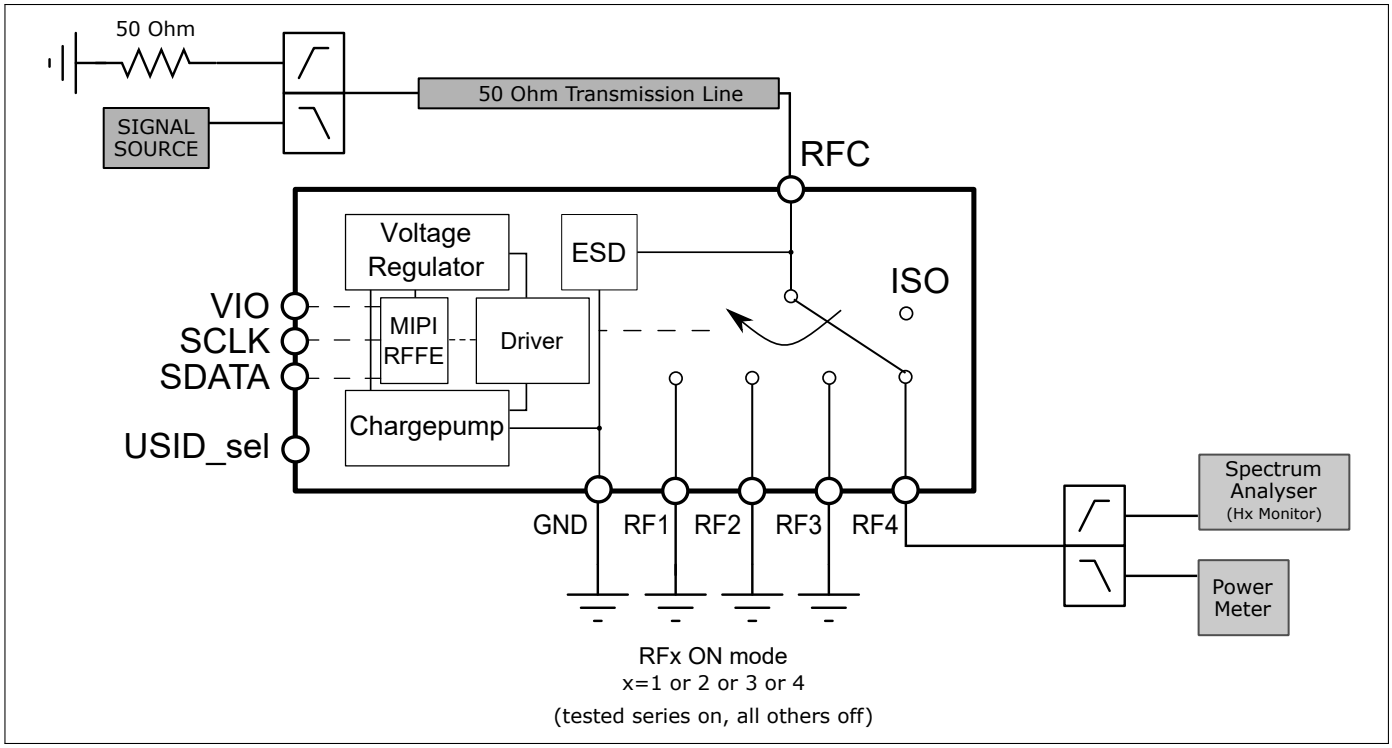

Figure 1: RF operating and harmonics generation measurement configuration - RFx ON mode (RF4 as example)

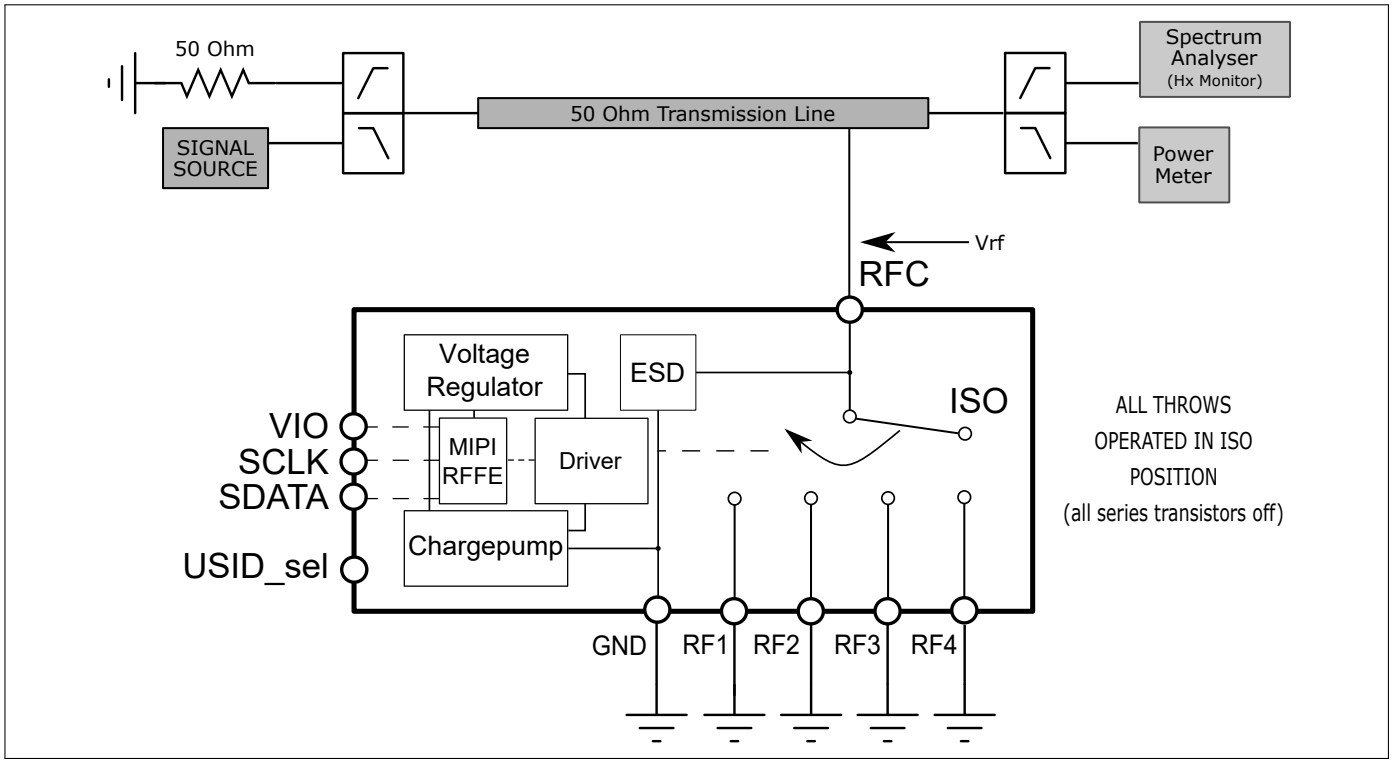

Figure 2: RF operating voltage measurement configuration - OFF mode at RFC

Maximum ratings

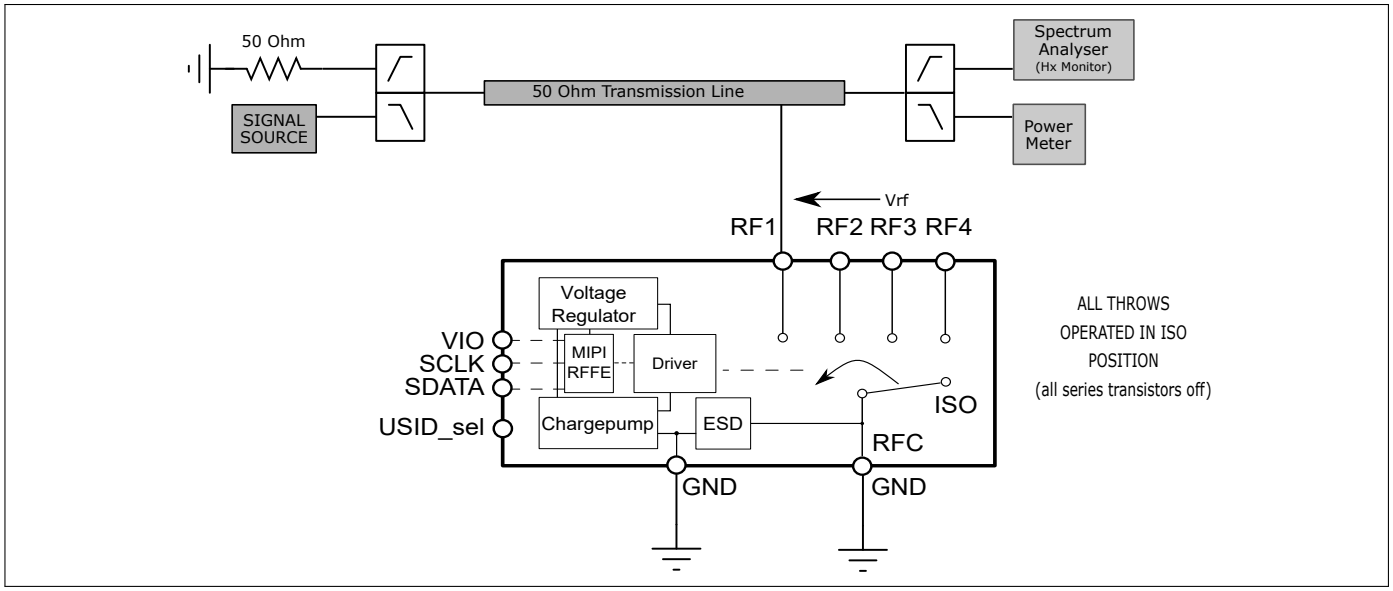

Figure 3: RF operating voltage measurement configuration - OFF mode at RFx

2 DC characteristics

Table 2: DC characteristics at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current [2]	I_{VIO}	–	22	40	µA	ACTIVE mode
		–	2 0.5 [3]	8 1 [3]	µA µA	SECONDARY_ACTIVE mode (LOW POWER) with analog circuitry powered OFF

[1] SCLK and SDATA
[2] No traffic on MIPI bus
[3] Supply current reduced after first MIPI RFFE command

3 RF small signal characteristics

Table 3: Parametric specifications using SP4T configuration

Parameter	Symbol	Values			Unit	State / Notes
		Min.	Typ.	Max.		
DC ON resistance RF1 or RF2 to RFC RF3 or RF4 to RFC	$R_{ON_{SP4T}}$ (1)	 – –	 0.95 0.85	 1.05 0.95	 Ω Ω	V_{IO} = 1.65 – 1.95 V, T_A = 25 °C, Z_0 = 50 Ω
DC OFF resistance RF1, RF2, RF3 or RF4 to RFC	$R_{OFF_{SP4T}}$	 240	 300	 –	 kΩ	
OFF capacitance, 1GHz RF1 or RF2 to RFC RF3 or RF4 to RFC	$C_{OFF_{SP4T}}$ (2)	 – –	 160 165	 170 175	 fF fF	

1) Smaller R_{ON} reachable by combining two or more SP4T RF throws
2) Off capacitance calculated from Y21 parameters

Table 4: RF electrical parameters

Insertion loss: RFC to RF1, RFC to RF2 (1,2,3)

Parameter	Symbol	Values			Unit	State / Notes
		Min.	Typ.	Max.		
600 - 960 MHz	IL_{SP4T}	–	0.15	0.25	dB	V_{IO} = 1.65 … 1.95 V, T_A = −40 °C... + 85 °C, Z_0 = 50 Ω
1160 - 1300 MHz		–	0.2	0.3	dB	
1400 - 1700 MHz		–	0.3	0.45	dB	
1700 - 2200 MHz		–	0.4	0.6	dB	
2200 - 2700 MHz		–	0.6	0.85	dB	
3300 - 4200 MHz		–	1.2	1.7	dB	
4400 - 5000 MHz		–	1.6	2.1	dB	
5150 - 5925 MHz		–	1.8	2.35	dB	
5950 - 7125 MHz		–	2.2	3.1	dB	

Insertion loss: RFC to RF3, RFC to RF4 (1,2,3)

Parameter	Symbol	Values			Unit	State / Notes
		Min.	Typ.	Max.		
600 - 960 MHz	IL_{SP4T}	–	0.15	0.25	dB	V_{IO} = 1.65 … 1.95 V, T_A = −40 °C... + 85 °C, Z_0 = 50 Ω
1160 - 1300 MHz		–	0.2	0.3	dB	
1400 - 1700 MHz		–	0.3	0.45	dB	
1700 - 2200 MHz		–	0.4	0.7	dB	
2200 - 2700 MHz		–	0.65	0.95	dB	
3300 - 4200 MHz		–	1.4	2.1	dB	
4400 - 5000 MHz		–	2.0	2.7	dB	
5150 - 5925 MHz		–	2.5	3.2	dB	
5950 - 7125 MHz		–	3.2	4.2	dB	

Return loss: RF1, RF2, RF3 or RF4 (1,2,3)

600 - 960 MHz	RL_{SP4T}	19	26	–	dB	V_{IO} = 1.65 … 1.95 V, T_A = −40 °C... + 85 °C, Z_0 = 50 Ω
1160 - 1300 MHz		17	23	–	dB	
1400 - 1700 MHz		14	20	–	dB	
1700 - 2200 MHz		12	17	–	dB	
2200 - 2700 MHz		10	14	–	dB	
3300 - 4200 MHz		6	10	–	dB	
4400 - 5000 MHz		5	8	–	dB	
5150 - 5925 MHz		5	7	–	dB	
5950 - 7125 MHz		4	7	–	dB	

Isolation: RFC to RF1, RF2, RF3, RF4 in all OFF mode (State 0) (1,2,3)

600 - 960 MHz	ISO_{OFF}	20	22	–	dB	V_{IO} = 1.65 … 1.95 V, T_A = −40 °C... + 85 °C, Z_0 = 50 Ω
1160 - 1300 MHz		17	19	–	dB	
1400 - 1700 MHz		15	17	–	dB	
1700 - 2200 MHz		13	15	–	dB	
2200 - 2700 MHz		12	14	–	dB	
3300 - 4200 MHz		11	12	–	dB	
4400 - 5000 MHz		10	11	–	dB	
5150 - 5925 MHz		9	11	–	dB	
5950 - 7125 MHz		9	11	–	dB	

1) Valid for all RF power levels, no compression behavior
2) Network analyser input power: P_{IN} = 0 *dBm*
3) On application board without any matching components

4 RF large signal characteristics

Table 5: RF large signal specifications at $T_A = -40$ °C... + 85 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
RF operating voltage	V_{RF_opr}	–	–	45	V	In isolation mode, 900MHz, T_A = 25 °C , Test condition schematic in Fig. 2/Fig. 3.
Harmonic distortion, ON mode						
All RF ports Second order harmonics	P_{H2}	–	-90	-75	dBm	26 dBm, 50 Ω, f_0 = 663 MHz
All RF ports Third order harmonics	P_{H3}	–	-90	-80	dBm	26 dBm, 50 Ω, f_0 = 663 MHz
All RF ports Second order harmonics	P_{H2}	–	-70	-60	dBm	35 dBm, 50 Ω, f_0 = 920 MHz
All RF ports Third order harmonics	P_{H3}	–	-60	-55	dBm	35 dBm, 50 Ω, f_0 = 920 MHz
All RF ports Second order harmonics	P_{H2}	–	-65	-55	dBm	33 dBm, 50 Ω, f_0 = 1910 MHz
All RF ports Third order harmonics	P_{H3}	–	-60	-55	dBm	33 dBm, 50 Ω, f_0 = 1910 MHz
All RF ports Second order harmonics	P_{H2}	–	-70	-60	dBm	29 dBm, 50 Ω, f_0 = 2690 MHz
All RF ports Third order harmonics	P_{H3}	–	-75	-65	dBm	29 dBm, 50 Ω, f_0 = 2690 MHz
All RF ports Second order harmonics	P_{H2}	–	-70	-60	dBm	29 dBm, 50 Ω, f_0 = 3500 MHz
All RF ports Third order harmonics	P_{H3}	–	-70	-60	dBm	29 dBm, 50 Ω, f_0 = 3500 MHz
All RF ports Second order harmonics	P_{H2}	–	-65	-55	dBm	29 dBm, 50 Ω, f_0 = 4200 MHz
All RF ports Third order harmonics	P_{H3}	–	-70	-60	dBm	29 dBm, 50 Ω, f_0 = 4200 MHz
All RF ports Second order harmonics	P_{H2}	–	-60	-55	dBm	29 dBm, 50 Ω, f_0 = 5000 MHz
All RF ports Third order harmonics	P_{H3}	–	-75	-65	dBm	29 dBm, 50 Ω, f_0 = 5000 MHz
All RF ports > Third order harmonics	P_{Hx}	–	–	-75	dBm	29 dBm, 50 Ω

Table 6: RF large signal specifications at T_A = −40 °C... + 85 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Intermodulation distortion IIP2						
IIP2, low	IIP2,l	115	125	–	dBm	IIP2 conditions in Tab. 7
IIP2, high	IIP2,h	115	125	–	dBm	
Intermodulation distortion IIP3						
IIP3, Band 1	IIP3	70	78	–	dBm	IIP3 conditions in Tab. 8
IIP3, Band 5	IIP3	76	82	–	dBm	
IIP3, Band 7	IIP3	68	78	–	dBm	

Table 7: IIP2 conditions table

Band	In-band frequency [MHz]	Blocker frequency 1 [MHz]	Blocker power 1 [dBm]	Blocker frequency 2 [MHz]	Blocker power 2 [dBm]
Band 1 low	2140	1950	23	190	0
Band 1 high	2140	1950	23	4090	0
Band 5 low	881.5	836.5	23	45	0
Band 5 high	881.5	836.5	23	1718	0
Band 7 low	2655	2535	23	120	0
Band 7 high	2655	2535	23	5910	0

Table 8: IIP3 conditions table

Band	In-band frequency [MHz]	Blocker frequency 1 [MHz]	Blocker power 1 [dBm]	Blocker frequency 2 [MHz]	Blocker power 2 [dBm]
Band 1	2140	1950	23	1760	0
Band 5	881.5	836.5	23	791.5	0
Band 7	2655	2535	23	2415	0

5 MIPI RFFE specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

Table 9: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below Register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz
Longer reach RFFE bus length feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended triggers and trigger masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	See Tab. 16

Table 10: Startup behavior

Feature	State	Comment
Power status	Low power	Device in SECONDARY_ACTIVE mode (LOW POWER) after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 11: Device control timing at V_{IO} = 1.65 – 1.95 *V*, T_A = −40 °C... + 85 °C, P_{IN} = 0 *dBm*

Parameter	Symbol	Values			Unit	State / Notes
		Min.	Typ.	Max.		
Power up settling time	t_{PUP}	–	8	15	µs	Time from 50% last SCLK rising edge of the register write command after analog circuitry powered on command to 10% / 90% of RF amplitude on the RF Path, see Fig. 4
Switching time RF path A to RF path B	t_{ST}	–	8	15	µs	Time from 50% last SCLK rising edge of the register write command to 90% of RF amplitude on the RF path B, see Fig. 4

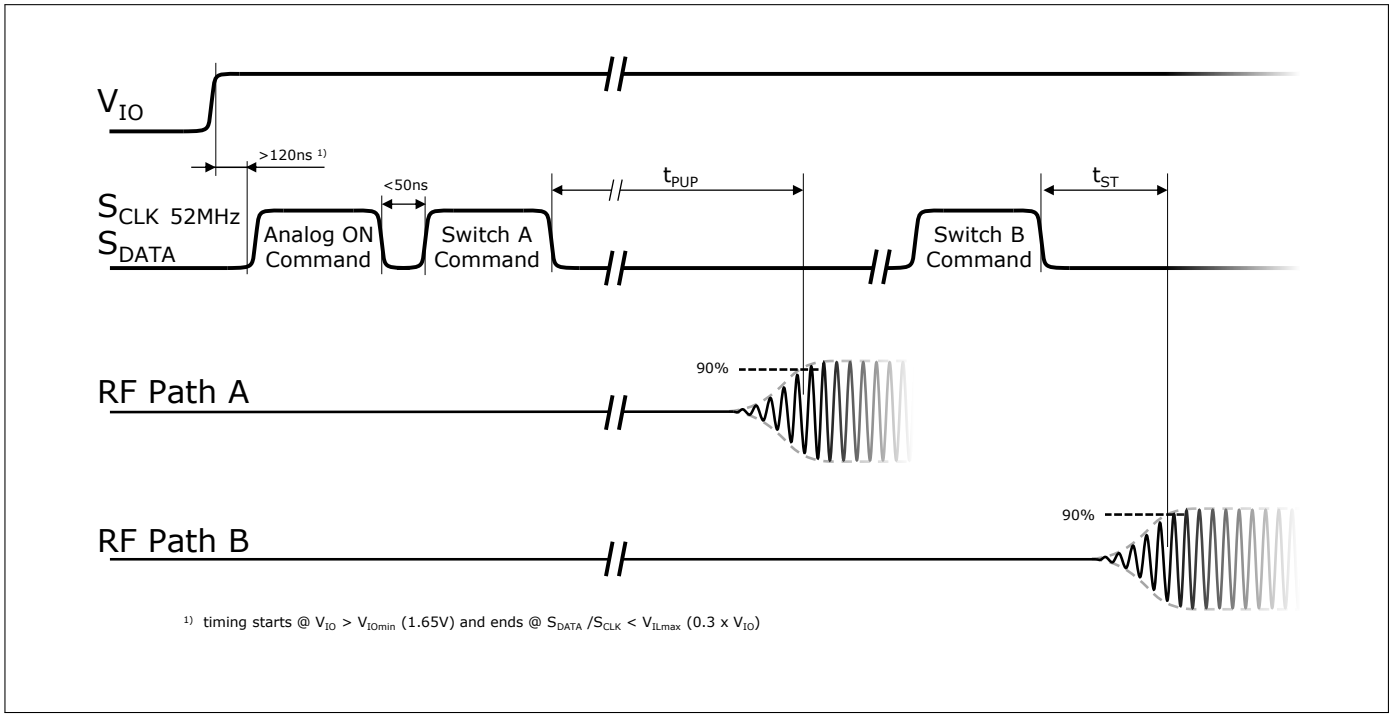

Figure 4: BGSA14M2N10 power up and state switching sequence

Table 12: Register mapping, table I

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	RF switch control	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation mode	0: Normal operation (ACTIVE) 1: Low power mode (SECONDARY_ACTIVE)	1	Yes	No	R/W MW
		6	PWR_MODE(0) State bit vector	0: No action (ACTIVE) 1: Powered reset (ACTIVE to STARTUP)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		2	TRIGGER_2	0: No action (data held in shadow REG) 1: Data transferred to active REG	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
		0	TRIGGER_0	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	01101010	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001			
		3:0	USID[3:0]	USID_Sel pin	See Tab. 16	No	No	R/W

Table 13: Register mapping, table II

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0000	No	No	R
		3:0	SUB_REVISION	Chip sub revision	0000			
0x22	GSID	7:4	GSID0[3:0]	Primary group slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary group slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Program the drive strength of the SDATA driver in readback modes. 0x0: 10 pF 0x1: 20 pF 0x2: 30 pF 0x3: 40 pF 0x4: 50 pF 0x5: 60 pF 0x6: 80 pF 0x7: 80 pF 0x8-0xF: reserved	0x4			

Table 14: Register mapping, table III

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_10 are masked. Data is held in shadow registers until the EXT_TRIGGER_10 bit is set to 1.	1	No	No	R/W
				1: Data writes to registers tied to EXT_TRIGGER_10 are not masked. Data writes go directly to the active registers.				MW
		6	TRIGGER_MASK_9	0: Data writes to registers tied to EXT_TRIGGER_9 are masked. Data is held in shadow registers until the EXT_TRIGGER_9 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_9 are not masked. Data writes go directly to the active registers.				
		5	TRIGGER_MASK_8	0: Data writes to registers tied to EXT_TRIGGER_8 are masked. Data is held in shadow registers until the EXT_TRIGGER_8 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_8 are not masked. Data writes go directly to the active registers.				
		4	TRIGGER_MASK_7	0: Data writes to registers tied to EXT_TRIGGER_7 are masked. Data is held in shadow registers until the EXT_TRIGGER_7 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_7 are not masked. Data writes go directly to the active registers.				
		3	TRIGGER_MASK_6	0: Data writes to registers tied to EXT_TRIGGER_6 are masked. Data is held in shadow registers until the EXT_TRIGGER_6 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_6 are not masked. Data writes go directly to the active registers.				
		2	TRIGGER_MASK_5	0: Data writes to registers tied to EXT_TRIGGER_5 are masked. Data is held in shadow registers until the EXT_TRIGGER_5 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_5 are not masked. Data writes go directly to the active registers.				
		1	TRIGGER_MASK_4	0: Data writes to registers tied to EXT_TRIGGER_4 are masked. Data is held in shadow registers until the EXT_TRIGGER_4 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_4 are not masked. Data writes go directly to the active registers.				
		0	TRIGGER_MASK_3	0: Data writes to registers tied to EXT_TRIGGER_3 are masked. Data is held in shadow registers until the EXT_TRIGGER_3 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_3 are not masked. Data writes go directly to the active registers.				

Table 15: Register mapping, table IV

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action. Data is held in shadow registers.	0	Yes	No	R/W
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_10				MW
		6	TRIGGER_9	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_9				
		5	TRIGGER_8	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_8				
		4	TRIGGER_7	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_7				
		3	TRIGGER_6	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_6				
		2	TRIGGER_5	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_5				
		1	TRIGGER_4	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_4				
		0	TRIGGER_3	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_3				

Table 16: Default MIPI USID selection

Address	Symbol	External condition at USID_SEL Pin
USID=0110	Addr6	to VIO
USID=0111	Addr7	Ground
USID=1000	Addr8	220 kΩ to VIO[1)]
USID=1001	Addr9	Floating[1)]

[1)] Total capacitance on the USID_SEL pin must be <5 pF.

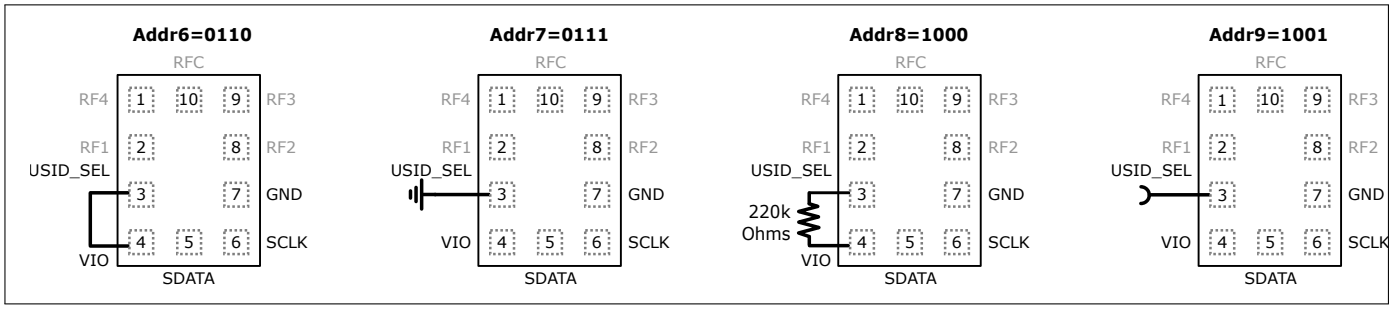

Figure 5: BGSA14M2N10 USID_Sel pin configuration

Table 17: Modes of operation (truth table), valid for Register_0

		Register bits							
State	**Mode**	**D7**[1]	**D6**[1]	**D5**[1]	**D4**	**D3**	**D2**	**D1**	**D0**
0	ALL OFF (Isolation)	x	x	x	0	0	0	0	0
1	RF1 ON	x	x	x	0	0	0	0	1
2	RF2 ON	x	x	x	0	0	0	1	0
3	RF1+RF2 ON	x	x	x	0	0	0	1	1
4	RF3 ON	x	x	x	0	0	1	0	0
5	RF1+RF3 ON	x	x	x	0	0	1	0	1
6	RF2+RF3 ON	x	x	x	0	0	1	1	0
7	RF1+RF2+RF3 ON	x	x	x	0	0	1	1	1
8	RF4 ON	x	x	x	0	1	0	0	0
9	RF1+RF4 ON	x	x	x	0	1	0	0	1
10	RF2+RF4 ON	x	x	x	0	1	0	1	0
11	RF1+RF2+RF4 ON	x	x	x	0	1	0	1	1
12	RF3+RF4 ON	x	x	x	0	1	1	0	0
13	RF1+RF3+RF4 ON	x	x	x	0	1	1	0	1
14	RF2+RF3+RF4 ON	x	x	x	0	1	1	1	0
15	RF1+RF2+RF3+RF4 ON	x	x	x	0	1	1	1	1

[1] Do not care, x = 0 or 1

6 Application information

Pin configuration and function

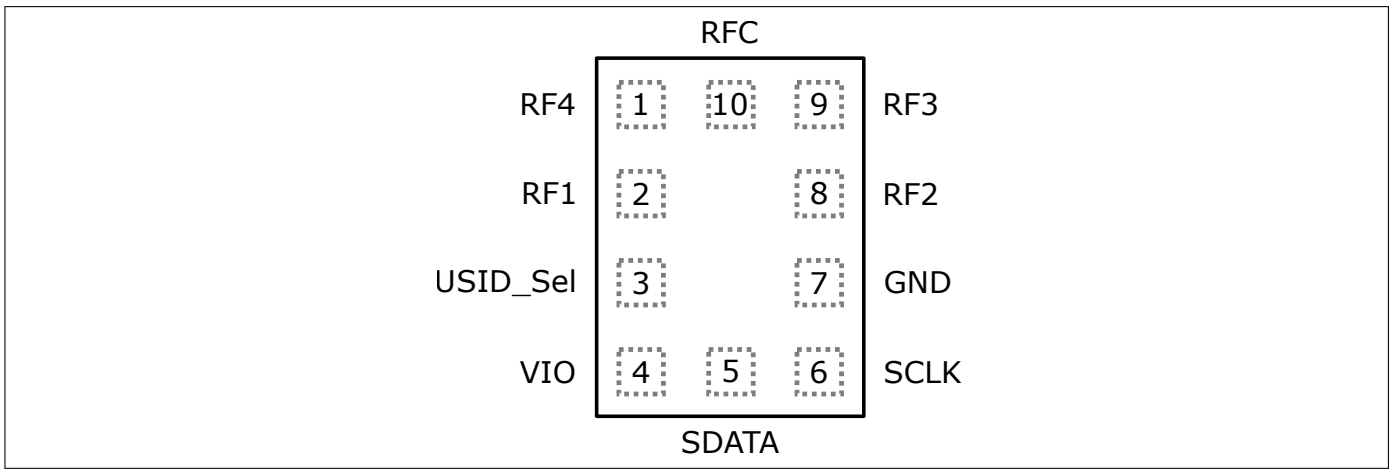

Figure 6: BGSA14M2N10 pin configuration (top view)

Table 18: Pin definition and function

Pin no.	Name	Function
1	RF4	RF4 port
2	RF1	RF1 port
3	USID_Sel	USID default address selection pin (see Tab. 16)
4	VIO	Voltage supply compatible with MIPI RFFE specification
5	SDATA	MIPI RFFE data input / output
6	SCLK	MIPI RFFE clock input
7	GND	Ground
8	RF2	RF2 port
9	RF3	RF3 port
10	RFC	Common RF port

Table 19: ESD robustness, System Level Test (SLT)

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
ESD SLT [1]	$V_{ESD_{SLT}}$	-8	–	+8	kV	RF vs system GND, with 27 nH shunt inductor
ESD SLT [1]	$V_{ESD_{SLT}}$	-6	–	+6	kV	RF vs system GND, with 56 nH shunt inductor

[1] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Evaluation board description

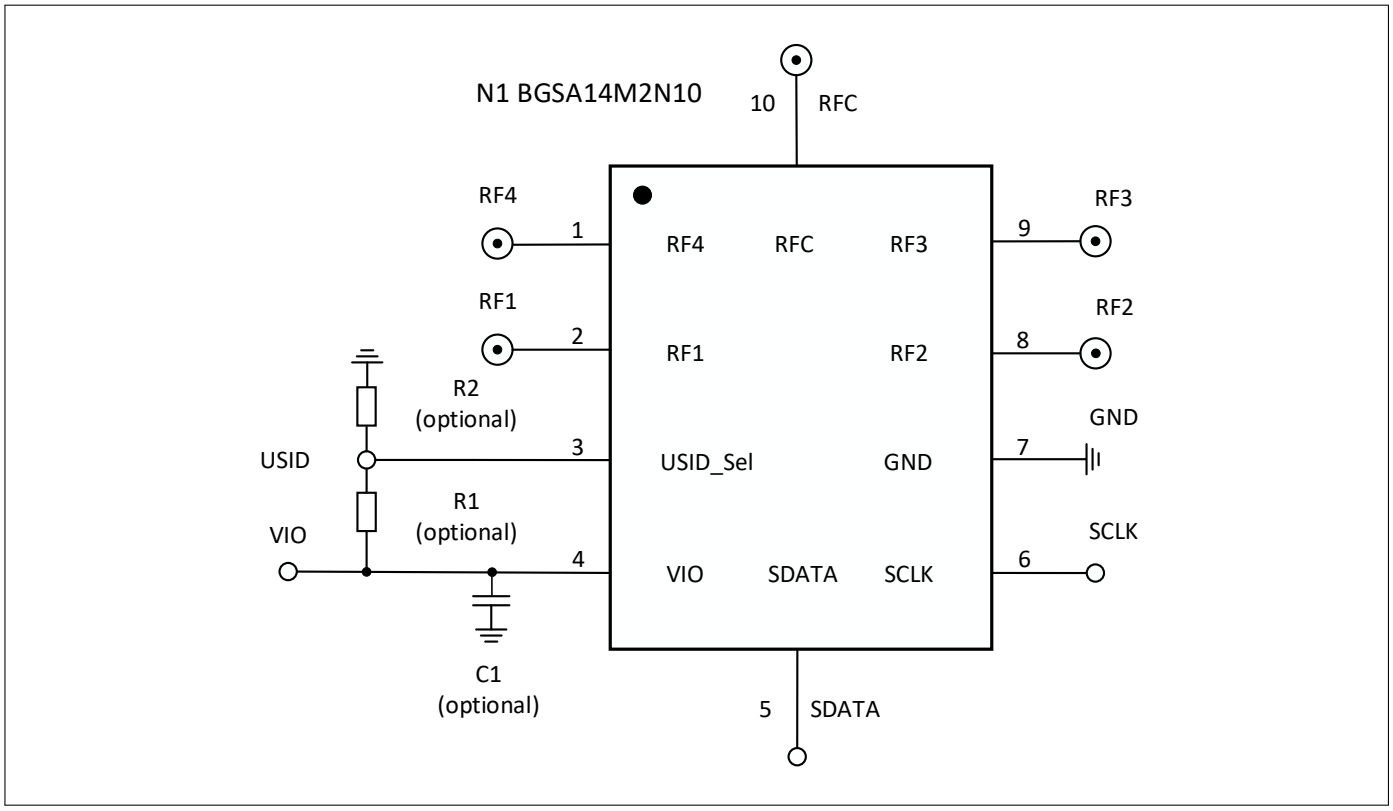

Figure 7: BGSA14M2N10 application schematic

Table 20: Bill of materials

Name	Part type	Package	Manufacturer	Function
C1 (1nF optional) [1)]	Capacitor	0402	Various	De-coupling capacitor
N1	BGSA14M2N10	TSNP-10-9/ TSNP-10-10	Infineon	Antenna tuner
R1 (0 Ω) R2 (do not place)	Resistor	0402	Various	Set USID default address to 6 (VIO)
R1 (do not place) R2 (0 Ω)	Resistor	0402	Various	Set USID default address to 7 (GND)
R1 (220 kΩ) R2 (0 Ω)	Resistor	0402	Various	Set USID default address to 8 (220 kΩ to VIO)
R1 (do not place) R2 (do not place)	Resistor	0402	Various	Set USID default address to 9 (FLOATING)

[1)] This capacitor is optional and value is only indicative. Decoupling capacitor value has to be chosen in order VIO ramp-up time is within MIPI RFFE version v2.1 specification

7 Package information

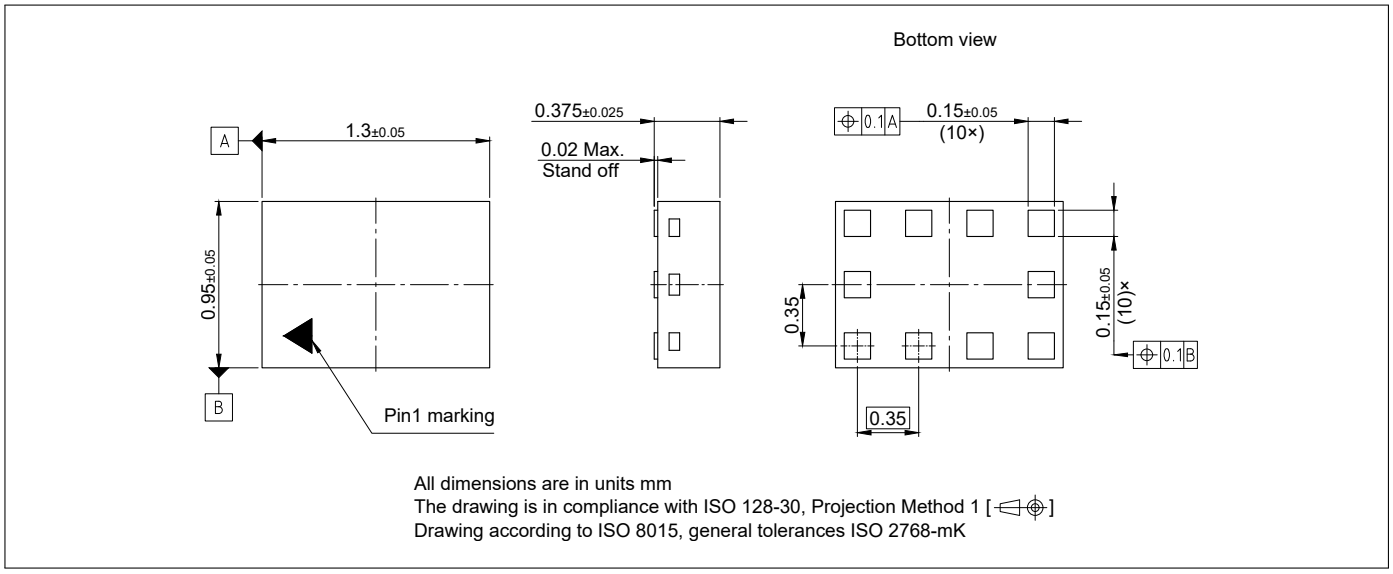

Figure 8: TSNP-10-9 package outline (top, side and bottom views)

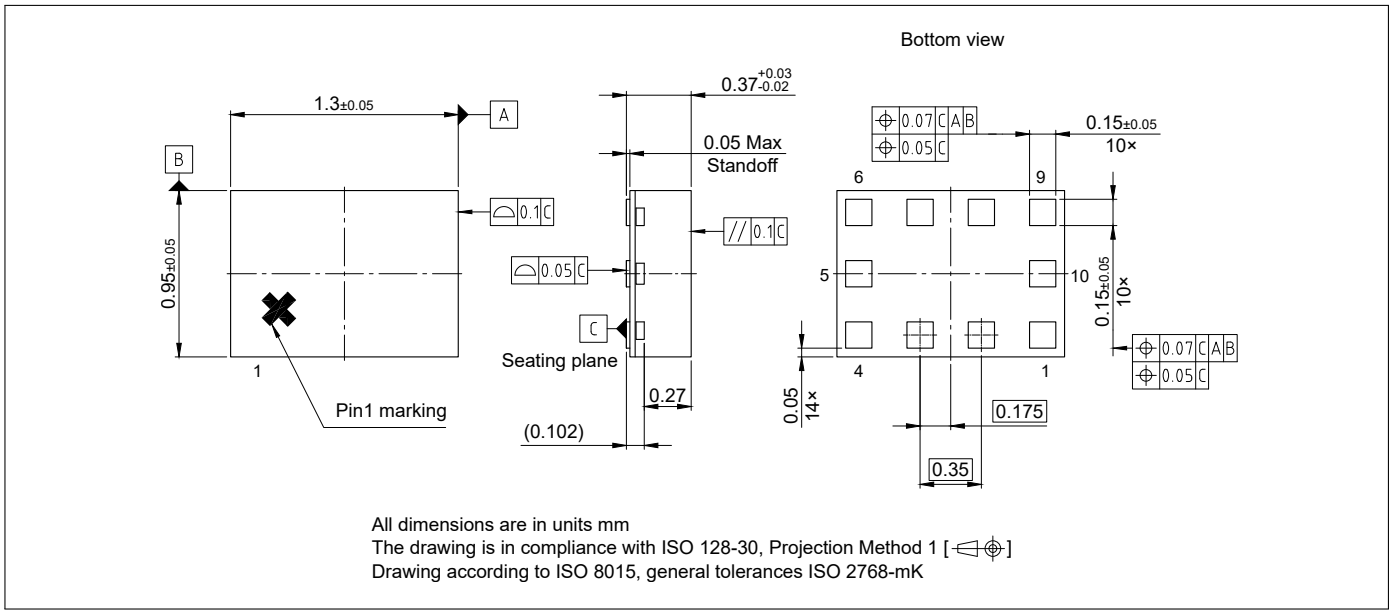

Figure 9: TSNP-10-10 package outline (top, side and bottom views)

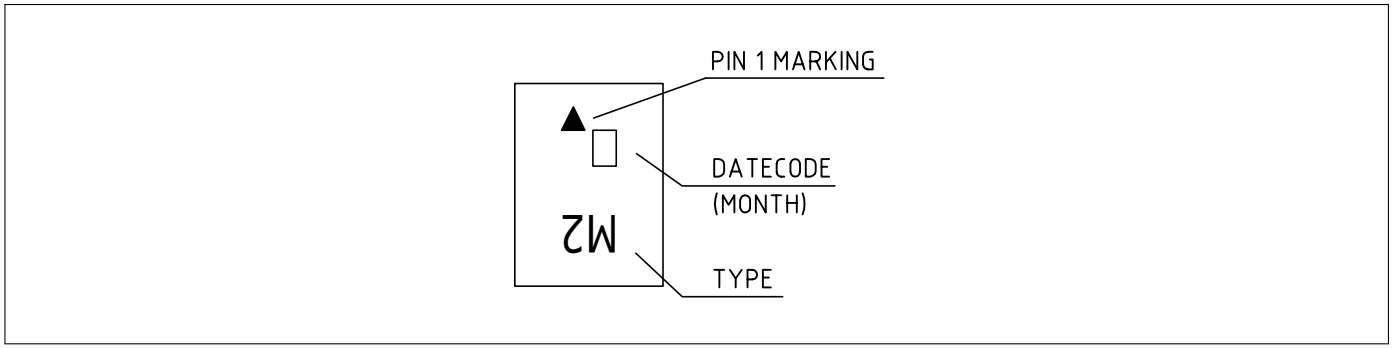

Figure 10: TSNP-10-9 marking specification (top view): month date code digit defined in Tab. 21

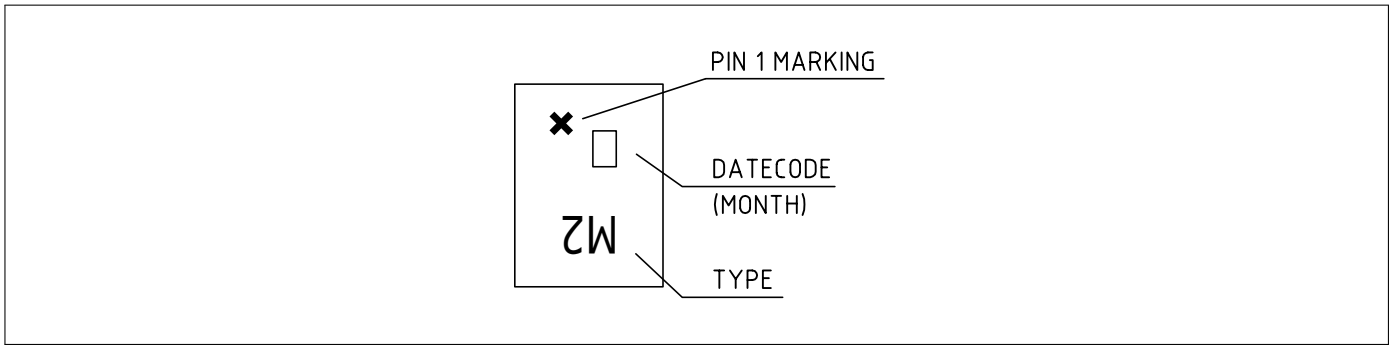

Figure 11: TSNP-10-10 marking specification (top view): month date code digit defined in Tab. 21

Table 21: Month date code marking - digit "M"

Month	2019	2020	2021	2022	2023	2024	2025	2026
01	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5

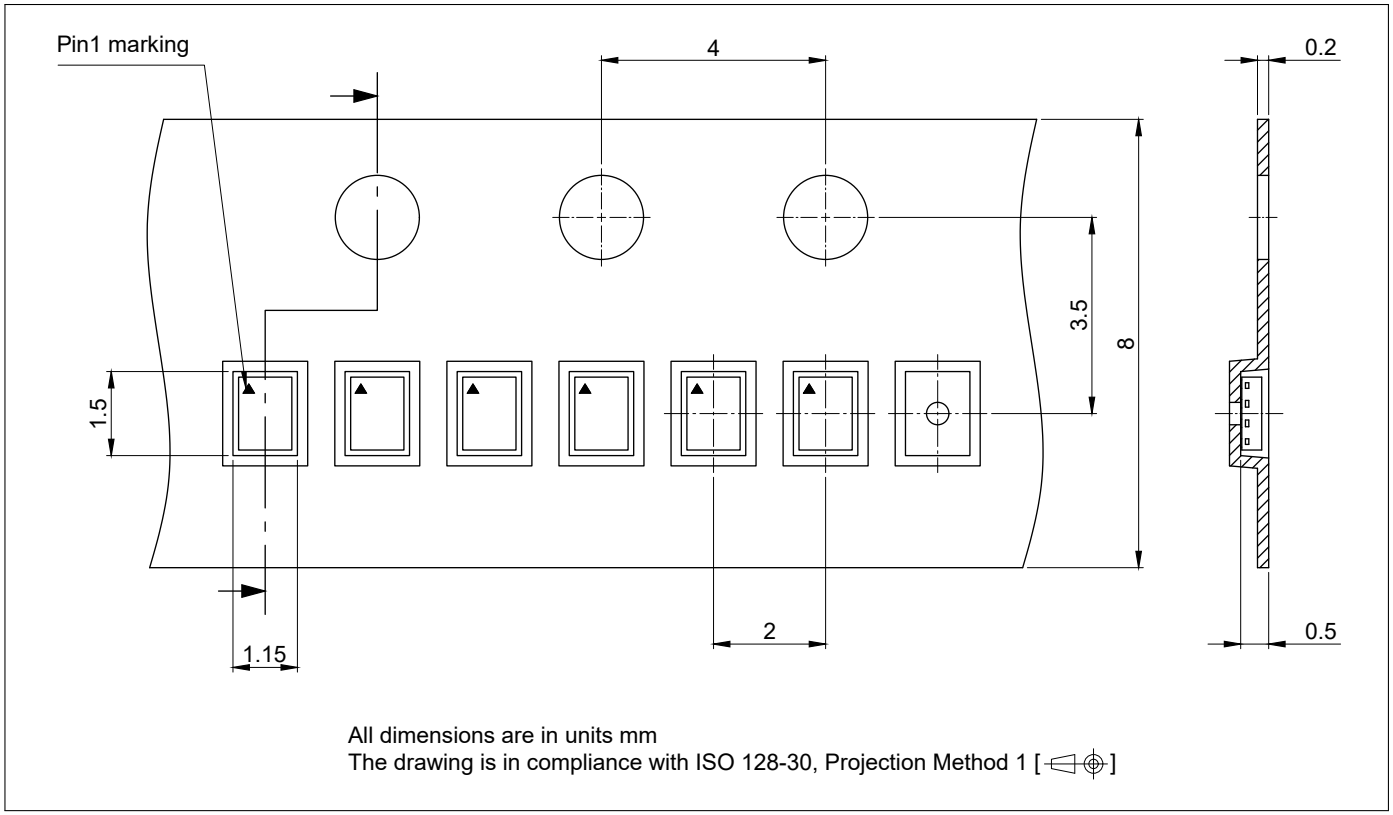

Figure 12: TSNP-10-9 carrier tape

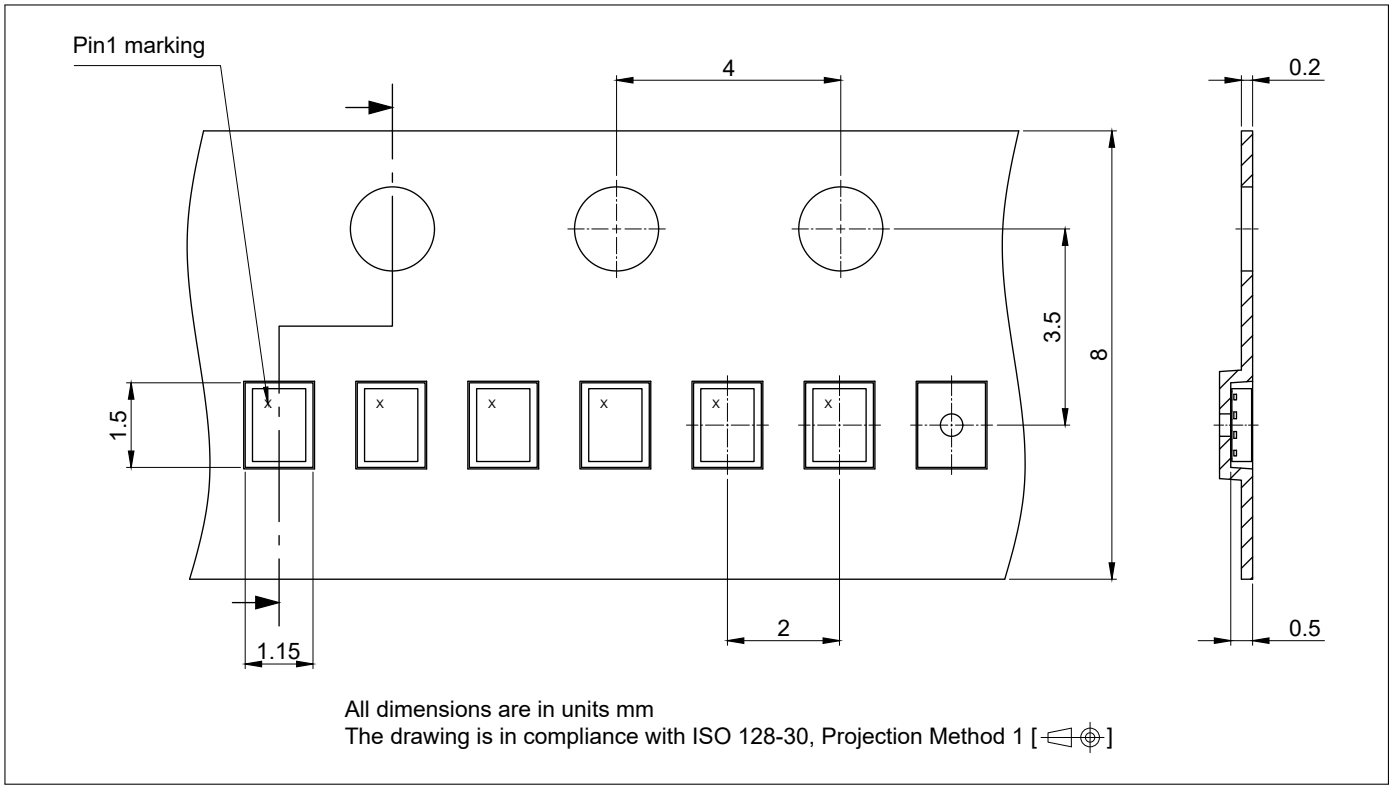

Figure 13: TSNP-10-10 carrier tape

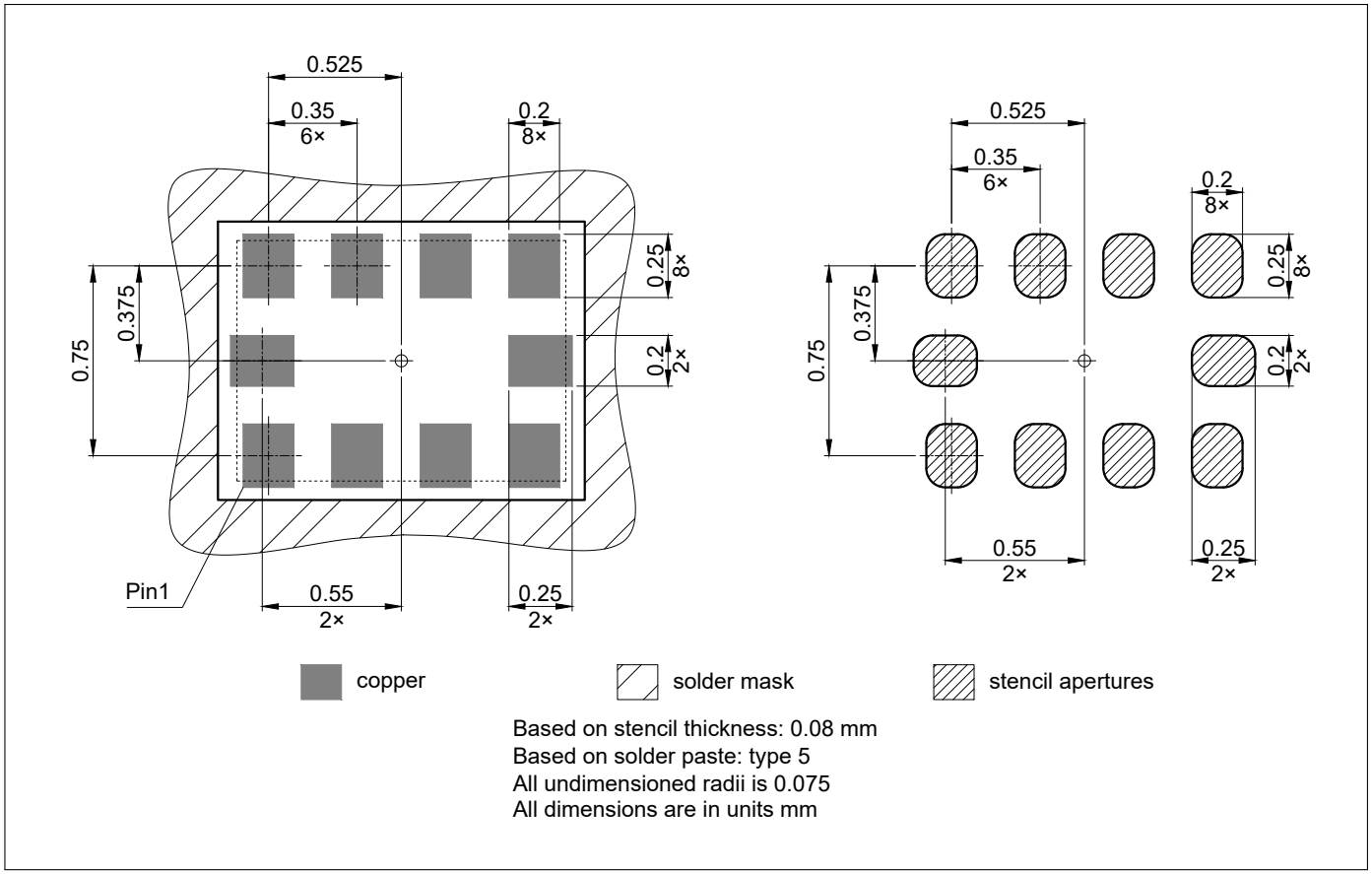

Figure 14: TSNP-10-9/TSNP-10-10 footprint recommendation

Revision history	
Page or item	**Subjects (major changes since previous revision)**
Revision 2.2, 2022-12-06	
8	Typo corrected in table 6

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