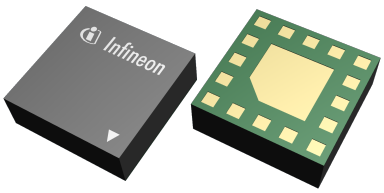
BGSX24M2U16

DP4T antenna cross switch with MIPI RFFE control interface

Features



- High linearity up to 39 dBm input power
- Fast switching time (max 2 µs) for 5G SRS applications
- Low insertion loss and high port-to-port isolation up to 7.125 GHz
- Fully compatible with MIPI 2.1 RFFE standard with 4 USIDs
- Low current consumption
- 1.2 V / 1.8 V V_{IO} support
- Software and hardware programmable USID
- Ultra low profile lead-less plastic package (MSL-1, 260 °C per IPC/JEDEC J-STD-20)

RoHS
Halogen-Free
Lead-Free
Green

Potential applications

- DP4T antenna routing/swapping for cellular mobile devices
- LTE and 5G applications

Product validation

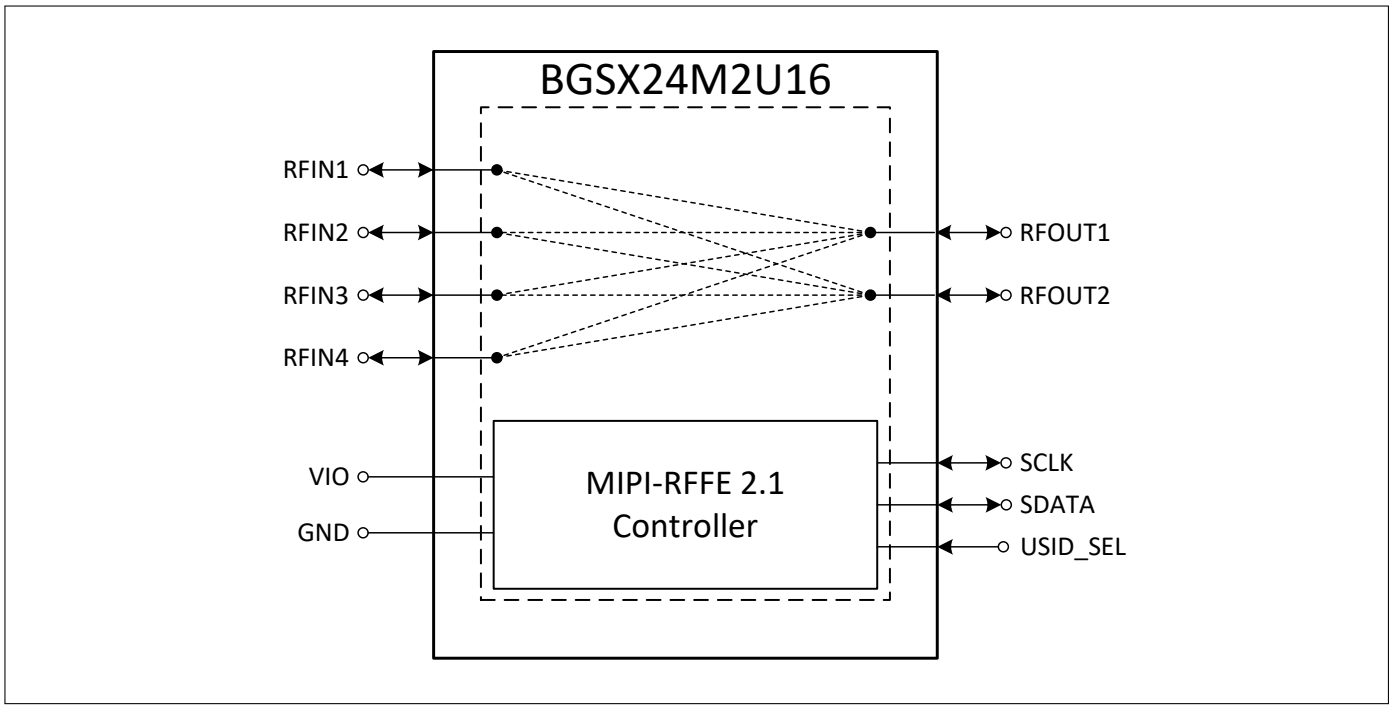
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The BGSX24M2U16 RF CMOS switch is specifically designed for LTE and 5G applications. This Dual Pole Four Throw (DP4T) cross-switch offers low insertion loss and low harmonic generation. The switch is controlled via a MIPI RFFE control interface. The on-chip controller permits very low power-supply voltage from 1.1 to 1.3V or the standard supply voltage from 1.65 to 1.95V. Unlike GaAs technology, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. The device has a very small size of only 2.0 mm x 2.0 mm and a thickness of 0.6 mm.

Type	Marking	Package	Ordering Information
BGSX24M2U16	X4	PG-ULGA-16-6	BGSX 24M2U16 E6327

Block diagram



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1 Absolute maximum ratings

Table 1: Absolute maximum ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Abs-Max RF input power	$P_{RF,max}$	–	–	39	dBm	Duty cycle of 25 %, through path, frequency 0.4–7.125 GHz, VSWR 1:1
ESD robustness, HBM [1]	$V_{ESD,HBM}$	-2	–	+2	kV	–
ESD robustness, CDM[2]	$V_{ESD,CDM}$	-1	–	+1	kV	–
Maximum DC-voltage on RF ports and RF-ground	V_{RFDC}	0	–	0	V	There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0 V
RFFE supply voltage	V_{IO}	-0.3	–	2.2	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}, V_{USID_SEL}	-0.3	–	V_{IO} + 0.5	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	-40	–	125	°C	–

[1] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[2] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

Warning: Stresses above the maximum values listed in Table 1 may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the maximum operation conditions specified in Table 2 may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 Operation ranges and general characteristics

Table 2: Operation ranges

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Max RF input power	$P_{RF,max}$	–	–	39	dBm	Peak envelope power of a 5G NR signal[1], through path, frequency 0.4–7.125 GHz, VSWR 1:1
		–	–	38	dBm	Pulsed RF input power, duty cycle of 25 % with T_{period} = 4615 µs, through path, frequency 0.4–7.125 GHz, VSWR 1:1
RFFE supply voltage	V_{IO}	1.1	1.2	1.3	V	MIPI 1.2 V bus
		1.65	1.8	1.95	V	MIPI 1.8 V bus
Ambient temperature	T_A	-40	25	85	°C	–

[1] MCS 27 (256 QAM) OFDM, 60 kHz sub carrier spacing, 100 MHz bandwidth, RMS power is 9 dB below peak power.

Table 3: General characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
RFFE supply current	I_{IO}	–	26	40	µA	ACTIVE mode, V_{IO} =1.2 V and P_{RF} = 0 dBm, no MIPI communication
		–	27	42	µA	ACTIVE mode, V_{IO} =1.8 V and P_{RF} = 0 dBm, no MIPI communication
		–	1.1	3.0	µA	SECONDARY_ACTIVE mode, P_{RF} = 0 dBm, no MIPI communication
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	2	3	pF	at SCLK, SDATA, and USID_SEL

[1] Valid for SDATA, SCLK, and USID_SEL

3 RF characteristics

Table 4: RF characteristics at T_A = −40 °C...85 °C, P_{RF} = 0 dBm, V_{IO} = 1.1 V...1.3 V and 1.65 V...1.95 V , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Insertion loss[1] at T_A = 25 °C						
RFINx — RFOUTy all other paths off x={1,..,4}and y={1,2}	$IL_{RFINx-RFOUTy}$	–	0.43	0.52	dB	617–960 MHz
		–	0.51	0.64	dB	1425–2200 MHz
		–	0.56	0.68	dB	2300–2690 MHz
		–	0.71	0.96	dB	3300–4200 MHz
		–	0.85	1.18	dB	4600–5000 MHz
		–	0.96	1.43	dB	5000–5925 MHz
		–	1.14	2.20	dB	5925–7125 MHz
Insertion loss[1]						
RFINx — RFOUTy all other paths off x={1,..,4}and y={1,2}	$IL_{RFINx-RFOUTy}$	–	0.43	0.60	dB	617–960 MHz
		–	0.51	0.72	dB	1425–2200 MHz
		–	0.56	0.75	dB	2300–2690 MHz
		–	0.71	1.03	dB	3300–4200 MHz
		–	0.85	1.29	dB	4600–5000 MHz
		–	0.96	1.59	dB	5000–5925 MHz
		–	1.14	2.35	dB	5925–7125 MHz
Return loss[1]						
RFINx — RFOUTy all other paths off x={1,..,4}and y={1,2}	$RL_{RFINx-RFOUTy}$	19	29	–	dB	617–960 MHz
		18	28	–	dB	1425–2200 MHz
		17	26	–	dB	2300–2690 MHz
		9	18	–	dB	3300–4200 MHz
		8	15	–	dB	4600–5000 MHz
		7	14	–	dB	5000–5925 MHz
		5	13	–	dB	5925–7125 MHz
Isolation[1]						
RFINx — RFOUTy x={1,..,4}and y={1,2}	$ISO_{RFINx-RFOUTy}$	36	47	–	dB	617–960 MHz
		30	41	–	dB	1425–2200 MHz
		29	38	–	dB	2300–2690 MHz
		27	36	–	dB	3300–4200 MHz
		27	36	–	dB	4600–5000 MHz
		25	36	–	dB	5000–5925 MHz
		21	35	–	dB	5925–7125 MHz

[1] Measured on application board, without any external matching components at RF ports.

Table 4: RF characteristics at T_A = −40 °C...85 °C, P_{RF} = 0 dBm, V_{IO} = 1.1 V...1.3 V and 1.65 V...1.95 V , unless otherwise specified (continued)

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Harmonic generation[1] at CW, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-82	-69	dBm	LTE LB, 663–915 MHz, P_{RF} = 26 dBm
		–	-74	-65	dBm	LTE MB, 1447–2020 MHz, P_{RF} = 26 dBm
		–	-71	-63	dBm	LTE HB, 2300–2690 MHz, P_{RF} = 26 dBm
		–	-67	-58	dBm	N77 NR, 3300–4200 MHz, P_{RF} = 26 dBm
		–	-69	-58	dBm	N79 NR, 4400–5000 MHz, P_{RF} = 26 dBm
3rd Harmonic	P_{H3}	–	-82	-70	dBm	LTE LB, 663–915 MHz, P_{RF} = 26 dBm
		–	-80	-73	dBm	LTE MB, 1447–2020 MHz, P_{RF} = 26 dBm
		–	-78	-70	dBm	LTE HB, 2300–2690 MHz, P_{RF} = 26 dBm
		–	-76	-68	dBm	N77 NR, 3300–4200 MHz, P_{RF} = 26 dBm
		–	-78	-71	dBm	N79 NR, 4400–5000 MHz, P_{RF} = 26 dBm
Harmonic generation[1] at 25 % duty cycle, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-63	-54	dBm	GSM LB, 824–915 MHz, P_{RF} = 35 dBm
		–	-61	-53	dBm	GSM HB, 1710–1910 MHz, P_{RF} = 33 dBm
3rd Harmonic	P_{H3}	–	-55	-49	dBm	GSM LB, 824–915 MHz, P_{RF} = 35 dBm
		–	-59	-51	dBm	GSM HB, 1710–1910 MHz, P_{RF} = 33 dBm
Intermodulation distortion IMD2[1]						
Band 1 IMD2 high	*IMD2*	–	-115	-108	dBm	Test conditions, see Table 5
Band 1 IMD2 low		–	-118	-109	dBm	
Band 5 IMD2 high		–	-123	-115	dBm	
Band 5 IMD2 low		–	-109	-96	dBm	
Band 7 IMD2 high		–	-113	-105	dBm	
Band 7 IMD2 low		–	-114	-102	dBm	
Band 3 + 5 IMD2 ULCA		–	-95	-87	dBm	
Band 3 + N77 IMD2 ENDC		–	-90	-82	dBm	

[1] Measured on application board, without any matching components at RF ports.

Table 4: RF characteristics at T_A = −40 °C...85 °C, P_{RF} = 0 dBm, V_{IO} = 1.1 V...1.3 V and 1.65 V...1.95 V , unless otherwise specified (continued)

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Intermodulation distortion IMD3[1]						
Band 1 IMD3 half duplex	*IMD3*	–	-124	-116	dBm	Test conditions, see Table 6
Band 1 IMD3 double duplex		–	-125	-115	dBm	
Band 5 IMD3 half duplex		–	-126	-117	dBm	
Band 5 IMD3 double duplex		–	-119	-112	dBm	
Band 7 IMD3 half duplex		–	-124	-113	dBm	
Band 7 IMD3 double duplex		–	-124	-114	dBm	
Band 1 + 3 IMD3 ULCA		–	-94	-84	dBm	
Band 5 + N77 IMD3 ENDC		–	-85	-78	dBm	

[1] Measured on application board, without any matching components at RF ports.

Table 5: IMD2 testcases[1]

Band	Symbol	In-band frequency (MHz)	Blocker frequency 1 (MHz)	Blocker power 1 (dBm)	Blocker frequency 2 (MHz)	Blocker power 2 (dBm)
Band 1	$B1_{IMD2,high}$	2140	1950	20	4090	-15
	$B1_{IMD2,low}$	2140	1950	20	190	-15
Band 5	$B5_{IMD2,high}$	881.5	836.5	20	1718	-15
	$B5_{IMD2,low}$	881.5	836.5	20	45	-15
Band 7	$B7_{IMD2,high}$	2655	2535	20	5190	-15
	$B7_{IMD2,low}$	2655	2535	20	120	-15
Band 3 + 5 IMD2 ULCA	$B3B5_{IMD2,ULCA}$	881.5	836.5	23	1718	10
Band 3 + N77 IMD2 ENDC	$B3N77_{IMD2,ENDC}$	1842.5	1747.5	23	3590	10

[1] Both blockers applied to same RF path.

Table 6: IMD3 testcases[1]

Band	Symbol	In-band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD3,\ half\ duplex}$	2140	1950	20	2045	-15
	$B1_{IMD3,\ double\ duplex}$	2140	1950	20	1760	-15
Band 5	$B5_{IMD3,\ half\ duplex}$	881.5	836.5	20	859	-15
	$B5_{IMD3,\ double\ duplex}$	881.5	836.5	20	791.5	-15
Band 7	$B7_{IMD3,\ half\ duplex}$	2655	2535	20	2595	-15
	$B7_{IMD3,\ double\ duplex}$	2655	2535	20	2415	-15
Band 1 + 3 IMD3 ULCA	$B1B3_{IMD3,ULCA}$	2140	1950	23	1760	10
Band 5 + N77 IMD3 ENDC	$B5N78_{IMD3,ENDC}$	2122	3780	23	829	10

[1] Both blockers applied to same RF path.

Table 7: Switching time[1] at T_A = −40 °C...85 °C, P_{RF} = 0 dBm, V_{IO} = 1.1 V...1.3 V and 1.65 V...1.95 V , unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Power up settling time	t_{PUP}	–	7	15	µs	Time from power up plus switch command, 50 % last SCLK falling edge to 90 % RF signal
Switching time	t_{ST}	–	1.3	2	µs	Time to switch between RF states, 50 % last SCLK falling edge to 90 % RF signal

[1] Measured on application board, without any external matching components at RF ports.

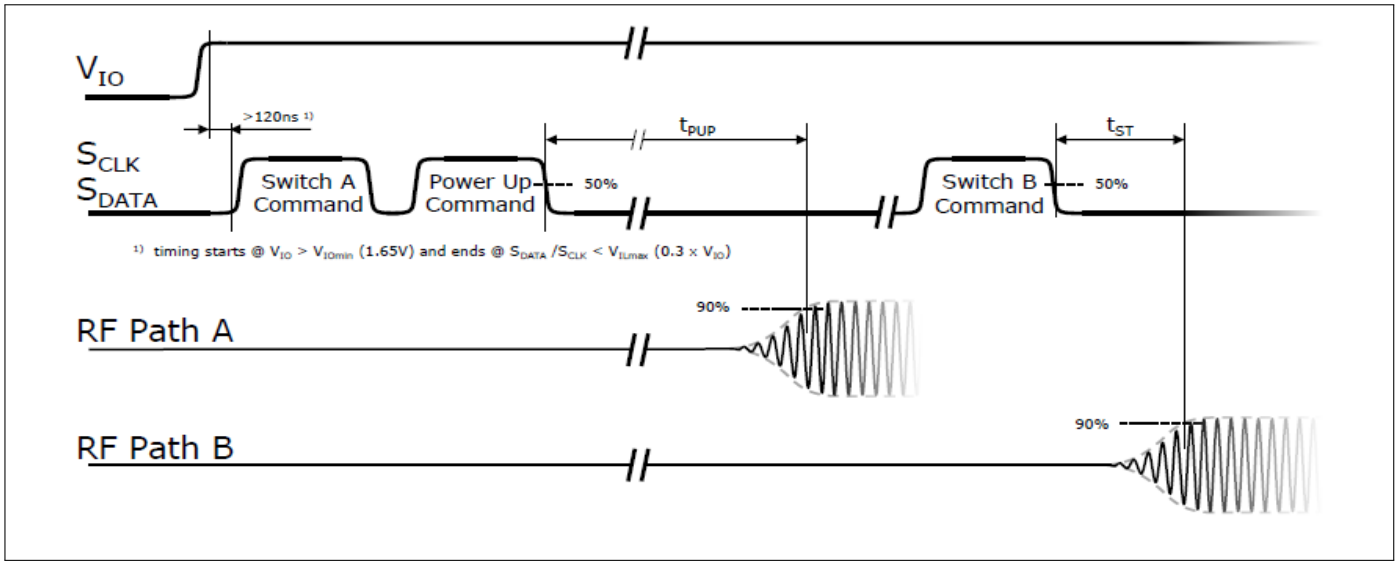

Figure 1: MIPI timing diagram

4 MIPI RFFE specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

Table 8: MIPI features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Standard reach RFFE bus length	Yes	RFFE Bus length of up to 15 cm (standard)
Longer reach RFFE bus length feature (MIPI RFFE 2.1 optional feature)	Yes	Longer reach allows for longer RFFE bus lengths. This requires a limitation to the standard frequency range of RFFE plus additional timing requirements for all devices on the bus
Programmable driver strength (MIPI RFFE 2.x feature)	Yes	Allows to program MIPI device bus driver strength (relevant for read back messages) up to 80 pF via BUS_LD-register (0x2B); Default value: 50 pF
Register 0 write command sequence	Yes	Shortened write sequence for register 0 Caution: only 7 LSBs in Reg 0 can be addressed
Register read and write command sequence	Yes	Standard register read/write procedure addressing standard register space of 0x00 – 0x1F
Extended register read and write command sequence	Yes	Register read/write procedure addressing extended register space of 0x00 – 0xFF
Masked write command sequence (MIPI 2.1 optional feature)	Yes	Allow only certain bits in a register to be updated during a write command. Relevant registers marked "MW" in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	SCLK range 32 kHz – 26 MHz for read and write commands
Support for extended frequency range operations for SCLK	Yes	SCLK range 26 MHz – 52 MHz for write commands
sRead (synchronous Read) full speed or half speed up to 26 MHz (MIPI 2.x feature)	Yes	Relaxed slave setup time requirements as master samples data on rising edge of SCLK signal
Regular read full speed or half speed up to 13 MHz (MIPI RFFE 1.10-2.x feature)	Yes	Stricter slave setup time requirements as master samples data on falling edge of SCLK signal
Product ID + extended product ID register	Yes	PRODUCT_ID (address 0x1D) and EXT_PRODUCT_ID (address 0x20) registers
Extended manufacturer ID (10->12 bit) (MIPI 2.1 optional feature)	Yes	The new 2 bits In MIPI 2.1 are placed in RFFE USID register at address 0x1F; value is 0 in IFX products
Revision ID register	Yes	This register contains the device revision (address 0x21)

Table 8: MIPI features (continued)

Feature	Supported	Comment
Programmable GSID (group slave identifier)	Yes	RFFE 2.x GROUP_SID register (at address 0x22); Only in case RFFE 1.1 backwards compatibility is supported: GROUP_SID0 bit-field access at address 0x1B (copy of GROUP_SID0)
Programmable USID (unique slave identifier)	Yes	Device can be also explicitly addressed via combination of (old) USID, Manufacturer ID, and (extended) product ID to reprogram USID via (extended) register write sequence (see MIPI RFFE Spec v2.1 Chapter 6.2.1)
Trigger functionality	Yes	3 "standard" triggers via PM_TRIG[5:0] consisting of 3 Mask- and 3 trigger bits
Ignored trigger handling in low power mode	No	When device is and stays in low power mode, write to trigger registers will be ignored (Note: when changing power mode, writing to trigger registers are not ignored)
Extended triggers and trigger masks (MIPI 2.1 optional feature)	Yes	additional eight triggers and the associated trigger masks, have been added in MIPI 2.1 (registers at addresses 0x2D and 0x2E)
Broadcast / GSID write to PM TRIG register	Yes	The above mentioned trigger register (and extended trigger register) can be accessed via Broadcast/GSID writes to trigger several MIPI devices snychronously. NOTE: Trigger Mask bits are nor changed with Broadcast/GSID writes
Reset	Yes	Reset is possible via VIO, PM TRIG or register SW_RST (0x23); NOTE: SW_RST only resets user defined registers, it does not reset the values of any reserved registers
Status / error sum register	Yes	RFFE 2.x ERR_SUM register (address 0x24); only in case RFFE 1.1 backwards compatibility is supported: RFFE_STATUS register access at address 0x1A (copy of ERR_SUM)
USID select via SDATA/SCLK swap feature	Yes	An alternate set of USIDs can be obtained by swapping SDATA/SCLK with the external pin (USID_SEL): see Table 9

Table 9: Default MIPI USID selection

USID	SCLK/SDATA swapping	USID_SEL	USID value (bin)	USID value (hex)
1	No	GND	1011	0xB
2	No	VIO	1010	0xA
3	Yes	GND	1001	0x9
4	Yes	VIO	1000	0x8

Table 10: Register mapping

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x00	SWITCH_CTRL_0	7:0	MODE_CTRL	Direct/cross mode selection. See logic table	00000000	No	Yes Trigger 0-10	R/W MW
0x01	SWITCH_CTRL_1	7:0	MODE_CTRL	Detailed mode selection. See logic table	00000000	No	Yes Trigger 0-10	R/W MW
0x02	SWITCH_CTRL_2	7:0	MODE_CTRL	Direct mapping mode selection. See logic table	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation mode	0: Normal operation (ACTIVE) 1: Low power mode (LOW POWER)	1	Yes	No	R/W MW
		6	PWR_MODE(0) State bit vector	0: No action (ACTIVE) 1: Powered reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow register) 1: Data not masked (ready for transfer to destination register)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow register) 1: Data not masked (ready for transfer to destination register)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow register) 1: Data not masked (ready for transfer to destination register)	0			
		2	TRIGGER_2	0: No action (data held in shadow register) 1: Data transferred to destination register	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow register) 1: Data transferred to destination register	0			
		0	TRIGGER_0	0: No action (data held in shadow register) 1: Data transferred to destination register	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11101111	n/a	n/a	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	n/a	n/a	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001	n/a	n/a	R
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID. These bits store the USID of the device.	See Table 9	No	No	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID	00000000	n/a	n/a	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0011	n/a	n/a	R
		3:0	SUB_REVISION	Chip sub revision	0001			
0x22	GSID	7:4	GSID0[3:0]	Primary group slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary group slave ID.	0000			

Table 10: Register mapping (continued)

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	n/a	n/a	R
		6	COMMAND_FRAME_PARITY_ERR	Command sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:4	RESERVED	Reserved for future use	0x0	No	No	R/W
		3:0	BUS_LD[3:0]	Program the drive strength of the SDATA driver in readback modes. 0x0: 10pF 0x1: 20pF 0x2: 30pF 0x3: 40pF 0x4: 50pF 0x5: 60pF 0x6: 80pF 0x7: 80pF 0x8-0xF: reserved	0x4			
0x2D	EXT_TRIG_MASK	7	EXT_TRIGGER_MASK_10	0: Data masked (held in shadow register)	1	No	No	R/W MW
				1: Data not masked (ready for transfer to destination register)				
		6	EXT_TRIGGER_MASK_9	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				
		5	EXT_TRIGGER_MASK_8	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				
		4	EXT_TRIGGER_MASK_7	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				
		3	EXT_TRIGGER_MASK_6	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				
		2	EXT_TRIGGER_MASK_5	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				
		1	EXT_TRIGGER_MASK_4	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				
		0	EXT_TRIGGER_MASK_3	0: Data masked (held in shadow register)	1			
				1: Data not masked (ready for transfer to destination register)				

Table 10: Register mapping (continued)

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x2E	EXT_TRIG	7	EXT_TRIGGER_10	0: No action (data held in shadow register)	0	Yes	No	R/W MW
				1: Data transferred to destination register				
		6	EXT_TRIGGER_9	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				
		5	EXT_TRIGGER_8	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				
		4	EXT_TRIGGER_7	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				
		3	EXT_TRIGGER_6	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				
		2	EXT_TRIGGER_5	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				
		1	EXT_TRIGGER_4	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				
		0	EXT_TRIGGER_3	0: No action (data held in shadow register)	0			
				1: Data transferred to destination register				

BGSX24M2U16 features a truth table shown in Table 14 which allows to connect multiple RFIN ports to any RFOUT port by combining individual states. As an example, all RFIN ports can be connected to RFOUT1 by combining states RFIN1-RFOUT1, RFIN2-RFOUT1, RFIN3-RFOUT1, and RFIN4-RFOUT1 by following register settings: SWITCH_CTRL_0 = 'xxxxxxxx', SWITCH_CTRL_1 = '00001111', and SWITCH_CTRL_2 = 'xxxxxxx1'.

Table 11: Truth table for operation mode selection

-	SWITCH_CTRL_0								SWITCH_CTRL_2							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
DP4T direct mode (enables Table 12)	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	0
DP4T cross mode (enables Table 13)	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	0
Direct mapping mode (enables Table 14)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

Table 12: Truth table for DP4T direct mode

-	SWITCH_CTRL_1							
Mode	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Isolation	x	x	0	0	0	0	0	0
RFIN1-RFOUT1;RFOUT2-Isolation	x	x	0	0	0	0	0	1
RFIN1-RFOUT1;RFIN2-RFOUT2	x	x	0	1	0	0	1	1
RFIN1-RFOUT1;RFIN3-RFOUT2	x	x	0	1	0	1	0	1
RFIN1-RFOUT1;RFIN4-RFOUT2	x	x	0	1	1	0	0	1
RFIN2-RFOUT1;RFOUT2-Isolation	x	x	0	0	0	0	1	0
RFIN2-RFOUT1;RFIN1-RFOUT2	x	x	1	0	0	0	1	1
RFIN2-RFOUT1;RFIN3-RFOUT2	x	x	0	1	0	1	1	0
RFIN2-RFOUT1;RFIN4-RFOUT2	x	x	0	1	1	0	1	0
RFIN3-RFOUT1;RFOUT2-Isolation	x	x	0	0	0	1	0	0
RFIN3-RFOUT1;RFIN1-RFOUT2	x	x	1	0	0	1	0	1
RFIN3-RFOUT1;RFIN2-RFOUT2	x	x	1	0	0	1	1	0
RFIN3-RFOUT1;RFIN4-RFOUT2	x	x	0	1	1	1	0	0
RFIN4-RFOUT1;RFOUT2-Isolation	x	x	0	0	1	0	0	0
RFIN4-RFOUT1;RFIN1-RFOUT2	x	x	1	0	1	0	0	1
RFIN4-RFOUT1;RFIN2-RFOUT2	x	x	1	0	1	0	1	0
RFIN4-RFOUT1;RFIN3-RFOUT2	x	x	1	0	1	1	0	0
RFIN1-RFOUT2;RFOUT1-Isolation	x	x	1	1	0	0	0	1
RFIN2-RFOUT2;RFOUT1-Isolation	x	x	1	1	0	0	1	0
RFIN3-RFOUT2;RFOUT1-Isolation	x	x	1	1	0	1	0	0
RFIN4-RFOUT2;RFOUT1-Isolation	x	x	1	1	1	0	0	0

Table 13: Truth table for DP4T cross mode

-	SWITCH_CTRL_1							
Mode	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Isolation	x	x	0	0	0	0	0	0
RFIN1-RFOUT2;RFOUT1-Isolation	x	x	0	0	0	0	0	1
RFIN1-RFOUT2;RFIN2-RFOUT1	x	x	0	1	0	0	1	1
RFIN1-RFOUT2;RFIN3-RFOUT1	x	x	0	1	0	1	0	1
RFIN1-RFOUT2;RFIN4-RFOUT1	x	x	0	1	1	0	0	1
RFIN2-RFOUT2;RFOUT1-Isolation	x	x	0	0	0	0	1	0
RFIN2-RFOUT2;RFIN1-RFOUT1	x	x	1	0	0	0	1	1
RFIN2-RFOUT2;RFIN3-RFOUT1	x	x	0	1	0	1	1	0
RFIN2-RFOUT2;RFIN4-RFOUT1	x	x	0	1	1	0	1	0
RFIN3-RFOUT2;RFOUT1-Isolation	x	x	0	0	0	1	0	0
RFIN3-RFOUT2;RFIN1-RFOUT1	x	x	1	0	0	1	0	1
RFIN3-RFOUT2;RFIN2-RFOUT1	x	x	1	0	0	1	1	0
RFIN3-RFOUT2;RFIN4-RFOUT1	x	x	0	1	1	1	0	0
RFIN4-RFOUT2;RFOUT1-Isolation	x	x	0	0	1	0	0	0
RFIN4-RFOUT2;RFIN1-RFOUT1	x	x	1	0	1	0	0	1
RFIN4-RFOUT2;RFIN2-RFOUT1	x	x	1	0	1	0	1	0
RFIN4-RFOUT2;RFIN3-RFOUT1	x	x	1	0	1	1	0	0
RFIN1-RFOUT1;RFOUT2-Isolation	x	x	1	1	0	0	0	1
RFIN2-RFOUT1;RFOUT2-Isolation	x	x	1	1	0	0	1	0
RFIN3-RFOUT1;RFOUT2-Isolation	x	x	1	1	0	1	0	0
RFIN4-RFOUT1;RFOUT2-Isolation	x	x	1	1	1	0	0	0

Table 14: Truth table for direct mapping mode

-	SWITCH_CTRL_1							
Mode	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RFIN1-RFOUT1 Isolation	x	x	x	x	x	x	x	0
RFIN1-RFOUT1	x	x	x	x	x	x	x	1
RFIN2-RFOUT1 Isolation	x	x	x	x	x	x	0	x
RFIN2-RFOUT1	x	x	x	x	x	x	1	x
RFIN3-RFOUT1 Isolation	x	x	x	x	x	0	x	x
RFIN3-RFOUT1	x	x	x	x	x	1	x	x
RFIN4-RFOUT1Isolation	x	x	x	x	0	x	x	x
RFIN4-RFOUT1	x	x	x	x	1	x	x	x
RFIN1-RFOUT2 Isolation	x	x	x	0	x	x	x	x
RFIN1-RFOUT2	x	x	x	1	x	x	x	x
RFIN2-RFOUT2 Isolation	x	x	0	x	x	x	x	x
RFIN2-RFOUT2	x	x	1	x	x	x	x	x
RFIN3-RFOUT2 Isolation	x	0	x	x	x	x	x	x
RFIN3-RFOUT2	x	1	x	x	x	x	x	x
RFIN4-RFOUT2 Isolation	0	x	x	x	x	x	x	x
RFIN4-RFOUT2	1	x	x	x	x	x	x	x

5 Application information

Pin configuration and function

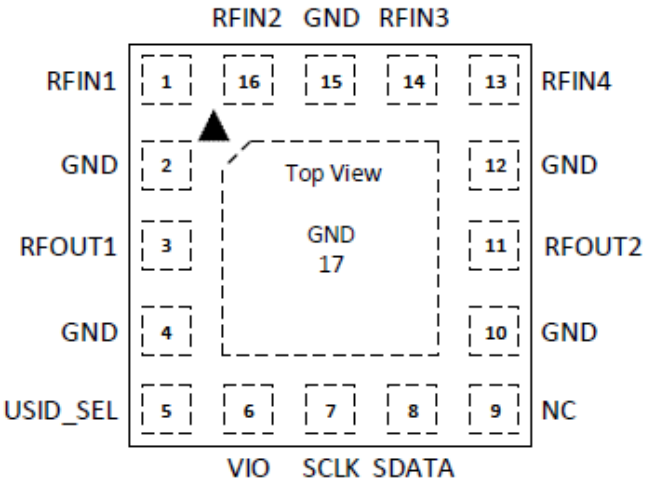

Figure 2: Footprint (top view)

Table 15: Pin definition and function

Pin No.	Name	Function
1	RFIN1	RF input 1
2	GND	Ground
3	RFOUT1	RF output 1
4	GND	Ground
5	USID_SEL	MIPI USID select pin (to be connected to VIO or GND)
6	VIO	MIPI RFFE supply
7	SCLK	MIPI RFFE clock
8	SDATA	MIPI RFFE data
9	NC	Not connected
10	GND	Ground
11	RFOUT2	RF output 2
12	GND	Ground
13	RFIN4	RF input 4
14	RFIN3	RF input 3
15	GND	Ground
16	RFIN2	RF input 2
17	GND	Ground

Application circuit

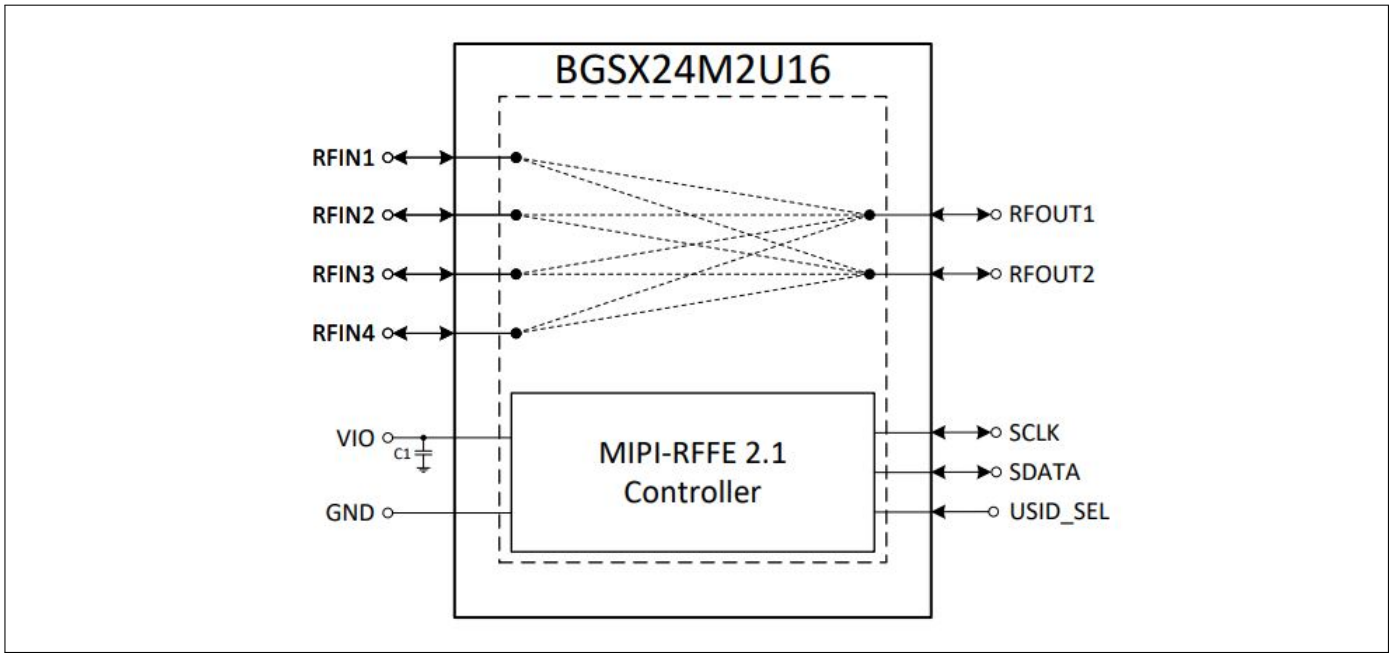

Figure 3: BGSX24M2U16 application schematic

Table 16: Bill of materials

Name	Value	Package	Manufacturer	Function
C1	10 nF	0201	Various	DC coupling

6 Package Information

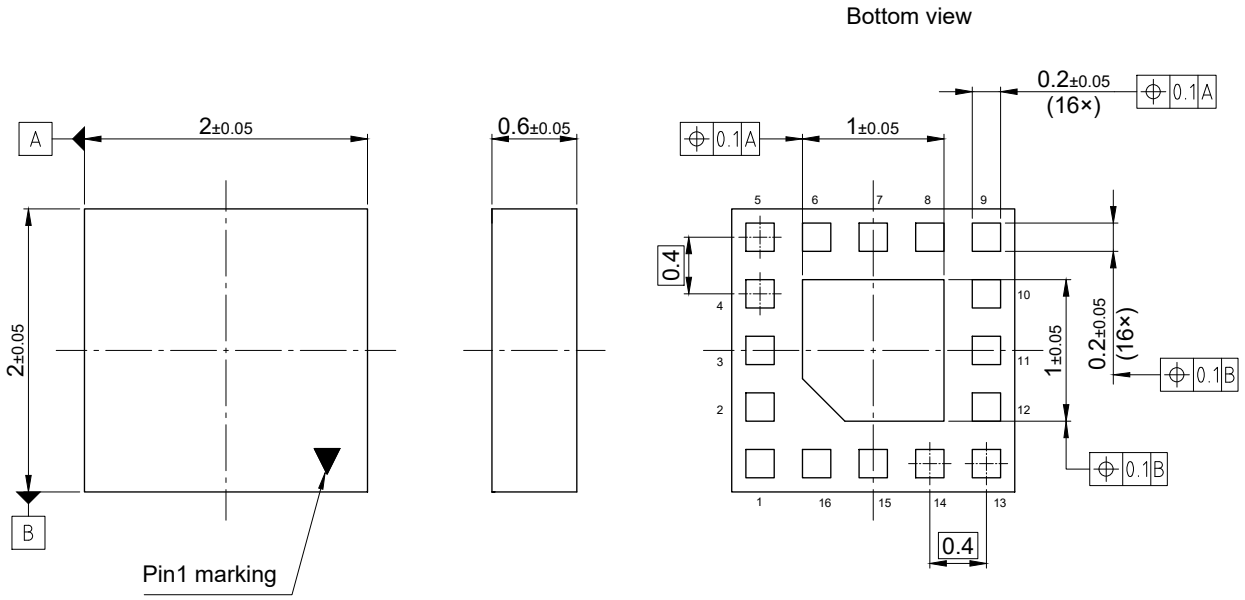

Figure 4: PG-ULGA-16-6 package outline drawing (top, side and bottom views)

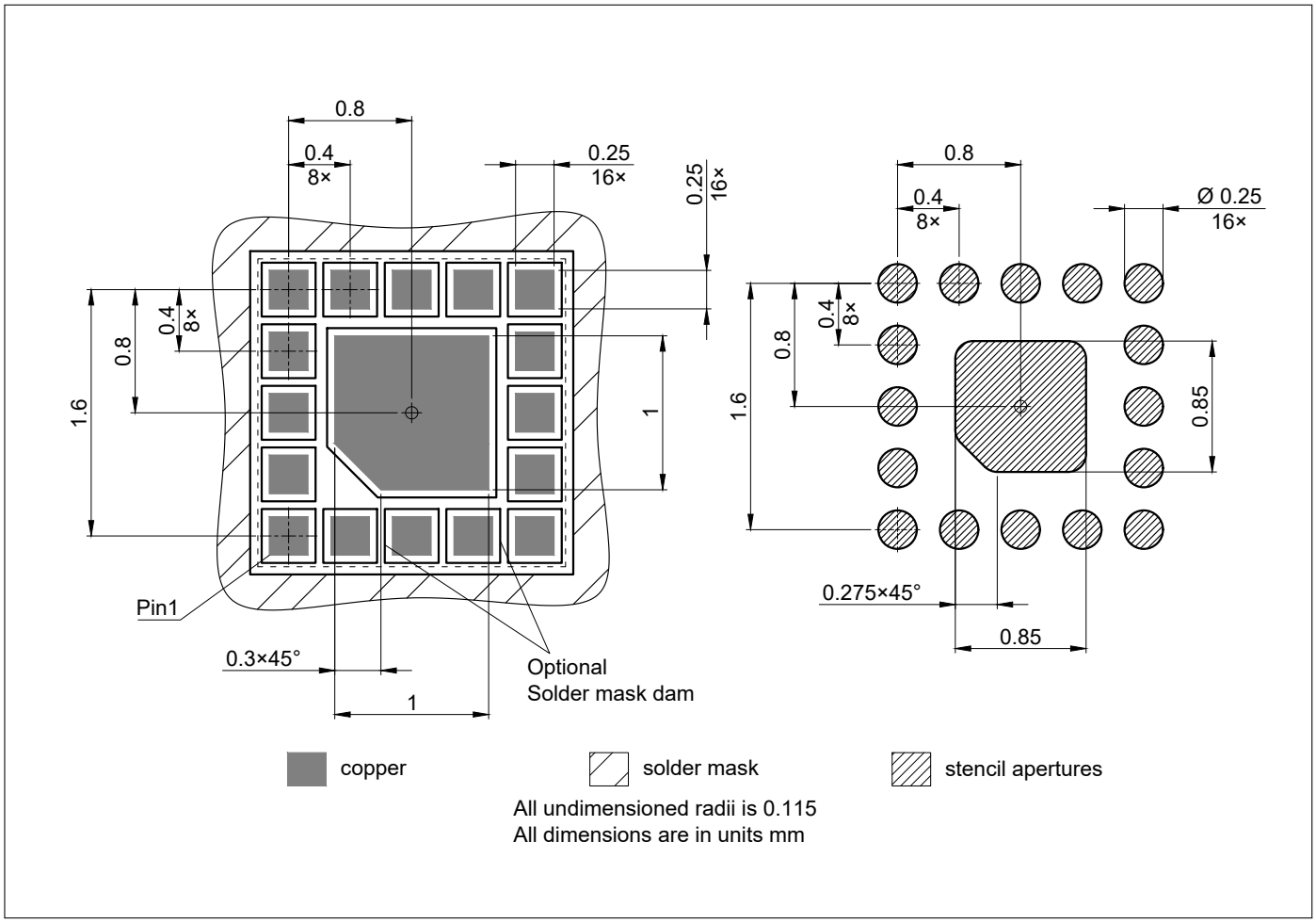

Figure 5: Footprint recommendation

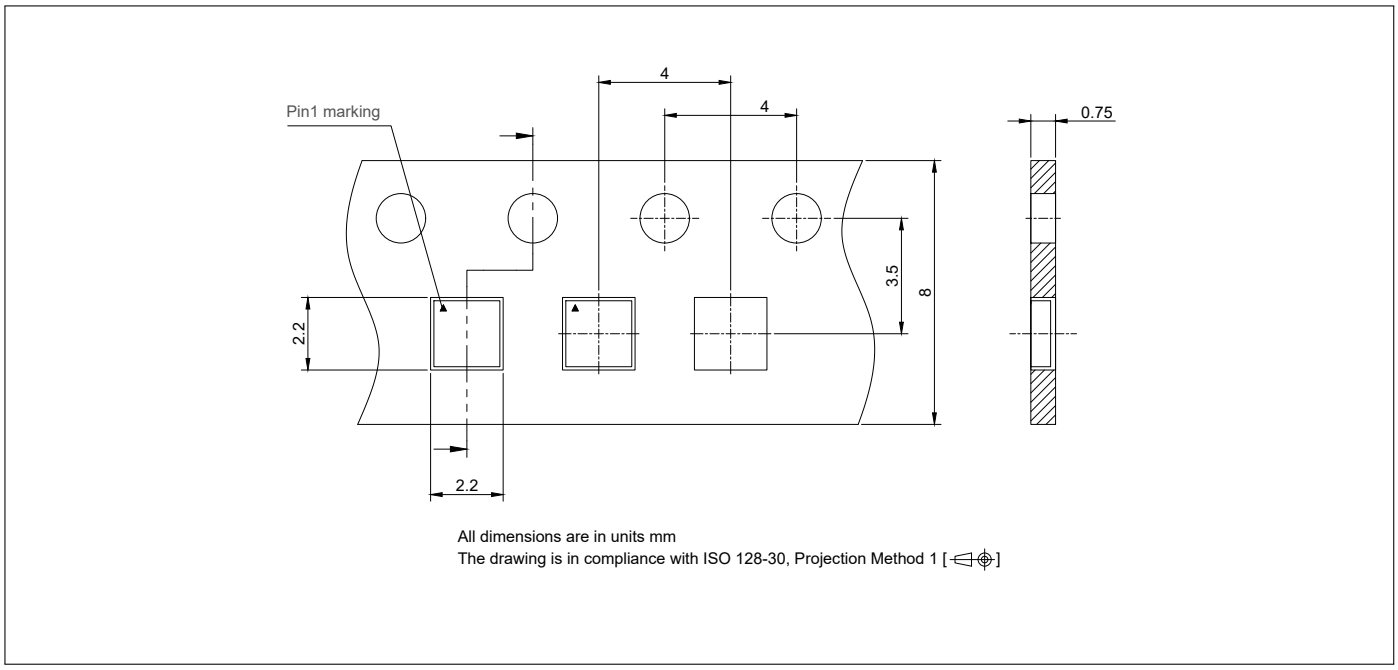

Figure 6: PG-ULGA-16-6 carrier tape drawing (top and side views)

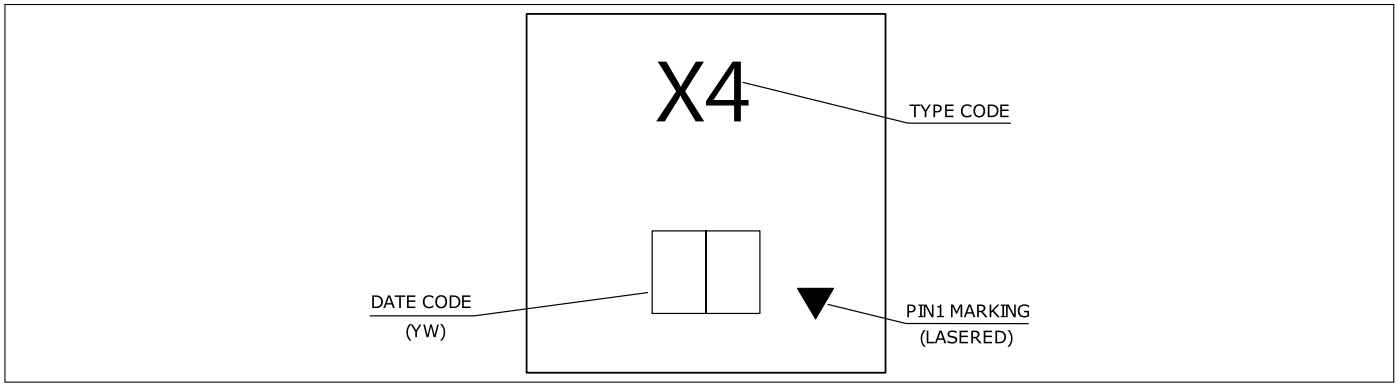

Figure 7: PG-ULGA-16-6 marking specification (top view): date code digits Y and W defined in Table 17 and 18

Table 17: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 18: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

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