

## MOSFET

### OptiMOS™ Power-MOSFET, 40 V

#### Features

- Optimized for synchronous rectification
- 175°C rated
- Very low on-resistance  $R_{DS(on)}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection

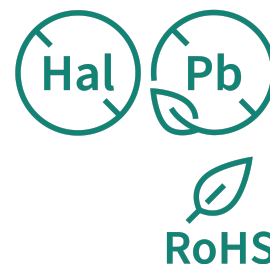
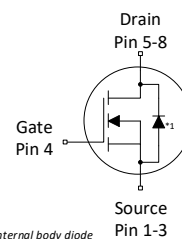
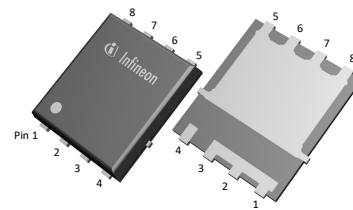
#### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	40	V
$R_{DS(on),max}$	1.0	mΩ
$I_D$	292	A
$Q_{OSS}$	84	nC
$Q_g(0V..10V)$	95	nC

PG-TDSON-8



Type/Ordering Code	Package	Marking	Related Links
BSC010N04LS	PG-TDSON-8	010N04LS	-



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## 1 Maximum ratings

unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	292	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
				206		
				256		
				181		
				39		
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	1168	A	$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	-	-	50	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	330	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage <sup>5)</sup>	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	167	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
				3.0		
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

<sup>5)</sup> The negative rating is for low duty cycle pulse occurrence. No continuous rating is implied

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>6)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>6)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.0 0.85	1.3 1.0	m $\Omega$	$V_{GS}=4.5\text{ V}, I_D=50\text{ A}$ $V_{GS}=10\text{ V}, I_D=50\text{ A}$
Gate resistance <sup>7)</sup>	$R_G$	-	0.8	1.6	$\Omega$	-
Transconductance	$g_{fs}$	140	270	-	S	$ V_{DS} >2 I_D  R_{DS(on)max}, I_D=50\text{ A}$

<sup>7)</sup> Defined by design. Not subject to production test

**Table 5 Dynamic characteristics <sup>8)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	6800	9520	pF	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	1900	2660	pF	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	160	320	pF	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	12	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	46	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	9	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=1.6\text{ }\Omega$

<sup>8)</sup> Defined by design. Not subject to production test

**Table 6 Gate charge characteristics <sup>9)</sup>**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	16	-	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	11	-	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	15	21	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$

**Table 6 Gate charge characteristics** <sup>9)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Switching charge	$Q_{sw}$	-	21	-	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	-	95	133	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.4	-	V	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	-	49	69	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	84	-	nC	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	84	118	nC	$V_{DD}=20\text{ V}, V_{GS}=0\text{ V}$

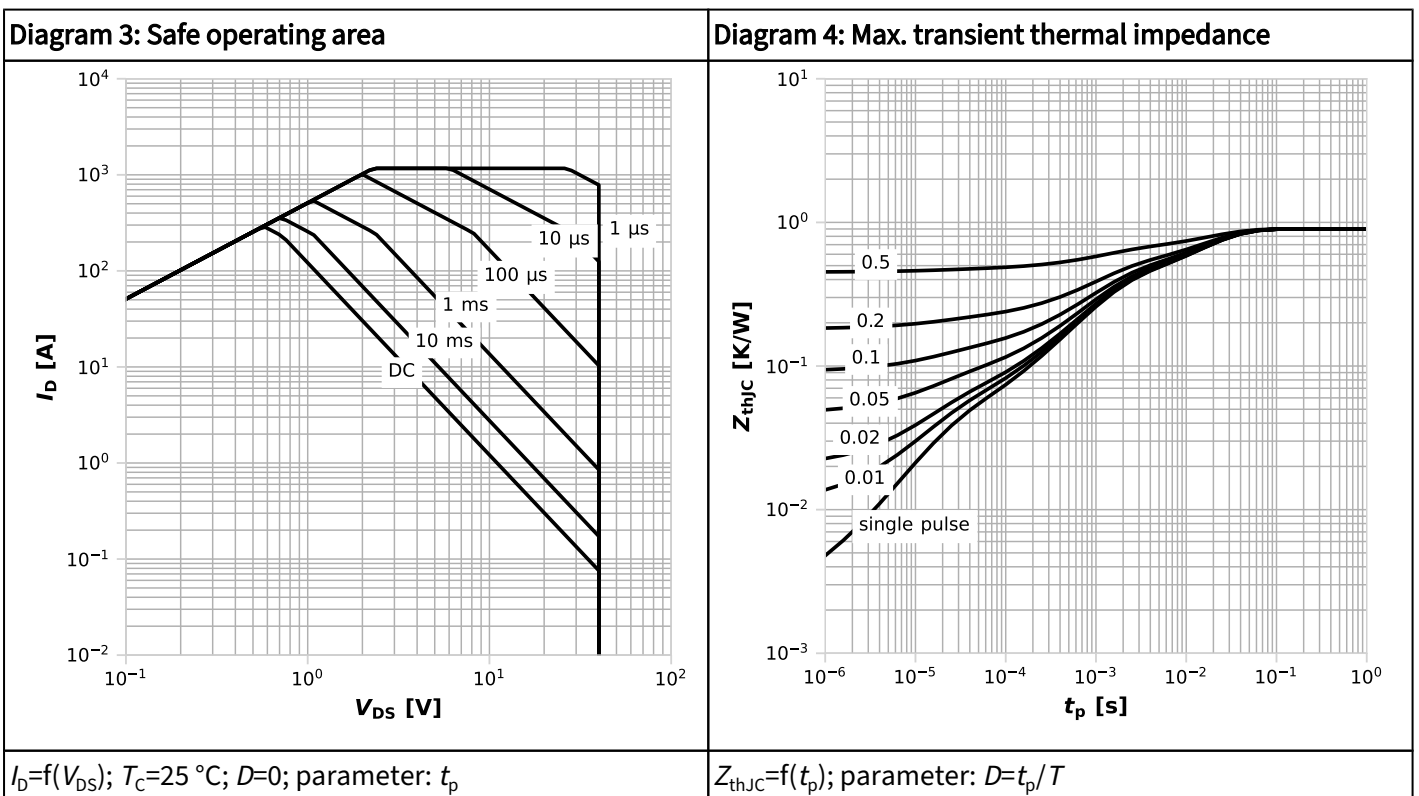
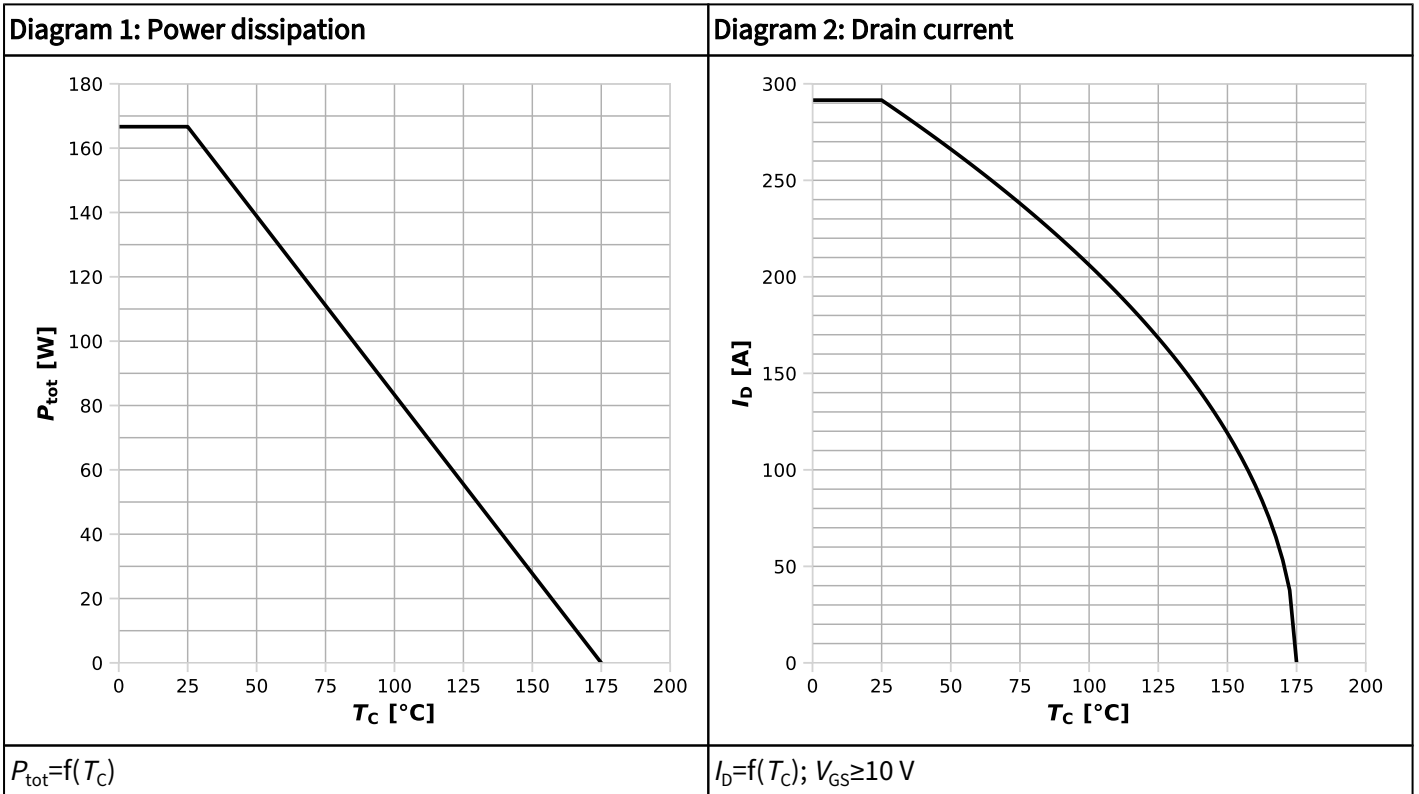
<sup>9)</sup> See "Gate charge waveforms" for parameter definition. Defined by design. Not subject to production test

**Table 7 Reverse diode**

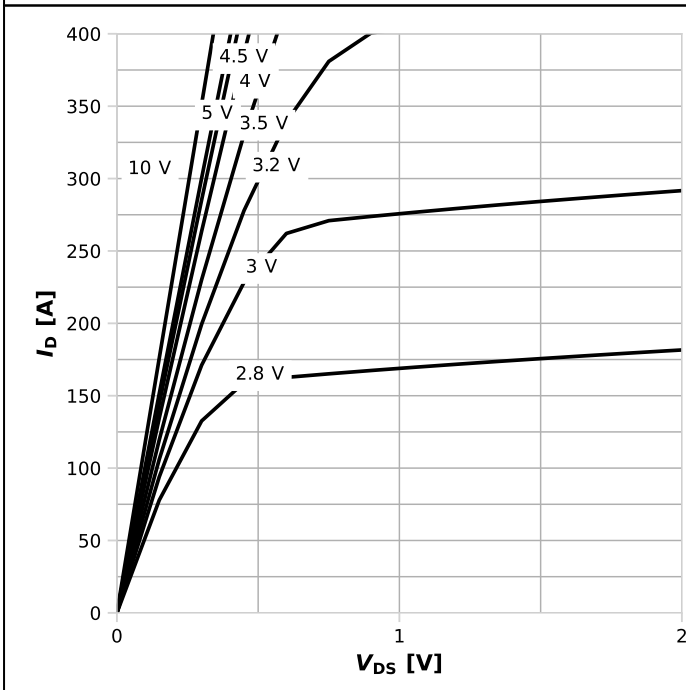
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	167	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1168	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.81	1	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>10)</sup>	$t_{rr}$	-	36	72	ns	$V_R=20\text{ V}, I_F=50\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>10)</sup>	$Q_{rr}$	-	50	-	nC	$V_R=15\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$

<sup>10)</sup> Defined by design. Not subject to production test

## 4 Electrical characteristics diagrams

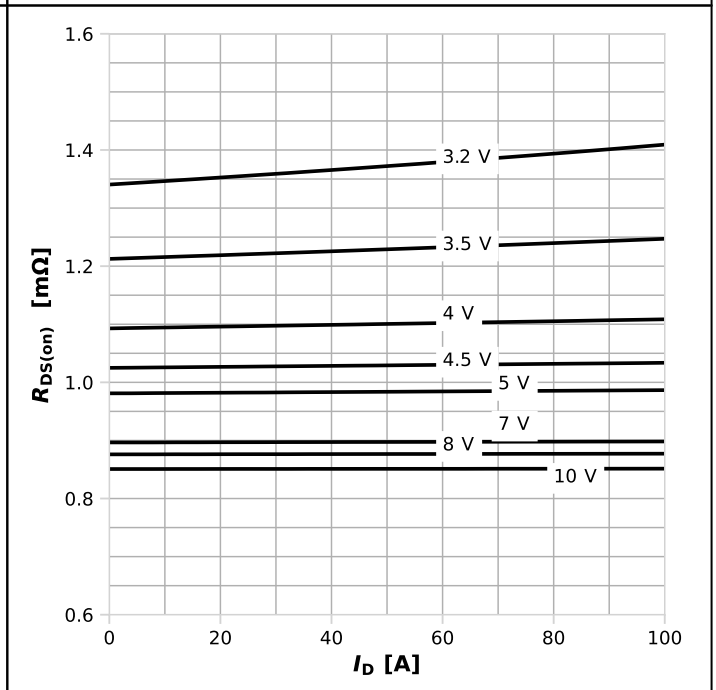


**Diagram 5: Typ. output characteristics**



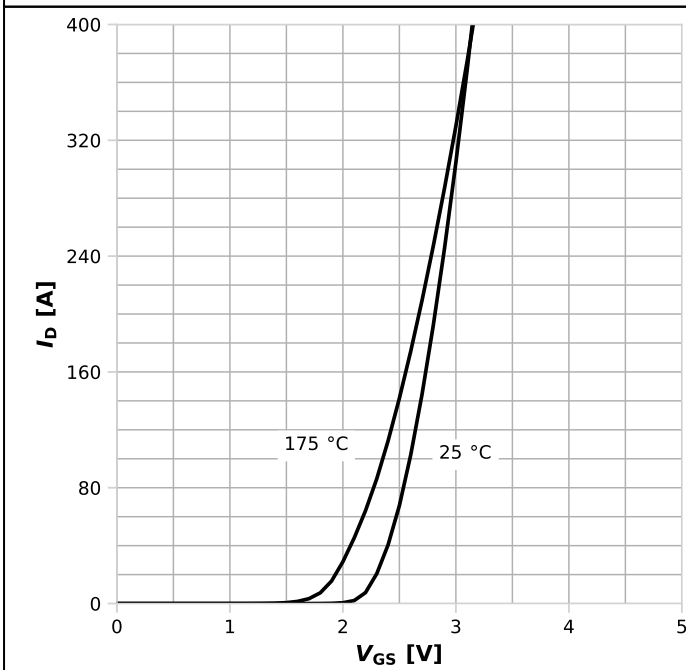
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



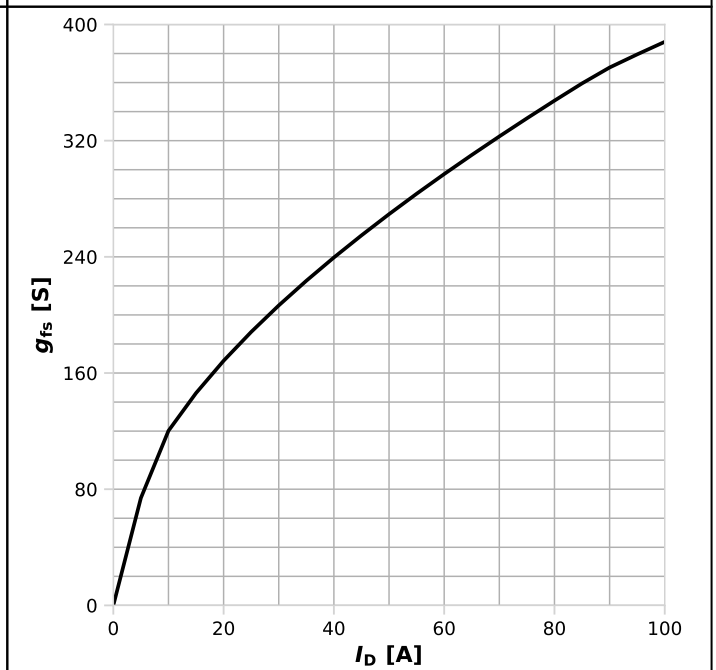
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

**Diagram 7: Typ. transfer characteristics**



$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

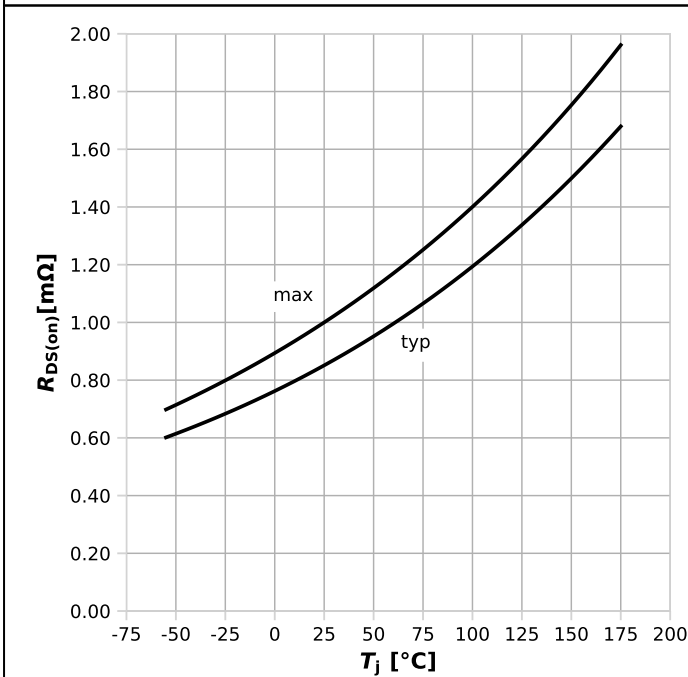
**Diagram 8: Typ. forward transconductance**



$g_{fs} = f(I_D); T_j = 25\text{ °C}$

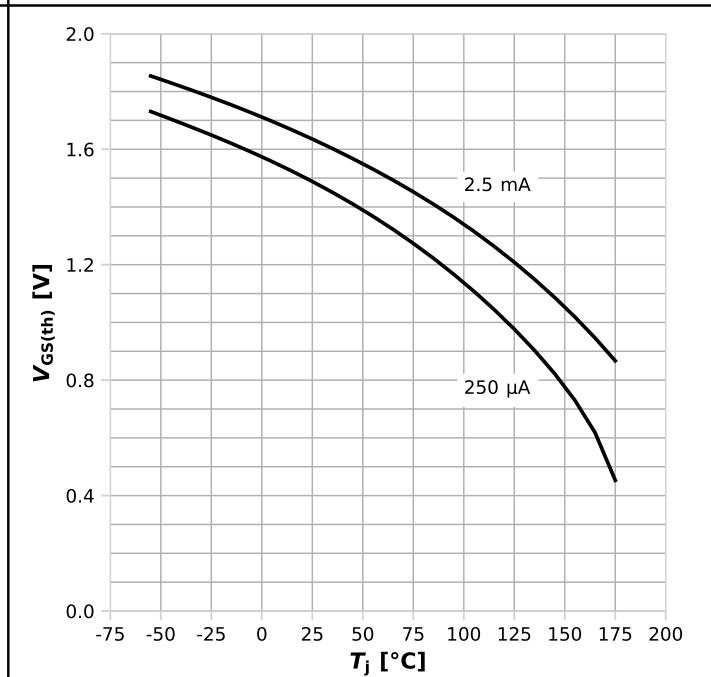


Diagram 9: Drain-source on-state resistance



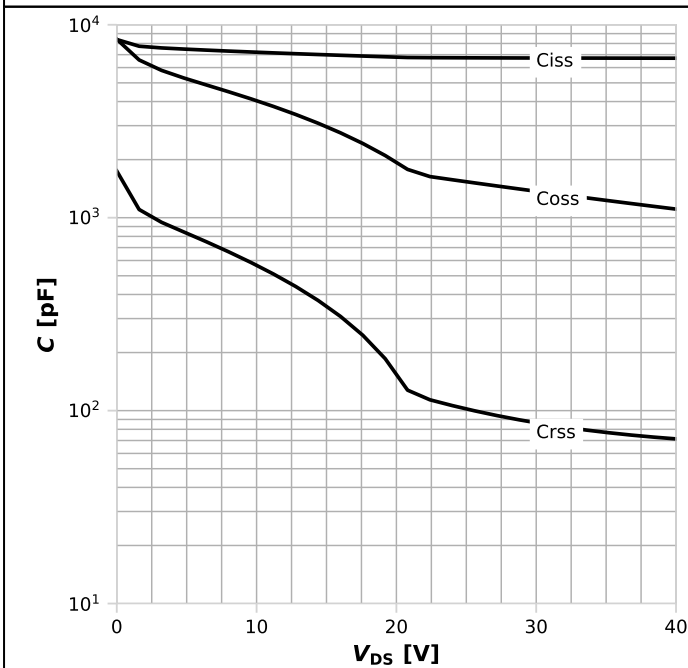
$$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



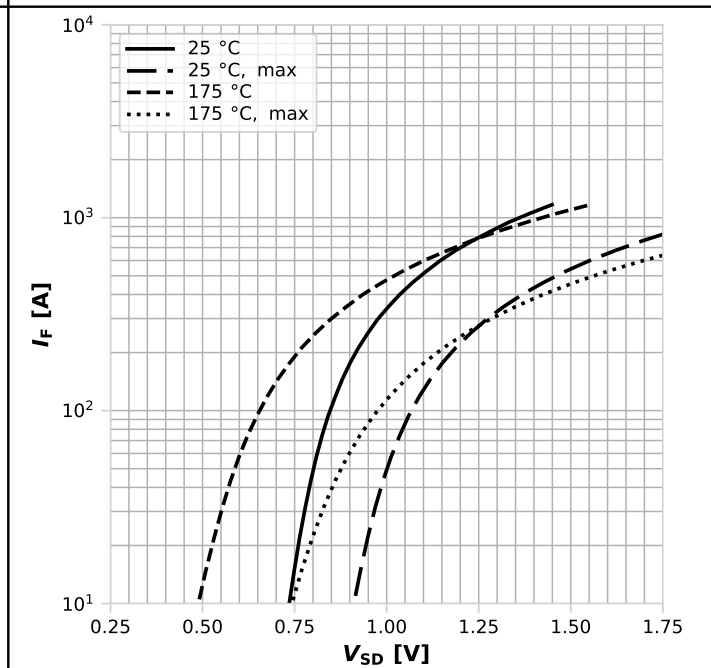
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{parameter: } I_D$$

Diagram 11: Typ. capacitances



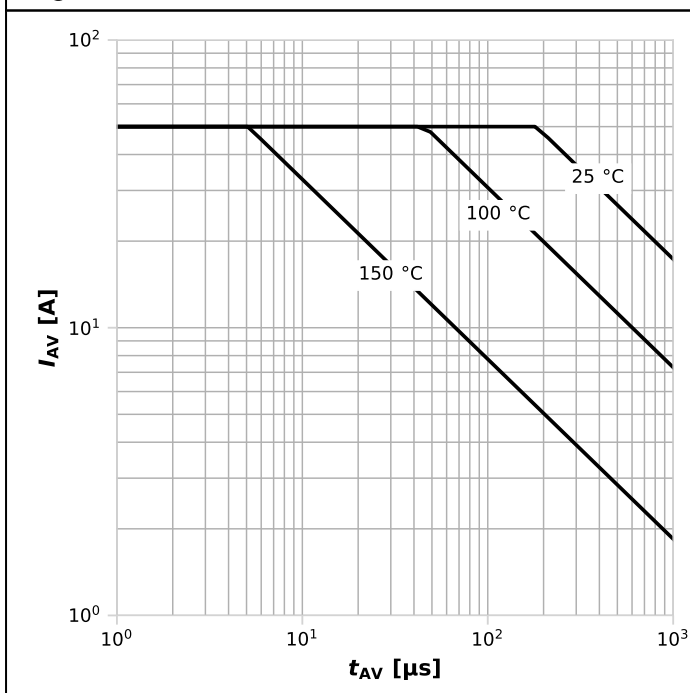
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



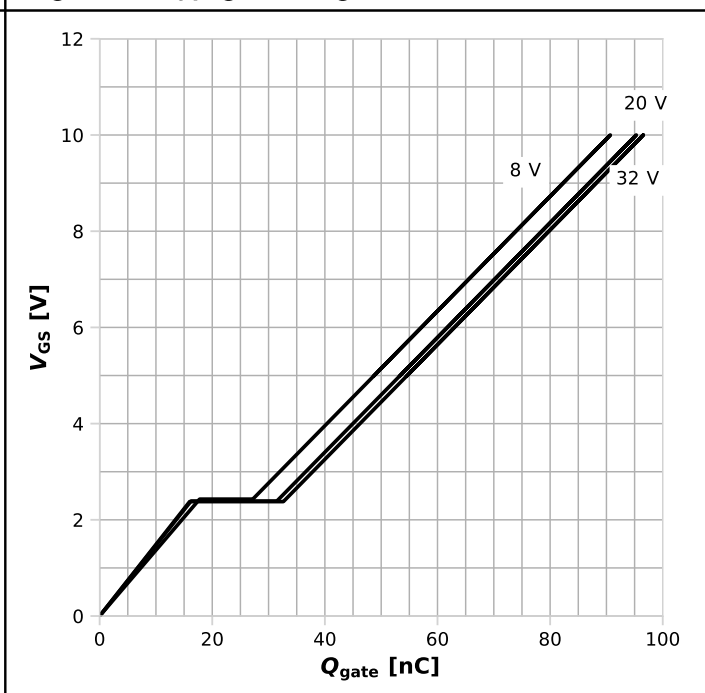
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

**Diagram 13: Avalanche characteristics**



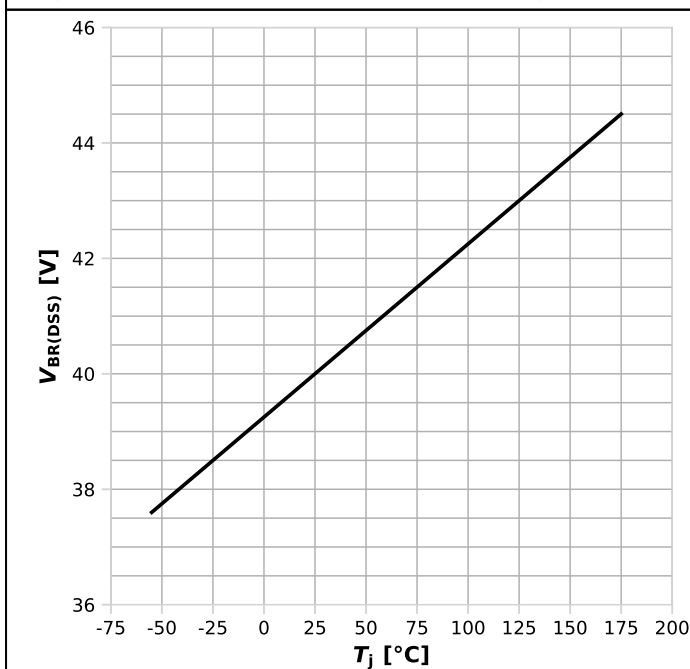
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega; \text{parameter: } T_{j(\text{start})}$

**Diagram 14: Typ. gate charge**



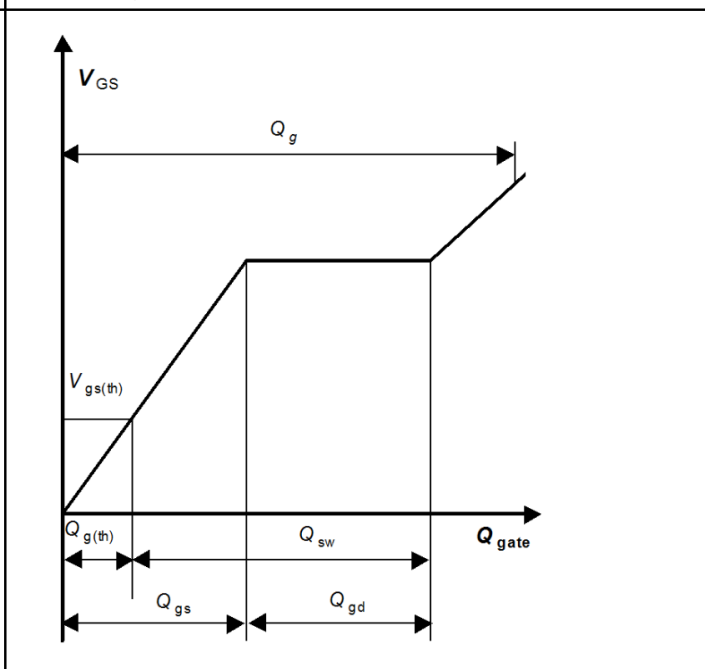
$V_{GS}=f(Q_{\text{gate}}); I_D=50 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



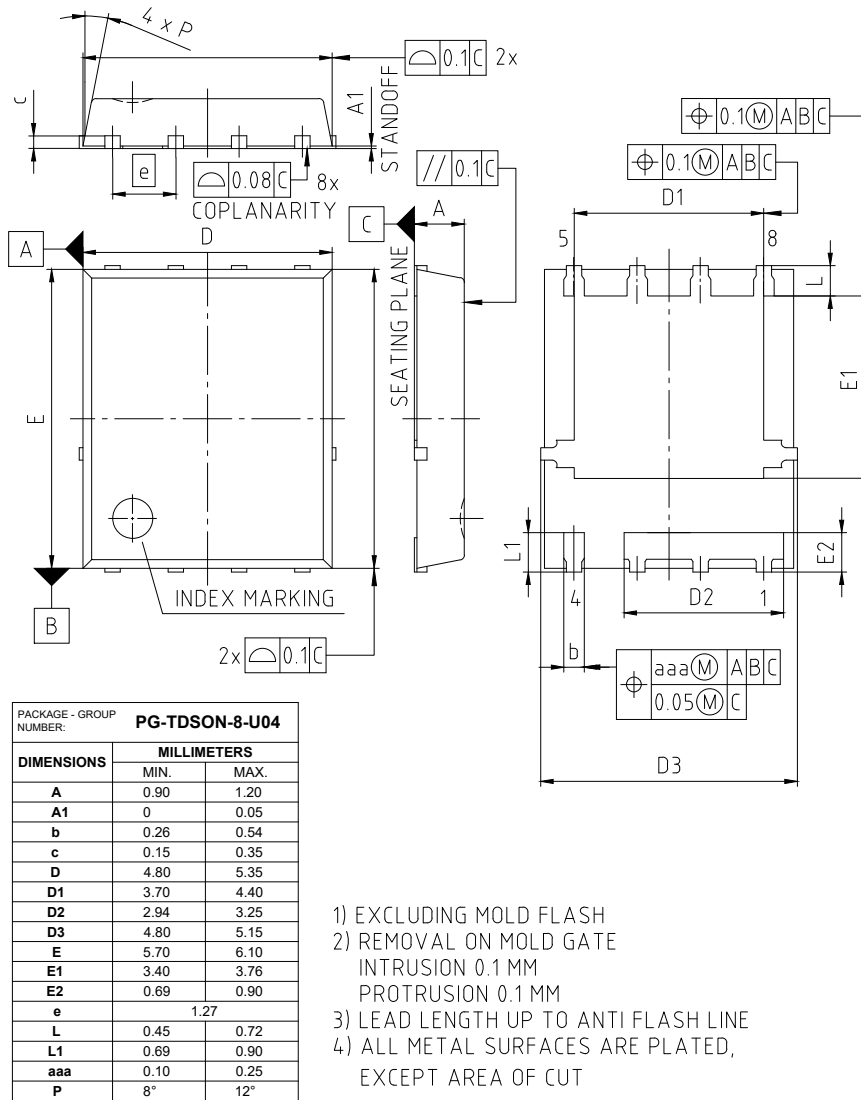
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



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## 5 Package Outlines



**Figure 1** Outline PG-TDSON-8, dimensions in mm

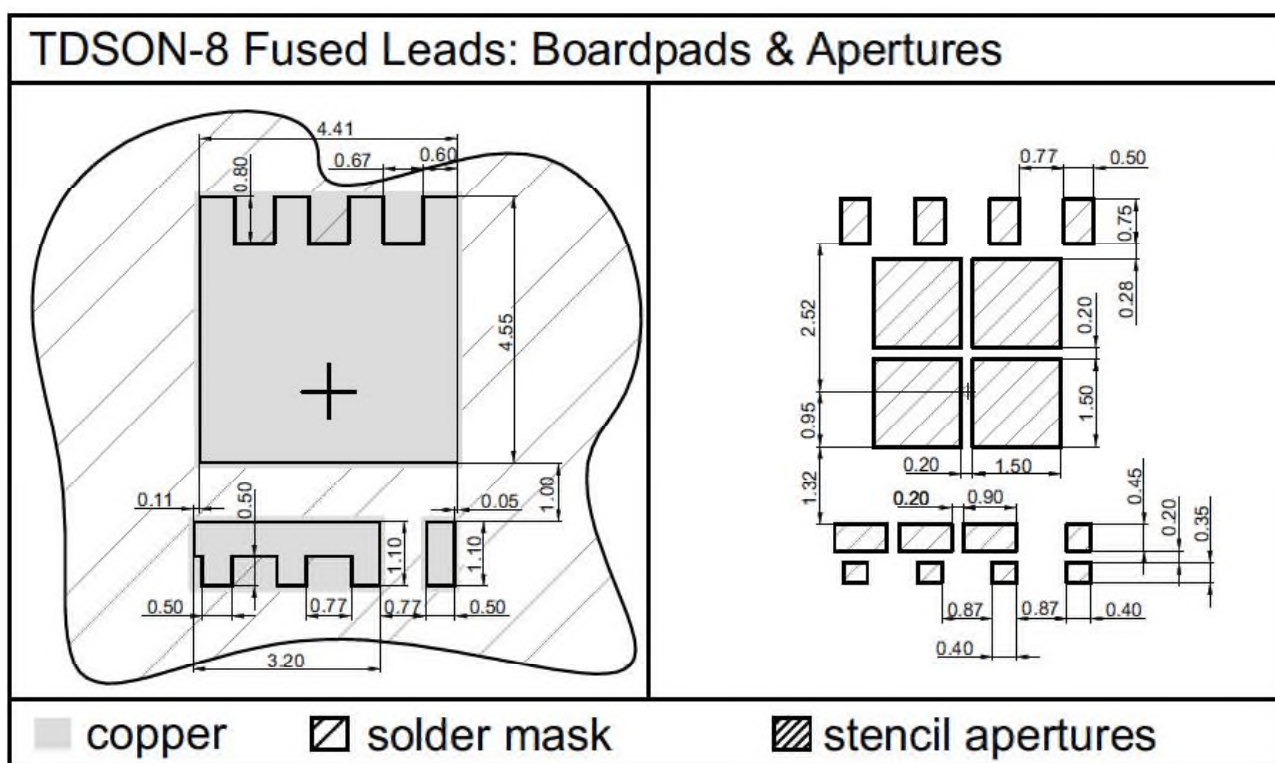


Figure 2 Outline PG-TDSON-8, dimensions in mm

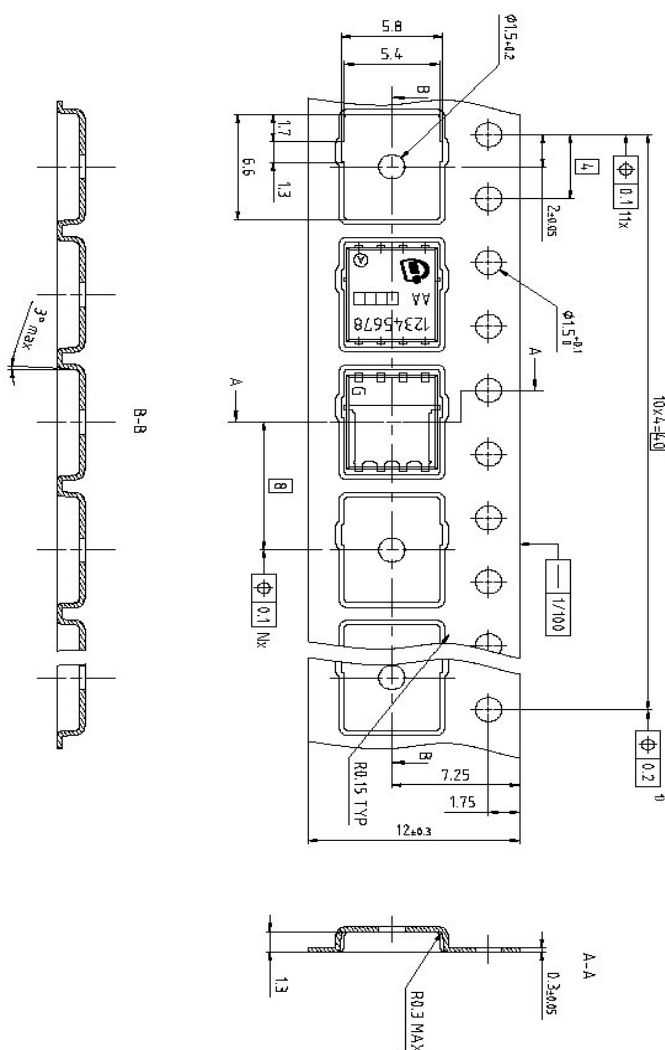


Figure 3 Outline PG-TDSON-8, dimensions in mm

## Revision History

BSC010N04LS

### Revision 2024-06-11, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2014-06-27	Rev. 2.2
2.3	2019-09-27	Update package drawings
2.4	2020-03-13	Update current rating
2.5	2024-06-11	Upgrade Operating and storage temperature max to 175°C. Update drawings in section 5 Package Outlines. Production validation added on page1.Updated foot notes.

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