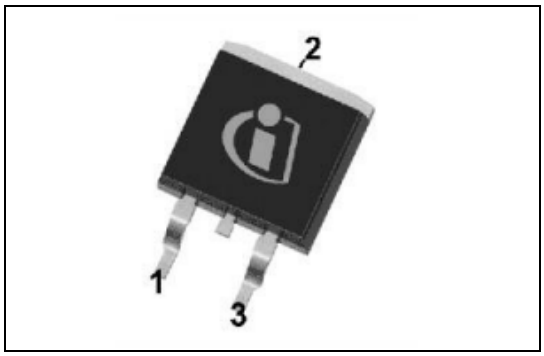
150V Radiation Tolerant power MOSFET

BUP15CN060L-01



Features

- Low $R_{DS(on)}$
- Single Event Effect (SEE) tolerant
- Total Ionisation Dose (TID) tolerant
  30 kRad approved
- N-channel

Product validation

Qualified according AEC Q101

Electrical parameters in Table 4 are guaranteed pre- and post-irradiation.

Description

Table 1 Product information

Type	Comment	Pin Configuration			Package
		1	2	3	
BUP15CN060L-01		G	D	S	D^2PAK (TO263)

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1 Maximum ratings

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain source voltage	V_{DS}	-	-	150	V	
Gate source voltage	V_{GS}	-20	-	20	V	static
Drain gate voltage	V_{DG}	-	-	150	V	
Continuous drain current [1]	I_D	- -	- -	36 22	A	T_C= 25 °C T_C= 100 °C
Continuous source current	I_S	-	-	36	A	
Drain current pulsed	I_{DM}	-	-	111	Apk	t_p limited by $T_{j,max}$
Total power dissipation [2]	P_{tot}	-	-	150	W	$T_C \leq 25$ °C
Operating temperature	T_{op}	-40	-	125	°C	
Storage temperature	T_{stg}	-55	-	150	°C	
Junction temperature	T_j	-40	-	150	°C	
Avalanche energy, single pulse	E_{AS}	-	-	310	mJ	V_{DD} = 50V, L = 108µH

[1] Limited by $T_{j,max}$

[2] For T_C > 25°C derating is required.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th,JC}$	-	-	0.83	K/W	
Thermal resistance, junction - ambient	$R_{th,JA}$	-	-	62	K/W	Device on PCB, minimal footprint
		-	35	-		Device on 40mm*40mm *1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling
Soldering temperature	T_{sol}	-	-	260	°C	Reflow MSL 1

3 Electrical characteristics

at T_A=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	BV_{DSS}	150	-	-	V	I_D= 0.25mA, V_{GS}= 0V
Gate threshold voltage	$V_{GS(th)}$	2	-	4	V	I_D= 1.0mA, $V_{DS} \geq V_{GS}$
Gate to source leakage current	I_{GSS}	-100 -200	- -	100 200	nA	V_{DS}= 0V, V_{GS}= +/- 20V, T_A= 25°C V_{DS}= 0V, V_{GS}= +/- 20V, T_A= 125°C
Zero gate voltage drain current	I_{DSS}	- -	- -	25 250	µA	V_{DS}= 120V, V_{GS}= 0V, T_A= 25°C V_{DS}= 120V, V_{GS}= 0V, T_A= 125°C
Drain source on-state resistance [1]	$R_{DS(ON)}$	- -	49 -	60 100	mΩ	V_{GS}= 10V, I_D= 15A, T_A= 25°C V_{GS}= 10V, I_D= 15A, T_A= 125°C
Diode forward voltage [1,2]	V_{SD}	-	-	1.1	V	V_{GS}= 0V, I_S= 23A

Table 5 Dynamic characteristics

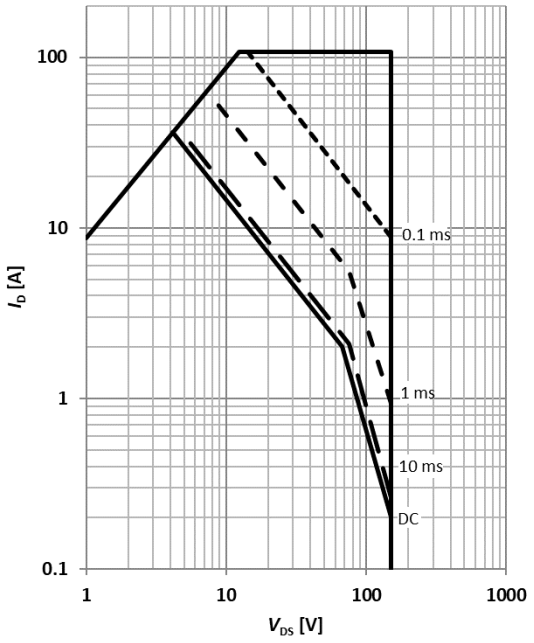
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Turn-on delay time	$t_{d(ON)}$	-	11	-	ns	V_{DD}= 50% V_{DS}, I_D= 15A, R_G= 4.7Ω
Rise time	t_r	-	11	-	ns	V_{DD}= 50% V_{DS}, I_D= 15A, R_G= 4.7Ω
Turn-off delay time	$t_{d(OFF)}$	-	22	-	ns	V_{DD}= 50% V_{DS}, I_D= 15A, R_G= 4.7Ω
Fall time	t_f	-	8	-	ns	V_{DD}= 50% V_{DS}, I_D= 15A, R_G= 4.7Ω
Reverse recovery time	t_{rr}	-	252	-	ns	$V_{DD} \leq$ 50V, I_D= 23 A
Common source input capacitance	C_{iss}	-	1.55	-	nF	V_{DS}= 100V, V_{GS}= 0V, f= 1.0MHz
Common source output capacitance	C_{oss}	-	158	-	pF	V_{DS}= 100V, V_{GS}= 0V, f= 1.0MHz
Common source reverse transfer capacitance	C_{rss}	-	32	-	pF	V_{DS}= 100V, V_{GS}= 0V, f= 1.0MHz
Total gate charge	Q_G	-	28.3		nC	V_{DD}= 50% V_{DS}, V_{GS}= 10V, I_D= 23 A

[1] Pulsed measurement: Pulse Width < 300µs, Duty Cycle <2.0%.

[2] Measured within 2.0 mm of case

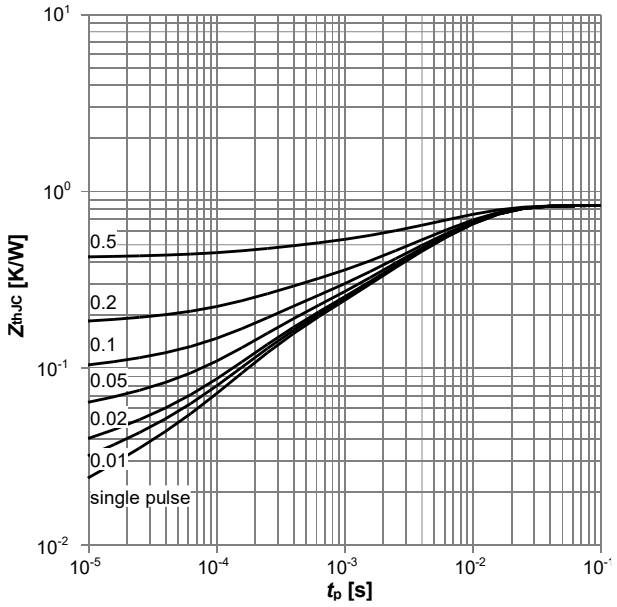
4 Electrical characteristics diagrams

Diagram 1: Safe operating area



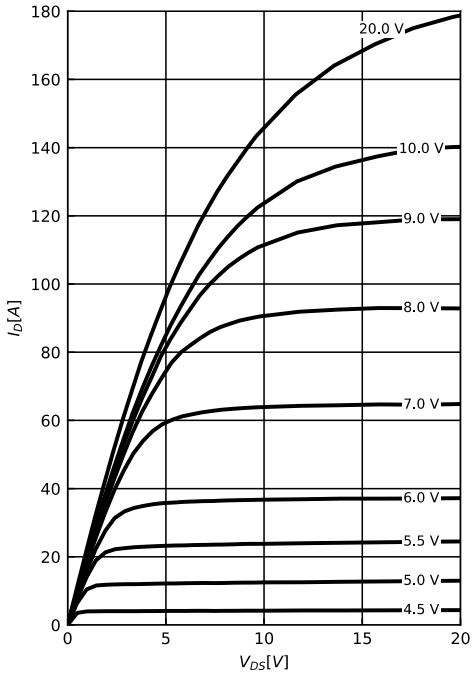
$I_D = f(V_{DS})$; $T_C = 25°C$; D=0; parameter: t_p

Diagram 2: Max. transient thermal impedance



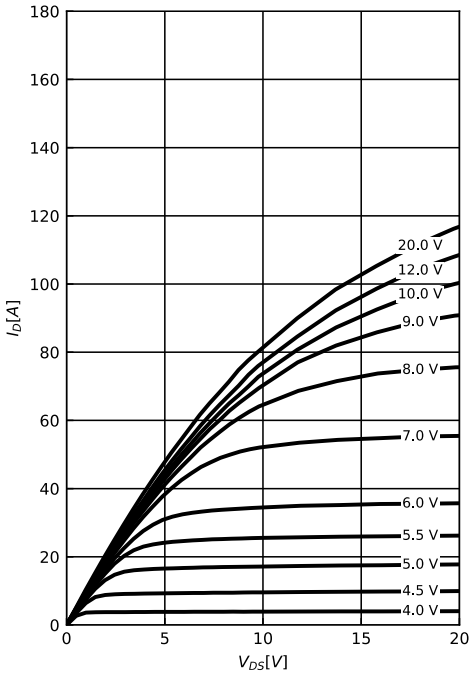
$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$

Diagram 3: Typ. output characteristics



$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}

Diagram 4: Typ. output characteristics



$I_D = f(V_{DS})$; $T_j = 150$ °C; parameter: V_G

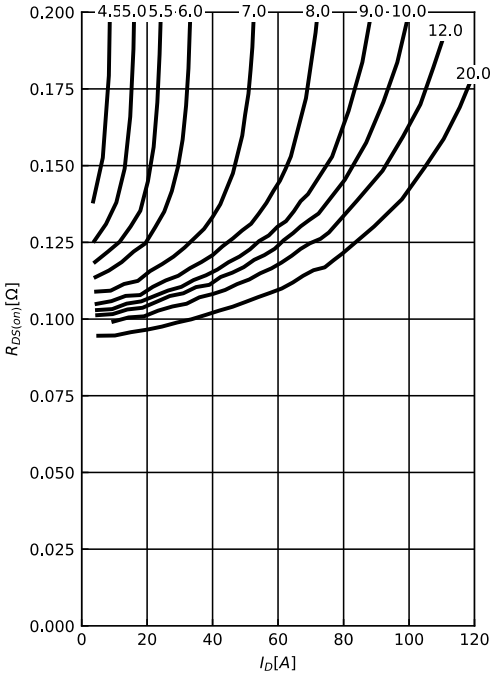
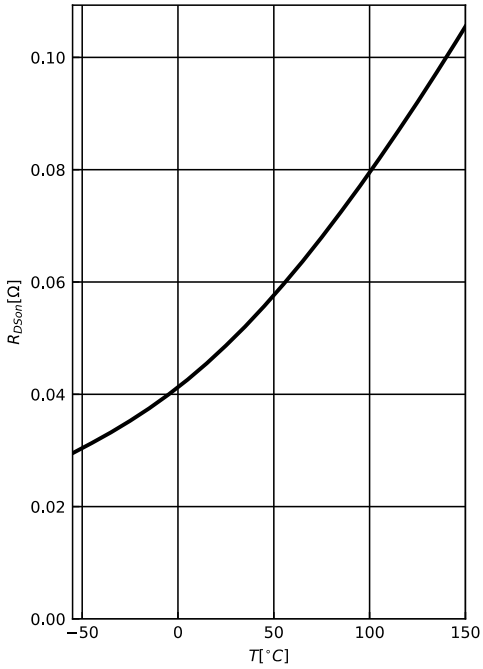
Diagram 5: Typ. drain-source on-state resistance	Diagram 6: Typ. drain-source on-state resistance
	
$R_{DS(on)}$ = f(I_D); T_j = 150 °C; parameter: V_{GS}	$R_{DS(on)}$ = f(T_j); I_D=15A

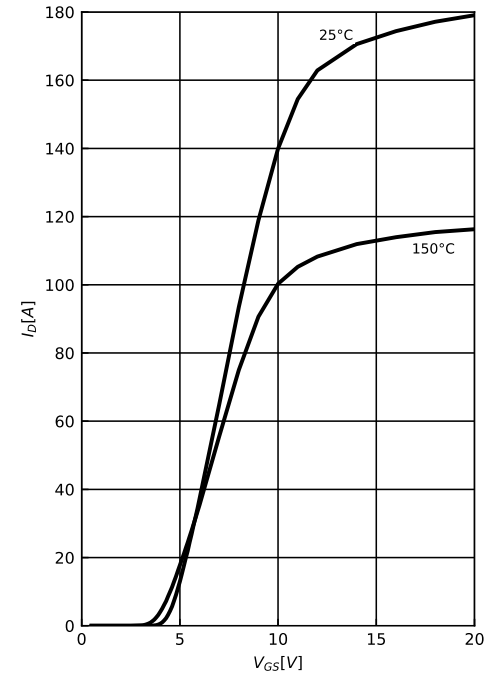
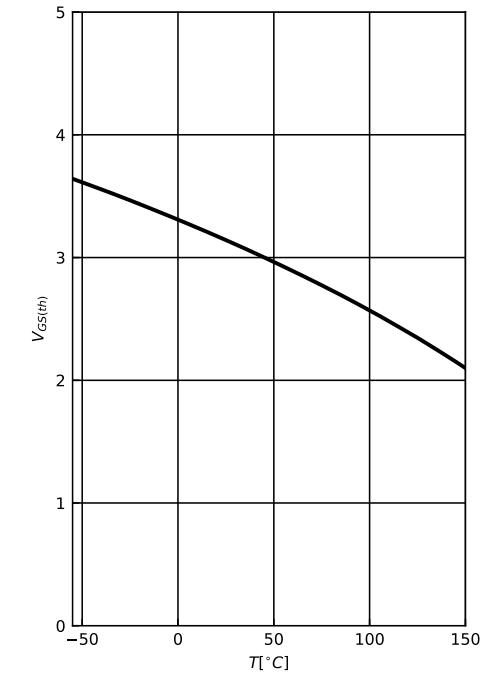
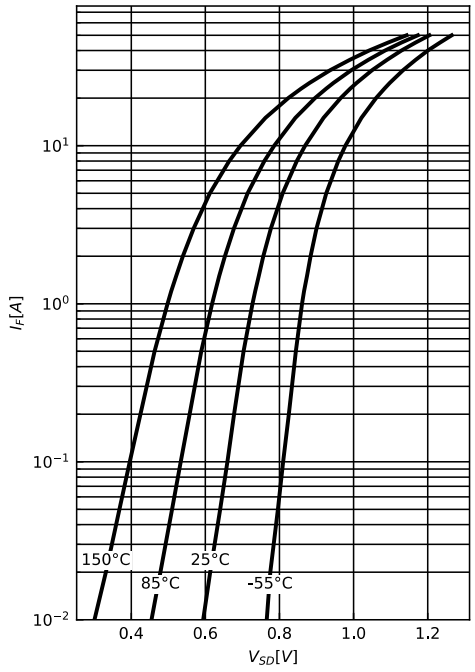
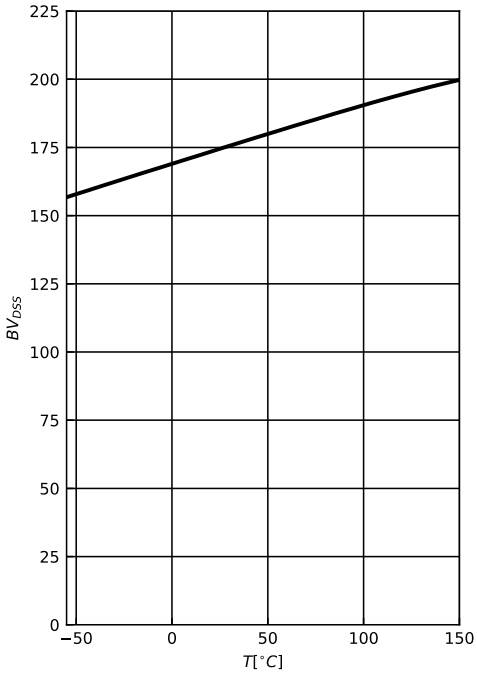
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. gate threshold voltage
	
I_D = f(V_{GS}); V_{DS} = 20V; parameter: T_j	I_D=f(T_j); I_D = 1mA

Diagram 9: Forward characteristics of reverse diode



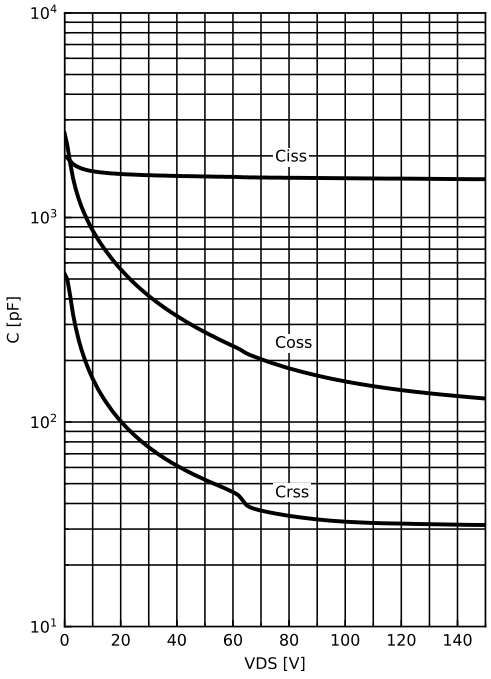
$I_F = f(V_{SD})$; parameter: T_j

Diagram 10: Drain-source breakdown voltage



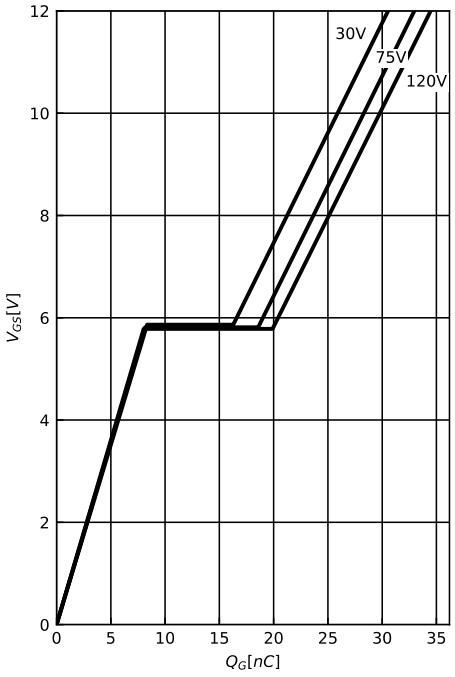
$BV_{DSS} = f(T_j)$; $I_D = 250\mu A$

Diagram 11: Typ. capacitances



$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

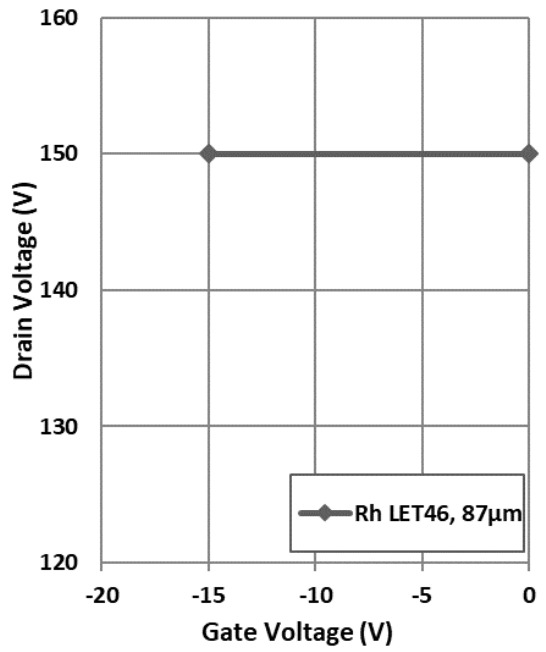
Diagram 12: Typ. gate charge



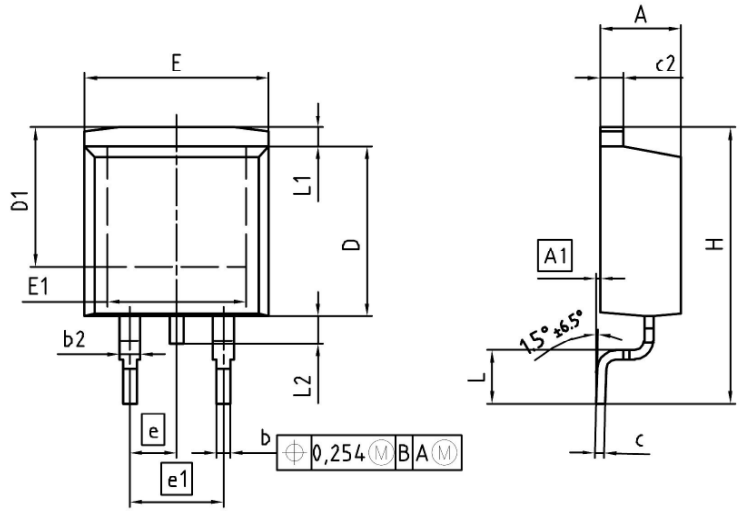
$V_{GS} = f(Q_{gate})$; $I_D = 23.0$ A pulsed; parameter: V_{DD}

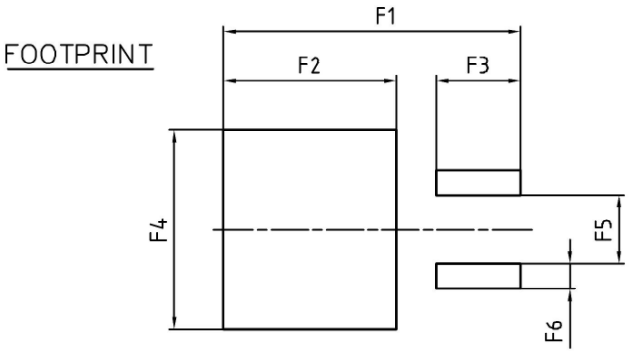
Electrical characteristics diagrams

Diagram 13: SEE – Safe operating area



5 Package outlines





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

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