CIPOS™ Micro IPM Application Note

For IM231-x6 Only

About this document

Scope and purpose

This application note describes the IM231-x6 portfolio of CIPOS™ Micro Intelligent Power Modules (IPM) and should be used in parallel with each part's datasheet. This document first gives an overview of the product lineups and datasheet information. It details the functionality of the modules and then provides recommendations for designing the external circuitry that interfaces with the modules. The application note ends with thermal-design considerations and heat-sinking guidelines.

Intended Audience

Power electronics engineers who want to design reliable and efficient motor drive applications with IM231-x6.

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1 Introduction

With the global emphasis on energy efficiency, there is an ever stricter requirement on the efficiency of motor drive systems. CIPOS™ IPMs are becoming more popular in home appliance and industrial motor drive applications, because they enable increased system efficiencies, smaller designs, easier assembly methods and shorter system development cycles.

Our next generation of CIPOS™ Micro IPM has been developed with a focus on providing added features, higher module efficiency and better long-term reliability. Integrating Infineon's TRENCHSTOP™ IGBT6 and latest gate driver technologies in one package allows for the shrinking of the package size, and hence increased power densities.

The IM231-series 3-phase IPMs are designed for high-efficiency appliance motor drives such as air-conditioner fans, refrigerator compressors, and small washing machines rated between 80 and 450 W. These advanced IPMs, available in both surface-mount and through-hole configurations, have several protection features including precise overcurrent protection and a UL-certified temperature sensor.

The application note concerns the following products:

IM231-L6T2B

IM231-L6S1B

IM231-M6T2B

IM231-M6S1B

1.1 Product portfolio

Table 1 IM231-x6 Product Line

Part Number	Rating		Topology	Package	Isolation Voltage (Vrms)
	Current (A)	Voltage (V)			
IM231-M6T2B	4	600 V	3ϕ bridge with open emitters	Through-hole	2000 Vrms sinusoidal, 1 min.
IM231-M6S1B				Surface-mount	
IM231-L6T2B	6			Through-hole	
IM231-L6S1B				Surface-mount	

1.2 Nomenclature

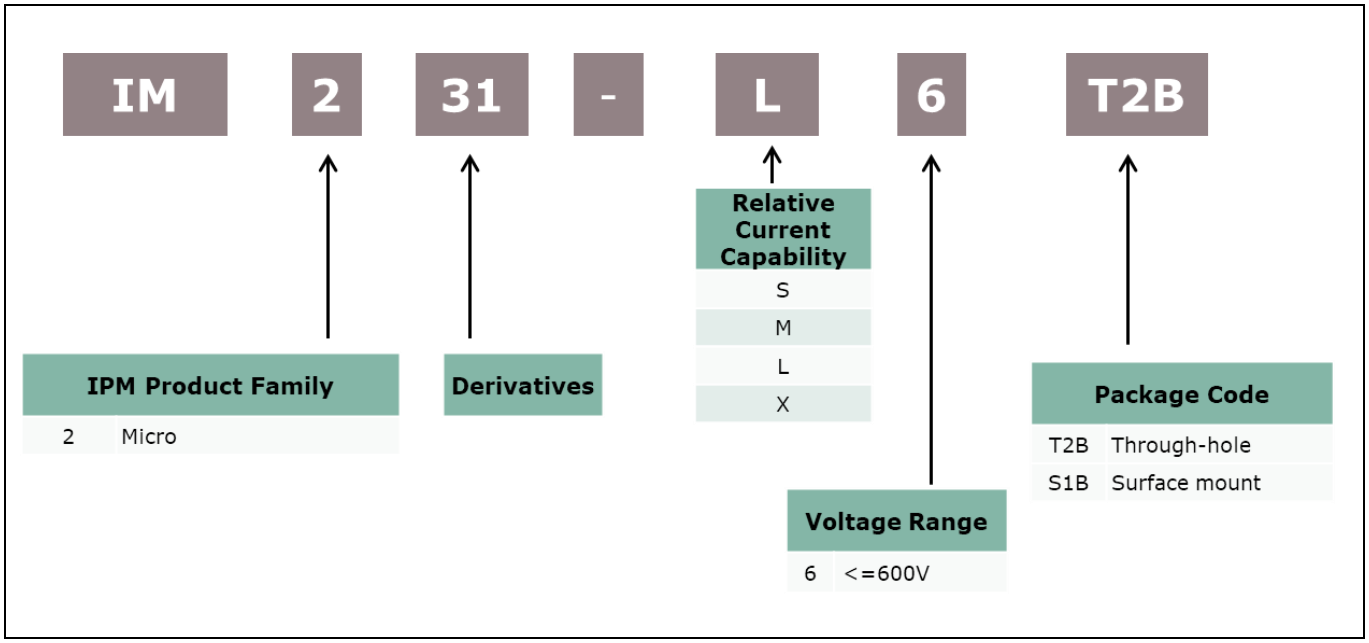

Figure 1 Nomenclature for CIPOS™ Micro IPM's IM231 series

2 Product overview and pin description

2.1 Internal circuit and features

Figure 2 illustrates the internal block diagram of the IM231-x6. These products consist of a three-phase IGBT inverter circuit and three half-bridge driver ICs with protection features.

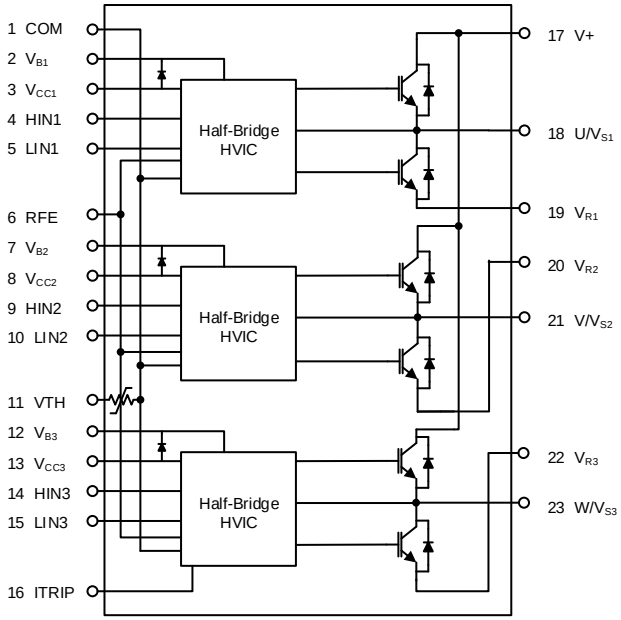

Figure 2 Internal block diagram

The detailed features and integrated functions of IM231-x6 are described as follows:

Key features:

- 600 V/4 A to 6 A rating in one physical package size (mechanical layouts are identical)
- Motor power range from 80 W to 450 W
- Surface-mount and through-hole dual-in-line package options
- Infineon low $V_{CE(ON)}$ TRENCHSTOP™ IGBTs with separate freewheeling diode
- Undervoltage lockout for all channels
- Rugged gate driver technology with stability against transient and negative voltage
- Integrated bootstrap functionality
- Matched delay times of all channels / Built in dead time
- Overcurrent protection
- Lead-free terminal plating; RoHS-compliant
- 3.3 V Schmitt-triggered input logic
- Cross conduction preventing logic
- Low-side emitter pins accessible for current monitoring
- Active high input signal logic
- Isolation 2000 Vrms min
- High operating case temperature, T_{cmax} = 125 C
- UL-certified temperature monitor

Product **overview and pin description**

Key benefits:

- Ease of design and short time-to-market
- Compact package with through-hole or surface-mount options
- Simplified design and manufacturing
- Lower losses than similar modules in the market
- Heat sink-less operation possible

2.2 Package variations

IM231-x6 are available in 2 package variations: surface-mount (SOP 29x12) and standard through-hole (DIP 29x12). These package variations are illustrated in Figure 3.

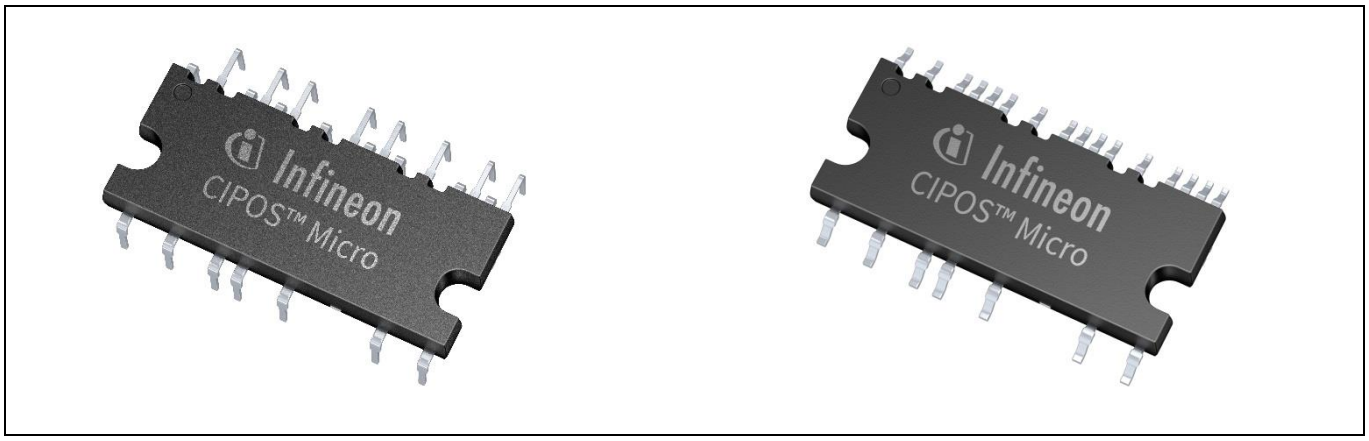

Figure 3 External view of IM231-x6: Through-hole package (DIP 29x12) on the left and surface-mount package (SOP 29x12) on the right

2.3 Input and output pins

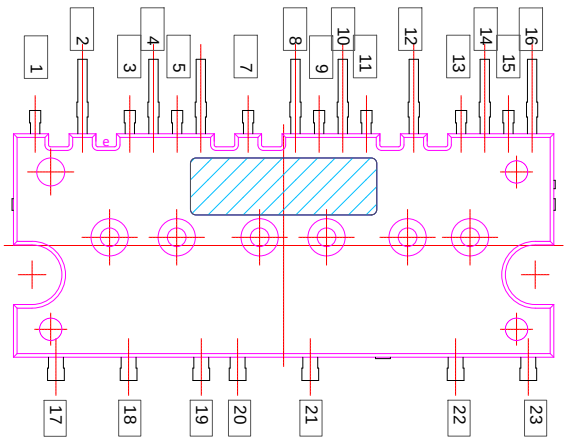

Figure 4 Module pinout

Table 2 Pin Assignment

Pin	Name	Description
1	COM	Logic ground
2	V_{B1}	High side floating supply voltage 1
3	V_{DD1}	Low side control supply 1
4	HIN1	Logic input for high side gate driver - Phase 1
5	LIN1	Logic input for low side gate driver - Phase 1
6	RFE	RCIN / Fault / Enable
7	V_{B2}	High side floating supply voltage 2
8	V_{DD2}	Low side control supply 2
9	HIN2	Logic input for high side gate driver - Phase 2
10	LIN2	Logic input for low side gate driver - Phase 2
11	VTH	Thermistor output
12	V_{B3}	High side floating supply voltage 3
13	V_{DD3}	Low side control supply 3
14	HIN3	Logic input for high side gate driver - Phase 3
15	LIN3	Logic input for low side gate driver - Phase 3
16	ITRIP	Current protection pin
17	V+	DC bus voltage positive
18	U/V_{S1}	Output - phase 1, high side floating supply offset 1
19	V_{R1}	Phase 1 low side emitter
20	V_{R2}	Phase 2 low side emitter
21	V/V_{S2}	Output - phase 2, high side floating supply offset 2
22	V_{R3}	Phase 3 low side emitter
23	W/V_{S3}	Output – phase 3, high side floating supply offset 3

2.4 Pin descriptions

HIN(1,2,3) and LIN(1,2,3) (Low side and high side control pins)

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The internal structure of these pins is depicted in Figure 5. The Schmitt-trigger input thresholds are designed to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 800 kΩ is internally provided to pre-bias inputs during supply start-up, and an ESD diode is provided for pin protection purposes. The input Schmitt trigger and a noise filter provide beneficial noise rejection to short input pulses. See Section 3.5 for more details about the advanced input filter featured in IM231-x6.

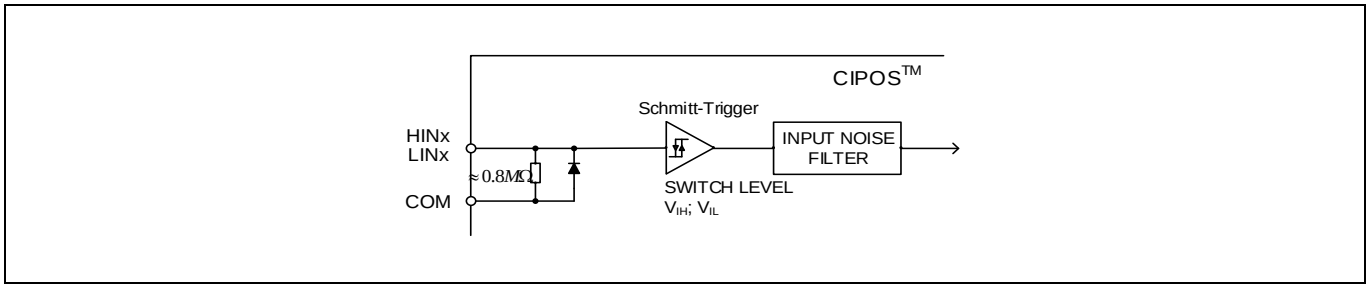

Figure 5 Input pin structure

The integrated gate drive also provides a shoot-through inhibiting capability, which prevents the simultaneous on-state of the high-side and low-side switch of the same inverter phase. A dead time of 300 ns (typical) is also inserted between the corresponding HIN and LIN signals by the gate driver IC in order to reduce cross-conduction of the IGBTs.

V_{DD}, COM (Low-side control supply and reference)

V_{DD} is the control supply, which provides power both to input logic and to output power stage. Input logic is referenced to COM ground.

The undervoltage circuit enables the device to operate at power ON when a supply voltage of at least a typical voltage of V_{DDUV+} = 11.1 V is present.

The IC shuts down all the gate drivers power outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 10.9 V. This prevents the external power switches from critically low gate voltage levels during the ON state, and therefore from excessive power dissipation.

$V_{B(1,2,3)}$ and $V_{S(1,2,3)}$ (High-side supplies)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to COM following the external high-side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typically V_{BSUV+} = 11.1 V and a falling threshold of V_{BSUV-} = 10.9 V.

$V_{S(1,2,3)}$ provide a high robustness against negative voltage in respect of COM. This ensures very stable designs even under rough conditions.

$V_{R(1,2,3)}$ (Low-side emitters)

The low-side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to the COM pin as short as possible in order to avoid unnecessary inductive voltage drops.

VTH (Thermistor output)

A UL-certified NTC is integrated in the module with one terminal of the chip connected to COM and the other to VTH. When pulled up to a rail voltage such as V_{DD} or 3.3 V by a resistor, the VTH pin provides an analog voltage signal corresponding to the temperature of the thermistor.

RFE (RCIN / Fault / Enable)

The RFE pin combines three functions in one pin: RCIN or RC-network-based programmable fault clear timer, fault output and enable input. See Section 3.2 for more details.

U/V_{S1}, V/V_{S2}, W/V_{S3} (High-side emitter and low-side collector)

These pins are motor U, V, W input pins.

V+ (Positive bus input voltage, Pin 23)

The high-side IGBTs are connected to the bus voltage. Note that the bus voltage does not exceed 450 V.

2.5 Outline drawings

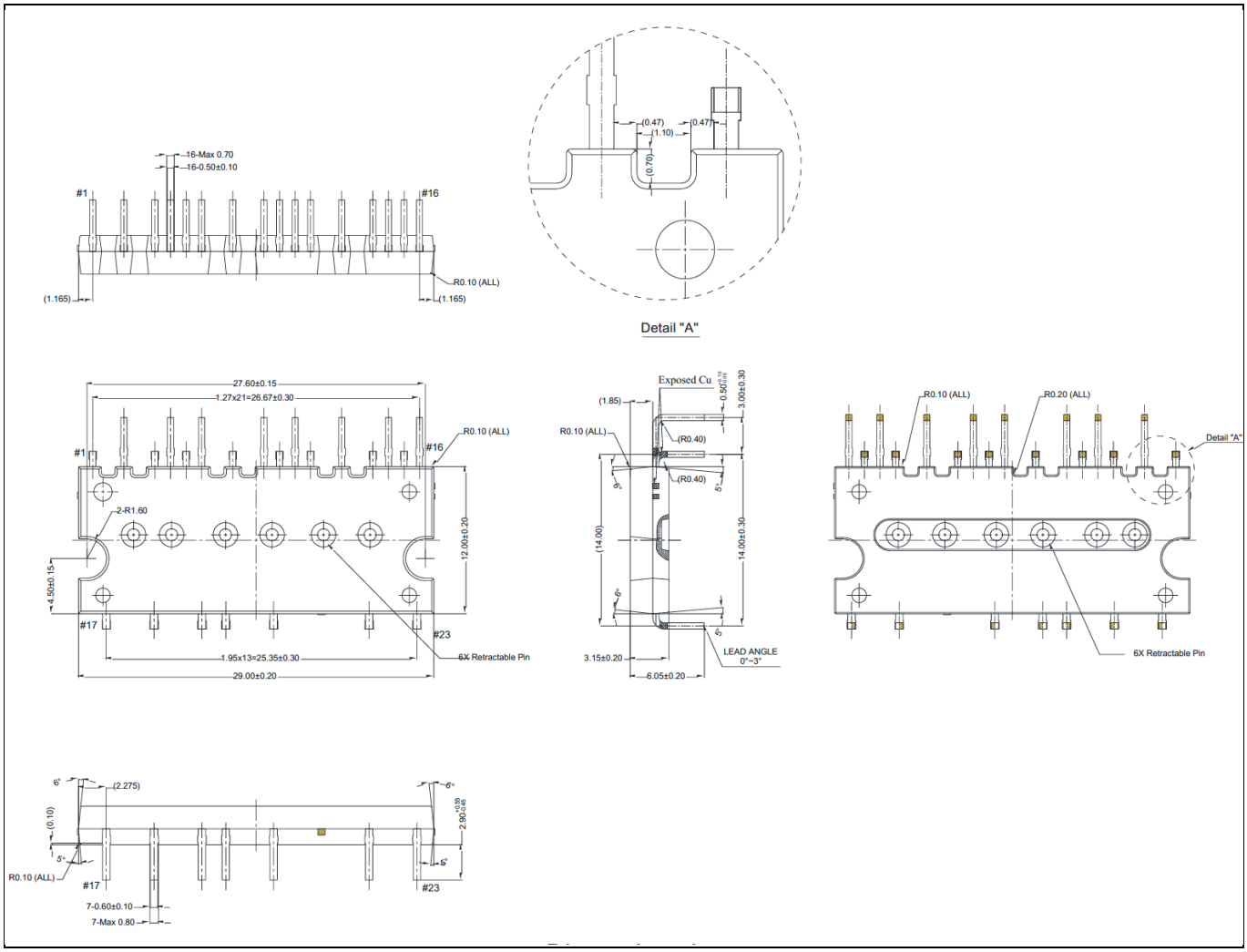

Figure 6 DIP 29x12 (dimensions in mm)

Figure 7

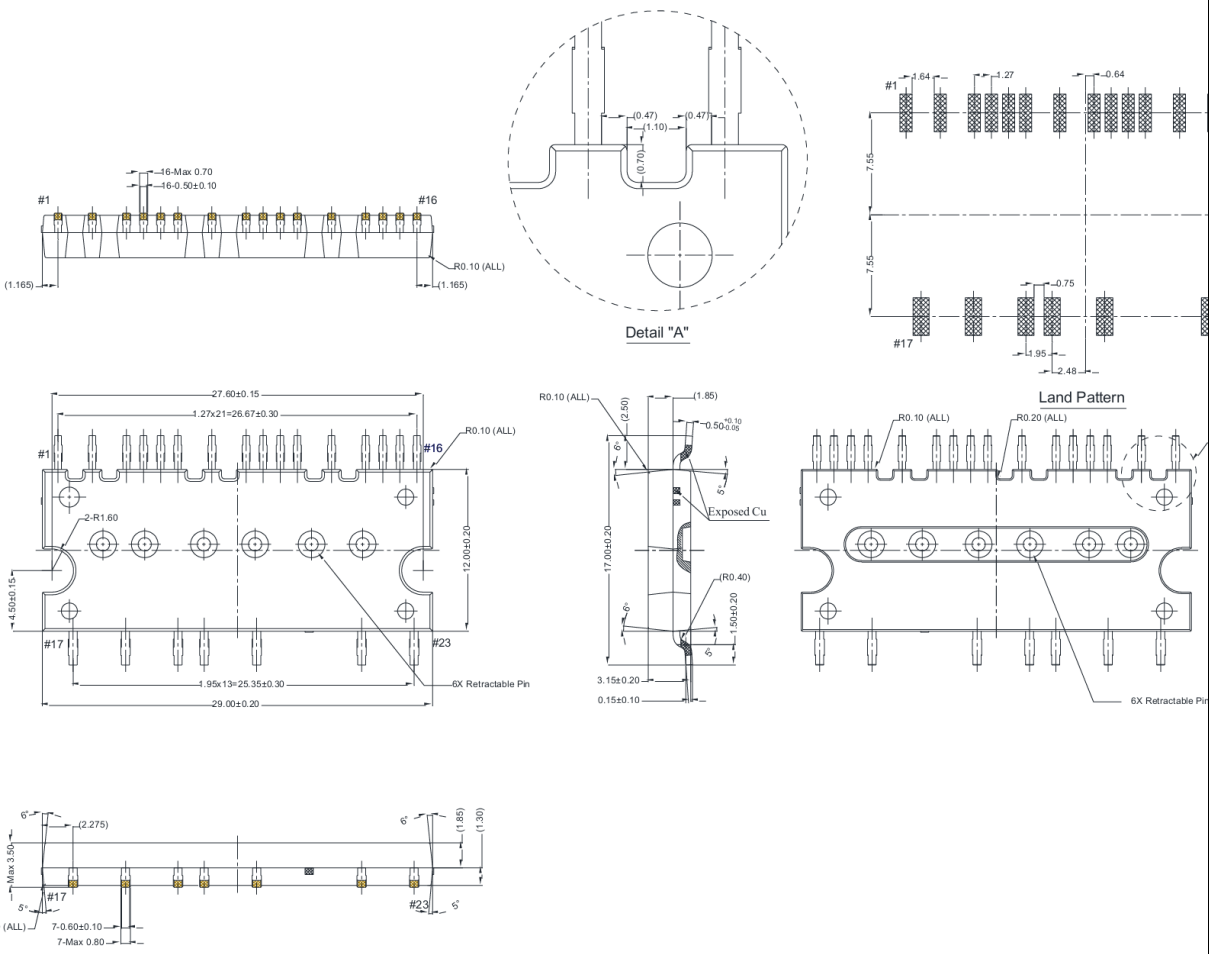

Figure 8 SOP 29x12 (dimensions in mm)

2.6 Maximum electrical rating

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested in production. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the tables. These values can be viewed in the specific part's datasheet. Appropriate design margins should be implemented to ensure that all absolute maximum ratings are observed at all times during operation. This includes abnormal conditions like start-up, shut-down, overload, short-circuit, and system failures. Section 6 provides detailed instructions to help assess the temperatures of the device based on operating conditions. Please see references below for more in-depth descriptions of these ratings.

Table 3 Module

Parameter	Symbol	Description
Storage temperature	T_{STG}	Storage temperature range for reliable performance over life of device
Operating case temperature	T_C	Temperature range of package top surface (surface with part marking)
Operating junction temperature	T_J	Temperature range of the internal junction of power switches and gate drivers.
Isolation test voltage	V_{ISO}	60 Hz voltage that can be applied for one minute between all pins and top surface of the module. This is a UL-certified rating (File number E252584).

Table 4 Inverter

Parameter	Symbol	Description
Max. blocking voltage	V_{CES}/I	Voltage that can be applied across each IGBT.
Output current	I_O	Current class to aid in selection of right part number.
Peak output current	I_{OP}	Pulsed output current capability from single switch at specified temperature and t_P (duration of time at peak).
Peak power dissipation per IGBT	P_{tot}	Total peak power dissipation per switch
Short-circuit withstand time	t_{SC}	At specified conditions

Table 5 Control

Parameter	Symbol	Description
Low-side control supply voltage	V_{DD}	Voltage range of input supply voltage
Input voltage LIN, HIN	V_{IN}	Voltage range in reference to V_{DD}
High-side floating supply voltage (V_B reference to V_S)	V_{BS}	Voltage range of input supply voltage

3 Protection features

3.1 Overcurrent protection

IM231-x6 is equipped with an ITRIP input pin. Together with one or more external shunt resistors, this functionality can be used to detect overcurrent events in the negative DC bus. The internal high-voltage gate driver will continuously monitor the voltage on the ITRIP pin. Whenever this voltage exceeds the reference voltage ($V_{IT,TH+}$ = 0.5 V with a ±5% variation), a fault signal will be generated on the RFE pin, and all six IGBTs will be turned OFF.

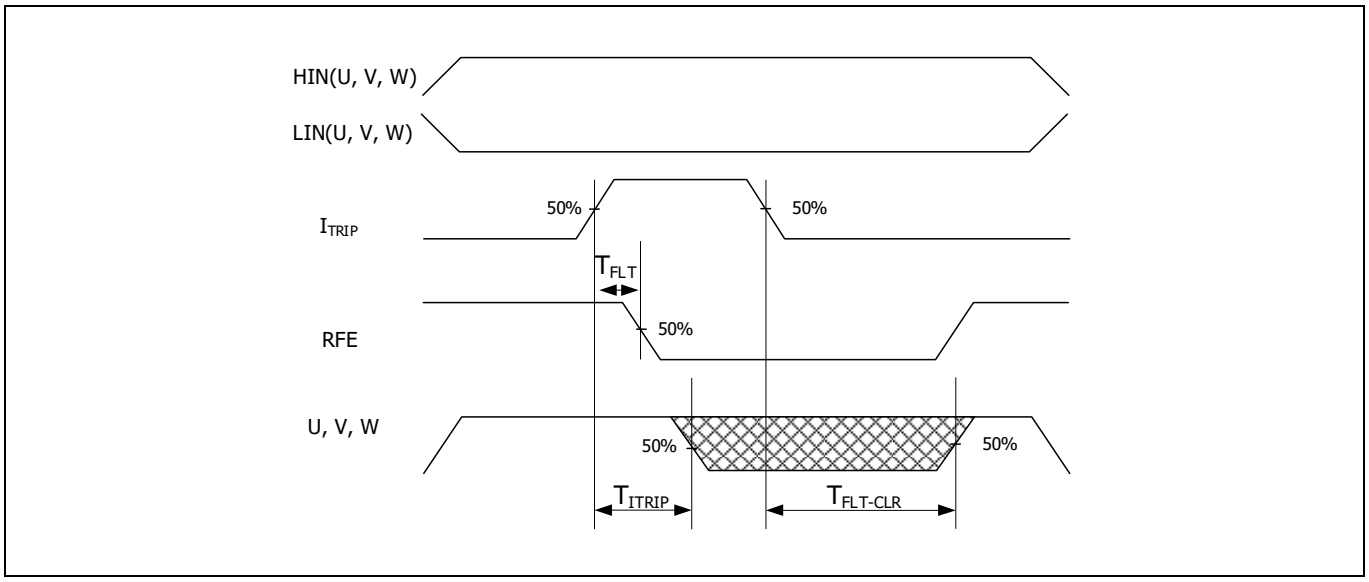

Figure 9 Timing chart for the overcurrent protection function

The threshold of overcurrent protection can be determined by $V_{IT,TH+}$ / R_{SHUNT}, if a single bus shunt is used and is directly connected to the ITRIP pin without any voltage-dividing circuit.

In case of a short-circuit event, the current level will rise very quickly to the saturation current of the IGBT. It is then critical to ensure that all IGBTs are turned OFF as soon as possible. Since IGBTs in IM231-x6 are short-circuit rated (see Table 6), the safe operation of the IPM is guaranteed by minimizing the delay of external current-sensing circuits and making sure its delay, plus the intrinsic IPM delay time, is lower than the IGBT short-circuit rating time. Since the IGBT short-circuit rating depends on its junction temperature and gate voltage (approximately equal to V_{DD} for low-side IGBTs and V_{BS} for high-side IGBTs), it is important to consider all possible operating conditions when designing the overcurrent protection scheme. Figure 9 shows the variation of short circuit time with V_{DD} and V_{th}.

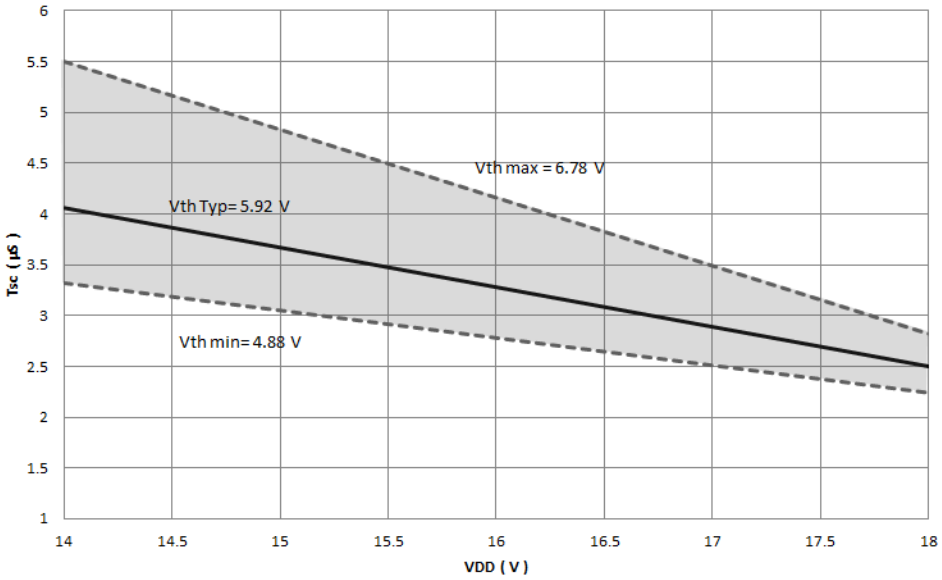

Figure 10 IM231-x6 t_{SC} vs V_{DD} with V_{DC} = 400 V and T_J = 150°C

For safe operation, taking into account V_{th} and V_{DD} variations, layout designs are advised to be done with t_{SC} = 3 µS

Table 6 Short-circuit withstand time

Item	Symbol	Condition	Value	Unit
Short-circuit withstand time	t_{SC}	T_J <150°C, V_{DC} =360 V, V_{DD} =15 V	3	µs

3.1.1 Selecting the current-sensing shunt resistor

The value of the current-sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive-going threshold voltage of IM231-x6, typically 0.50 V. I_{OC} is the trip current level.

I_{OC} should be lower than the repetitive peak collector current in the datasheet.

The following should be considered to determine the power rating of a single shunt resistor:

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at T_C=25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH}=100°C according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated by the following equation:

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times \text{margin}}{\text{derating ratio}} \quad (2)$$

For example, in case of IM231-L6 and R_{SH}=89 mΩ:

- Max. load current of the inverter : 4 A_{rms}
- Power derating ratio of shunt resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{4^2 \times 0.089 \times 1.3}{0.8} = 2.3\,W$$

A proper power rating of a single shunt resistor should then be over 2.3 W. A strategy to reduce the power dissipation requirement for one single shunt resistor is to use two or more shunt resistors in parallel.

3.1.2 Delay time

When an overcurrent event occurs in the inverter, there is a delay between the occurrence of this event and the IPM turning off all its IGBTs. This delay arises from circuit-design choices made external to the IPM, and from intrinsic delays within the IPM.

Let us examine the delay due to circuit design choices external to the IPM first. An RC circuit is typically placed between the shunt resistor and the ITRIP pin. This low pass filter is necessary to prevent spurious triggering of the overcurrent protection feature due to noise. Assuming no voltage-dividing circuit is present, when the sensing voltage on the shunt resistor exceeds ITRIP positive-going threshold ($V_{IT,TH+}$), this voltage is filtered by the RC network and then applied to the ITRIP pin of IM231-x6 with a delay determined by the RC time constant, t_{RC}.

Next let us examine the intrinsic delays within the IPM. The IPM has a built-in filter of $t_{FIL,ITRIP}$ =500 ns (typical) to reject pulses on the ITRIP pin that are that shorter than $t_{FIL,ITIRP}$. In addition there is the shutdown propagation delay of ITRIP (t_{ITRIP}) shown in Table 7. With no capacitor on RFE, the IPM requires a typical 1.3 µs to shut down all the IGBTs after ITRIP crosses $V_{IT,TH+}$. If a capacitor is placed on RFE, this delay will increase by the time required to discharge the capacitor to a voltage below V_{RFE-}. To minimize the overall delay, keep the capacitance connected to RFE low (~1nF), and pull up RFE to 3.3V or 5V rather than V_{DD}. Refer to Section 3.2 for more information on RFE.

Table 7 Internal delay time of OC protection circuit

Parameter	Condition	Min.	Typ.	Max.	Unit
t_{ITRIP}	V+=300 V, no capacitor on RFE	-	1.3	-	µs

Therefore, the total time from the ITRIP positive-going threshold ($V_{IT,TH+}$) to shut down all six IGBTs becomes:

$t_{TOTAL} = t_{RC} + t_{ITRIP}$ (with no capacitor on RFE).

t_{TOTAL} must be designed to be less than the short-circuit withstand time of the IGBT under the operating conditions of the system.

3.2 RFE functions

The RFE pin is normally connected to an RC network on the PCB as per the schematic in Figure 10. Under normal operating conditions, R_{RCIN} pulls the RFE pin to 3.3 V, thus enabling all the functions in the IPM. The microcontroller can pull this pin low to disable the IPM functionality. This is the Enable function.

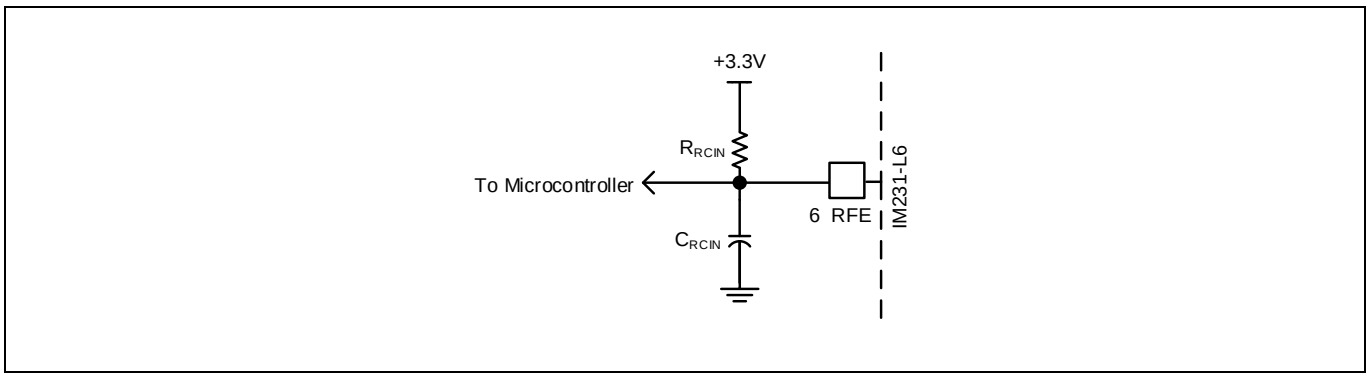

Figure 11 Typical PCB circuit connected to the RFE pin

The Fault function allows the IPM to report a Fault condition to the microcontroller by pulling the RFE pin low in one of two situations. The first is an undervoltage condition on $V_{DD,}$ and the second is when the ITRIP pin detects a voltage rise above $V_{IT,TH+}$.

The programmable fault-clear timer function provides a means of automatically re-enabling the module operation to a preset amount of time ($t_{FLT-CLR}$) after the fault condition has disappeared. Figure 11 shows the RFE-related circuit block diagram inside the IPM.

The length of $T_{FLT-CLR}$ can be determined by using the formula below.

$V_{RFE}(t) = 3.3\ V * (1 - e^{-t/RC})$

$t_{FLT-CLR} = -R_{RCIN} * C_{RCIN} * \ln(1-V_{IN,TH+}/3.3\ V)$

For example, if R_{RCIN} is 1.2 MΩ and C_{RCIN} is 1 nF, the $t_{FLT-CLR}$ is about 1.7 ms with $V_{IN,TH+}$ of 2.5 V. It is also important to note that C_{RCIN} needs to be minimized in order to make sure it is fully discharged in case of an overcurrent event.

Since the ITRIP pin has a 500 ns input filter, it is appropriate to ensure that C_{RCIN} will be discharged below $V_{IN,TH-}$ by the open-drain MOSFET, after 350 ns. Therefore, the max C_{RCIN} can be calculated as follows:

$V_{RFE}(t) = 3.3\ V * e^{-t/RC} < V_{IN,TH-}$

$C_{RCIN} < 500\ ns / (- \ln (V_{IN,TH-} / 3.3\ V) * R_{RFE\_ON})$

Considering a $V_{IN,TH-}$ of 0.8 V and R_{RFE_ON} of 50 Ω, C_{RCIN} should be less than 7 nF. It is also suggested to use a R_{RCIN} of between 0.5 MΩ and 2 MΩ.

Finally, to minimize the delay in the overcurrent protection circuit, we recommend pulling up RFE with R_{RCIN} to 3.3 V or 5 V instead of V_{DD}.

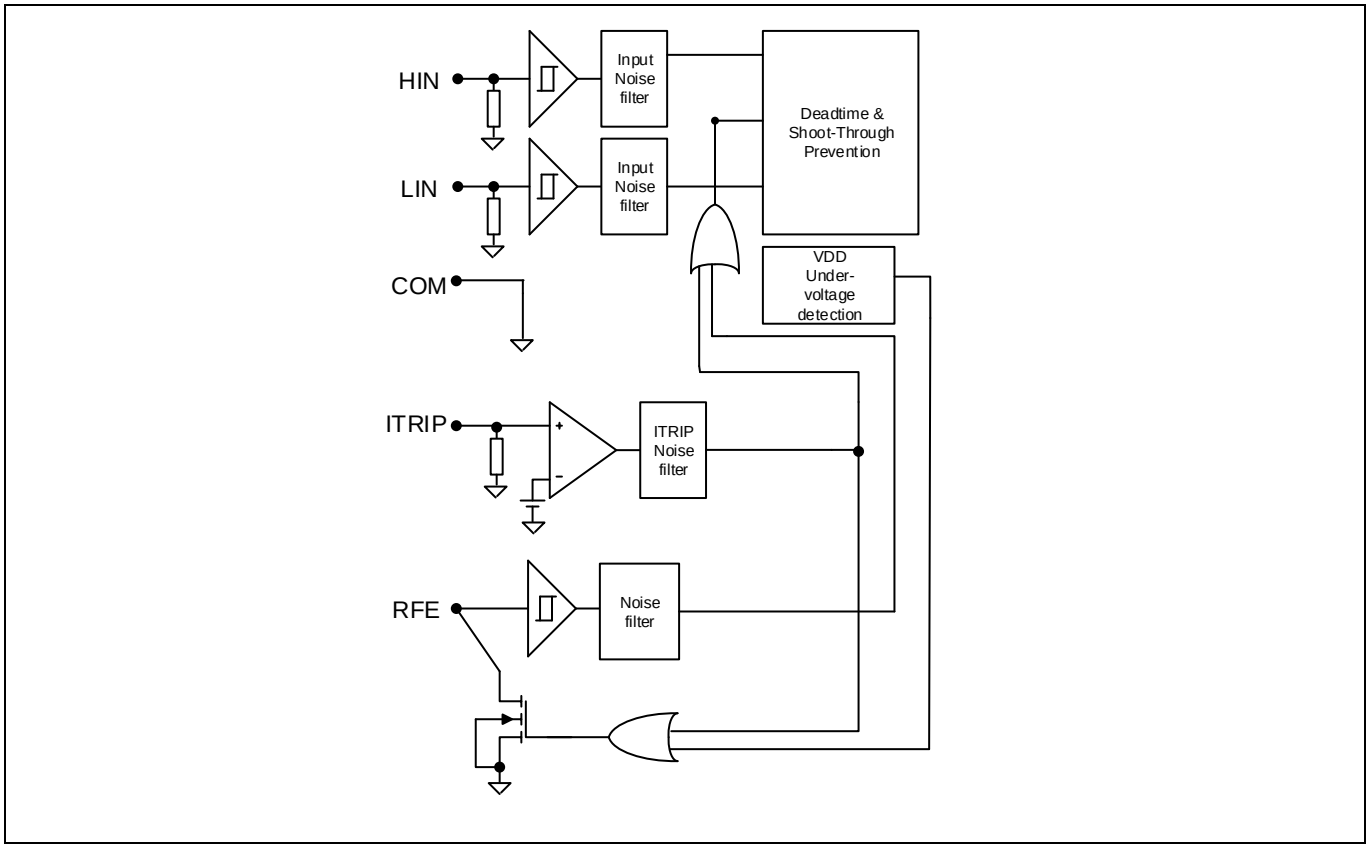

Figure 12 RFE internal circuit structure

3.3 Undervoltage lockout

The gate drivers inside IM231-x6 provide Undervoltage Lockout (UVLO) on both the $V_{DD(1-3)}$ (logic and low-side circuitry) power supplies, and also $V_{BS(1-3)}$ (high-side circuitry power supplies). UVLO's threshold, labeled as $V_{DDUV+/-}$ (or $V_{BSUV+/-}$) in Figure 12 below, is the voltage level of $V_{DD(1-3)}$ or $V_{BS(1-3)}$ where UVLO is enabled or disabled depending on whether the power supply voltage is rising or falling.

Upon power-up, should the $V_{DD(1-3)}$ voltage fail to reach the V_{DDUV+} threshold, the driver will not turn ON. Additionally during operation, if the $V_{DD(1-3)}$ voltage decreases below the V_{DDUV-} threshold during operation, the UVLO circuitry will recognize a fault condition and shut down the high and low-side gate drive outputs.

Upon power-up, should the $V_{BS(1-3)}$ voltage fail to reach the V_{BSUV+} threshold, the driver will not turn ON. Additionally during operation, if the $V_{BS(1-3)}$ voltage decreases below the V_{BSUV-} threshold, the UVLO circuitry will recognize a fault condition, and shut down the high-side gate outputs of the driver.

UVLO ensures that the drivers will turn on the corresponding IGBTs only when the gate supply voltage is sufficient enough to fully enhance the IGBTs. Without this feature, the gates of the IGBT could be driven with a low voltage causing the IGBTs to conduct current with a high saturation voltage. This could result in very high conduction losses within the power device, and could lead to IPM failure.

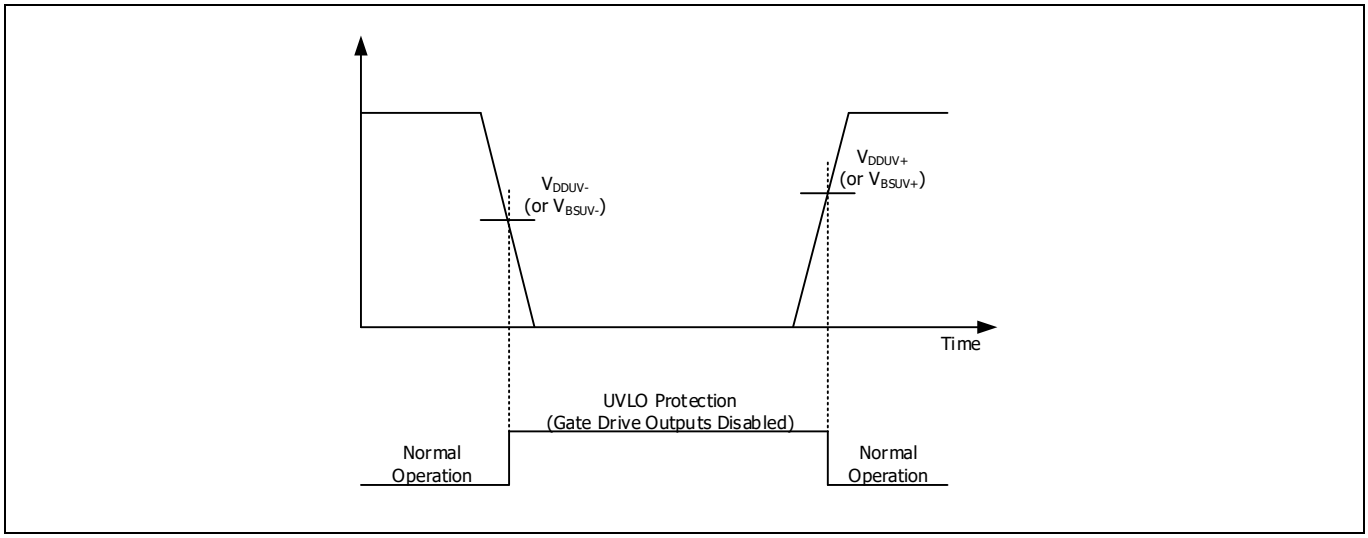

Figure 13 UVLO protection

Table 8 describes the functionality of the IPM over a range of control power supply voltages. We recommend connecting a low-impedance (low ESR, low ESL) electrolytic capacitor and high-frequency decoupling capacitors as close to the V_{DD} pins of the IPM as possible. Maximum ripple of the supply should not exceed ± 1 V/µs to prevent the internal drivers from malfunctioning.

The potential at the module's COM terminal is different from that at the $V_{R(1-3)}$ power terminals by the voltage drop across the shunt resistor(s). All control circuits and power supplies should refer to COM and not to the $V_{R(1-3)}$ nodes.

Table 8 CIPOS™ IPM versus control power supply voltage

Control voltage [V]	Functionality
0-2.5 V	IPM gate drivers are not functional, supply is not sufficient to have working active devices.
2.5-9.6 V (positive going) 2.5-8.6 V(negative going)	Gate driver logic circuits are working, the gate drivers are in UVLO, IGBTs are kept off.
11.2-13.5 V	Conduction and switching losses will be higher than under normal conditions. High-side transistors may not operate after $V_{B(1-3)}$ initial charging, as the $V_{B(1-3)}$ voltage level may not reach V_{BSUV+}.
13.5-16.5 V for $V_{DD(1-3)}$ 12.5-17.5 V for $V_{B(1-3)}$	Normal operation.
16.5-20 V for $V_{DD(1-3)}$ 17.5~20 V for $V_{B(1-3)}$	Because the control supply voltage is above the recommended range, the transistor's switching will be faster, which will cause an increase in system noise. Peak short-circuit current might be too large for proper operation of short-circuit protection.
Over 20 V	Damage of module may occur.

3.4 Over-temperature protection

All IM231-x6 IPMs have an internal negative-temperature coefficient (NTC) thermistor to sense the module temperature. The NTC thermistor is integrated in the module with one terminal of the chip connected to COM,

and the other to the VTH, which can be used to monitor the line temperature of the IPM. The resistance of the NTC can be calculated at any temperature as follows:

$$R_{TH} = R_{25} \cdot e^{[B\left(\frac{1}{T_{TH}} - \frac{1}{T_{25}}\right)]}$$

B (B-constant), R_{25} (resistance at 25°C), and R_{125} (resistance at 125°C) are given in the specific datasheet where an NTC is implemented. Characterization of the thermistor's resistance depending on temperature is shown in Table 9 below.

Table 9 Raw data of the thermistor used in IM231-x6

T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]	T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]
-40	1438.40	1568.15	1705.34	8.7%	45	18.930	20.097	21.282	5.9%
-35	1040.65	1130.82	1225.73	8.4%	50	15.448	16.432	17.436	6.1%
-30	761.64	825.03	891.47	8.1%	55	12.695	13.531	14.385	6.3%
-25	563.53	608.58	655.58	7.7%	60	10.4830	11.1942	11.9238	6.5%
-20	421.23	453.57	487.16	7.4%	65	8.6961	9.3033	9.9279	6.7%
-15	317.53	340.93	365.14	7.1%	70	7.2454	7.7652	8.3016	6.9%
-10	241.62	258.72	276.33	6.8%	75	6.0619	6.5084	6.9703	7.1%
-5	185.51	198.10	211.02	6.5%	80	5.0922	5.4767	5.8755	7.3%
0	143.62	152.98	162.53	6.2%	85	4.3017	4.6342	4.9800	7.5%
5	112.35	119.37	126.51	6.0%	90	3.6482	3.9366	4.2372	7.6%
10	88.440	93.740	99.109	5.7%	95	3.1056	3.3565	3.6186	7.8%
15	70.033	74.055	78.112	5.5%	100	2.6533	2.8721	3.1012	8.0%
20	55.770	58.837	61.918	5.2%	105	2.2748	2.4661	2.6669	8.1%
25	44.650	47.000	49.350	5.0%	110	1.9567	2.1245	2.3009	8.3%
30	35.772	37.737	39.711	5.2%	115	1.6886	1.8360	1.9913	8.5%
35	28.801	30.449	32.110	5.5%	120	1.4616	1.5915	1.7287	8.6%
40	23.298	24.682	26.084	5.7%	125	1.2690	1.3837	1.5050	8.8%

An external resistor network should be connected to the NTC to provide temperature readings. When pulled up to a rail voltage such as V_{DD} or 3.3 V by a resistor, the VTH pin provides an analog voltage signal corresponding to the temperature of the thermistor. This circuit can be connected to the ADC terminal of the microcontroller to shut down the module if the temperature reading is too high. An example of this circuit is shown below in Figure 13.

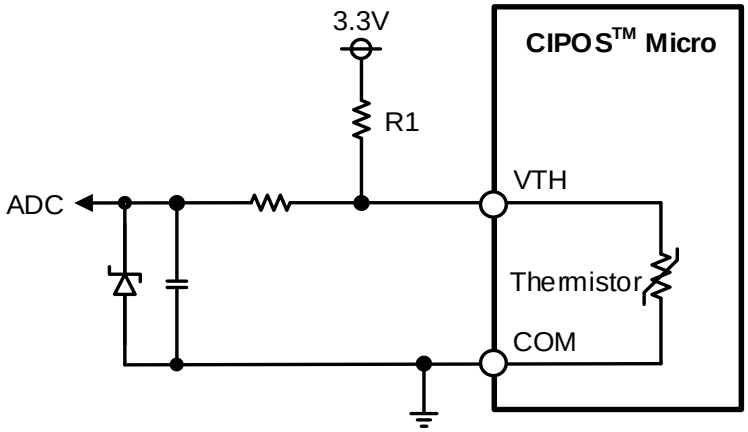

Figure 14 Example of over-temperature protection circuit

Please note that it remains the responsibility of the system designer to implement protection strategies against overheating that are appropriate for the system operating conditions. While the NTC provides temperature-reading outputs, it is remote from the power switches, which are the major heat source inside the IPM. Because of this, the NTC does not necessarily reflect the temperature of all internal components, as there will always be a timing and temperature difference. The actual NTC reading is affected by the thermal system design specified by the system designer, so some calibration of readings and actual temperature may be required depending on the application.

3.5 Advanced input filter

IM231-x6 includes an advanced noise filter providing beneficial noise rejection to short input pulses applied to LIN and HIN. The noise filter suppresses control pulses which are below the filter time T_{FILIN}. The filter acts according to Figure 14.

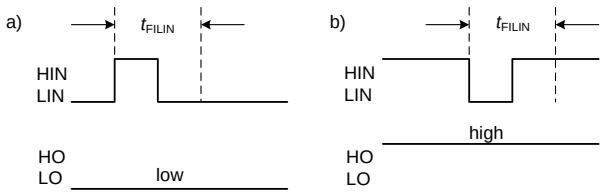

Figure 15 Input filter timing diagram

Compared to noise filters in competitor products, the advanced input filter also allows for an improvement in the input/output pulse symmetry of the gate driver. The working principle of the filter as compared with the standard competitor input filter is shown in Figure 15.

The figure shows the advanced input filter of the gate driver in IM231-x6, and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms

(Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

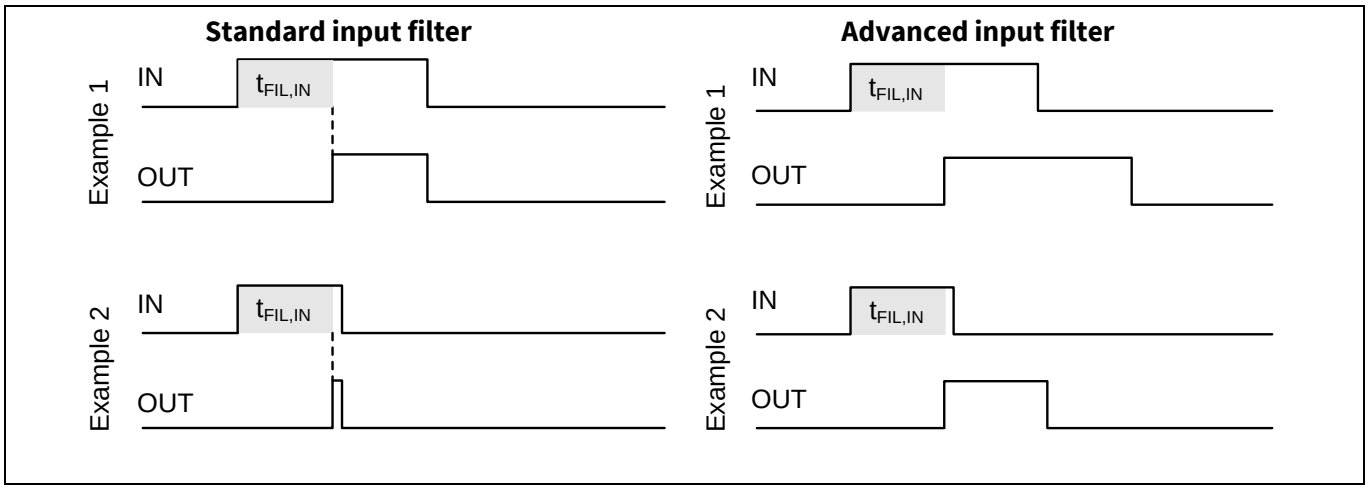

Figure 16 Standard input filter found in competitor products (left) and the advanced input filter in IM231-x6 (right)

4 Interface circuits and layout guide

4.1 Input/output signal connection

The following shows the I/O interface circuit between microcontroller and IM231-x6. The IPM input logic is high-active with weak 800 kΩ internal pull-down resistors. It is recommended to use external pull-down resistors on each PWM input pin in the range of 10 kΩ to 100 kΩ. The RFE output is configured as an open-drain MOSFET. This signal should thus be pulled up to 5 V or 3.3 V external logic power supply with a resistor. The resistor should be carefully chosen as per Section 3.2.

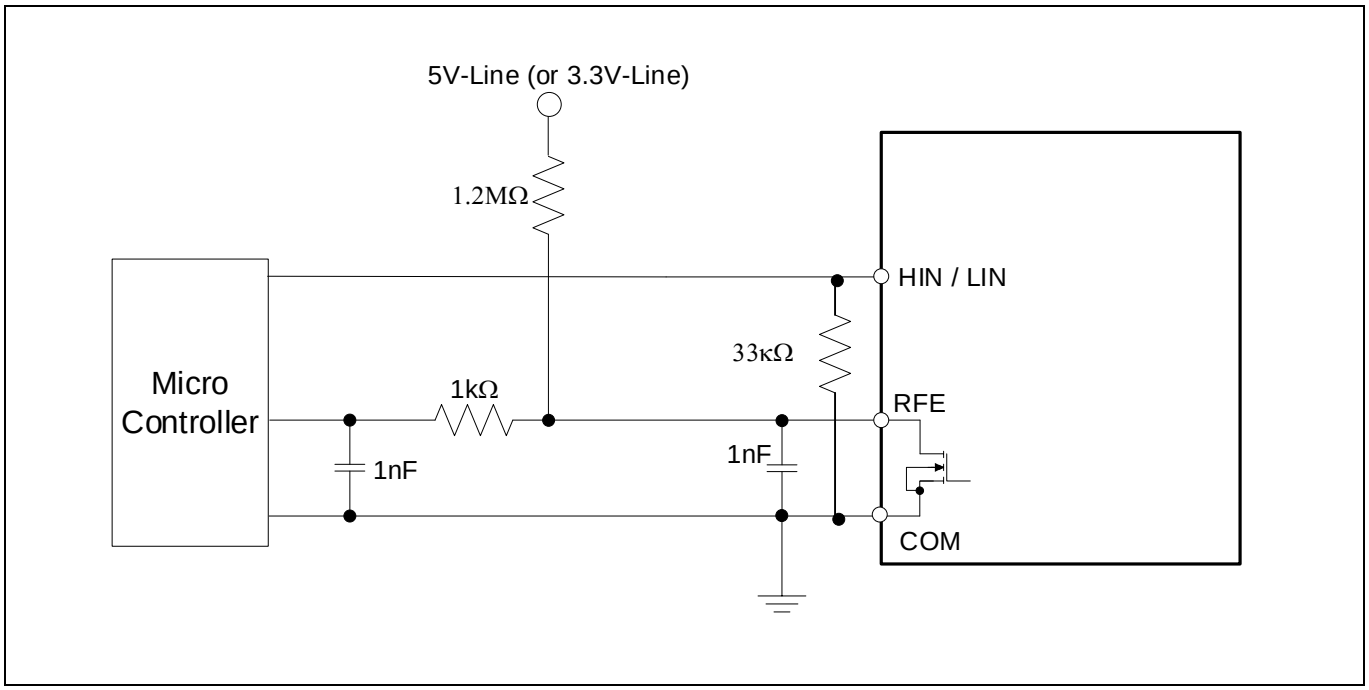

Figure 17 Recommended microcontroller I/O interface circuit

Table 10 Maximum rating of input and RFE pin

Item	Symbol	Condition	Rating	Unit
Module supply voltage	V_{DD}	Applied between V_{DD} – COM	-0.3 ~ 20	V
Input voltage	V_{IN}	Applied between HIN(1,2,3)– COM, LIN(1,2,3) – COM, ITRIP to COM	-0.3 ~ 20	V
Fault output supply voltage	RFE	Applied between RFE – COM	-0.3 ~ 20	V

The input and fault output maximum rating voltages are listed in Table 10. The fault output is open-drain configured and is rated up to 20V. However, it is recommended that the fault output be pulled up to 5 V or 3.3V logic supply used for the inputs. We recommend connecting bypass capacitors as close as possible to the RFE pin to avoid any noise that might turn on the open-drain MOSFET .

4.2 General interface circuit example

Figure 17 shows a typical application circuit interface schematic with control signals connected directly to the microcontroller.

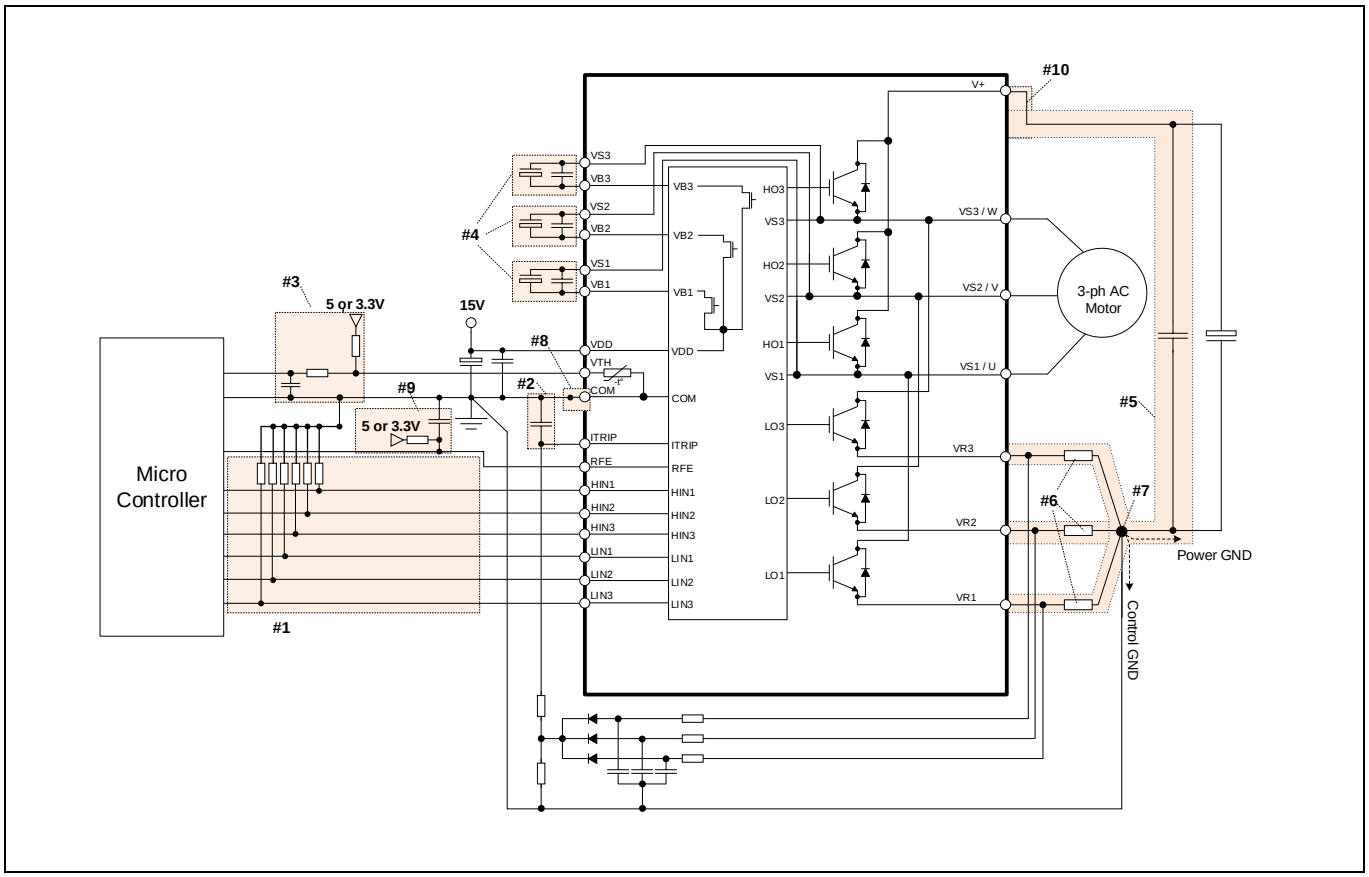

Figure 18 Example of application circuit

1. **Input circuit**
   - Pull-down resistors on each PWM input (~30 kΩ)
2. **Itrip circuit**
   - To prevent faulty operation of the protection function, an RC filter is recommended
   - The capacitor must be located close to Itrip and COM terminals.
3. **VTH circuit**
   - To define suitable voltage for temperature monitoring, this terminal should be pulled up to the bias voltage of 5 V/3.3 V by a proper resistor.
   - It is recommended that the RC filter be placed close to the controller.
4. **VB-VS circuit**
   - Capacitors for high-side floating supply voltage should be placed close to VB and VS terminals.
   - Additional high-frequency capacitors, typically 0.1 mF, are strongly recommended.
   - Overlap of pattern-to-motor and pattern-to-bootstrap capacitors should be minimized.
5. **Snubber capacitor**
   - The snubber capacitor and shunt resistors should be as short as possible.
6. **Shunt resistor**
   - SMD type shunt resistors are strongly recommended to minimize internal stray inductance.

7. **Ground pattern**
   - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at the common end of shunt resistors only for the same potential.
9. **RFE circuit**
   - To set up R and C parameters for fault-clear time.
   - RFE is low-active. The pin should always be pulled up to 3.3 V or 5 V.
   - This R is also mandatory for the fault-reporting function because it is an open-drain structure.
   - Please refer to Section 3.2 for additional details.

4.3 Recommended circuit current of power supply

Control and gate driver power is normally provided by a single 15-V supply that is connected to the module VDD pins. The circuit current of V_{DD} control supply is shown below in Table 11. Please note these values are for reference only, and are not tested during production.

Table 11 The circuit current of control power supply of IM231-L6T2B [mA]

Item		Static (typical)	Dynamic (typical)	Total (typical)
V_{DD}=15 V	F_{SW}=5 KHz	6.6	1.2	7.8
	F_{SW}=15 KHz	6.6	1.8	8.4
V_{DD}=20 V	F_{SW}=20 KHz	10.2	2.9	13.1

And, the circuit current of the 5-V logic power supply (VTH, RFE and input terminal) is about 20 mA.

Finally, the recommended minimum current of the power supply is shown in Table 12 below. This value considers ripple and sufficient margins at given conditions.

Table 12 The recommended minimum circuit current of power supply [mA]

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
$V_{DD} \le 20$ V, $F_{SW} \le 20$ KHz	90	45

4.4 Recommended layout pattern for OCP and SCP functions

It is recommended that the ITRIP filter capacitor connections to the IM231-x6 pins be as short as possible. The ITRIP filter capacitor should be connected to the COM pin directly without an overlapped ground pattern. The signal ground and power ground should be as short as possible, and connected at only one point via the filter capacitor of V_{DD} line. The ITRIP function combined with the external shunt resistor can be used to detect overcurrent events in the ground path that will result in the damaging of the IPM. The internal gate driver will continuously monitor the voltage on the ITRIP pin. If this voltage exceeds the reference voltage (typ. 0.5 V) a fault signal will be generated on the RFE pin, and all six IGBTs will be turned OFF.

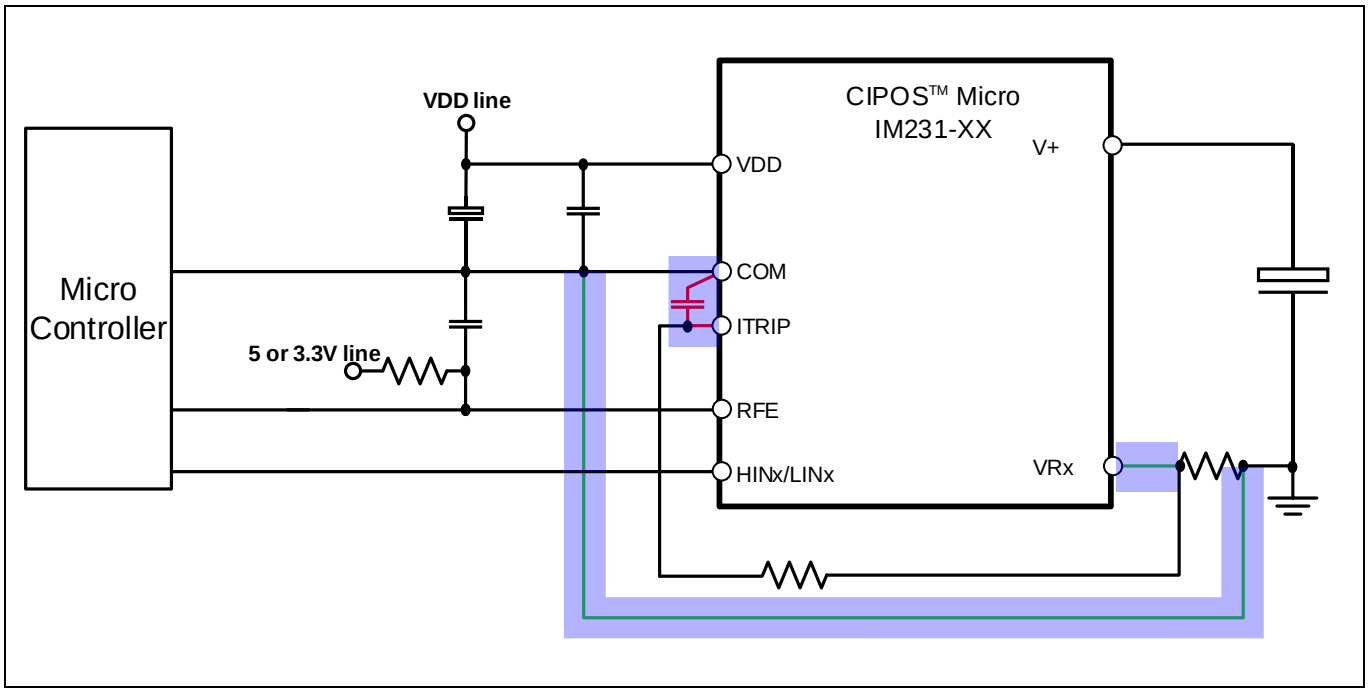

Figure 19 Recommended layout for ground and overcurrent protection traces.

4.5 Recommended wiring of shunt resistor and snubber capacitor

External current-sensing resistors are applied to detect the overcurrent of phase currents. A long wiring pattern between the shunt resistors and IM231-x6 will cause excessive surges that might damage the IPM's internal gate drivers and current-detection components. This may also distort the sensing signals that may lead to loss of control when driving a motor. To decrease the pattern inductance, the wiring between the shunt resistors and IPM should be as short as possible, and any loop should be avoided.

As shown in Figure 19, snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally, a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location ('1' as shown in Figure 19), the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in location '2', the charging and discharging currents generated by the wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal, and the SC protection level will be a bit lower than the calculated design value. The '2' position surge suppression effect is greater than in location '1' or '3'. The '3' position is a reasonable compromise with better suppression than location '1' without impacting the current-sensing signal accuracy. For this reason, the location '3' is generally used.

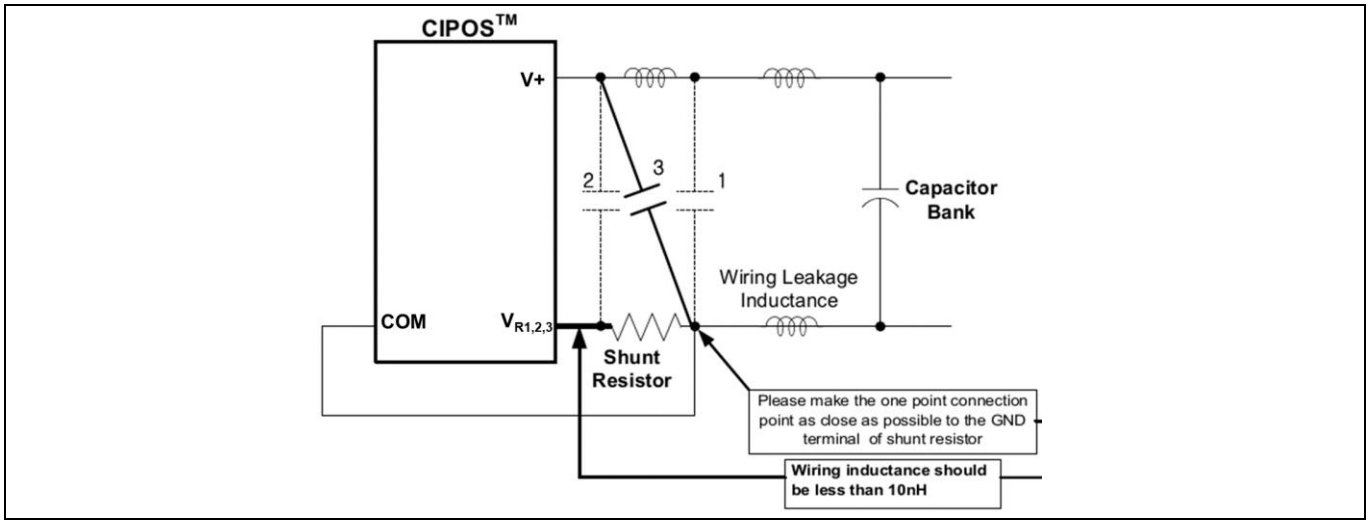

Figure 20 Proper snubber capacitor use

General suggestions and summary:

- PCB traces should be designed as short as possible and the area of the circuit (power or signal) should be minimized to avoid any noise.
- Make sure there is a good distance between switching lines with high dI/dt and dV/dt and the signal lines, as they are very sensitive to electrical noise. Specifically, the trace of each OUT phase carrying significant fast current and voltage transition should be separated from the logic lines and analog sensing circuits (ITRIP, RFE).
- Place shunt resistors as close as possible to the low-side emitter pins of the IPM. Parasitic inductance should be as low as possible. Use of low inductance SMD resistors is recommended.
- Avoid any ground loop. Only a single path must connect to COM.
- Place each RC filter as close as possible to the IPM pins to increase their efficiency.
- Fixed voltage tracks such as GND and high-voltage lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines.

4.6 Pin and screw hole coordinates for IM231-x6 footprint

Figure 20 shows the pinout of IM231-x6T2B. The coordinates of each pin and screw hole (in mm) relative to Pin 1 are shown in Table 13.

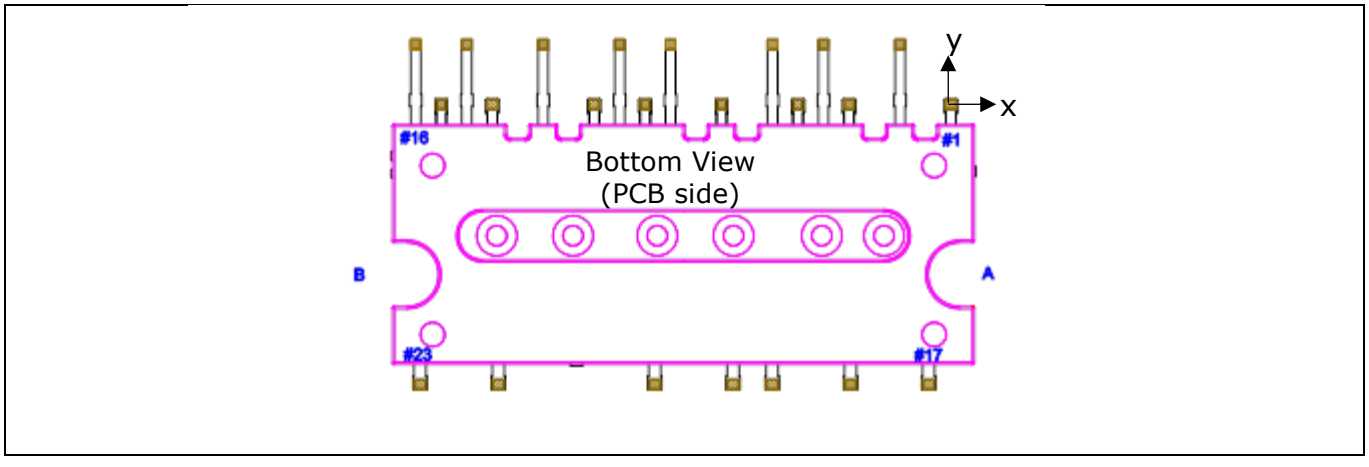

Figure 21 IM231-x6 pin positions on PCB

Table 13 Pin and screw hole coordinates respectively relative to Pin 1

Pin	x	y
1	0.00	0.00
2	-2.54	3.00
3	-5.08	0.00
4	-6.35	3.00
5	-7.62	0.00
6	-8.89	3.00
7	-11.43	0.00
8	-13.97	3.00
9	-15.24	0.00
10	-16.51	3.00
11	-17.78	0.00
12	-20.32	3.00
13	-22.86	0.00
14	-24.13	3.00
15	-25.40	0.00
16	-26.67	3.00
17	-1.11	-14.00
18	-5.01	-14.00
19	-8.91	-14.00
20	-10.86	-14.00
21	-14.76	-14.00
22	-22.56	-14.00
23	-26.46	-14.00

Screw Hole	x	y
A	0.47	-8.50
B	-27.14	-8.50

5 Bootstrap circuit

5.1 Bootstrap-circuit operation

The V_{BS} voltage, which is the voltage difference between V_B (1-3) and V_S (1-3), supplies voltage to the high-side circuitry of the gate driver, and must be in the range of 12.5~17.5 V. As described in Section 3.3, all CIPOS™ Micro IPMs including IM231-x6 have an undervoltage protection function for V_{BS}.

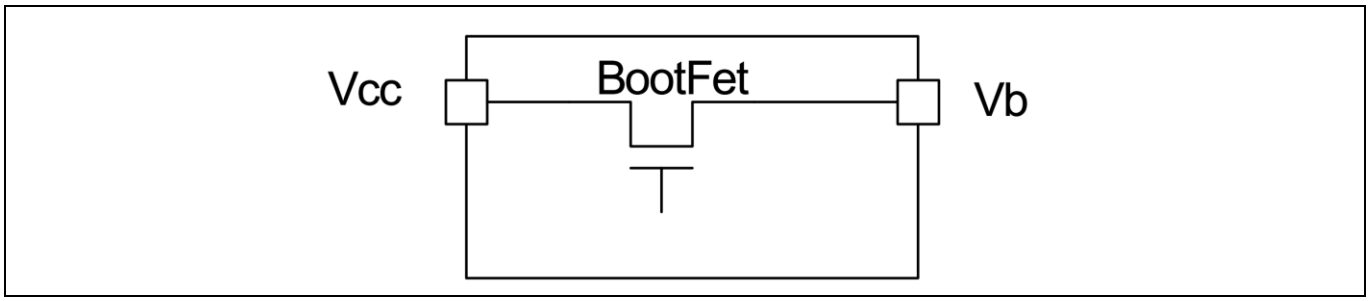

Figure 22 Simplified BootFET internal connection

Internal bootstrap circuitry consists of three high-voltage bootFETs that eliminate the need for any external high-voltage diodes and resistors. One bootFET is integrated for each high-side output channel, and is connected between V_{DD} supply and its respective floating supply (V_{B1}, V_{B2}, V_{B3}) as shown in Figure 21. The integrated bootFET is turned ON during the time when LO is 'high', and has a limited source current due to intrinsic R_{BS}. V_{BS} will increase each cycle depending on the duration of LO, value of the C_{BS} capacitor, the collector-emitter drop of the corresponding low-side IGBT, and the low-side, free-wheeling diode drop.

The bootFET of each channel follows the state of low-side output stage, i.e. the bootFET is ON when LO is 'high', unless the V_B voltage is higher than V_{DD}. In that case, the bootstrap FET is designed to remain off until V_B returns below that threshold. This concept is illustrated in Figure 22.

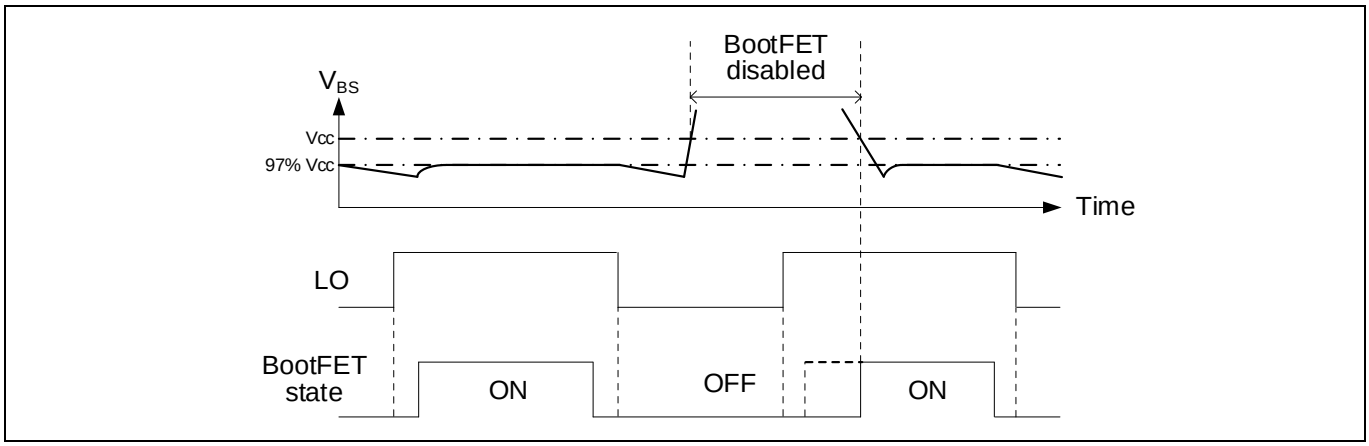

Figure 23 BootFET timing diagram

A bootFET is suitable for most PWM modulation schemes, and can be used either in parallel with an external bootstrap network (diode + resistor) or as replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may, however, have some limitations. An example of this limitation may arise when this functionality is used in non-complementary PWM schemes and at very high PWM duty cycles. In these cases, superior performance can be achieved by using an external bootstrap diode and resistor in parallel with the internal bootstrap network.

5.2 Initial charging of bootstrap capacitor

To charge the bootstrap capacitor, a sufficient on-time duration of the low-side IGBT is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq \frac{C_{BS} \cdot R_{BS}}{\delta} \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(\min)} - V_{LS}}\right)$$

Where,

- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- V_{LS} = Voltage drop across the low-side IGBT
- δ = Duty ratio of PWM
-

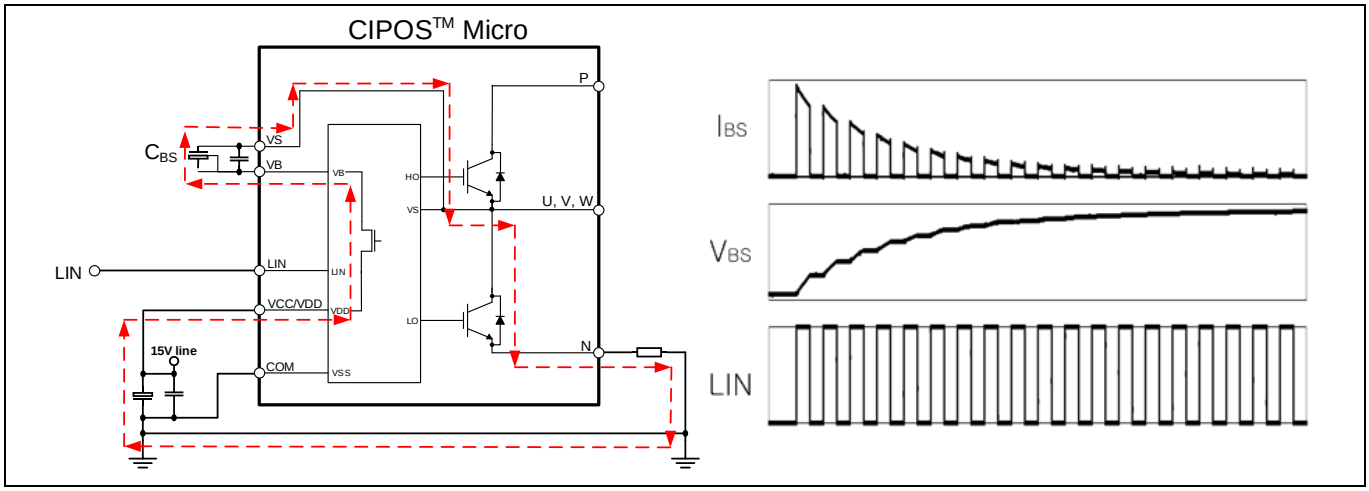

Figure 24 BootFET circuit operation and timing chart of initial FET charging

5.3 Bootstrap capacitor selection

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \cdot \Delta t}{\Delta V_{BS}}$$

Where,

- Δt = maximum ON pulse width of high-side IGBT
- ΔV_{BS} = the allowable discharge voltage of the C_{BS}
- I_{leak}= maximum discharge current of the C_{BS} mainly via the following mechanisms:
  - Gate charge for turning on the high-side IGBT
  - Quiescent current to the high-side circuit in the IC
  - Level-shift charge required by level shifters in the IC
  - Leakage current in the bootstrap diode
  - C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
  - Bootstrap-diode reverse-recovery charge

In practice, a leakage current of 1 mA is recommended as a calculation basis. By taking into consideration dispersion and reliability, the capacitance is generally selected to be 2~3 times higher than the calculated one.

The C_{BS} is only charged when the high-side IGBT is off and the VS voltage is pulled down to ground. Therefore, the ON-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum ON-time of the low-side IGBT (or OFF-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the module pins as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the IPM is essential if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

5.4 Charging/ discharging of bootstrap capacitor during operation

The bootstrap capacitor C_{BS} charges through the bootFET from the V_{DD} supply when the high-side IGBT is off, and the VS voltage is pulled down to ground. It discharges when the high-side IGBT or diode are on.

5.4.1 Example 1: Selection of initial charging time

An example calculation of the minimum value of the initial charging time:

Conditions:

- C_{BS}=4. 7 µF, R_{BS} = 200 Ω, Duty Ratio (δ)= 0.5, V_{DD} = 15 V
- $V_{BS\,(min)}$ = 12.5 V
- V_{LS} = 0.1 V
- $t_{charge} \geq 4.7\mu F \times 200\Omega \times \frac{1}{0.5} \times \ln(\frac{15V}{15V-12.5V-0.1V})$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

5.4.2 Example 2: Minimum value of bootstrap capacitor

Based on the conditions given above, a minimum value of bootstrap capacitor can be chosen based on switching frequency.

Conditions:

- ΔV_{BS}=0.1 V, I_{leak}= 1 mA

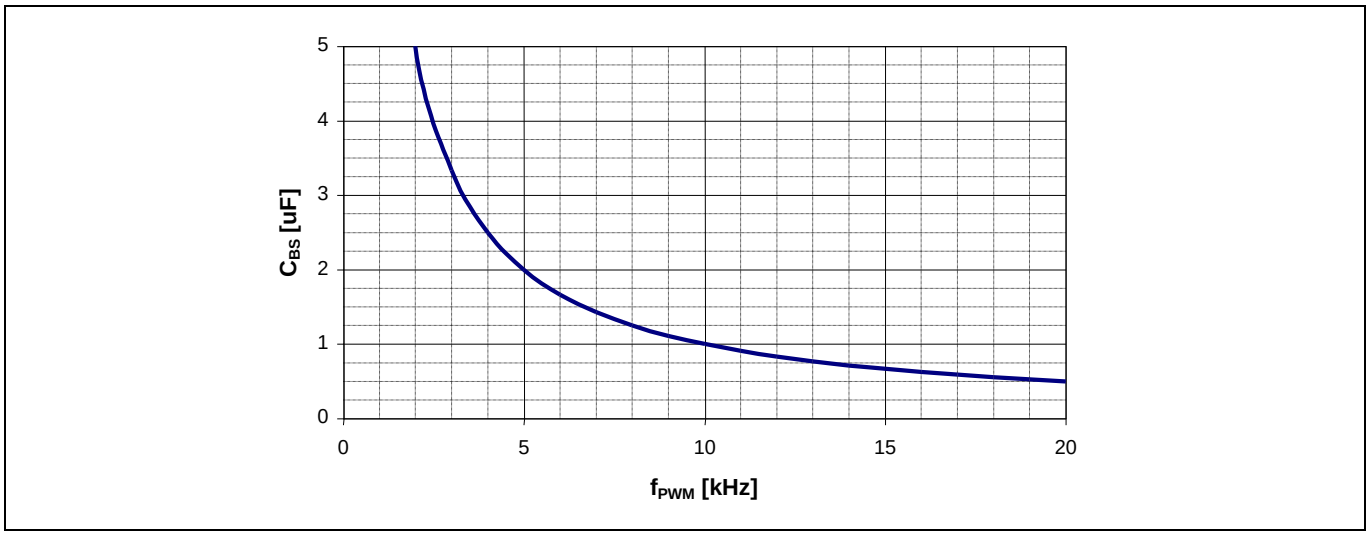

Figure 25 Bootstrap capacitance as a function of switching frequency

Figure 24 shows the curve for a continuous sinusoidal modulation if the voltage ripple (ΔV_{BS}) is 0.1 V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range of up to 2.2 µF for most common switching frequencies.

It is recommended that the system design considers the actual control pattern when designing the bootstrap circuit.

6 Thermal system design

The thermal design of a system is a key issue included in electronic systems such as drives. In order to avoid overheating and/or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing CIPOS™ Micro as an intelligent power module for the application. A good thermal design allows the user to either maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction to power losses and heat sinks, helping to understand the mode of operation, and to find the right heat sink for a specific application if needed.

For the thermal design, the following is required:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,\ max}$ of the power semiconductors
- The maximum allowable ambient temperature $T_{A,\ max}$
- The junction-to-ambient thermal resistance impedance $Z_{th,\ J\text{-}A}$. For steady-state considerations, the static thermal resistance $R_{th,J\text{-}A}$ is sufficient. This thermal resistance comprises the junction-to-case thermal resistance $Rth_{,J\text{-}C}$ as provided in datasheets, the case-to-heat sink thermal resistance $R_{th,C\text{-}HS}$ accounting for the heat flow through the thermal interface material between heat sink and the power module, and the heat sink-to-ambient thermal resistance $R_{th,HS\text{-}A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances.

6.1 Online motor-drive-simulation tool

The CIPOS™ IPM Motor Drive Simulation Tool, which is available on Infineon's website (www.infineon.com/plex-ipm), offers help to users for part selection and design decisions. This tool allows the user to simulate and compare IPM parts using three-phase motor conditions to determine which module best suits their needs. The tool shows the expected temperature of the selected IPM, the approximate losses of the system, and also generates output voltage, current, junction temperature and loss waveforms. It is recommended to test parts with planned motor conditions in the simulation tool prior to physical design. A user manual and video tutorial to aid in tool use is provided on the webpage.

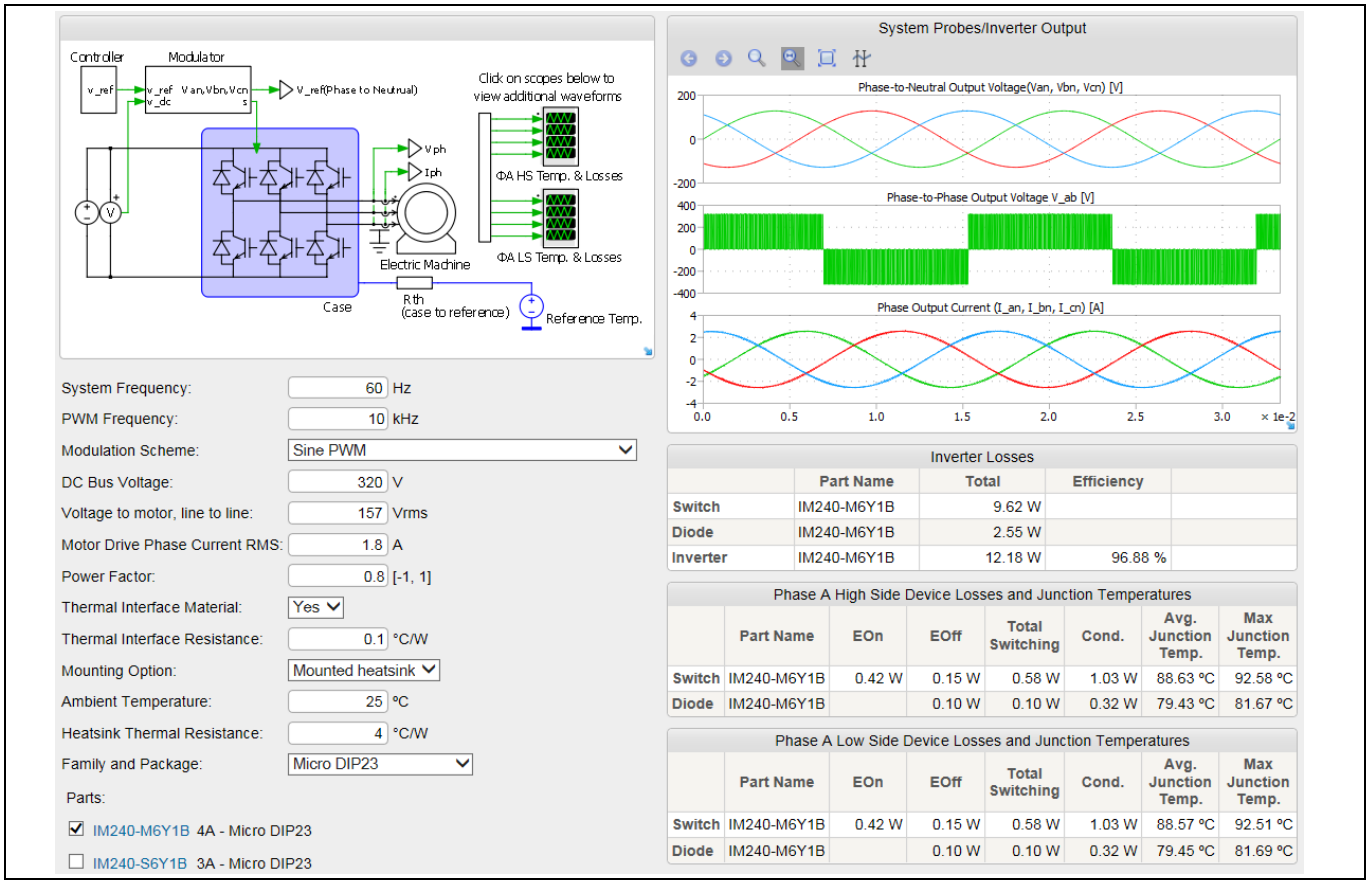

Figure 26 CIPOS™ IPM motor-drive-simulation tool example for IM240-M6Y1B

This tool provides a breakdown of losses, and can provide a glimpse of the tradeoff between switching and conduction losses in the module for given conditions and design. Alternatively, these losses can be calculated based on the formulas discussed in the next sections.

6.2 Power loss

Total power losses in the module are composed of conduction and switching losses in the power switch.

Detailed equations are provided below to calculate both conduction and switching losses of the module for a three-phase continuous sinusoidal modulation scheme. For other cases, like three-phase discontinuous modulation, please see [1].

6.2.1 Conduction loss

Conduction losses depend on the DC electrical characteristics of the device, i.e., saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature.

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively:

$$V_{IGBT} = V_I + R_I \cdot i$$

$$V_{DIODE} = V_D + R_D \cdot i$$

Where,

- V_I=Threshold voltage of IGBT
- V_D= Threshold voltage of monolithic body diode
- R_I= ON-state slope resistance of IGBT
- R_D=ON-state slope resistance of monolithic body diode
- Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal and can be calculated by:
- $i = I_{Peak} \cdot \cos(\theta - \varphi)$

Where,

- φ = phase angle difference between output voltage and current.
- Using the equations above, the conduction loss of one IGBT and its monolithic body diode can be obtained as follows:
- $P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \delta(V_{IGBT} \cdot i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_I + \frac{{I_{peak}}^2}{3\pi}R_I MI\cos\varphi$
- $P_{con.D} = \frac{1}{2\pi}\int_0^{\pi}(1-\delta)(V_{DIODE} \cdot i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_D - \frac{{I_{peak}}^2}{3\pi}R_D MI\cos\varphi$
- $P_{con} = P_{con.I} + P_{con.D}$
- Where,
- δ= duty cycle given in PWM method.
- This can be calculated by:
- $\delta = \frac{1+MI\cos(\theta)}{2}$
- Where,
- MI = PWM modulation index (MI, defined as the peak phase voltage divided by half of DC link voltage).
- It should be noted that the total inverter conduction losses are six times that of P_{con}.

6.2.2 Switching loss

Switching losses are determined by dynamic characteristics like turn-on and off time as well as the presence of overvoltage and overcurrent transients. Hence, in order to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency and the power circuit layout, operating current and operating temperature should be considered.

Therefore the linear dependency of the switching energy loss on the switched current is expressed during one switching period as follows:

$$E_I = E_{I.on} + E_{I.off}$$

$$E_D = E_{D.on} + E_{D.off}$$

Where,

- E_I = switching loss energy of the IGBT
- E_D= switching loss energy of monolithic diode
- E_I and E_D can be considered a constant.

As mentioned in the conduction-loss explanation, the output current can be considered a sinusoidal waveform, and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore depending on the switching frequency, f_{sw}, the switching loss of one device is the following equation:

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_I + E_D)\cdot i \cdot f_{sw}d\varphi = \frac{(E_I + E_D)\cdot f_{sw}\cdot I_{peak}}{\pi}$$

- These constants should be derived by experimental measurement. From the above equation, it should be noted that the switching losses are a linear function of current, and directly proportional to switching frequency.

6.3 Thermal impedance

During operation, power losses generate heat, which elevates the temperature in the semiconductor junctions. High junction temperatures limit the performance and the lifetime of the module. Thus, the thermal design of the package is a very important factor in the module development stage. Thermal design is also important in the development of the motor drive system. The heat generated from the module must be properly transferred to the environment using an adequate cooling system.

Thermal impedance qualifies the capability of a given thermal path to transfer heat in the steady state.

$$Z_{TH}(t) = \frac{\Delta T(t)}{P}$$

Thermal impedance is typically represented by an RC equivalent circuit as shown in Figure 26.

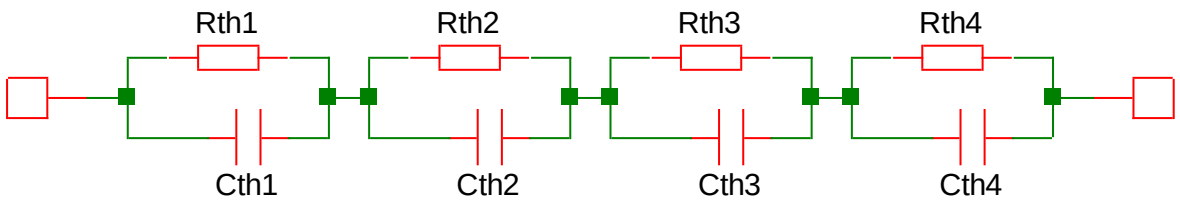

Figure 27 Thermal impedance RC equivalent circuit (Foster model)

Under sinusoidal modulation, the power loss has to be calculated in each switching cycle, as the device current changes within each half modulation cycle, as illustrated in Figure 27. The upper portion is the high-side switch current which is used to calculate E_{ON} and E_{OFF} of the switch. The lower portion in Figure 27 is the low-side diode current for E_{RR}.

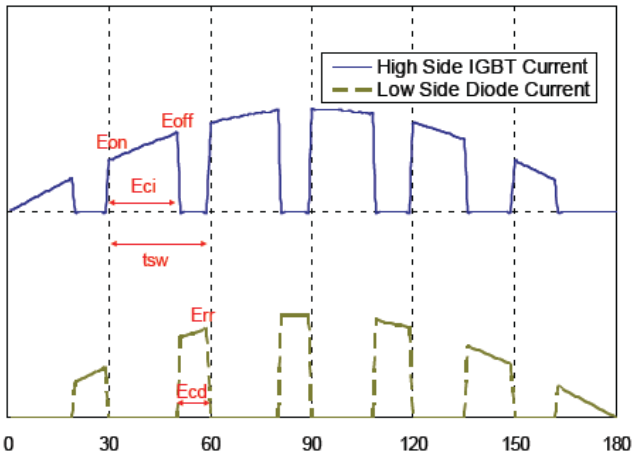

Figure 28 Loss calculation of sinusoidal modulation

Because the loss is not constant over time, its shape depends on current waveforms and device parameters. Figure 28 illustrates the power loss of a single switch in a typical case.

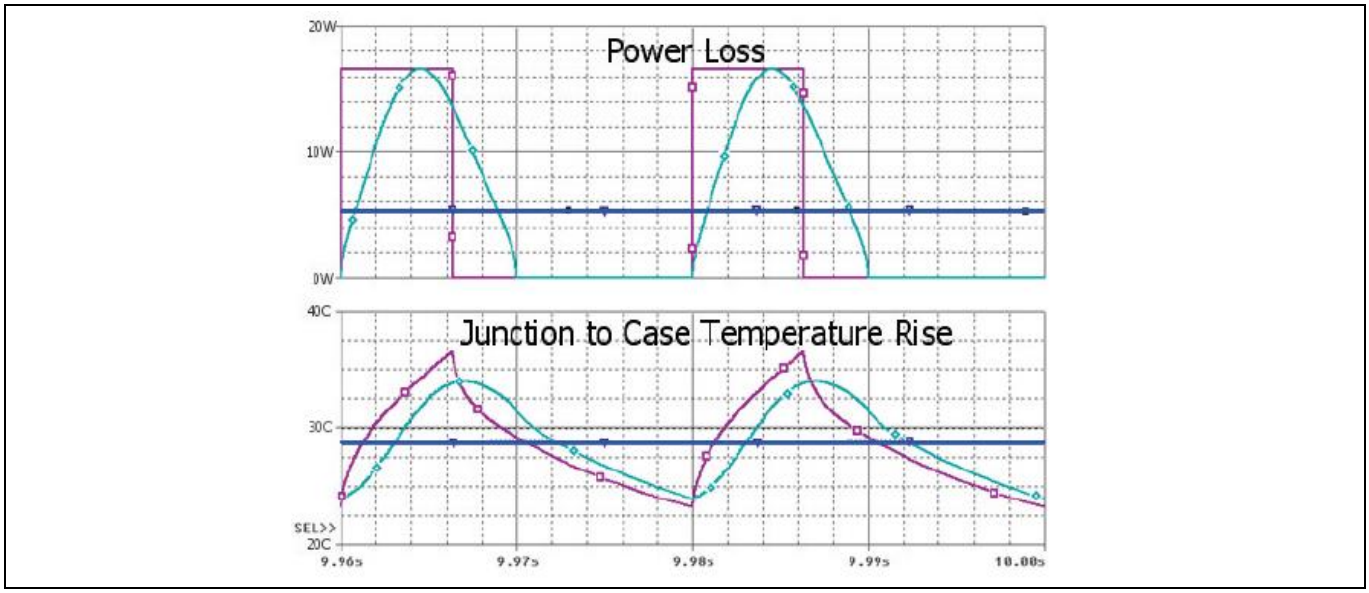

Figure 29 Junction-temperature calculations under sinusoidal modulation

6.4 Heat sink selection guide

6.4.1 Required heat sink performance

If the power losses (P_{SW}), junction-to-case thermal resistance ($R_{th\,(J\text{-}C)}$), and maximum ambient temperature are known, the required heat sink thermal resistance and the thermal interface material can be calculated for the specific application. This can be done using the formula:

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + \max(P_{sw,i} \cdot R_{th,JC,i})$$

For three-phase IPMs, it can be assumed that all power switches dissipate the same power and have the same $R_{th(J\text{-}C)}$ within reason. The required thermal resistance from case to ambient can then be calculated:

$$R_{th,C-A} = R_{th,C-S} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}}$$

6.4.1.1 Calculating required heat sink performance example

The power switches of an outdoor fan drive dissipate 0.8 W maximum each. The maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th\,(J\text{-}C)}$ of the module is 6°K/W. With this information, $Rth_{(C\text{-}A)}$ can be calculated:

$$R_{th,C-A} \leq \frac{150°C - 0.8W \cdot 6\frac{°K}{W} - 50°C}{6 \cdot 0.8W} = 19.8\frac{°K}{W}$$

If the heat sink temperature is limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \leq \frac{100°C - 50°C}{6 \cdot 0.8W} = 10.4\frac{°K}{W}$$

Smaller heat sinks with higher thermal resistance may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink, the larger its thermal capacitance, i.e., the longer it takes to heat up.

6.4.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to heat sink
- Heat transfer within the heat sink (to all the surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

6.4.2.1 Heat transfer from heat source to heat sink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heat sink:

- Flatness of the contact area
- Due to the unevenness of surfaces, a thermal interface material needs to be supplied between heat source and heat sink. Such materials have a rather low thermal conductivity (<10 K/W) and therefore should be as thin as possible. The material still needs to fill out the space between heat source and heat sink, and an unevenness of the inserted material should be avoided. In addition, the particle size of the interface material must fit to the roughness of the module and the heat sink surfaces. Particles that are too large will unnecessarily increase the thickness of the interface layer, and increase the overall thermal resistance. Particles that are too small will not provide a good contact between the two surfaces, and will also lead to a higher thermal resistance.
- Mounting pressure

The higher the mounting pressure, the better the interface material disperses. Excessive interface material is squeezed out resulting in a thinner interface layer with a lower thermal resistance.

6.4.2.2 Heat transfer within heat sink

The heat transfer within the heat sink is mainly determined by:

- Heat sink material
- The material needs to be a good thermal conductor. Most heat sinks are made of aluminum ($\lambda \approx 200$ W/ (m·K)). Copper is heavier and more expensive but also nearly twice as efficient ($\lambda \approx 400$ W/ (m·K)).
- Fin thickness
- If the fins are too thin, the thermal resistance from the heat source to each fin will be too high, and the efficiency of the fins reduced. Hence, it does not make sense to make the fins as thin as possible to increase the surface area by including more fins.

Please note that heat sinks have a thermal spreading resistance in which not all points of the heat sink will be at the same temperature, which may lead to local hotspots at the center of the IPM. This must be considered in order to calculate heat transfer accurately.

6.4.2.3 Heat transfer from heat sink surface to ambient

Heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as:

$$R_{th,conv} = \frac{1}{\alpha \cdot A} V$$

Where,

- α = heat transfer coefficient

- A = surface area
- This leads to two important factors:
- Surface area
- Heat sinks require a huge surface area in order to easily transfer the heat to ambient. Since the heat source is assumed to be concentrated at one point, and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in Section 6.4.7.2.
- Heat transfer coefficient
- This coefficient is strongly dependent on the air flow velocity, as shown in Figure 29. If externally induced, air flow is used to aid in the transfer of heat; this is called forced convection. Otherwise, the transfer of heat with no additional help is considered natural convection. Heat sinks with very small fin spacing do not allow a good air flow. If a fan is used (forced convection), then the fin gaps of the heat sink may be reduced, as the fan forces the air through the space between the fins.

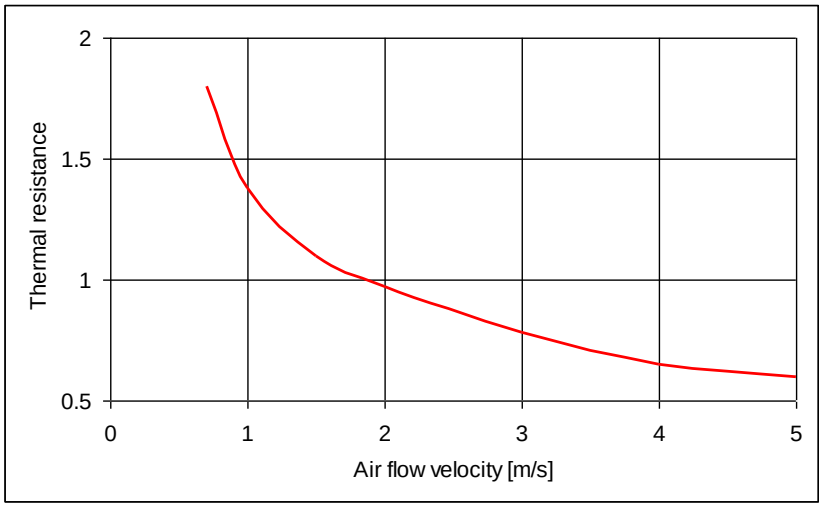

Figure 30 Thermal resistance vs. air flow velocity

In cases of natural convection, the heat sink efficiency depends on the temperature difference between heat sink and ambient (i.e. on the dissipated power). Some manufacturers, like Aavid Thermalloy, provide a correction table which allows the calculation of thermal resistance dependent on the temperature difference [2]. Figure 30 shows the heat sink efficiency degradation for natural convection as provided by Aavid Thermalloy in [2]. As per this correction chart, please note that the thermal resistance is 25% higher at 30 W than at 75 W.

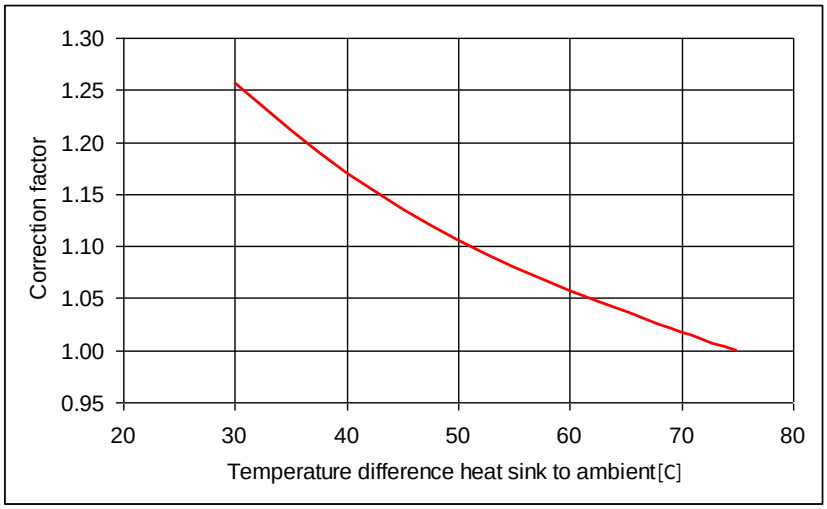

Figure 31 Correction factors for temperature

The positioning of the heat sink also plays an important role. In the case of natural convection, the best heat sink mounting position is with the fins of the heat sink mounted vertically, as the heated air tends to move upwards. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well supporting the heat transfer from heat sink to ambient. In order to increase the dissipation via radiation, one can use anodized heat sinks with a black surface. While radiated heat is negligible in forced convection conditions, it does slightly decrease the thermal resistance of the heat sink in cases of natural convection. Black heat sinks are thus preferable in natural convection conditions.

The discussions in this section clearly show that there cannot be only one thermal resistance value assigned to a certain heat sink.

6.4.2.4 Selecting a heat sink

Unfortunately, there is no straightforward method for selecting a heat sink. Finding a sufficient heat sink most likely will include an iterative process of choosing and testing heat sinks. In order to get a first rough estimation of the required volume of a heat sink, one can start with estimated volumetric thermal resistances, as given in Table 14 below (taken from [3]). This table only gives initial values, as the actual resistance varies for multiple parameters like dimensions, type, orientation, etc.

Table 14 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm³ °C/W]
Natural convection	500~800
1.0	150~250
2.5	80~150
5.0	50~80

It can be roughly assumed that the volume of a heat sink needs to be quadrupled in order to halve its thermal resistance. This gives an idea about whether natural convection is sufficient for the available space, or forced convection is required.

In order to select an optimized heat sink for a given application, one needs to contact heat sink manufacturers or consultants.

When contacting heat sink manufacturers, please check the conditions under which the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heat sink. Also take care that the fin spacing is optimized for the corresponding flow conditions.

7 Heat sink mounting and handling

7.1 Heat sink mounting guidelines

An adequate heat sinking capability of the IM231-x6 is only achievable if it is properly mounted. The following general points should be observed when mounting IM231-x6 on a heat sink.

- There should be no burrs on aluminum or copper heat sinks.
- There should be no unevenness or scratches in the heat sink.
- The surface of the module must be completely in contact with the heat sink.
- There should be no oxidation, stain or burrs on the heat sink surface.

To improve the thermal conductivity, apply thermal grease to the contact surface between the IM231-x6 and heat sink. Spread a homogenous layer of grease with a thickness of 100 µm over the IM231-x6 surface. Non-planar surfaces of the heat sink may require a thicker layer of thermal grease. Please refer to the specifications of the heat sink manufacturer. It is important to note that the heat sink covers the complete top surface of the module. There may be different functional behavior if there is a portion of the top surface which is not in contact with the heat sink.

In general, if your heat sink surface roughness is greater than 3 µm Ra, we advise you to use a thermal pad. We do not recommend using a heat sink surface with greater than 20 µm Ra even with a thermal pad.

It is considered the basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, assembled with the final production process, to help achieve high-quality applications.

As shown in Table 15, the recommended tightening torque for M3 screws is 0.8 Nm (typical) for a standard thermal grease interface. Table 15 also shows the recommended tightening torque for M3 screws for the Bergquist® SIL-PAD 1500ST thermal pad. Thermal pads can vary significantly in their properties. We thus recommend a detailed study of torque requirements be performed for thermal pads or interface materials not shown in this table.

Table 15 Mechanical characteristics and ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Curvature of module backside	BC	See datasheet Figure 9	-50	-	50	µm
Mounting Torque	T	M3 screw & washer, thermal grease	-	0.8	1.2	Nm
		M3 screw & washer, SIL-PAD 1500ST	-	0.6	1.0	Nm

Screws are commonly used to fasten the module to the heat sink. It is recommended that M2.5 or M3 screws are used in conjunction with a spring washer and a plain washer of standard or small corresponding size. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool. The tightening process is as follows:

- Align module with the fixing holes
- Insert screw A with washers only until the module surface, screw head and washers begin to come into contact with each other
- Repeat for screw B
- Tighten screw A to half the final torque
- Tighten screw B to half the final torque
- Tighten screw A to the final torque
- Tighten screw B to the final torque

When installing a module to a heat sink, excessive and uneven torque may degrade or damage the module.

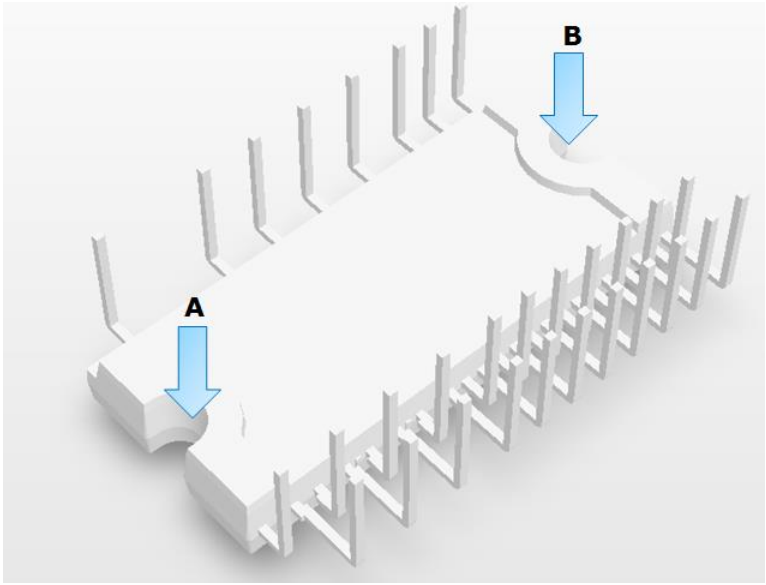

Figure 32 Recommended screw tightening order

7.2 Handling guidelines

Properly apply thermal conductive grease over the contact surface between the module and the heatsink. This is also useful for preventing corrosion to the contact surface. The grease should be of stable quality and long-term durability within a wide operating temperature range. Ensure there are no debris remaining on the contact surface between the module and the heat sink. All equipment, which is used to handle or mount the module, should comply with the relevant ESD standards. This includes transportation, storage and assembly. The module itself is an ESD-sensitive device. It may therefore be damaged in the case of ESD shocks.

Do not shake or handle the system board by gripping only the heat sink. This could cause the IPM package to crack or the leads to bend.

7.3 Recommended storage conditions

Temperature: 5 ~ 35

Relative humidity: 45 ~ 75%

- Avoid leaving the IM231-x6 exposed to moisture or direct sunlight. Be careful during periods of rain or snow.
- Use storage areas where there is minimal temperature fluctuation.
- Rapid temperature changes can cause moisture condensation on the stored IM231-x6, resulting in lead oxidation or corrosion and degraded solderability.
- Do not allow the IM231-x6 to be exposed to corrosive gasses or dusty conditions.
- Do not allow excessive external forces or loads to be applied to the IM231-x6 while they are in storage.

8 References

[1] D. Chung, S. Sul, "Minimum-Loss Strategy for three-Phase PWM Rectifier", IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June 1999

[2]Aavid Thermalloy, https://web.archive.org/web/20100917053159/http://aavidthermalloy.com/technical/correct.shtml

[3] S. Lee, "How to select a heat sink", Electronics Coolings, Vol.1, No.1, June 1995

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