

# EZ-PD™ PAG2-PD highly-integrated Power Delivery controller for power adapter

## General description

EZ-PD™ PAG2-PD CYPAS2174 is an integrated secondary-side controller which supports USB Power Delivery extended power range (EPR) mode. EZ-PD™ PAG2-PD is targeted towards USB-C power adapters, it fits well into high-efficiency AC-DC flyback designs with USB Power Delivery, Qualcomm Quick Charge, and other standard charging protocols. EZ-PD™ PAG2-PD also supports USB PD extended power range (EPR) mode.

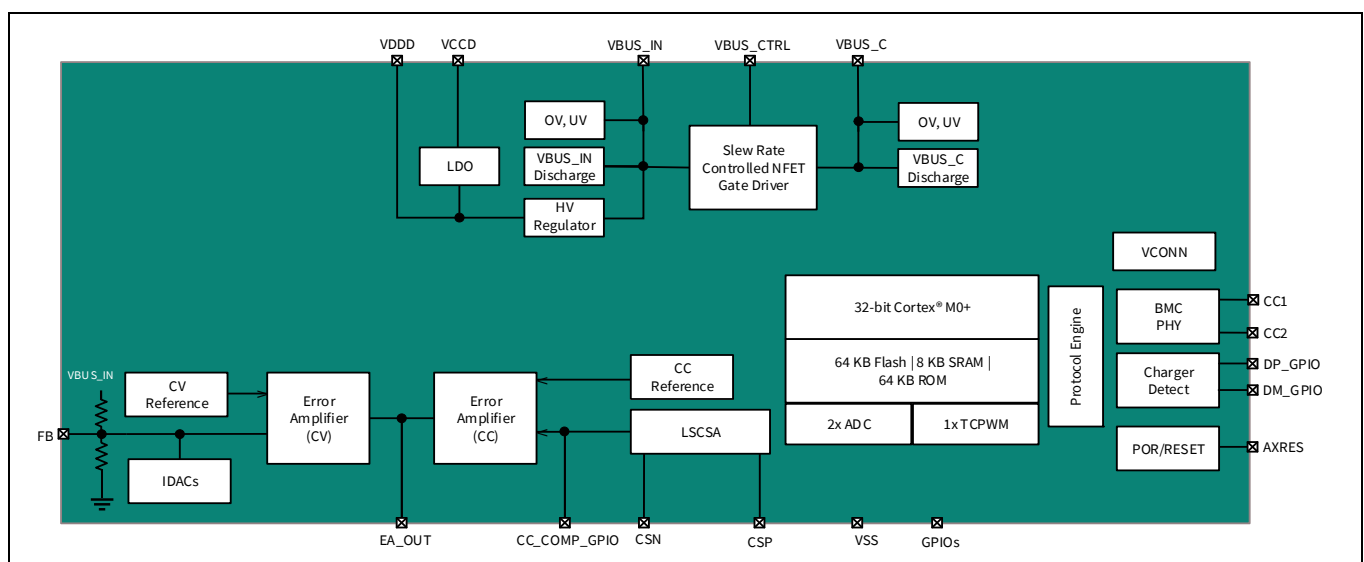
## Applications

- USB-C chargers and adapters
- USB-C chargers and adapters with EPR
- Power adapters supporting both USB PD and legacy charging
- 28 V EPR chargers and adapters, wall sockets

## Features

- USB PD 3.1-compliant with extended power range (EPR) support of up to 28 V VBUS
- Supports USB PD 2.0, PD 3.0 with programmable power supply (PPS), QC5.0, QC4+, QC 4.0, QC 3.0, QC 2.0, Samsung AFC, Apple Charging, and Battery Charging (BC) V1.2 charging protocols
- Integrates low-side current sense amplifier (LSCSA), 2x VBUS discharge FETs, and an NFET gate driver to drive the load switch and VCONN FETs to support EMCA cables
- Configurable VBUS overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), short-circuit protection (SCP), and system overtemperature protection (OTP)
- Protects against accidental VBUS to CC short; electrostatic discharge (ESD) protection on CC, VBUS, DP/DM lines, and overvoltage on DP/DM lines
- Integrates a 32-bit Cortex® M0+ with 64 KB flash, 8 KB SRAM, and 64 KB ROM
- 32-lead QFN packages with -40°C to +150°C junction temperature range

## Functional block diagram

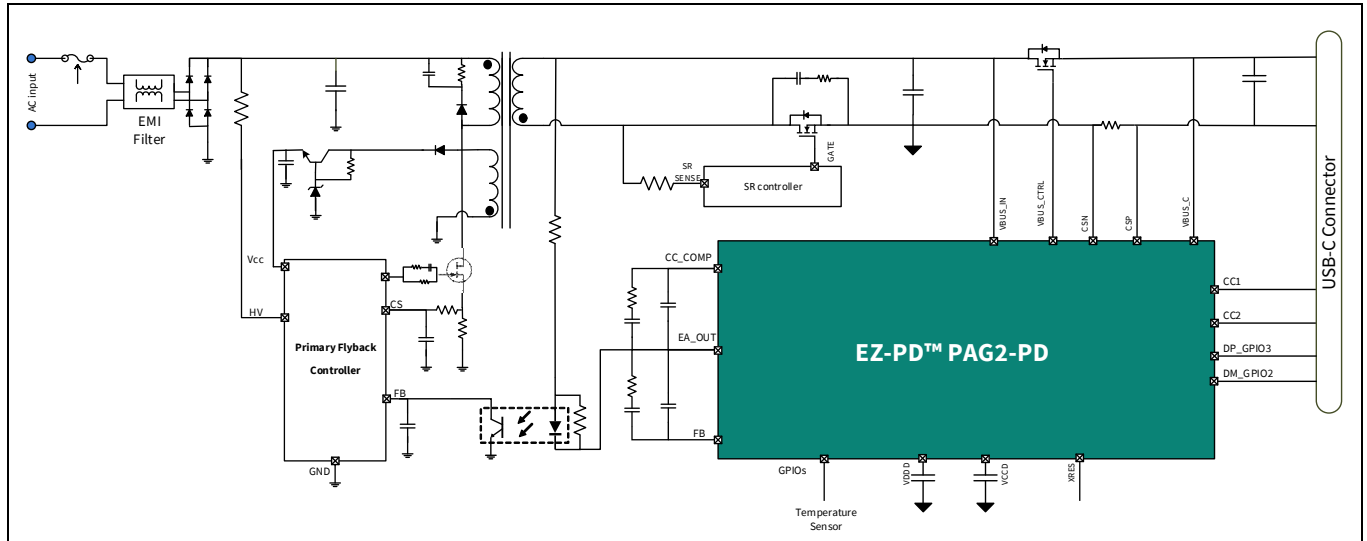


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## 1 Application overview

**Figure 1** shows a power adapter application diagram implementing a primary side-controlled synchronous flyback system. In this system, EZ-PD™ PAG2-PD engages the internal error amplifier (EA) to take the feedback from the secondary side and pass it on to the primary controller over an isolation barrier like an optocoupler. The primary side controller can be any standard flyback controller. In this topology, EZ-PD™ PAG2-PD integrates two key features: charging protocol control, and fault protection.



**Figure 1** USB PD adapter with primary side flyback control

Pinouts

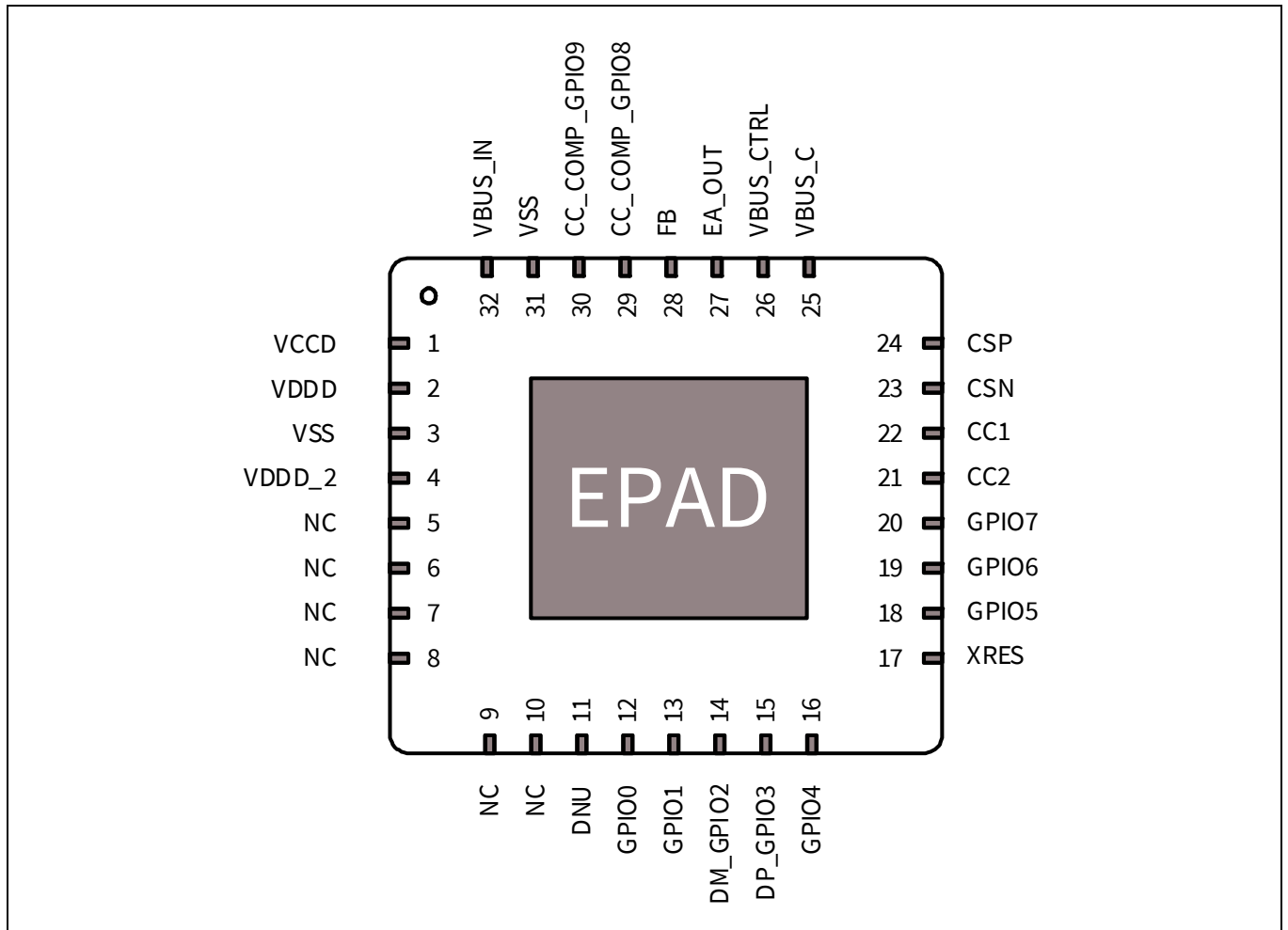
## 2 Pinouts

### 2.1 Pin definitions

**Table 1 32-lead QFN pin description**

Pin number	Pin name	Pin description
1	VCCD	1.8 V core voltage LDO output
2	VDDD	3.0 V to 5.5 V internal LDO output
3	VSS	Ground
4	VDDD_2	Short to pin#2
5	DNU	Do Not Use, keep floating
6	DNU	Do Not Use, keep floating
7	VDDD_VSS	Ground
8	DNU	Do Not Use, keep floating
9	DNU	Do Not Use, keep floating
10	DNU	Do Not Use, keep floating
11	DNU	Do Not Use, keep floating
12	GPIO0	GPIO
13	GPIO1	
14	DM_GPIO2	USB D-/GPIO/SWD_DAT
15	DP_GPIO3	USB D+/GPIO/SWD_CLK
16	GPIO4	Not connected
17	XRES	External reset input
18	GPIO5	GPIO
19	GPIO6	GPIO/TCPWM
20	GPIO7	GPIO
21	CC2	Power Delivery communication channel 2
22	CC1	Power Delivery communication channel 1
23	CSN	Low-side current sense amplifier negative input
24	CSP	Low-side current sense amplifier positive input
25	VBUS_C	USB Type-C VBUS monitor input
26	VBUS_CTRL	Load switch NFET gate control
27	EA_OUT	Error amplifier output
28	FB	Error amplifier feedback
29	CC_COMP_GPIO8	Pin for constant current mode compensation capacitor/GPIO/TCPWM
30	CC_COMP_GPIO9	
31	VSS	Ground
32	VBUS_IN	3.3 V to 30 V power source input for regulator

Pinouts



**Figure 2 32-lead QFN pin map**

## 2.2 Pin description

### 2.2.1 FB, EA\_OUT, CC\_COMP\_GPIOx

EZ-PD™ PAG2-PD integrates two error amplifier blocks that handle secondary output sensing and feedback for both constant voltage and constant current modes of operation. The error amplifier output can be used to regulate the current drawn through the external optocoupler. The negative input of the error amplifier is the feedback (FB) pin and the positive input is an internal voltage reference. Based on the desired VBUS output, the voltage at the FB pin will be varied using internal current source/sink IDACs. An external compensation network is required between the FB pin and EA\_OUT pin, as shown in the application diagram (see [Figure 1](#)). The constant current operation makes use of an internal low-side current sense amplifier (LSCSA), the output of which feeds into an independent error amplifier as shown in the functional block diagram. Constant current mode regulation requires an external compensation network between CC\_COMP\_GPIOx and EA\_OUT as shown in [Figure 1](#).

PAG2-PD error amplifier can ensure constant voltage regulation from 3.3 V to 28 V range and constant current regulation from 1 A to 5 A as required by the USB PD PPS EPR specification.

### 2.2.2 FB, EA\_OUT, CC\_COMP\_GPIOx

PAG2-PD integrates two error amplifier blocks that handle secondary output sensing and feedback for both constant voltage and constant current modes of operation. The error amplifier output can be used to regulate the current drawn through the external optocoupler. The negative input of the error amplifier is the feedback (FB) pin and the positive input is an internal voltage reference. Based on the desired VBUS output, the voltage at the FB pin will be varied using internal current source/sink IDACs. An external compensation network is required between the FB pin and EA\_OUT pin, as shown in the application diagram (see [Figure 1](#)). The constant current operation makes use of an internal low-side current sense amplifier (LSCSA), the output of which feeds into an independent error amplifier as shown in the functional block diagram. Constant current mode regulation requires an external compensation network between CC\_COMP\_GPIOx and EA\_OUT as shown in [Figure 1](#). EZ-PD™ PAG2-PD error amplifier can ensure constant voltage regulation from 3.3 V to 28 V range and constant current regulation from 1 A to 5 A as required by the USB PD PPS EPR specification.

### 2.2.3 VBUS\_IN, VDDD, VCCD

PAG2-PD integrates a high-voltage regulator, which is powered from the VBUS\_IN rail, the output of the regulator powers the VDDD rail. The input to the regulator can range from 3.3 V minimum to 30 V maximum. This regulator is intended to deliver PAG2-PD current consumption and is not expected to drive any external loads or ICs. PAG2-PD also has an internal configurable discharge path for the VBUS\_IN rail, which is used to discharge the VBUS rail during negative voltage transitions. The discharge resistor strength is configurable through firmware settings.

The regulated supply VDDD is either used to directly power some internal analog blocks or further regulated down to 1.8 V VCCD, which powers the majority of the core. VDDD and VCCD are brought out onto pins to connect external capacitors for regulator stability and these are not meant to be used as power supplies.

### 2.2.4 VBUS\_C, VBUS\_CTRL

VBUS\_C is used to monitor the voltage at the Type-C connector. VBUS\_C has an internal configurable discharge path, which is used to discharge the VBUS\_C rail during negative voltage transitions. The discharge resistor strength is configurable through firmware settings. The load switch is between VBUS\_IN and VBUS\_C. PAG2-PD integrates an NFET gate driver to control this load switch. VBUS\_CTRL is the output of this gate driver. There is an optional slow turn-on feature which is meant to avoid the sudden in-rush current.

### 2.2.5 CSP, CSN

PAG2-PD integrates a low-side current sense amplifier (LSCSA) to monitor the load current. CSP is the positive input pin for the LSCSA and CSN is the negative input. Suggested Rsense for LSCSA is 5 mΩ.

## 2.2.6 CC1, CC2

CC1 and CC2 are the communication channels for the USB PD protocol. EZ-PD™ PAG2-PD integrates a USB PD transceiver consisting of a transmitter (TX) and receiver (RX) that communicate Biphase Mark Code (BMC) encoded data over the Configuration Channel (CC) channels as per the USB PD standard. All communication is half-duplex. The physical layer implements collision avoidance to minimize communication errors on the channel. This block includes all termination resistors ( $R_p$ ) and their switches as required by the USB PD specification.

To support active cable applications, PAG2-PD also integrates VCONN FETs to power CC lines. An external 390-pF capacitor is required on both the CC1 and CC2 pins.

## 2.2.7 DP\_GPIOx, DM\_GPIOx

The DP and DM lines are the standard USB D+ and D- lines. PAG2-PD integrates a charge detect block, which handles legacy charging protocols such as BC 1.2, Quick Charge, Apple Charging, and Samsung AFC. This block integrates all the terminations required for these charging protocols and no external components are required. When legacy charging is not required in the system, the same DP and DM lines can be re-used as standard GPIOs. Charger detect block also supports impedance detection on DP/DM lines.

## 2.2.8 GPIOx, XRES

PAG2-PD has multiple GPIOs, out of which some are dedicated GPIOs and the rest are multiplexed with other functionalities. These GPIOs support multiple drive modes and configurable threshold options. During power-on and reset, the GPIOs are forced to the tristate so as not to crowbar any inputs and/or cause excess turn on current.

The XRES pin can be used to initiate a reset, this pin is internally pulled high and needs to be pulled low externally to trigger a reset.

## 3 Functional description

### 3.1 Fault protection

#### 3.1.1 VBUS OVP, UVP, OCP, and SCP

VBUS undervoltage and overvoltage faults are monitored using internal VBUS\_IN/VBUS\_C resistor dividers. VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. The fault thresholds and response mechanisms are firmware configurable.

#### 3.1.2 OTP

The overtemperature monitoring is done using an external thermistor and internal ADC. The thermistor can be connected to any free GPIO. EZ-PD™ PAG2-PD highly-integrated Power Delivery controller for power adapter has integrated 8-bit SAR ADC, this is available for general purpose analog to digital conversions. The fault thresholds and response mechanisms are firmware configurable.

#### 3.1.3 ESD, CC OVP, and DP/DM OVP

PAG2-PD offers ESD protection on all the pins. Further, the chip integrates protection against accidental short of CC pins to high voltage VBUS\_C rail and also protects against over-voltage on DP/DM pins.

### 3.2 Power modes

PAG2-PD supports multiple power modes - Active, Sleep, and Deep Sleep. Transitions between these modes is handled by the application firmware depending on the operating conditions.

### 3.3 MCU subsystem

PAG2-PD integrates a 32-bit Cortex®-M0+ MCU with 64 KB flash, 8 KB SRAM, and 64 KB ROM. PAG2-PD also supports 1x TCPWM and 2x ADC.



## 4 Electrical specifications

### 4.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings**

Parameter	Description	Min	Typ	Max	Unit
V <sub>BUS_IN_MAX</sub>	Maximum input supply voltage	-0.3	-	34	V
V <sub>DDD_MAX</sub>	V <sub>DDD</sub> supply voltage	-		6	-
V <sub>CC_PIN_ABS</sub>	Voltage on CC1, CC2 pins	-		34	-
V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5		V <sub>DDD</sub> + 0.5	-
I <sub>GPIO_ABS</sub>	Current per GPIO	-		25	mA
I <sub>LU</sub>	Pin current for latch-up	-100		100	
ESD_HBM	Electrostatic discharge human body model	-		2000	V
ESD_CDM	Electrostatic discharge charged device model	-		500	

### 4.2 Device-level specifications

**Table 3 Device-level specifications**

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>Memory size</b>						
FLASH_SIZE	Flash memory size	-	64	-	KB	SONOS flash amount (bytes)
SRAM_SIZE	SRAM memory size		8			SRAM amount (bytes)
SROM_SIZE	SROM memory size		64			
<b>Silicon power</b>						
V <sub>DDD_REG</sub>	V <sub>DDD</sub> output with V <sub>BUS</sub> 5.5 V to 30 V	4.6	5	5.4	V	-
V <sub>DDD_MIN</sub>	V <sub>DDD</sub> output with V <sub>BUS</sub> 3.15 V to 5.5 V	V <sub>BUS</sub> - 0.33	-	-		
V <sub>BUS_IN</sub>	Power supply input voltage	3.15	-	30.0		
V <sub>CCD</sub>	Output voltage for core logic	-	1.8	-		
V <sub>DDWRITE</sub>	Supply voltage for flash write	3	-	5.5		
C <sub>efc</sub>	External regulator voltage bypass for V <sub>CCD</sub>	80	100	120	nF	X5R ceramic or better
C <sub>exc</sub>	Power supply capacitor for V <sub>DDD</sub>	4	4.7	-	μF	-
C <sub>exv</sub>	Power supply decoupling capacitor for V <sub>BUS_IN</sub>	-	1	-		
I <sub>gpio_abs</sub>	Current per GPIO	-	-	25	mA	Absolute maximum
T <sub>sleep</sub>	Wakeup from Sleep mode	-	0	-	μs	-

## Electrical specifications

**Table 3** Device-level specifications (continued)

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Tdeepsleep	Wakeup from Deep Sleep mode	-	35	-	mA	-
IDD_A	Active current from VBUS_IN (Type-C Attached)		25.0			VBUS_IN = 11 V, TA = 25°C, CC1/CC2 in TX or RX, CPU at 24 MHz, EA/ADC/CSA/UVOV blocks ON
IDD_A4	Current from VBUS_IN (Type-C attached)		3			VBUS_IN = 28 V, TA = 25°C, Deep Sleep, No toggling on CC
IDD_DS2_UA	Deep Sleep current from VBUS_IN (Type-C unattached)		400		μA	VBUS_in = 5 V, TA = 25°C, Type-C unattached, DFP mode
L_SEC	Secondary side inductor	3	-		μH	Secondary side inductor

### 4.3 Functional block specifications

**Table 4 Functional block specifications**

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>GPIO</b>						
I_LU	Latch up current limits	-100	-	100	mA	
RPU	Pull-up resistor value	3.5	5.6	8.5	kΩ	-
RPD	Pull-down resistor value					
IIL	Input leakage current (Absolute value)	-	-	2	nA	+25°C TA, 3 V VDDD
CPIN_A	Max pin capacitance			22	pF	Capacitance on DP, DM pins
CPIN	Max pin capacitance			3		
Voh	Output voltage high level	VDDD - 0.6	-	-	V	Ioh = -4 mA
Vol	Output voltage low level	-		0.6		Iol = 10 mA
Vih_CMOS	Input voltage high threshold	0.7 × VDDD		-		
Vil_CMOS	Input voltage low threshold	-		0.3 × VDDD		
Vih_TTL	LVTTL input	2		-		
Vil_TTL	LVTTL input	-		0.8		
Vhysttl	Input hysteresis LVTTL	80	-	-	mV	-
Vhyscmos	Input hysteresis CMOS	0.1 × VDDD	-			
IDIODE	Current through protection diode to VDDD/VSS	-	-	100	μA	
TriseF	Rise time in Fast Strong mode	1	-	15	ns	Load = 25 pF
TfallF	Fall time in Fast Strong mode			15		
TriseS	Rise time in Slow Strong mode	10	-	70		-
TfallS	Fall time in Slow Strong mode					
FGPIO_OUT1	GPIO Fout; 2.85 V ≤ VDDD ≤ 5.5 V. Fast Strong mode.	-	-	28	MHz	-
FGPIO_OUT2	GPIO Fout; 2.85 V ≤ VDDD ≤ 5.5 V. Slow Strong mode.			6		
FGPIO_IN	GPIO input operating frequency; 2.85 V ≤ VDDD ≤ 5.5 V			28		

## Electrical specifications

**Table 4** Functional block specifications (continued)

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>Flash macro</b>						
FLASH_ERASE	Row erase time			15.5	ms	-
FLASH_WRITE	Row (Block) write time (Erase and program)	-		20		
FLASH_DR	Flash data retention	15		-	Years	25°C to 55°C, all VDDD
FLASH_ENPB	Flash write endurance	100K			Cycles	25°C to 85°C, all VDDD
FLASH_ENPB1	Flash write endurance	10K				25°C to 125°C, all VDDD
FLASH_ROW_PGM	Row program time after erase	-		7	ms	
TBULKERASE	Bulk erase time (32 KB)	-	-	35		
TDEVPROG	Total device program time	-		7.5	s	
FRET1	Flash retention, TA ≤ 55°C, 100K P/E cycles	15		-	Years	-
FRET2	Flash retention, TA ≤ 85°C, 10K P/E cycles	10				
FRET3	Flash retention, TA ≤ 105°C, 10K P/E cycles	3				
<b>SWD</b>						
F_swddclk1	All VDDD	-		14	MHz	
T_swddi_setup	T = 1/f SWDCLK	0.25 × T	-	-	ns	-
T_swddi_hold				-		
T_swddo_valid				0.50 × T		
T_swddo_hold				-		
<b>ILO / IMO / POR</b>						
FIMO	IMO frequency	24	36	48	MHz	-
IMO_STL	IMO settling time when trim register is changed	-	-	200	ns	25°C TA, All VDDD, 48 MHz ≥ FIMO ≥ 24 MHz
FCPU	CPU input frequency			48	MHz	-
FILO	ILO frequency	15	40	80	kHz	
Fimotol	Frequency variation at 24 and 48 MHz (trimmed)	-2		2	%	
TSTARTIMO	IMO start-up time			7	μs	
TSTARTILO1	ILO start-up time	-		2	ms	
EXTCLKFREQ	External clock input frequency			16	MHz	
EXTCLKDUTY	Duty cycle	45		55	%	
TCLKSWITCH	System clock source	3	-	4	Period s	-
VRISEIPOR	Power-on reset (POR)	0.72		1.5	V	
VFALLIPOR	Power-on reset (POR) falling trip voltage	0.62		1.4		
VDDD_BOD	Brownout detect (BOD) trip voltage Active/ Sleep modes	2.34		3		
VCCD_BOD		1.64		2		
VCCD_BOD_DPSLP		1.1		2		

## Electrical specifications

**Table 4** Functional block specifications (continued)

Parameter	Description	Min	Typ	Max	Unit	Details/conditions			
<b>Timer</b>									
SYS_TIM_RES	Sys timer resolution	-	16	-	bits	-			
WDT_RES	Watchdog timer resolution		16		bits				
<b>TCPWM</b>									
TCPWMFREQ	Operating frequency	-	-	Fc	MHz	Fc max = CLK_SYS			
TPWMEXT	Output trigger pulse widths	2/Fc		-	-	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs		
TCRES	Resolution of counter	1/Fc							Minimum time between successive counts
PWMRES	PWM resolution								Minimum pulse width of PWM output
<b>PD transceiver</b>									
vSwing	Transmitter output high voltage	1.05	-	1.2	V	-			
vSwing_low	Transmitter output low voltage	-		0.075					
zDriver	Transmitter output impedance	33		75	Ω				
Idac_std	Source current for USB standard advertisement	64	-	96	μA	-			
Idac_1p5a	Source current for 1.5 A @ 5 V advertisement	166		194					
Idac_3a	Source current for 3 A @ 5 V advertisement	304		356					
zOPEN	CC impedance to ground when disabled	108		-	kΩ				
DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15	-	0.25	V	-			
DFP_1.5A_0p4	CC voltages on DFP side - 1.5 A	0.35		0.5					
DFP_3A_0p8	CC voltages on DFP side - 3 A	0.75		0.85					
DFP_3A_2p6	CC voltages on DFP side - 3 A	2		2.75					
Vattach_ds	Deep Sleep attach threshold	0.30		0.6	-				
Rattach_ds	Deep Sleep pull-up resistor	10		50	kΩ				

## Electrical specifications

**Table 4 Functional block specifications** (continued)

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>LS-CSA DC specifications</b>						
Csa_Acc1	CSA accuracy with 5 mV < Vsense < 10 mV	-0.75	-	0.75	mV	-
Csa_Acc2	CSA accuracy with 10 mV < Vsense < 15 mV					
Csa_Acc3	CSA accuracy with 15 mV < Vsense < 25 mV					
Csa_Acc4	CSA accuracy with Vsense = 50 mV					
SCP_6A	Short circuit current detect @ 6 A	5.4	6	6.6	A	
SCP_10A	Short circuit current detect @ 10 A	9	10	11		
SCP_20A	Short circuit current detect @ 20 A	18	20	22		
OCP Threshold	OCP Trip with 5 mΩ and current > 4 A	117	130	143	%	
Av	Nominal gain values supported: 40, 60	30	-	60	V/V	
<b>LS-CSA AC specifications</b>						
Tscp_gate	Delay from SCP threshold trip to external NFET power gate turn off	-	2.5	-	μs	1nF NFET gate capacitance, VBUS_IN = 28 V
Tscp_gate_1			7.5			3nF NFET gate capacitance, VBUS_IN = 28 V
<b>UVOV</b>						
VTHOV	Overvoltage threshold accuracy, 4 V to 30 V	-3	-	3	%	-
VTHUV1	Undervoltage threshold accuracy, 3 V to 4 V	-4		4		
VTHUV2	Undervoltage threshold accuracy, 4 V to 30 V	-3		3		
<b>VBUS gate driver DC specs</b>						
GD_VGS	Gate to source overdrive during ON condition	5	-	10	V	NFET driver is on
GD_Rpd	Resistance when pull-down enabled	-		2	KΩ	Applicable on VBUS_CTRL to turn off external NFET
GD_drv	Programmable typical gate current	0.3		9.75	μA	Gate driver output current
<b>VBUS gate driver AC specs</b>						
Ton	VBUS_ctrl LOW to HIGH (1 V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	VBUS_in = 5 V
Toff	VBUS_ctrl HIGH to LOW (90% to 10%) with 3 nF external capacitance	-	7.5	-	μs	VBUS_in = 28 V

## Electrical specifications

**Table 4** Functional block specifications (continued)

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>VBUS discharge</b>						
R1	NMOS on resistance for DS = 1 on VBUS_IN	1000		4000		Measured at 0.5 V
R2	NMOS on resistance for DS = 2 on VBUS_IN	500		2000		
R4	NMOS ON resistance for DS = 4 on VBUS_IN	250		1000	Ω	
R8	NMOS ON resistance for DS = 8 on VBUS_IN	125		500		
R16	NMOS ON resistance for DS = 16 on VBUS_IN	62.5		250		
R32	NMOS ON resistance for DS = 32 on VBUS_IN	31.25		150		
Vbus_stop_error	Error percentage of final VBUS value from setting	–		10	%	When VBUS is discharged to 5 V
R1A	NMOS on resistance for DS = 1 on VBUS_C	1000	–	2000	Ω	Measured at 0.5 V
R127A	NMOS ON resistance for DS = 127 on VBUS_C	6.5		38		
<b>Voltage regulation DC specifications</b>						
VOUT	Typical VBUS_IN output voltage range	3.3	–	28	V	–
VR	VBUS voltage regulation accuracy		±3	±5	%	
Ika_off	Off-state cathode current	–	2.2	10	μA	
Ika_on	Current through EA_OUT pin when in sink mode for optocoupler application		–	5	mA	
<b>VBUS regulator specifications</b>						
VOLTAGE_DETECT	Voltage detect threshold voltage on VBUS_IN	1.65	2.1	2.4	V	–
Tstart	Total startup time for the regulator supply outputs with 4.7 μF load capacitance	–	50	200	μs	
<b>ADC DC specifications</b>						
Resolution	ADC resolution	–	8	–	bits	–
INL	Integral non-linearity	–2.5		2.5	LSB	Reference voltage generated from VDDD
INL	Integral non-linearity	–1.5	–	1.5		Reference voltage generated from bandgap
VREF_ADC1	Reference voltage of ADC	VDDD min		VDDD max	V	Reference voltage generated from VDDD
VREF_ADC2		1.96	2	2.04		Reference voltage generated from bandgap

## Electrical specifications

**Table 4** Functional block specifications (continued)

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
<b>VCONN switch specifications</b>						
VCONN_OUT	VCONN minimum output voltage with 20 mA load current with VBUS = 5 V to 30 V	4.5	-	-	V	-
Ileak	Connector side pin leakage current	-	-	10	μA	-
<b>VCONN switch AC specifications</b>						
Ton	Switch turn on time	-	-	600	μs	-
Toff	Switch turn off time	-	-	10		



## 5 Ordering information

**Table 5 EZ-PD™ PAG2-PD ordering information**

Product	Application	Package type	Si ID	Si rev
CYPAS2174A1-32LQXQ	USB PD adapter - Primary side flyback control	32-lead QFN	0x3B20	A1
CYPAS2174A1-32LQXQT				

### 5.1 Ordering code definitions

CY	PA	S	X	XX	XX	-	XX	XX	X	X	XX	X
												T = Tape and reel
												ES (optional field) = Pre-production engineering samples only. Non orderable.
												Temperature range: Q = Extended industrial (-40°C to +105°C)
												X = Pb-free
												Package type: LQ = QFN; S = SOIC
												Number of pins in the package
												Si Rev
												Application and feature combination designation
												Product type: 2 = Second-generation product family
												Product type: S = Secondary side controller
												Marketing code: PA = Power adapter
												Company ID: CY = CYPRESS (an Infineon company)

Packaging

## 6 Packaging

**Table 6 Package characteristics**

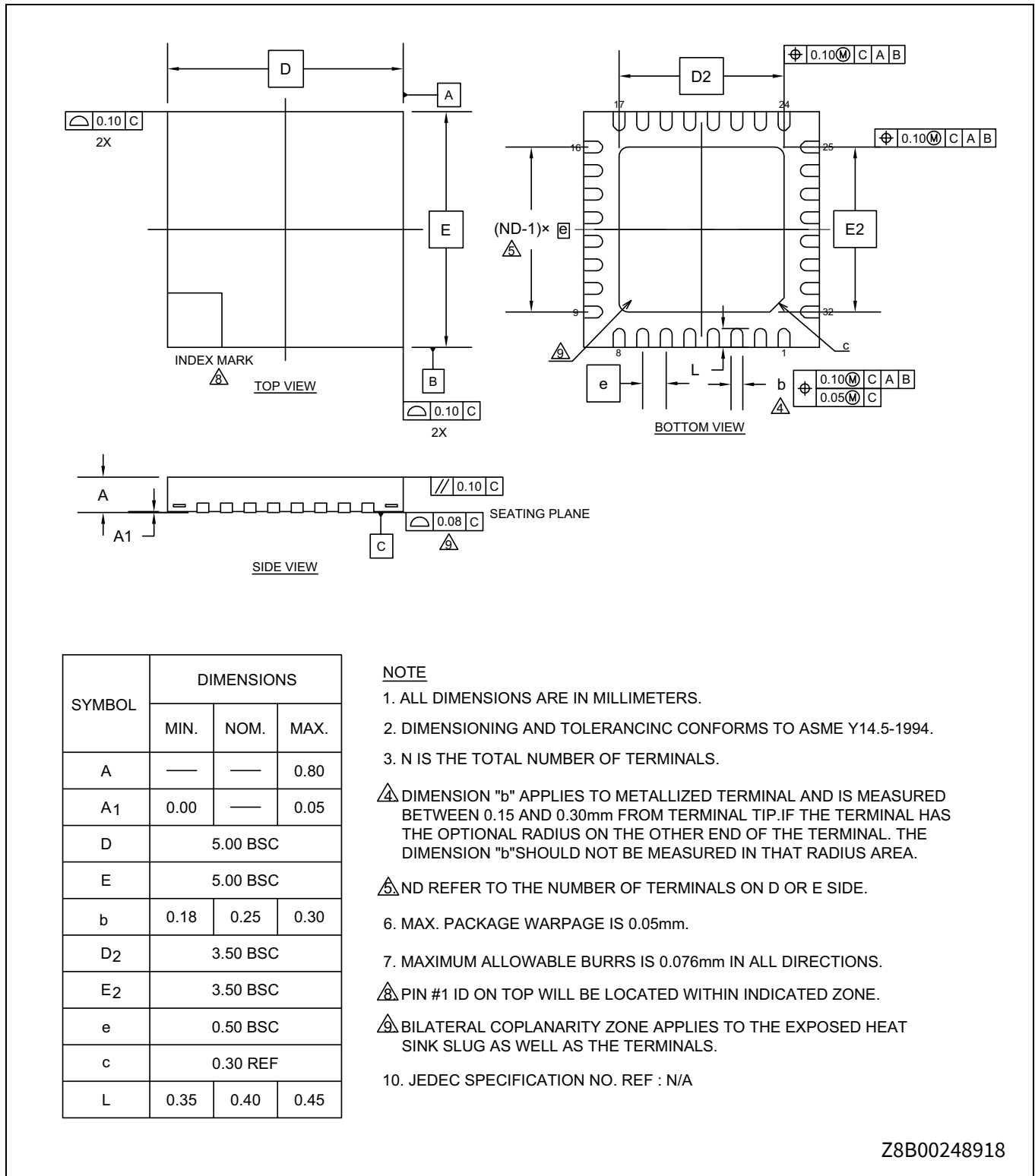
Parameter	Description	Conditions	Min	Typ	Max	Unit
T <sub>A</sub>	Operating ambient temperature	Extended industrial	-40	-	105	°C
T <sub>J</sub>	Operating junction temperature				150	
T <sub>JA</sub>	Package Theta-JA for 32-lead	-	-	23.4	-	°C/W
T <sub>JB</sub>	Package Theta-JB for 32-lead			4.85		
T <sub>JC</sub>	Package Theta-JC for 32-lead			27.2		

**Table 7 Solder reflow peak temperature**

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
32-lead QFN	260°C	30 s

**Table 8 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
32-lead QFN	MSL3



**Figure 3** 32-lead QFN (5.0 × 5.0 × 0.8 mm) WNP032 3.5 × 3.5 mm E-pad (SAWN) package outline (PG-VQFN-32)

## 7 Acronyms

**Table 9 Acronyms used in this document**

<b>Acronym</b>	<b>Description</b>
ACF	active clamp flyback
ADC	analog-to-digital converter
Arm®	advanced RISC machine, a CPU architecture
BOD	brownout detect
BMC	biphase mark code
CC	constant current
CCM	continuous conduction mode
CPU	central processing unit
CrCM	critical conduction mode
CS	current sense
CSN	current sense negative
CSP	current sense positive
DCM	discontinuous conduction mode
DFP	downstream facing port
DP	data plus
DM	data minus
EA	error amplifier
EMI	electromagnetic interference
EPR	extended power range
ESD	electrostatic discharge
FB	feedback
FS	full-speed
GPIO	general-purpose input/output
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LSCSA	low-side current sense amplifier
LVTTL	low-voltage transistor-transistor logic
NMOS	N-type metal-oxide-semiconductor
OCP	overcurrent protection
OVP	overvoltage protection
PD	Power Delivery
PHY	physical layer
POR	power-on reset
PPS	programmable power supply
PWM	pulse-width modulator
QR	quasi-resonant

## Acronyms

**Table 9** Acronyms used in this document (continued)

Acronym	Description
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RX	receive
SAR	successive approximation register
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
USB	Universal Serial Bus
WDT	watchdog timer
XRES	external reset I/O pin
ZCD	zero crossing defect
ZVS	zero voltage switching

## 8 Document conventions

### 8.1 Units of measure

**Table 10** Units of measure

Symbol	Unit of measure
°C	degrees celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

## Revision history

Document revision	Date	Description of changes
**	2024-04-10	Initial release.
*A	2024-06-25	Updated <b>“General description”</b> on page 1. Updated <b>“Applications”</b> on page 1. Added CYPAS2174A1-32LQXQT in <b>“Ordering information”</b> on page 17. The package diagram Spec#: 002-15160 is obsolete. Replaced the Spec# with Z8B00248918 (mentioned in the <b>ECN # 8022625</b> ).

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