

# AIROC™ Bluetooth® & Bluetooth® LE system on chip

## General description

The CYW20819 is a Bluetooth® 5.4 core spec compliant single-chip solution targeted for Internet of Things (IoT) applications. The CYW20819 is a highly integrated device which delivers up to 4.5 dBm transmit output power in LE mode, 5 dBm in BR mode and up to 0 dBm in EDR mode, allowing device makers to reduce product footprints and decrease overall system costs associated with implementing Bluetooth® solutions.

The CYW20819 integrates ultra low power (ULP) Bluetooth® LE along with the capability to add Bluetooth® classic functionality to enhance the user experience for fitness wearables and trackers. It also provides best-in-class receiver sensitivity for both Bluetooth® basic rate (BR) and enhanced data rate (EDR). Using advanced design techniques and process technology to reduce active and idle power, the CYW20819 addresses the needs of a diverse class of low power Bluetooth® enabled devices that require minimal power consumption and compact size. The device is intended for use in home automation, sensors (medical, home, security and industrial), lighting, Bluetooth® Mesh or any Bluetooth® connected IoT application. The datasheet provides details of the functional, operational, and electrical characteristics of the CYW20819 device. It is intended for hardware, design, application, and original equipment manufacturer (OEM) engineers.

## Features

- Bluetooth® subsystem
  - Complies with Bluetooth® core specification version 5.4
  - Includes support for BR, EDR 2 Mbps and 3 Mbps, eSCO, Bluetooth® LE, and LE 2 Mbps
  - Programmable TX power up to +5 dBm (BR)
  - Excellent receiver sensitivity (-95 dBm for Bluetooth® LE 1 Mbps)
- Microcontroller
  - Powerful Arm® Cortex®-M4 core with a maximum speed of 96 MHz
  - Bluetooth® stack in ROM allowing standalone operation without any external MCU
  - 256-KB on-chip flash
  - 176-KB on-chip RAM
  - Bluetooth® stack, peripheral drivers, security functions built into ROM (1 MB) allowing application to efficiently use on-chip flash
  - AES-128 and true random number generator (TRNG)
  - Security functions in ROM including ECDSA signature verification
  - Over-the-air (OTA) firmware updates
- Peripherals
  - Up to 22 GPIOs
  - I<sup>2</sup>C, I2S, UART, and PCM interfaces
  - Two Quad-SPI interfaces
  - Auxiliary ADC with up to 28 analog channels
  - Programmable key scan 20 × 8 matrix
  - Three-axis quadrature signal decoder
  - General-purpose timers and PWM
  - Real-time clock (RTC) and watchdog timers (WDT)

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## Applications

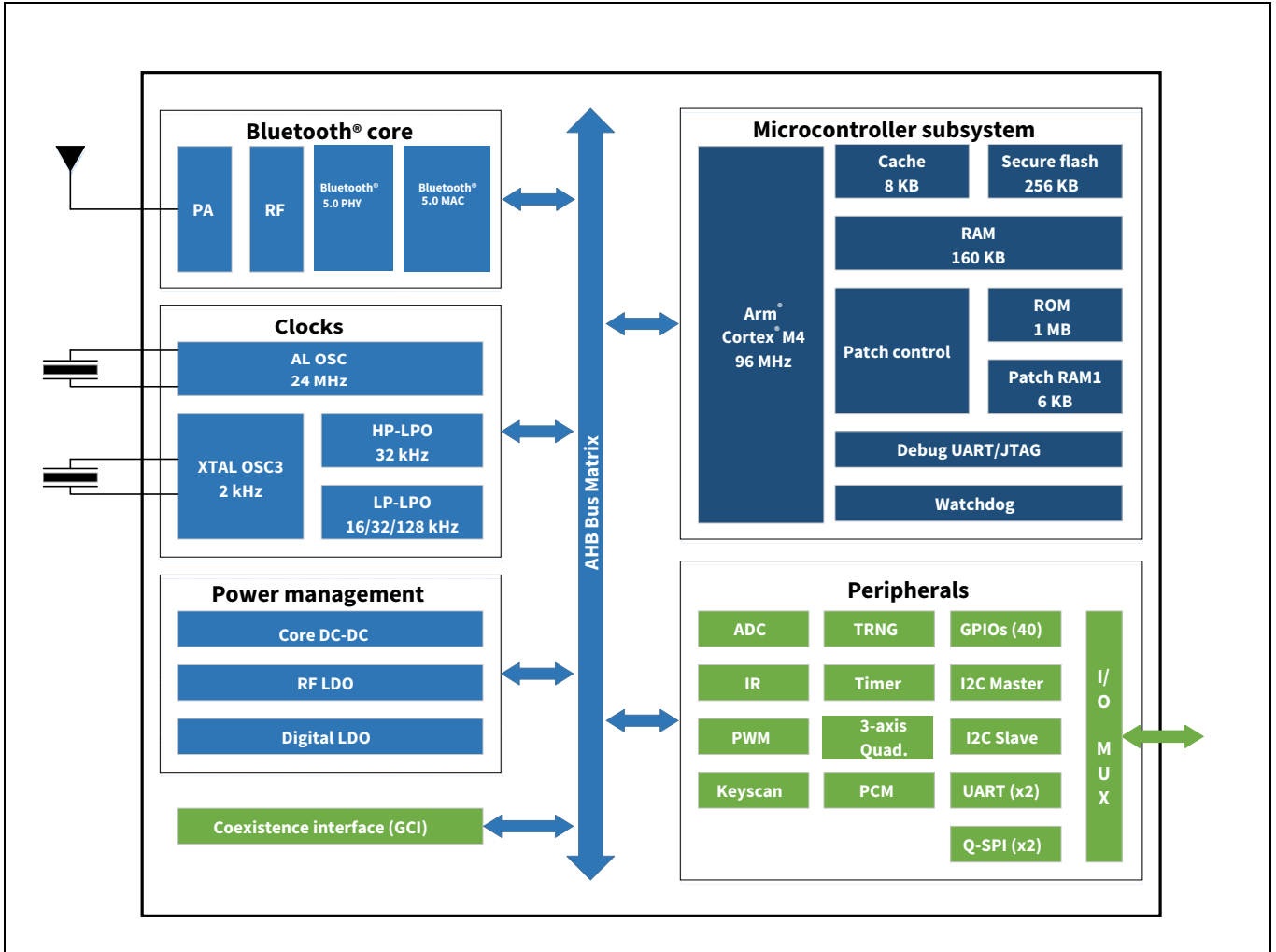
- Power management
  - On-chip power-on reset (POR)
  - Integrated buck (DC-DC) and LDO regulators
  - On-chip software controlled power management unit
  - On-chip 32 kHz LPO with optional external 32 kHz crystal oscillator support
- Wi-Fi coexistence
  - Global coexistence interface (GCI) for Infineon Wi-Fi parts
  - Serial enhanced coexistence interface (SECI)
  - Supported in ModusToolbox™
  - Package types
    - 62-pin FPBGA
    - RoHS compliant

## Applications

- Wearables and fitness bands
- Home automation
- Blood pressure monitors and other medical applications
- Proximity sensors
- Key fobs
- Thermostats and thermometers
- Toys
- Remotes

Functional block diagram

**Functional block diagram**



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Bluetooth® baseband core

## 1 Bluetooth® baseband core

The Bluetooth® baseband core (BBC) implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all ACL, SCO, eSCO, LE, and 2 Mbps LE connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening. **Table 1** lists key Bluetooth® features supported by the CYW20819.

**Table 1 Key Bluetooth® features supported by CYW20819**

<b>Bluetooth® features</b>		
<b>Bluetooth® 1.0</b>	<b>Bluetooth® 1.2</b>	<b>Bluetooth® 2.0</b>
Basic rate	Interlaced scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive frequency hopping	-
Paging and inquiry	eSCO	-
Page and inquiry scan	-	-
Sniff	-	-
<b>Bluetooth® 2.1</b>	<b>Bluetooth® 3.0</b>	<b>Bluetooth® 4.0</b>
Secure simple pairing	Unicast connectionless data	Bluetooth® Low Energy
Enhanced inquiry response	Enhanced power control	-
Sniff subrating	eSCO	-
<b>Bluetooth® 4.1</b>	<b>Bluetooth® 4.2</b>	<b>Bluetooth® 5.0</b>
Low duty cycle advertising	Data packet length extension	LE 2 Mbps
Dual mode	LE secure connection	Slot availability mask
LE link layer topology	Link layer privacy	High duty cycle advertising

### 1.1 BQB and regulatory testing support

The CYW20819 fully supports Bluetooth® test mode as described in Part I:1 of the specification of the Bluetooth® system v3.0. This includes the transmitter tests, normal and delayed loop back tests, and reduced hopping sequence.

In addition to the standard Bluetooth® test mode, the CYW20819 also supports enhanced testing features to simplify RF debugging and qualification. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

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Bluetooth® baseband core

## 1.2 Wi-Fi coexistence support

The CYW20819 includes support for:

- Global coexistence interface for use with Wi-Fi parts
- Serial enhanced coexistence interface (SECI) for use with SECI compatible Wi-Fi parts

## 2 Microprocessor unit

The CYW20819 includes a Cortex® M4 processor with 1 MB of program ROM, 176K RAM, and 256 KB of flash. The CM4 has a maximum speed of 96 MHz. The 256 KB of flash is supported by an 8 KB cache allowing direct code execution from flash at near maximum speed and low power consumption.

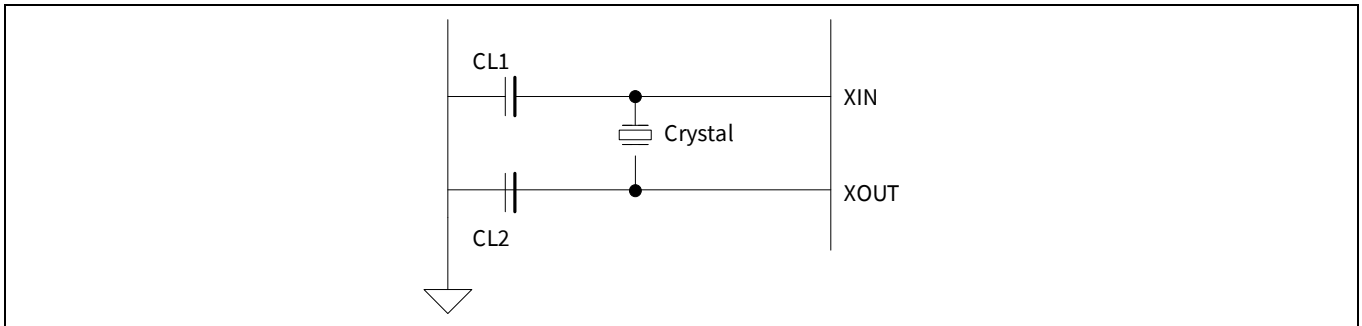
The CM4 runs all the Bluetooth® layers as well as application code. The ROM includes LMAC, HCI, L2CAP, GATT, as well as other stack layers freeing up most of the flash for application usage.

A standard serial wire debug (SWD) interface provides debugging support. Refer to the **“Firmware”** on page 22 section for details on the architecture and layers that are included in the ROM.

### 2.1 Main crystal oscillator

The CYW20819 uses a 24 MHz crystal oscillator (XTAL).

The XTAL must have an accuracy of  $\pm 20$  ppm as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see **Figure 1**).



**Figure 1 Recommended oscillator configuration**

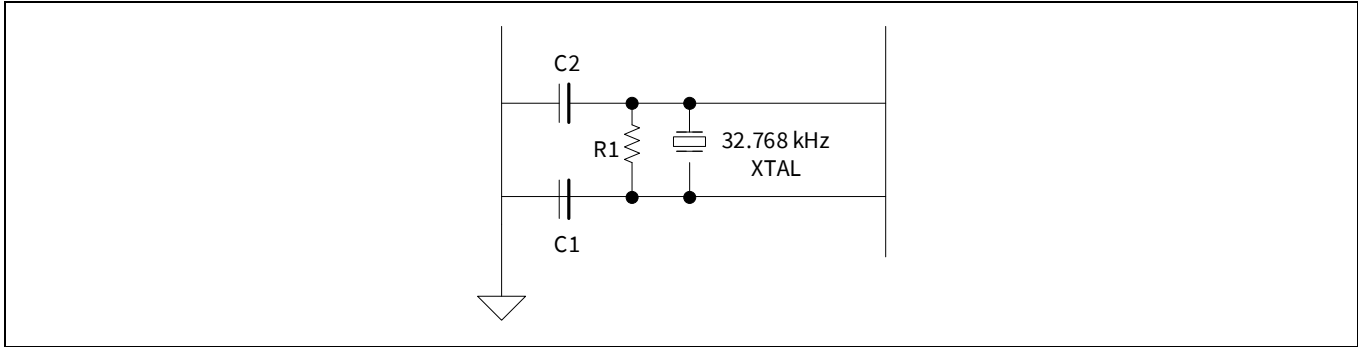
**Table 2 Reference crystal electrical specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	–	24.000	–	MHz
Oscillation mode	–	<b>Fundamental</b>			–
Frequency accuracy	Includes operating temperature range and aging	–	–	$\pm 20$	ppm
Equivalent series resistance	–	–	–	60	$\Omega$
Load capacitance	–	–	8	–	pF
Drive level	–	–	–	200	$\mu W$
Shunt capacitance	–	–	–	2	pF



## 2.2 32 kHz crystal oscillator

The CYW20819 includes a 32 kHz oscillator to provide accurate timing during low power operations. **Figure 2** shows the 32 kHz XTAL oscillator with external components and **Table 3** lists the oscillator’s characteristics. This oscillator can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The XTAL must have an accuracy of  $\pm 250$  ppm or better per the Bluetooth® spec over temperature and including aging. The default component values are: R1 = 10 M $\Omega$  and C1 = C2 = ~6 pF. The values of C1 and C2 are used to fine-tune the oscillator.



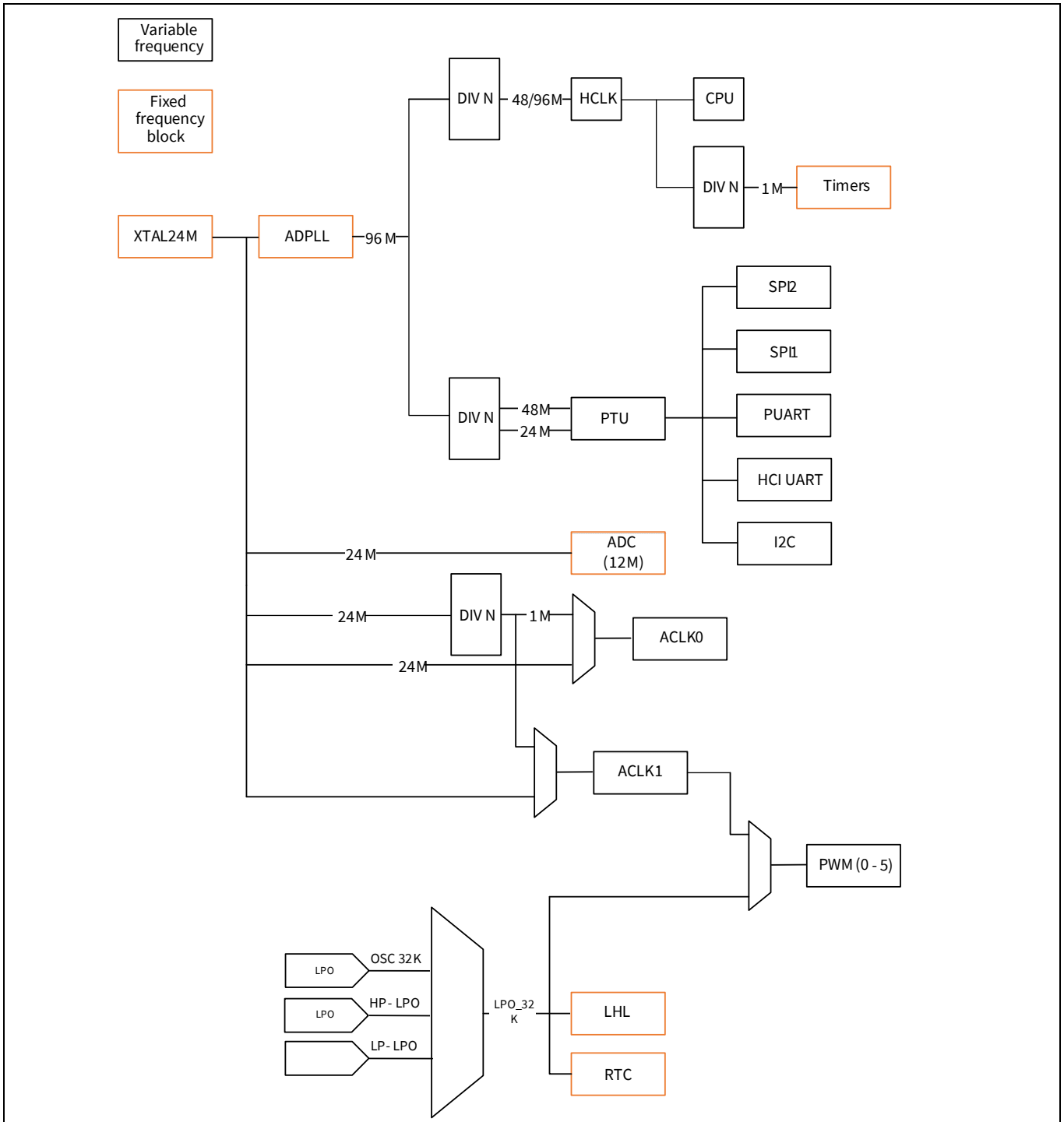
**Figure 2 32 kHz oscillator block diagram**

**Table 3 XTAL oscillator characteristics**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F <sub>oscout</sub>	–	–	32.768	–	kHz
Frequency tolerance	–	Over temperature and aging	–	–	250	ppm
XTAL drive level	P <sub>drv</sub>	For crystal selection	–	–	0.5	$\mu$ W
XTAL series resistance	R <sub>series</sub>	For crystal selection	–	–	70	k $\Omega$
XTAL shunt capacitance	C <sub>shunt</sub>	For crystal selection	–	–	2.2	pF

### 2.3 Low-frequency clock sources

The 32-kHz low-frequency clock (LPO\_32K on the following figure) can be obtained from multiple sources. There are two internal low-power oscillators (LPOs), called the LP-LPO and HP-LPO, as well as external crystal connections (OSC32K). The firmware determines the clock source to use among the available LPOs depending on the accuracy and power requirements. The preferred source is the external LPO (OSC32K) because it has good accuracy with the lowest current consumption. Internal LP-LPO has low current consumption and low accuracy whereas HP-LPO has higher accuracy and higher current consumption. The firmware assumes the external LPO has less than 250 PPM error with little or no jitter.



**Figure 3 Simplified clock source**

## 2.4 Power modes

The CYW20819 supports the following HW power modes:

- Active mode: Normal operating mode in which all peripherals are available and CPU is active
- Idle mode - CPU is paused: In this mode, the CPU is in “wait for interrupt” (WFI) and the HCLK, which is the high frequency clock derived from the main crystal oscillator, is running at a lower clock speed. Other clocks are active and the state of the entire chip is retained.
- Sleep mode: All systems clocks idle except for the LPO. The chip can wake up either after a programmed period of time has expired or if an external event is received via one of the GPIOs. In this mode, CPU is in WFI and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. State of the entire chip is retained, the internal LDOs run at a lower voltage (where the voltage is managed by the PMU), and SRAM is retained.
- PDS (power down sleep) mode: Radio powered down and digital core mostly powered down except for RAM, registers, and some core logic. CYW20819 can wake up either after a programmed period of time has expired or if an external event is received via one of the GPIOs.
- ePDS (extended PDS) mode: This is an extension of the PDS mode. In this mode, only the main RAM and ePDS control circuitry retains power. As in other modes, the CYW20819 can wake up either after a programmed period or upon receiving an external event.
- HID-OFF (deep sleep) mode: Core, radio, and regulators powered down. Only the LHL IO domain is powered. In this mode, the CYW20819 can be woken up either by an event on one of the GPIOs or after a certain amount of time has expired. After wakeup, the part will go through full FW initialization although it will retain enough information to determine that it came out of HID-OFF and the event that caused the wake up. LPO and RTC are turned OFF in this mode. Either an internal LPO or an external input would provide a measure of time.

Transition between power modes is handled by the on-chip firmware with host/application involvement. In general ePDS is the most power efficient mode for most active use cases. HID-OFF generally works for non connectable beacon type use cases with long advertisement intervals. Refer to the [“Firmware”](#) on page 22 section for more details.

## 2.5 Watchdog

CYW20819 includes an onboard watchdog timer with a period of approximately 4 seconds. The watchdog timer generates an interrupt to the FW after 2 seconds of inactivity and resets the parts after 4 seconds.

## 2.6 True random number generator

The CYW20819 includes a hardware TRNG. Applications can access the random number generator via the firmware driver. Refer to the [ModusToolbox™](#) documentation for details.

### 3 Power on and external reset

Figure 4 shows power on and reset timing of the CYW20819. After VBAT is applied and reset is inactive, the internal buck turns on, followed by the RF and digital LDOs. Once the LDO outputs have stabilized, the PMU allows the digital core to come out of reset. As shown in the figure below, external reset can be applied at any time subsequent to power up.

**Note:** The host TXD and RTS signals should be configured to open-drain or High-Z until 10 ms after the CYW20819 reset is released.

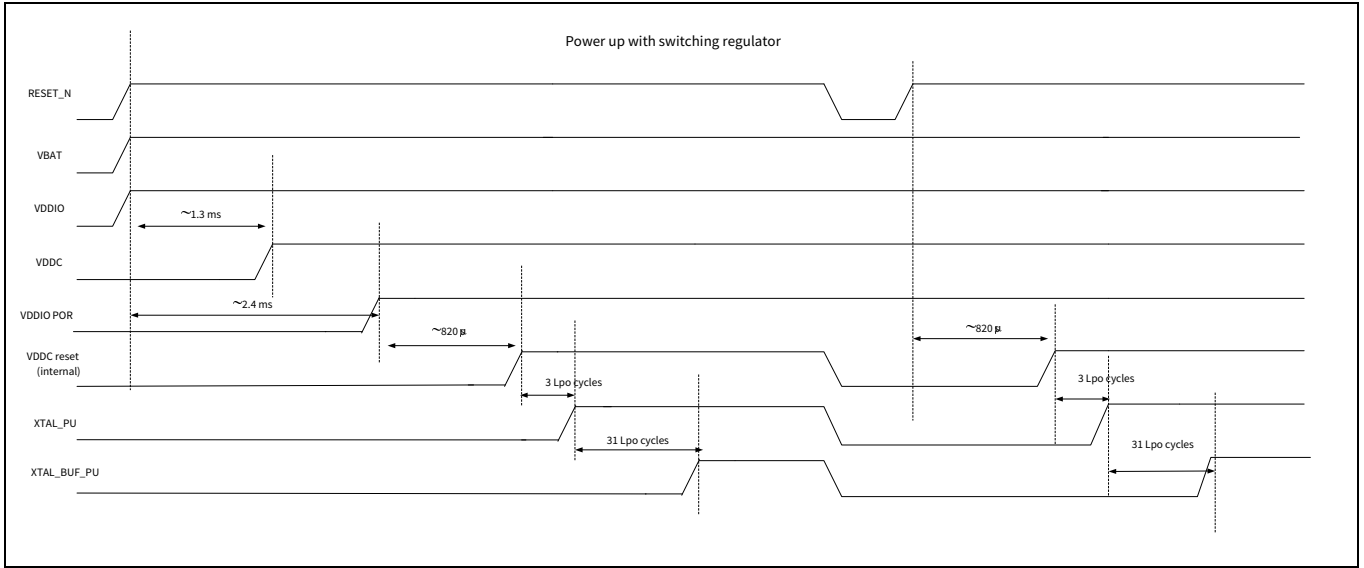
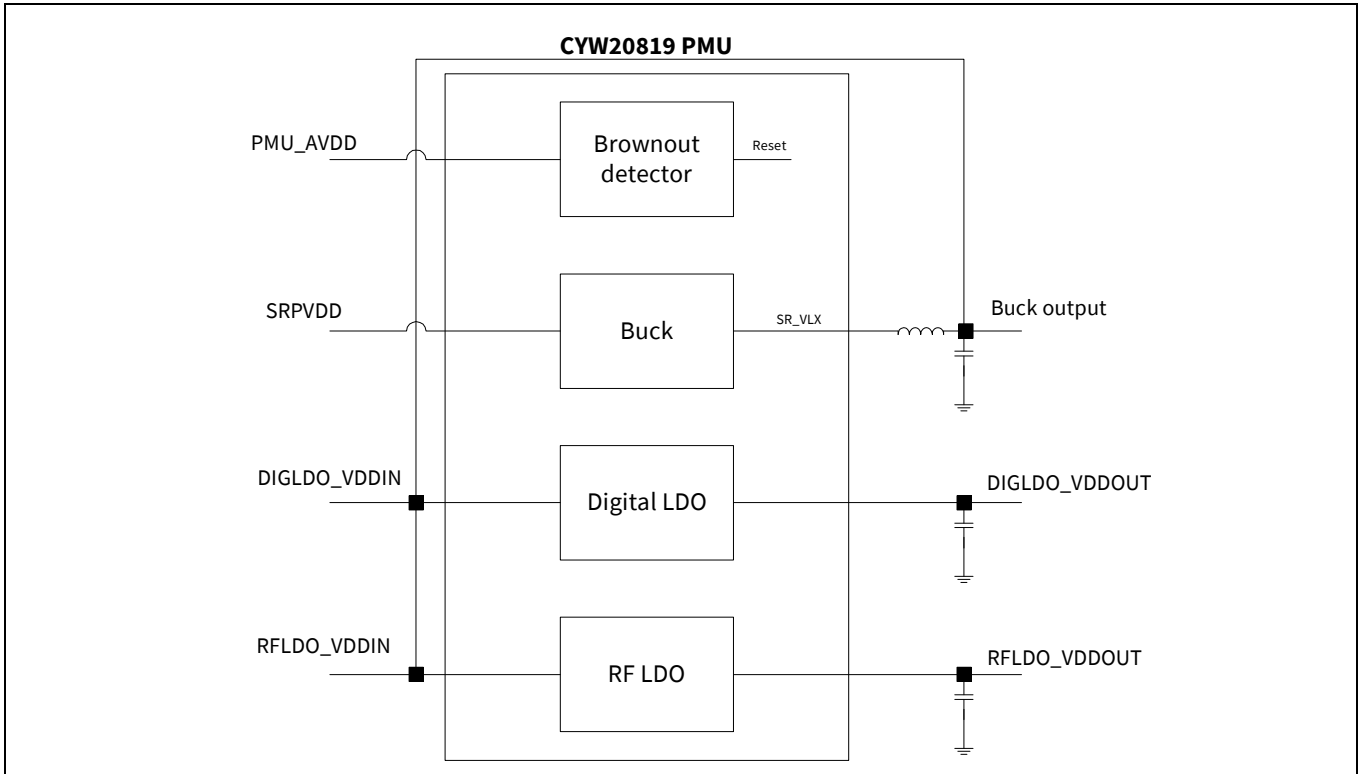


Figure 4 Reset timing

## 4 Power management unit

**Figure 5** shows the CYW20819 power management unit (PMU) block diagram. The CYW20819 includes an integrated buck regulator, a digital LDO for the digital core, and an RF LDO for the radio. The PMU also includes a brownout detector which places the part in shutdown when input voltage is below a certain threshold.



**Figure 5 Power management unit**

## 5 Power configurations

CYW20819 supports three power configurations as described in the following table.

**Table 4 Power configurations**

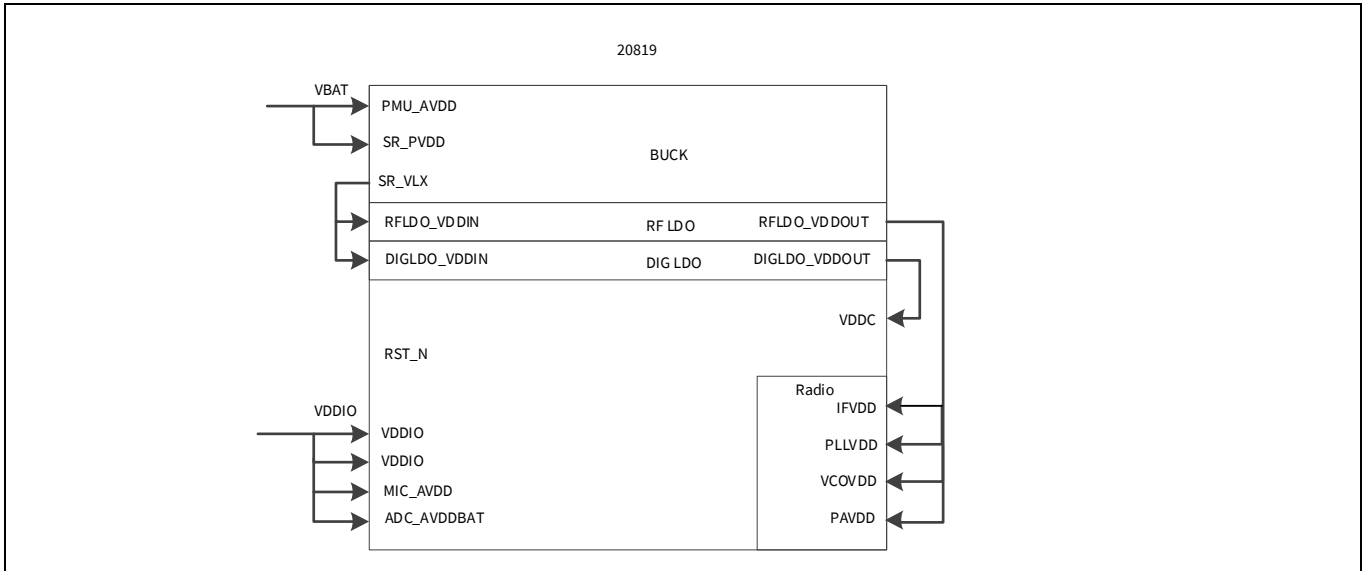
Configuration	Description
VBAT and VDDIO	VBAT and VDDIO are supplied externally and are used to generate all other supplies on the device. Reset may be left floating as it has an internal pull-up, may be connected to an external RC, or may be driven externally.
External supplies	PMU is disabled and on-chip regulators are not used. All supplies are provided externally. Reset is driven from the outside.
LDOs and VDDIO	On-chip LDOs are used to generate internal supplies but the on-chip buck is not used. Reset is driven externally.

### 5.1 Configuration 1 - VBAT and VDDIO

In this configuration the device is provided with two supplies (which can also be tied together). RST\_N is either left floating and relies on the internal pull-up to VDDIO to bring the device out of reset or tied to an external RC, or driven externally. All other required supplies are generated on-chip (see the [Figure 6](#)). Note that VDDIO must be supplied at the same time or before VBAT is supplied.

The device may require an external reset when any supply voltages drop below 1 V. POR operation not guaranteed below 1 V.

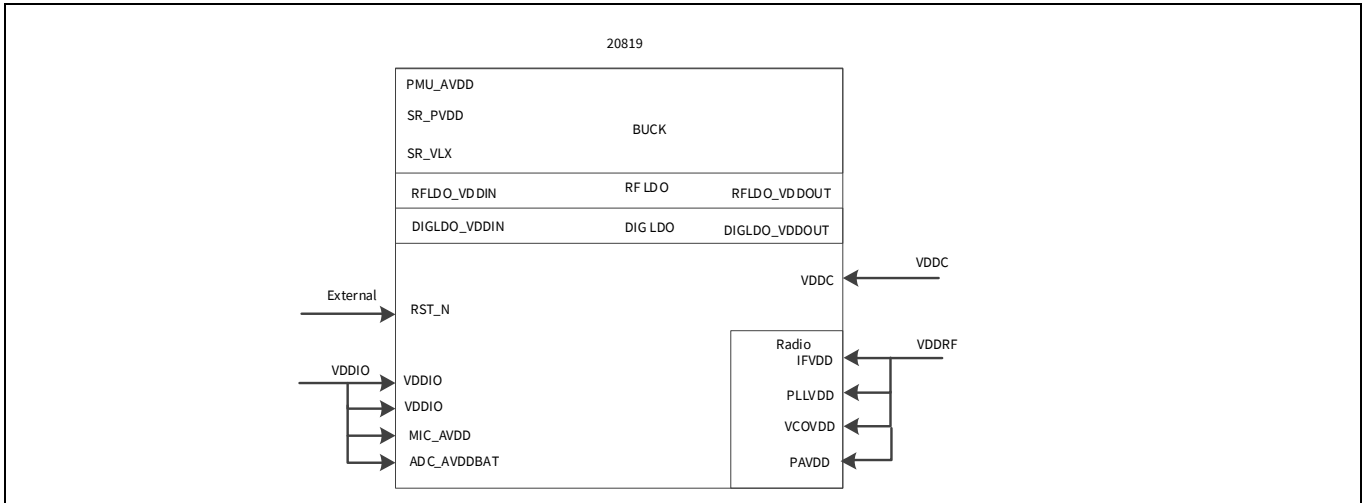
**Note:** RST\_N needs to be held low for additional 4 ms after VDDIO reaches high state.



**Figure 6 Configuration 1 - VBAT and VDDIO**

## 5.2 Configuration 2 - External supplies

In this configuration the internal regulators are not used and VBAT is not supplied. VDDIO is supplied along with externally generated core and radio supplies. This is shown in the following figure.



**Figure 7 Configuration 2 - External supplies**

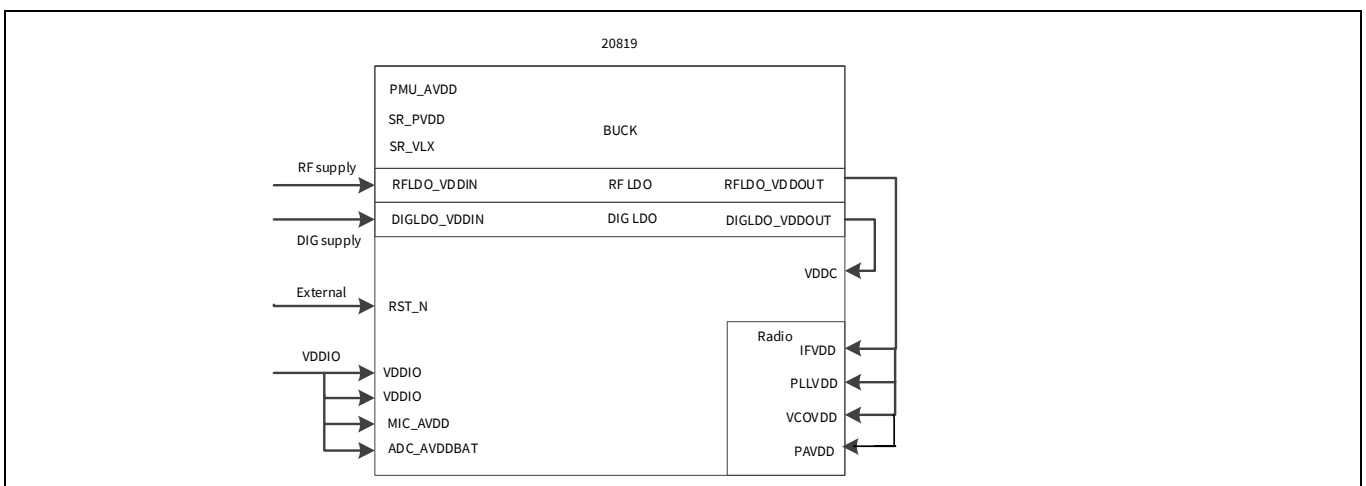
Note that VDDIO must be provided simultaneously or before the rest of the supplies and the device must be held in reset until all supplies are within normal operating ranges.

The device may require a reset if any supply goes outside the normal operating range.

## 5.3 Configuration 3 - LDOs and VDDIO

In this configuration the internal buck regulator is not used. Instead, power is supplied to the internal LDOs which are responsible for supplying the rest of the device.

**Note:** RST\_N needs to be held low for additional 4 ms after VDDIO reaches high state.



**Figure 8 Configuration 3 - LDOs and VDDIO**

Note that VDDIO must be provided simultaneously or before the rest of the supplies and the device must be held in reset until all supplies are within normal operating ranges. The internal LDOs have a small turn-on time which should be accounted for before releasing reset, see [Table 15](#) for Digital LDO and [Table 17](#) for RF LDO.

The device may require a reset if any supply goes outside the normal operating range.

## 6 Integrated radio transceiver

The CYW20819 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth® radio specification 3.0 and meets or exceeds the requirements to provide the highest communication link quality of service.

### 6.1 Transmitter path

The CYW20819 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

#### 6.1.1 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

#### 6.1.2 Power amplifier

The CYW20819 has an integrated power amplifier (PA) that can transmit up to +4 dBm for class 2 operation.

### 6.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYW20819 to be used in most applications without off-chip filtering.

#### 6.2.1 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

#### 6.2.2 Receiver signal strength indicator

The radio portion of the CYW20819 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

### 6.3 Local oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the band. The CYW20819 uses an internal loop filter.



## 7 Peripherals

### 7.1 I<sup>2</sup>C compatible master

The CYW20819 provides a 2-pin I<sup>2</sup>C compatible master interface to communicate with I<sup>2</sup>C compatible peripherals. The I<sup>2</sup>C compatible master supports the following clock speeds:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I<sup>2</sup>C-compatible speed)
- 1 MHz (Compatibility with high-speed I<sup>2</sup>C-compatible devices is not guaranteed.)

The I<sup>2</sup>C compatible master is capable for doing read, write, write followed by read, and read followed by write operations where read/write can be up to 64 bytes.

SCL and SDA lines can be routed to any of the P0-P39 GPIOs allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. I<sup>2</sup>C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

### 7.2 Serial peripheral interface

The CYW20819 has two independent SPI interfaces. Both interfaces support Single, Dual, and Quad mode SPI operations. Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20819 has optional I/O ports that can be configured individually and separately for each functional pin.

SPI I/O voltage depends on VDDO/VDDM.

### 7.3 HCI UART interface

The CYW20819 includes a UART interface for factory programming as well as when operating as a Bluetooth® HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 3 Mbps. Typical rates are 115200, 921600, 1500000, and 3,000,000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYW20819 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%. The UART interface CYW20819 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

During HCI mode, the DEV\_WAKE signal can be programmed to wake up the CYW20819 or allow the CYW20819 to sleep when radio activities permit. The CYW20819 can also wake up the host as needed or allow the host to sleep via the HOST\_WAKE signal. Combined, the two signals allow the host and the CYW20819 to optimize system power consumption by allowing independent control of low power modes. DEV\_WAKE and HOST\_WAKE signals can be enabled via a vendor specific command.

The FW UART driver allows applications to select different baud rates.

### 7.4 Peripheral UART interface

The CYW20819 has a second UART that may be used to interface to peripherals. Functionally, the peripheral UART is the same as the HCI UART except for 256-byte TX/RX FIFOs. The peripheral UART is accessed through the I/O ports, which can be configured individually and separately for each functional pin. The CYW20819 can map the peripheral UART to any GPIO.

## 7.5 GPIO ports

The CYW20819 has 22 general purpose I/Os labeled P0-P21. All GPIOs support the following:

- Programmable pull-up/down of approx 45 kΩ
- Input disable, allowing pins to be left floating or analog signals connected without risk of leakage
- Source/sink 8 mA at 3.0 V and 4 mA at 1.8 V
- P26/P27/P28/P29 sink/source 16 mA at 3.0 V and 8 mA at 1.8 V

Most peripheral functions can be assigned to any GPIO. For details, see [Table 6](#) and [Table 7](#).

## 7.6 Keyboard scanner

The CYW20819 includes a HW key scanner that supports a maximum matrix size of 20x8. The scanner has 8 inputs (also referred to as rows) and 20 outputs (also referred to as columns). Keys are detected by driving the columns down sequentially and sampling the rows. The HW scanner includes support for ghost key detection and debouncing. The scanner can also operate in sleep and PDS modes allowing low power operation while continuing to detect/store all key strokes, up or down. In other low power modes, the scanner can continue to monitor the matrix and initiate exit to active mode upon detecting a change of state.

The application can access the key scanner via the associated firmware driver. Refer to the “[Firmware](#)” on page 22 section for more details.

## 7.7 Mouse quadrature signal decoder

The CYW20819 includes one double-axis and one single axis quadrature decoders. There are two input lines for each axis and a programmable control signal that can be active HIGH or LOW.

The application can access the quadrature interface via the driver included in the firmware.

## 7.8 ADC

The CYW20819 includes a  $\Sigma$ - $\Delta$  ADC designed for audio and DC measurements. The ADC can measure the voltage on 15 GPIOs (P0, P1, P8–P15, P17, P28, P29, P32, and P37). When used for analog inputs, the GPIOs must be placed in digital input disable mode to disconnect the digital circuit from the pin and avoid leakage. The internal bandgap reference has  $\pm 5\%$  accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in direct current (DC) mode.

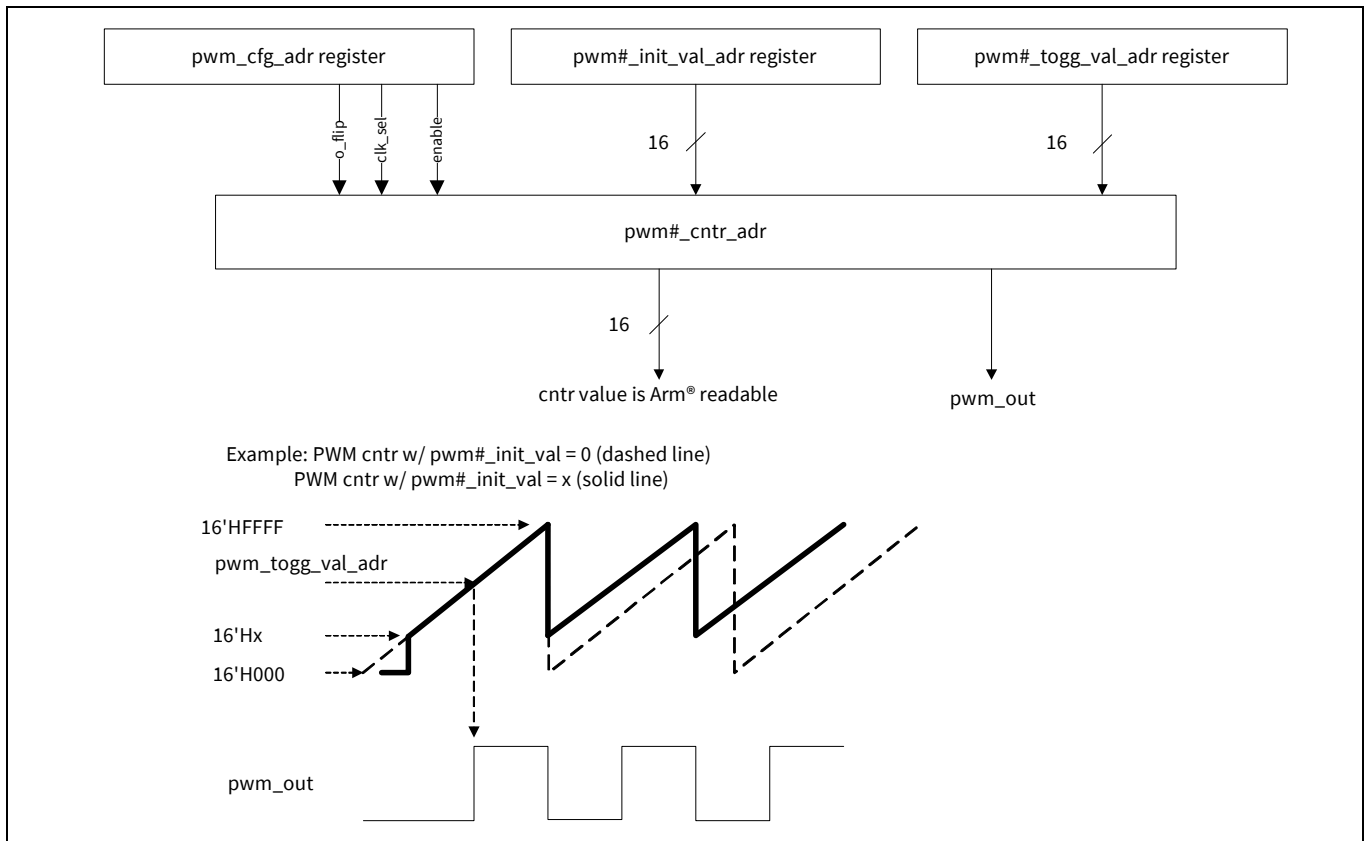
The application can access the ADC through the ADC driver included in the firmware.

## 7.9 PWM

The CYW20819 has six internal PWMs, labeled PWM0-5.

- Each of the six PWM channels contains the following registers:
  - 16-bit Initial Value Register (read/write)
  - 16-bit Toggle Register (read/write)
  - 16-bit PWM Counter Value Register (read)
- PWM Configuration Register is shared among PWM0–5 (read/write). This 18-bit register is used:
  - To enable/disable each PWM channel
  - To select the clock of each PWM channel
  - To invert the output of each PWM channel. The application can access the PWM module through the FW driver.

**Figure 9** shows the structure of one PWM channel.



**Figure 9** PWM block diagram

### 7.10 PDM microphone

The CYW20819 accepts a  $\Sigma\Delta$ -based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM inputs share the filter path with the Aux ADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4 MHz clock generated by the CYW20819 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

## 7.11 I<sup>2</sup>S interface

The CYW20819 supports a single I<sup>2</sup>S digital audio port with both master and slave modes. The I<sup>2</sup>S signals are:

- I<sup>2</sup>S clock: I<sup>2</sup>S SCK
- I<sup>2</sup>S word select: I<sup>2</sup>S WS
- I<sup>2</sup>S data out: I<sup>2</sup>S DO
- I<sup>2</sup>S data in: I<sup>2</sup>S DI

I<sup>2</sup>S SCK and I<sup>2</sup>S WS become outputs in Master mode and inputs in slave mode, while I<sup>2</sup>S DO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I<sup>2</sup>S bus, per I<sup>2</sup>S specifications. The MSB of each data word is transmitted one bit clock cycle after the I<sup>2</sup>S WS transition, synchronous with the falling edge of bit clock. Left channel data is transmitted when I<sup>2</sup>S WS is LOW, and right-channel data is transmitted when I<sup>2</sup>S WS is HIGH. Data bits sent by the CYW20819 are synchronized with the falling edge of I<sup>2</sup>S SCK and should be sampled by the receiver on the rising edge of the I<sup>2</sup>S SCK.

The clock rate in Master mode is as follows:

- 16 kHz × 16 bits per frame = 256 kHz

The master clock is generated from the reference clock using an N/M clock divider. In the slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

## 7.12 PCM interface

The CYW20819 includes a PCM interface that can connect to linear PCM codec devices in Master or Slave mode. In Master mode, the CYW20819 generates the PCM\_CLK and PCM\_SYNC signals. In Slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW20819. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

**Note:** The PCM interface shares HW with the I<sup>2</sup>S interface and only one can be used at any time. Only audio source (other than SCO) use cases are supported on CYW20819.

### 7.12.1 Slot mapping

The CYW20819 supports up to three simultaneous full-duplex channels through the PCM Interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

### 7.12.2 Frame synchronization

The CYW20819 supports both short- and long-frame synchronization in both Master and Slave modes. In short Frame Synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In Long-Frame Synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

### 7.12.3 Data formatting

The CYW20819 may be configured to generate and accept several different data formats. For conventional Narrow Band Speech mode, the CYW20819 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

## 8 Firmware

The CYW20819 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the Bluetooth®/LE baseband, LMAC, HCI, GATT, ATT, L2CAP, and SDP layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes. The ROM also supports OTA firmware update and acts as a root of trust

The CYW20819 is fully supported by the ModusToolbox™. ModusToolbox™ releases provide the latest ROM patches, drivers, and sample applications allowing customized applications using the CYW20819 to be built quickly and efficiently.

Refer to the [ModusToolbox™](#) documentation for details on the software and how to write applications/profiles using the CYW20819.

## 9 Pin assignments and GPIOs

This section addresses both 62-pin FBGA assignment and general purpose IO's (GPIOs) for the CYW20819 device.

### 9.1 62-pin FBGA assignment

**Table 5 62-pin FBGA assignment**

Pin name	Pin number	I/O	Power domain	Description
	FBGA-62			
<b>Baseband supply</b>				
VDDO1	B8	I	VDDO	I/O pad power supply
VDDO2	D1	I	VDDO	I/O pad power supply
VDDC	C8, E1	I/O	VDDC	Baseband core power supply
<b>RF power supply</b>				
IFVDD	F6	I	IFVDD	IFPLL power supply
PLLVDD	G8	I	PLLVDD	RFPLL and crystal oscillator supply
PAVDD	H5	I	PAVDD	PA supply
VCOVDD	H8	I	VCOVDD	VCO supply
<b>Onboard LDO's</b>				
DIGLDO_- VDDOUT	G4	O	-	Internal digital LDO output
RFLDO_- VDDOUT	H4	O	-	RF LDO output
RFLDO_DIGLD O_VDDIN	E5	I	-	Internal digital LDO and RF LDO input
SR_PVDD	H3	I	-	Core buck input
SR_VLX	H2	O	-	Core buck output
PMU_AVDD	G3	I	-	PMU supply
<b>Ground pins</b>				
VSSC	C3, C6, E3	I	VSS	Ground
ADC_AVSS	A8	I	AVSS	Analog ground
PMU_AVSS	F4	I	VSS	PMU ground
PLLVSS	F7	I	VSS	Ground
PAVSS	G6	I	VSS	Ground
VCOVSS	G7	I	VSS	Ground
SR_PVSS	H1	I	VSS	Ground
IFVSS	H7	I	VSS	Ground
<b>UART</b>				
UART_CTS_N	C7	I, PU	VDDO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
UART_RTS_N	E6	O, PU	VDDO	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
UART_RXD	D7	I	VDDO	UART serial input. Serial data input for the HCI UART interface.

## Pin assignments and GPIOs

**Table 5** 62-pin FBGA assignment (continued)

Pin name	Pin number	I/O	Power domain	Description
	FBGA-62			
UART_TXD	D6	O, PU	VDDO	UART serial output. Serial data output for the HCI UART interface.
<b>Crystal</b>				
XTALI	F8	I	PLLVD	Crystal oscillator input. See “The XTAL must have an accuracy of $\pm 20$ ppm as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent ( <b>Figure 1</b> )” for options.
XTALO	E8	O	PLLVD	Crystal oscillator output
XTALI_32K	B7	I	VDDO	Low-power oscillator input
XTALO_32K	A7	O	VDDO	Low-power oscillator output
<b>Other</b>				
RF	H6	–	–	RF antenna port
RST_N	G1	I	VDDO	Active-low system reset with internal pull-up resistor
JTAG_SEL	G2	–	–	Arm® JTAG debug mode control. Connect to GND for all applications.
<b>Reserved pins</b>				
Reserved	F5, G5	N/A	N/A	Reserved. Leave unconnected.
<b>GPIOs</b>				
HOST_WAKE	D8	O	VDDO	A signal from the CYW20819 device to the host indicating that the Bluetooth® device requires attention.
DEV_WAKE	E7	I	VDDO	A signal from the host to the CYW20819 indicating that the host requires attention.
P0	D2	I/O	VDDO	Recommended functions for P0 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI0</li> <li>• A/D converter input 29</li> <li>• Peripheral UART: puart_tx</li> <li>• SPI_1: MOSI (master only)</li> <li>• UART1_TXD</li> </ul> P0 can also be remapped using Supermux I/O functions as defined in <b>Table 6</b> and <b>Table 7</b> .
P1	C1	I/O	VDDO	Recommended functions for P1 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI1</li> <li>• A/D converter input 28</li> <li>• Peripheral UART: puart_rts</li> <li>• SPI_1: MISO (slave only)</li> <li>• UART1_RXD</li> </ul> Can also be remapped using Supermux I/O functions as defined in <b>Table 6</b> and <b>Table 7</b> .



Pin assignments and GPIOs

**Table 5** 62-pin FBGA assignment (continued)

Pin name	Pin number	I/O	Power domain	Description
	FBGA-62			
P2	B5	I/O	VDDO	Recommended functions for P2 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI2</li> <li>• Quadrature: QDX0</li> <li>• SPI_1: MOSI (master only)</li> <li>• UART1_RTS_N</li> </ul> P2 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P3	A5	I/O	VDDO	Recommended functions for P3 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI3</li> <li>• Quadrature: QDX1</li> <li>• UART1_CTS_N</li> <li>• SPI_1: SPI_CLK (master only)</li> </ul> P3 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P4	C5	I/O	VDDO	Recommended functions for P4 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI4</li> <li>• Quadrature: QDY0</li> <li>• SPI_1: MOSI (master only)</li> </ul> P4 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P5	B4	I/O	VDDO	Recommended functions for P5 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI5</li> <li>• Quadrature: QDY1</li> <li>• Peripheral UART: puart_tx</li> <li>• SPI_1: MISO (slave only)</li> <li>• I<sup>2</sup>C: SDA</li> </ul> P5 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P6	A4	I/O	VDDO	Recommended functions for P6 <ul style="list-style-type: none"> <li>• Keyboard scan input (row): KSI6</li> <li>• Quadrature: QDZ0</li> <li>• Peripheral UART: puart_rts</li> <li>• PWM2</li> </ul> P6 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .

## Pin assignments and GPIOs

**Table 5**      **62-pin FBGA assignment** (continued)

Pin name	Pin number	I/O	Power domain	Description
	FBGA-62			
P8	A6	I/O	VDDO	Recommended functions for P8 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO0</li> <li>• A/D converter input 27</li> <li>• External T/R switch control: ~tx_pd</li> </ul> P8 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P9	A2	I/O	VDDO	Recommended functions for P9 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO1</li> <li>• A/D converter input 26</li> <li>• External T/R switch control: tx_pd</li> </ul> P9 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P10	C2	I/O	VDDO	Recommended functions for P10 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO2</li> <li>• A/D converter input 25</li> <li>• External PA ramp control: PA_Ramp</li> </ul> P10 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P11	B2	I/O	VDDO	Recommended functions for P11 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO3</li> <li>• A/D converter input 24</li> </ul> P11 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P12	A1	I/O	VDDO	Recommended functions for P12 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO4</li> <li>• A/D converter input 23</li> </ul> P12 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P13	B1	I/O	VDDO	Recommended functions for P13 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO5</li> <li>• A/D converter input 22</li> <li>• PWM3</li> </ul> P13 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P14	B3	I/O	VDDO	Recommended functions for P14 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO6</li> <li>• A/D converter input 21</li> <li>• PWM2</li> </ul> P14 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .

Pin assignments and GPIOs

**Table 5**      **62-pin FBGA assignment** (continued)

Pin name	Pin number	I/O	Power domain	Description
	FBGA-62			
P15	B6	I/O	VDDO	Recommended functions for P15 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO7</li> <li>• A/D converter input 20</li> </ul> P15 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P17	A3	I/O	VDDO	Recommended functions for P17 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO9</li> <li>• A/D converter input 18</li> </ul> P17 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P26	D4	I/O	VDDO	Recommended functions for P26 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO18</li> <li>• PWM0</li> <li>• SPI_1: SPI_CS (slave only)</li> <li>• Optical control output: QOC0</li> <li>• Current: 16 mA sink</li> </ul> P26 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P27	F1	I/O	VDDO	Recommended functions for P27 <ul style="list-style-type: none"> <li>• Keyboard scan output (column): KSO19</li> <li>• PWM1</li> <li>• SPI_1: MOSI (master only)</li> <li>• Optical control output: QOC1</li> <li>• Current: 16 mA sink</li> </ul> P27 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P28	C4	I/O	VDDO	Recommended functions for P28 <ul style="list-style-type: none"> <li>• PWM2</li> <li>• SCL3 (master and slave)</li> <li>• Optical control output: QOC2</li> <li>• A/D converter input 11</li> <li>• Current: 16 mA sink</li> </ul> P28 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .

Pin assignments and GPIOs

**Table 5** 62-pin FBGA assignment (continued)

Pin name	Pin number	I/O	Power domain	Description
	FBGA-62			
P29	D3	I/O	VDDO	Recommended functions for P29 <ul style="list-style-type: none"> <li>• PWM3</li> <li>• SDA3 (master and slave)</li> <li>• Optical control output: QOC3</li> <li>• A/D converter input 10</li> <li>• Current: 16 mA sink</li> </ul> P29 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P32	F2	I/O	VDDO	Recommended functions P32 <ul style="list-style-type: none"> <li>• A/D converter input 7</li> <li>• Quadrature: QDX0</li> <li>• Auxiliary clock output: ACLK0</li> <li>• Peripheral UART: puart_tx</li> </ul> P32 Can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
P37	E2	I/O	VDDO	Recommended functions for P37 <ul style="list-style-type: none"> <li>• A/D converter input 2</li> <li>• Quadrature: QDZ1</li> <li>• SPI_1: MISO (slave only)</li> <li>• Auxiliary clock output: ACLK1</li> <li>• I<sup>2</sup>C: SCL</li> </ul> P37 can also be remapped using Supermux I/O functions as defined in <a href="#">Table 6</a> and <a href="#">Table 7</a> .
<b>Strapping pins</b>				
PMU_LDO_ONLY_STRAP	E4	I	VDDO	Strap pin to indicate LDO-only mode



Pin assignments and GPIOs

**Table 6**      **GPIO Supermux input functions**

<b>Input</b>
SWDCK
SWDIO
SPI1_CLK
SPI1_CS
SPI1_MOSI
SPI1_MISO
SPI1_IO2
SPI1_IO3
SPI1_INT
SPI2_CLK
SPI2_CS
SPI2_MOSI
SPI2_MISO
SPI2_IO2
SPI2_IO3
SPI2_INT
puart_rx
puart_cts_n
SCL
SDA
SCL2
SDA2
PCM_IN
PCM_CLK
PCM_SYNC
I2S_DI
I2S_WS
I2S_CLK
PDM_IN_Ch_1
PDM_IN_Ch 2

**Table 7 GPIO Supermux output functions**

<b>Output</b>
do_P# (data out of GPIO. For example: P0)
do_PCM_IN
do_PCM_OUT
do_PCM_CLK
do_PCM_SYNC
do_I2S_DO
do_I2S_DI
do_I2S_WS
do_I2S_CLK
do_CLK_REQ
IR_TX
kso0
kso1
kso2
kso3
kso4
kso5
kso6
kso7
kso8
kso9
kso10
kso11
kso12
kso13
kso14
kso15
kso16
kso17
kso18
kso19
do_P# pwm0
do_P# pwm1
do_P# pwm2
do_P# pwm3
do_P# pwm4
do_P# pwm5
aclk0
aclk1
HID_OFF

**Table 7** GPIO Supermux output functions *(continued)*

<b>Output</b>
pa_ramp
tx_pd
~tx_pd
SWDIO
SDA2
SCL2
puart_tx (uart2_tx)
puart_rts_n (uart2_rts_n)
SPI1_CLK
SPI1_CS
SPI1_MOSI
SPI1_MISO
SPI1_IO2
SPI1_IO3
SPI2_CLK
SPI2_CS
SPI2_MOSI
SPI2_MISO
SPI2_IO2
SPI2_IO3

**9.2 I/O states**

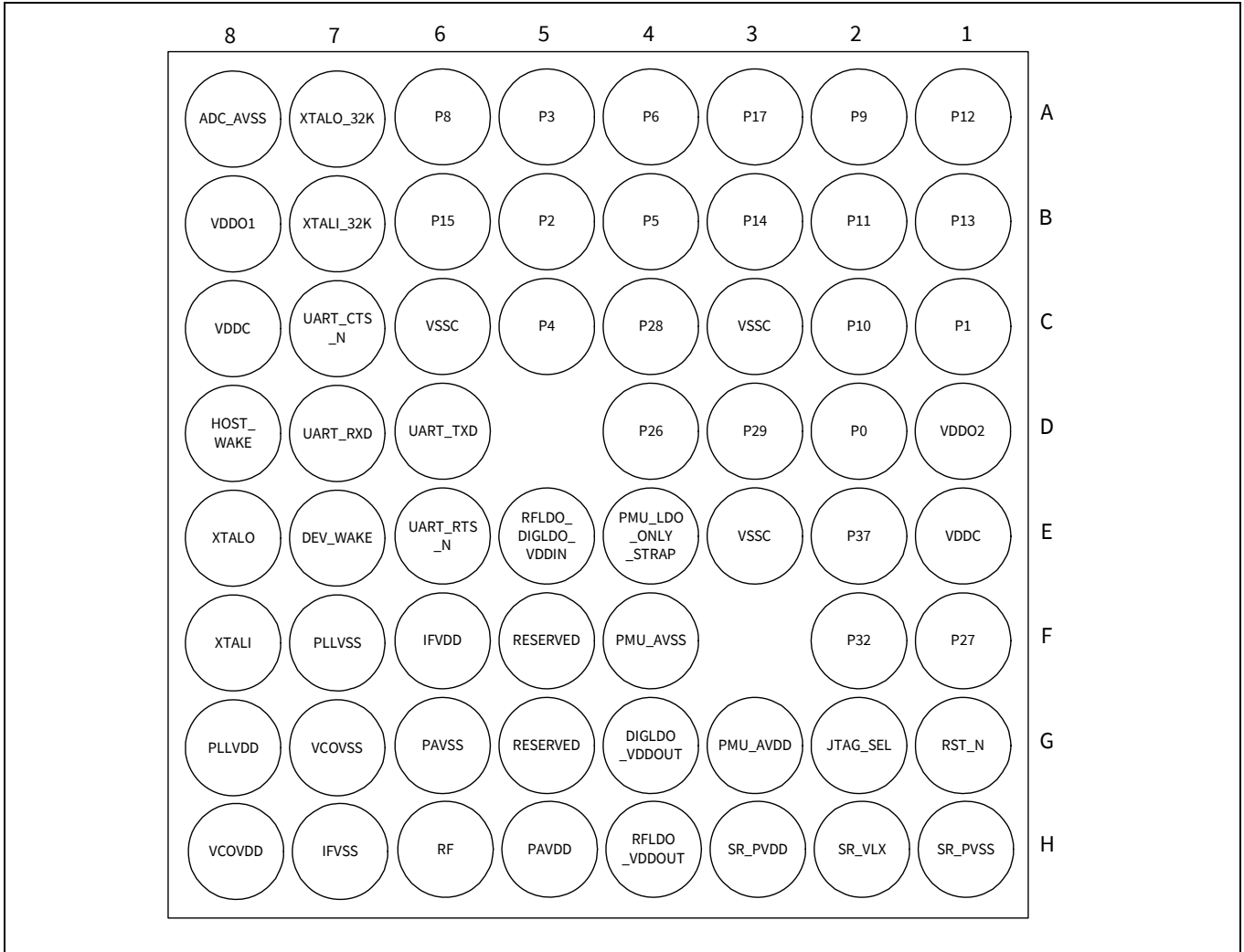
When RST\_N = 0 (during reset), all GPIOs (P0 to P39) are input-pins, no pull-up/pull-down and input-disabled. In auto-baud (RST\_N = 1 and no FW programming), all GPIOs (P0 to P39) are input-pins and no pull-up/pull-down. Input signals are allowed to pass.

Ball maps

## 10 Ball maps

### 10.1 62-pin FBGA pin map

The CYW20819 62-pin FBGA package is shown in [Figure 10](#).



**Figure 10** 62-pin FBGA ball map

**Note:** Pins F5 and G5 are used as PALDO\_VDDIN and PALDO\_VDDOUT on CYW20820 respectively. Please refer to CYW20820 datasheet for detail.



Specifications

## 11 Specifications

### 11.1 Electrical characteristics

**Caution!** The absolute maximum ratings in **Table 8** indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 8 Absolute maximum ratings**

Requirement parameter	Specification			Unit
	Min	Nom	Max	
Maximum junction temperature	–	–	125	°C
VDDO1/VDDO2	–0.5	–	3.45	V
IFVDD/PLLVDD/VCOVDD/VDDC	–0.5	–	1.38	
PMUAVDD/SR_PVDD	–0.5	–	3.45	
DIGLDO_VDDIN	–0.5	–	1.65	
RFLDO_VDDIN	–0.5	–	1.65	
MIC_AVDD	–0.5	–	3.45	

**Table 9 ESD/latchup**

Requirement parameter	Specification			Unit
	Min.	Nom.	Max.	
ESD tolerance HBM	–2000	–	2000	V
ESD tolerance CDM	–500	–	500	
Latch-up	–	200	–	mA

**Table 10 Environmental ratings**

Characteristic	Value	Unit
Operating temperature	–30 to +85	°C
Storage temperature	–40 to +150	

Specifications

**Table 11 Recommended operating conditions**

Parameter	Specification			Unit
	Min.	Typ.	Max.	
VDDC	1.045 <sup>[1]</sup>	1.2	1.26	V
IFVDD <sup>[3]</sup>	1.14	1.2	1.26	
PLLVD <sup>[3]</sup>	1.14	1.2	1.26	
VCOVDD <sup>[3]</sup>	1.14	1.2	1.26	
PAVDD <sup>[3]</sup>	1.14	1.2	1.26	
VDDO1 <sup>[2]</sup>	1.71	3.0	3.3	
VDDO2 <sup>[2]</sup>	1.71	3.0	3.3	
PMU_AVDD	1.71	3.0	3.3	
SR_PVDD	1.71	3.0	3.3	
RFLDO_VDDIN	1.26	1.26	1.38	
DIGLDO_VDDIN	1.26	1.26	1.38	

**11.2 Brown out**

The CYW20819 uses an onboard low voltage detector to shut down the part when supply voltage (VDDBAT3V) drops below the operating range.

**Table 12 Shutdown voltage**

Parameter	Specification			Unit
	Min.	Typ.	Max.	
V <sub>SHUT</sub>	1.5	1.56	1.7	V

**Notes**

1. 1.14 V for > 48 MHz operation.
2. VDDO1 must be equal to VDDO2. Recommend that these be provided from the same source.
3. IFVDD, PLLVD, VCOVDD, and PAVDD must all be equal. Recommend providing from the same supply.

## Specifications

**11.3 Core buck regulator**
**Table 13 Core buck regulator**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply, VBAT	DC range	1.71	3.0	3.3	V
Output current	Active mode	–	< 60	100	mA
	PDS mode	–	< 60	70	
Output voltage	Active mode	1.1	1.26	1.4	V
	PDS mode, 40 mV min regulation window.	0.76	0.94 Avg	1.4	
Output voltage accuracy	Active mode, includes line and load regulation. Before trim	–4	–	+4	%
Ripple voltage	Active mode 2.2 $\mu\text{H} \pm 25\%$ inductor, DCR = 114 m $\Omega \pm 20\%$ 4.7 $\mu\text{F} \pm 10\%$ capacitor, Total ESR < 20 m $\Omega$	–	3	–	mV
	PDS mode	–	–	–	
Output inductor, L	Refer to the <b>“Recommended component”</b> on page 35 for more details.	1.6 <sup>[4]</sup>	2.2	–	$\mu\text{H}$
Output capacitor, C <sub>OUT</sub>		3.0 <sup>[4]</sup>	4.7	–	$\mu\text{F}$
Input capacitor, C <sub>IN</sub>		4.0 <sup>[4]</sup>	10	–	
Input supply voltage ramp time	0 to 3.3 V	40	–	–	$\mu\text{s}$

**11.4 Recommended component**
**Table 14 Recommended component**

Parameter	Conditions	Min.	Typ.	Max.	Unit
External inductor, L	2.2 $\mu\text{H} \pm 25\%$ , DCR = 114 m $\Omega \pm 20\%$ , ACR < 1 (for frequency < 1 MHz)	1.6	2.2	–	$\mu\text{H}$
External output capacitor, C <sub>OUT</sub>	4.7 $\mu\text{F} \pm 10\%$ , 6.3 V, 0603 inch, X5R, MLCC capacitor + board total-ESR < 20 m $\Omega$	3.0	4.7	–	$\mu\text{F}$
External input capacitor, C <sub>IN</sub>	For SR_VDDBAT pin, ceramic, X5R, 0402, ESR < 30 m $\Omega$ at 4 MHz, +/-20%, 6.3 V, 10 $\mu\text{F}$	4	10	–	

**Note**

4. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

## Specifications

**11.5 Digital LDO**
**Table 15 Digital LDO**

Parameter	Condition	Min	Typ	Max	Unit
Input supply, DIGLDO_-VDDIN	Min must be met for correct operation	$V_{OUT} + 20$ mV	1.26	1.4	V
Output voltage, DIGLDO_VDDOUT	Range	0.9	1.2	1.275	
	Step	–	25	–	mV
	Accuracy	–4	–	+4	%
Dropout voltage	At max load current	–	–	20	mV
Output current	DC load	–	30	60	mA
Quiescent current	At $T \leq 85^\circ\text{C}$ , $V_{IN} = 1.4$ V	–	–	50	$\mu\text{A}$
Output load capacitor, $C_{OUT}$	Total trace + cap ESR must be $< 80$ m $\Omega$	1.55 <sup>[5]</sup>	2.2	–	$\mu\text{F}$
Line regulation	$1.235$ V $\leq V_{IN} \leq 1.4$ V	–	–	10	mV/V
Load regulation	$V_{OUT} = 1.2$ V, $V_{IN} = 1.26$ V, $1$ mA $\leq I_{OUT} \leq 25$ mA	–	–	1	mV/mA
Load step error	$I_{OUT}$ step 1 mA $\leftrightarrow$ 20 mA @ 1 $\mu\text{s}$ rise/fall, $C_{OUT} = 2.2$ $\mu\text{F}$ , $V_{IN} = 1.235$ V, $V_{OUT} = 1.2$ V	–24	–	+24	mV
Leakage current	Power down mode, $V_{IN} = 1.4$ V, temp = $25^\circ\text{C}$	–	–	50	nA
	Power down mode, $V_{IN} = 1.4$ V, temp = $125^\circ\text{C}$	–	–	2	$\mu\text{A}$
In-rush current	$C_{OUT} = 2.2$ $\mu\text{F}$ , $V_{IN} = 1.4$ V, $V_{OUT} = 1.2$ V	–	–	100	mA
LDO turn on time	$C_{OUT} = 2.2$ $\mu\text{F}$ , $V_{IN} = 1.4$ V, $V_{OUT} = 1.2$ V, $I_{OUT} = 20$ mA	–	–	120	$\mu\text{s}$
PSRR	$C_{OUT} = 2.2$ $\mu\text{F}$ , $1.235$ V $\leq V_{IN} \leq 1.4$ V, $V_{OUT} = 1.2$ V, $I_{OUT} = 20$ mA $f = 1$ kHz $f = 100$ kHz	25	–	–	dB
		13	–	–	

**11.6 Recommended component**
**Table 16 Recommended component**

Parameter	Conditions	Min.	Typ.	Max.	Unit
External output capacitor, $C_{OUT}$	2.2 $\mu\text{F} \pm 10\%$ , 10 V, 0402 inch, X5R, MLCC capacitor + board total- ESR $< 20$ m $\Omega$	1.55	2.2	–	$\mu\text{F}$

**Note**

5. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

## Specifications

**11.7 RF LDO**
**Table 17 RF LDO**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply, RFLDO_VDDIN	Min must be met for correct operation	$V_{OUT} + 20 \text{ mV}$	1.26	1.4	V
Output voltage, RFLDO_-VDDOUT	Range	1.1	1.2	1.275	
	Step	–	25	–	mV
	Accuracy	–4	–	+4	%
Dropout voltage	At max load current	–	–	20	mV
Output current	DC load	–	20	60	mA
Quiescent current	At $T \leq 85^\circ\text{C}$ , $V_{IN} = 1.4 \text{ V}$	–	–	50	$\mu\text{A}$
Output load capacitor, $C_{OUT}$	Total trace + cap ESR must be $< 80 \text{ m}\Omega$	1.55 <sup>[6]</sup>	2.2	–	$\mu\text{F}$
Line regulation	$1.235 \text{ V} \leq V_{IN} \leq 1.4 \text{ V}$	–	–	10	mV/V
Load regulation	$V_{OUT} = 1.2 \text{ V}$ , $V_{IN} = 1.26 \text{ V}$ , $1 \text{ mA} \leq I_{OUT} \leq 25 \text{ mA}$	–	–	1	mV/mA
Load step error	$I_{OUT}$ step $1 \text{ mA} \leftrightarrow 20 \text{ mA}$ @ $1 \mu\text{s}$ rise/fall, $C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.235 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$	–24	–	+24	mV
Leakage current	Power down mode, $V_{IN} = 1.4 \text{ V}$ , temp = $25^\circ\text{C}$	–	–	50	nA
	Power down Mode, $V_{IN} = 1.4 \text{ V}$ , temp = $125^\circ\text{C}$	–	–	2	$\mu\text{A}$
In-rush current	$C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$	–	–	100	mA
LDO turn on time	$C_{OUT} = 2.2 \mu\text{F}$ , $V_{IN} = 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ , $I_{OUT} = 20 \text{ mA}$	–	–	120	$\mu\text{s}$
PSRR	$C_{OUT} = 2.2 \mu\text{F}$ , $1.235 \text{ V} \leq V_{IN} \leq 1.4 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ , $I_{OUT} = 20 \text{ mA}$ $f = 1 \text{ kHz}$ $f = 100 \text{ kHz}$	25 13	–	–	dB

**Note**

6. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

## Specifications

**11.8 Digital I/O characteristics**
**Table 18 Digital I/O characteristics**

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Input low voltage (VDDO = 3 V)	$V_{IL}$	–	–	0.8	V
Input high voltage (VDDO = 3 V)	$V_{IH}$	2.4	–	–	
Input low voltage (VDDO = 1.8 V)	$V_{IL}$	–	–	0.4	
Input high voltage (VDDO = 1.8 V)	$V_{IH}$	1.4	–	–	
Output low voltage	$V_{OL}$	–	–	0.4	
Output high voltage	$V_{OH}$	VDDO – 0.4	–	–	
Input low current	$I_{IL}$	–	–	1.0	μA
Input high current	$I_{IH}$	–	–	1.0	
Output low current (VDDO = 3 V, $V_{OL}$ = 0.4 V)	$I_{OL}$	–	–	4.0	mA
Output low current (VDDO = 3 V, $V_{OL}$ = 1.8 V)	$I_{OL}$	–	–	2.0	
Output high current (VDDO = 3 V, $V_{OH}$ = 2.6 V)	$I_{OH}$	–	–	8.0	
Output high current (VDDO = 1.8 V, $V_{OH}$ = 1.4 V)	$I_{OH}$	–	–	4.0	
Input capacitance	$C_{IN}$	–	–	0.4	pF

## 11.9 ADC electrical characteristics

**Table 19 Electrical characteristics**

Parameter	Symbol	Conditions/comments	Min.	Typ.	Max.	Unit
Current consumption	$I_{TOT}$	–	–	2	3	mA
Power down current	–	At room temperature	–	1	–	$\mu$ A
<b>ADC core specification</b>						
ADC reference voltage	$V_{REF}$	From BG with $\pm 3\%$ accuracy	–	0.85	–	V
ADC sampling clock	–	–	–	12	–	MHz
Absolute error	–	Includes gain error, offset and distortion. Without factory calibration.	–	–	5	%
		Includes gain error, offset and distortion. After factory calibration.	–	–	2	%
ENOB	–	For audio application	12	13	–	Bit
		For static measurement	10	–	–	
ADC input full scale	FS	For audio application	–	1.6	–	
		For static measurement	1.8	–	3.3	
Conversion rate	–	For audio application	8	16	–	kHz
Signal bandwidth	–	For audio application	20	–	8K	Hz
		For static measurement	–	DC	–	
Input impedance	$R_{IN}$	For audio application	10	–	–	k $\Omega$
		For static measurement	500	–	–	
Startup time	–	For audio application	–	10	–	ms
		For static measurement	–	20	–	
<b>MIC bias specifications</b>						
MIC bias output voltage	–	At 3 V supply, 25°C, default settings	–	2.4	–	V
MIC bias loading current	–	–	–	–	3	mA
MIC bias noise	–	Refers to PGA input 20 Hz to 8 kHz, A-weighted	–	–	3	$\mu$ V
MIC bias PSRR	–	at 1 kHz	40	–	–	dB
ADC SNR	–	A-weighted 0 dB PGA gain, temperature= 25°C	–	78	–	dB
ADC THD + N	–	–3 dBFS input 0 dB PGA gain, temperature = 25°C	–	70	–	dB
GPIO input voltage	–	Always lower than avddBAT	–	–	3.3	V
GPIO source impedance <sup>[7]</sup>	–	Resistance	–	–	1	k $\Omega$
		Capacitance	–	–	10	pF

**Note**

7. Conditional requirements for the measurements of 10  $\mu$ s. Relaxed with longer measurements time for each GPIO input channel.

Specifications

**11.10 Current consumption**

**Table 20** provides the current consumption measurements taken at input of LDOIN and VDDIO combined (LDOIN = VDDIO = 3.0 V).

**Table 20 Current consumption**

Operational mode	Conditions	Typical	Unit
HCI	48 MHz with pause	1.3	mA
	48 MHz without pause	2.55	
RX	Continuous RX (BR)	6.1	
	Continuous RX (EDR)	6.69	
	Continuous RX (Bluetooth® LE)	6.15	
TX	Continuous TX (BR)	6.16	
	Continuous TX (EDR)	11.28	
	Continuous TX (Bluetooth® LE)	6.6	
PDS	-	16.5	μA
ePDS	All RAM retained	8.7	
HID-OFF (deep sleep)	32 kHz XTAL ON	1.75	



## Specifications

**11.11 RF specifications**

**Note:** [Table 21](#) and [Table 22](#) apply to single-ended industrial temperatures. Unused inputs are left open.

**Table 21 BR/EDR - receiver RF specifications**

Parameter	Mode and conditions	Min	Typ	Max	Unit
<b>Receiver section</b>					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, BDR GFSK 0.1% BER, 1 Mbps	–	–91.5 <sup>[8]</sup>	–	dBm
	EDR 2M	–	–94.5	–	dB
	EDR 3M	–	–88.0	–	
Maximum input	–	–20	–	–	dBm
<b>Interference performance</b>					
C/I co-channel	GFSK, BDR GFSK 0.1% BER <sup>[9]</sup>	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, BDR GFSK 0.1% BER <sup>[9]</sup>	–	–	–4.0	
C/I 2 MHz adjacent channel	GFSK, BDR GFSK 0.1% BER <sup>[9]</sup>	–	–	–31.5	
C/I ≥ 3 MHz adjacent channel	GFSK, BDR GFSK 0.1% BER <sup>[9]</sup>	–	–	–42.5	
C/I image channel	GFSK, BDR GFSK 0.1% BER <sup>[9]</sup>	–	–	–24.0	
C/I 1 MHz adjacent to image channel	GFSK, BDR GFSK 0.1% BER <sup>[9]</sup>	–	–	–35.0	
<b>Out-of-Band blocking performance (CW)<sup>[10]</sup></b>					
30 MHz to 2000 MHz	BDR GFSK 0.1% BER	–	–10.0	–	dBm
2000 MHz to 2399 MHz	BDR GFSK 0.1% BER	–	–27	–	
2498 MHz to 3000 MHz	BDR GFSK 0.1% BER	–	–27	–	
3000 MHz to 12.75 GHz	BDR GFSK 0.1% BER	–	–10.0	–	
<b>Intermodulation performance<sup>[9]</sup></b>					
Bluetooth®, interferer signal level	BDR GFSK 0.1% BER	–	–	–39.0	dBm
<b>Spurious emissions</b>					
30 MHz to 1 GHz	–	–	–	–57.0	dBm
1 GHz to 12.75 GHz	–	–	–	–47.0	

**Notes**

8. The receiver sensitivity is measured at BER of 0.1% on the device interface with dirty TX OFF.
9. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
10. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).

## Specifications

**Table 22 BR/EDR - Transmitter RF specifications**

Parameter	Min	Typ	Max	Unit
<b>Transmitter section</b>				
Frequency range	2402	–	2480	MHz
Class 2: BR TX power	–	5.0	–	dBm
Class 2: EDR 2M and 3M TX power	–	0	–	
20 dB bandwidth	–	930	1000	kHz
<b>Adjacent channel power</b>				
$ M - N  = 2$	–	–	–20	dBm
$ M - N  \geq 3$ <sup>[11]</sup>	–	–	–40	
<b>Out-of-Band spurious emission</b>				
30 MHz to 1 GHz	–	–	–36.0	dBm
1 GHz to 12.75 GHz	–	–	–30.0	
1.8 GHz to 1.9 GHz	–	–	–47.0	
5.15 GHz to 5.3 GHz	–	–	–47.0	
<b>LO performance</b>				
Initial carrier frequency tolerance	–75	–	+75	kHz
<b>Frequency drift</b>				
DH1 packet	–25	–	+25	kHz
DH3 packet	–40	–	+40	
DH5 packet	–40	–	+40	
Drift rate	–20	–	20	kHz/50 μs
<b>Frequency deviation</b>				
Average deviation in payload (sequence used is 00001111)	140	–	175	kHz
Maximum deviation in payload (sequence used is 10101010)	115	–	–	
Channel spacing	–	1	–	MHz

**Note**

11.Meet SIG specification.

Specifications

**Table 23 Bluetooth® LE RF specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sensitivity <sup>[12]</sup>	GFSK, BDR GFSK 0.1% BER 0.1% BER, 1 Mbps	–	–95.0	–	dBm
TX power	N/A	–	4.5	–	
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max <sup>[13]</sup>	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	–	–	%

**Table 24 BLE2 RF specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
RX sensitivity <sup>[14]</sup>	–	–	–90.5	–	dBm
TX power	–	–	5.0	–	

**Notes**

12.Dirty TX is OFF.

13.At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

14.255 packet.

Specifications

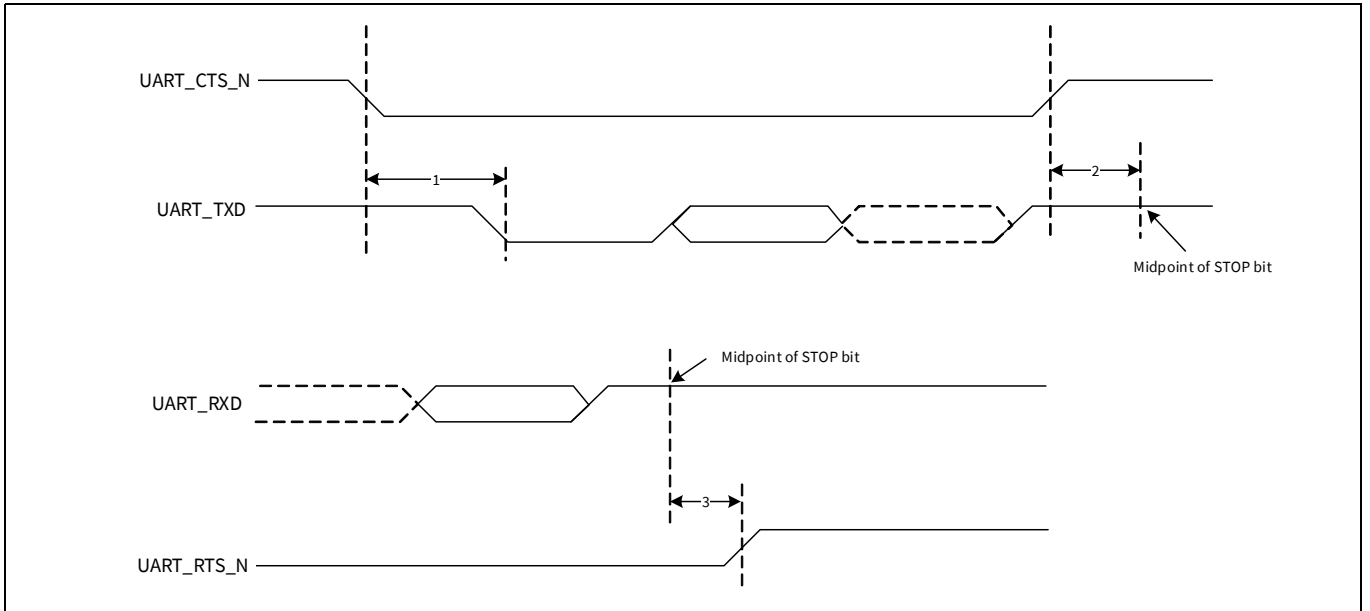
**11.12 Timing and AC characteristics**

In this section, use the numbers listed in the Reference column of each table to interpret the timing diagrams shown in **Figure 11** through **Figure 16**.

**11.12.1 UART timing**

**Table 25** UART timing specifications

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.67	
3	Delay time, midpoint of stop bit to UART_RTS_N HIGH	-	-	1.33	



**Figure 11** UART timing

Specifications

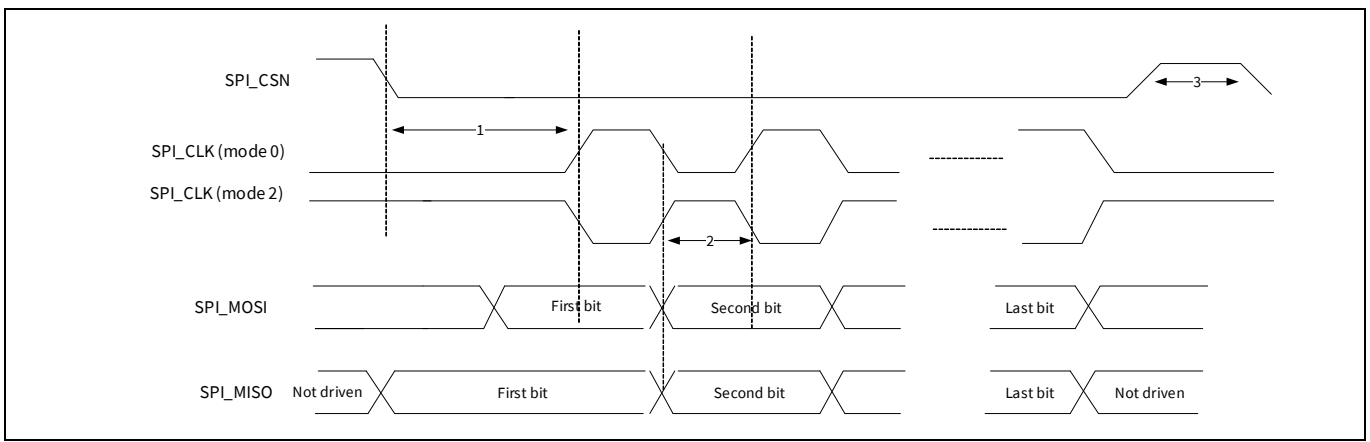
**11.12.2 SPI timing**

The SPI interface can be clocked up to 12 MHz.

**Table 26** and **Figure 12** show the timing requirements when operating in SPI mode 0 and 2.

**Table 26 SPI mode 0 and 2**

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Setup time for MOSI data lines	6	½ SCK	
3	Idle time between subsequent SPI transactions	1 SCK	–	

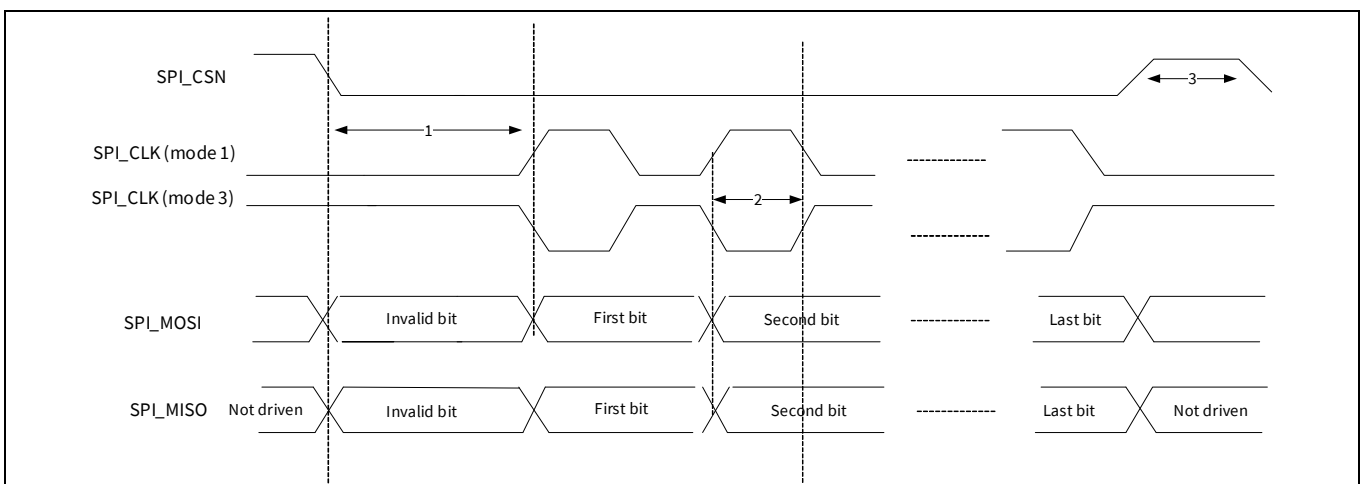


**Figure 12 SPI timing, mode 0 and 2**

**Table 27** and **Figure 13** show the timing requirements when operating in SPI mode 1 and 3.

**Table 27 SPI mode 1 and 3**

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Setup time for MOSI data lines	6	½ SCK	
3	Idle time between subsequent SPI transactions	1 SCK	–	



**Figure 13 SPI timing, mode 1 and 3**

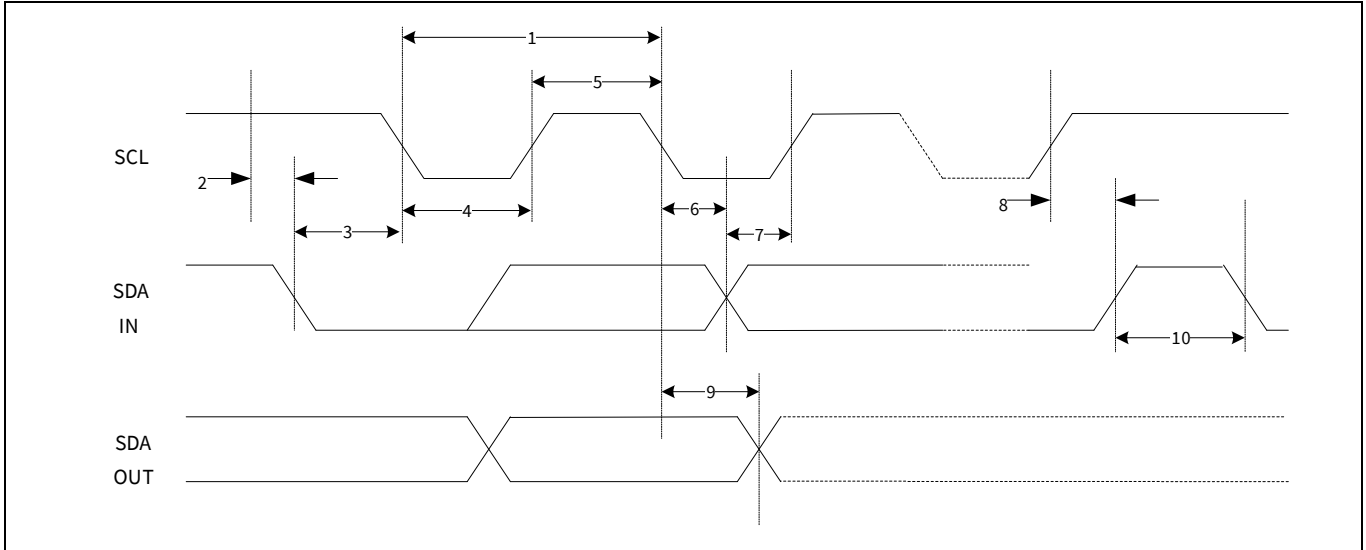
Specifications

**11.12.3 I<sup>2</sup>C interface timing**

The specifications in **Table 28** references **Figure 14**.

**Table 28 I<sup>2</sup>C interface timing specifications (up to 1 MHz)**

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	-	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	-	ns
3	START condition hold time	280	-	
4	Clock low time	650	-	
5	Clock high time	280	-	
6	Data input hold time <sup>[15]</sup>	0	-	
7	Data input setup time	100	-	
8	STOP condition setup time	280	-	
9	Output valid from clock	-	400	
10	Bus free time <sup>[16]</sup>	650	-	



**Figure 14 I<sup>2</sup>C interface timing diagram**

**Notes**

- 15.As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- 16.Time that the CBUS must be free before a new transaction can start.

## Specifications

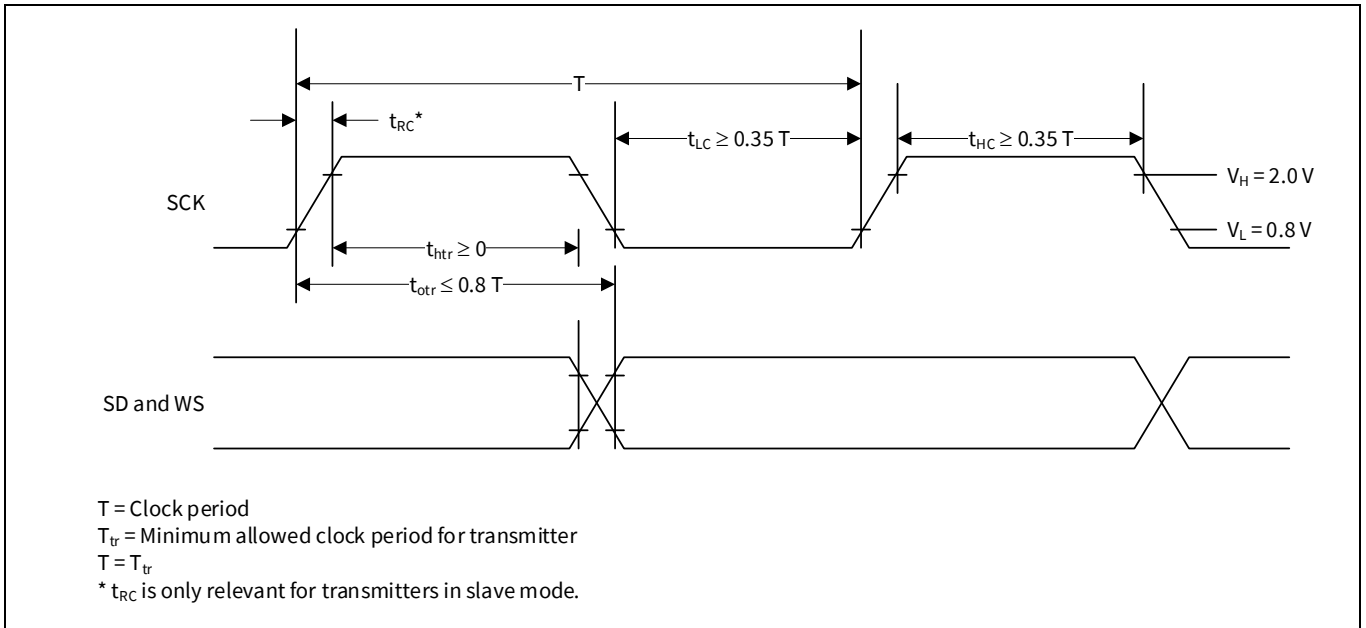
**11.12.4 I<sup>2</sup>S**
**Table 29 Timing for I<sup>2</sup>S transmitters and receivers**

	Transmitter				Receiver				Note
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period $T$	$T_{tr}$	–	–	–	$T_r$	–	–	–	[17]
Master mode: Clock generated by transmitter or receiver									
HIGH $t_{HC}$	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	–	[18]
LOW $t_{LC}$	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	–	[18]
Slave mode: Clock accepted by transmitter or receiver									
HIGH $t_{HC}$	–	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	[17]
LOW $t_{LC}$	–	$0.35 \times T_{tr}$	–	–	–	$0.35 \times T_{tr}$	–	–	[17]
Rise time $t_{RC}$	–	–	$0.15 \times T_{tr}$	–	–	–	–	–	[18]
Transmitter									
Delay $t_{dtr}$	–	–	–	$0.8 \times T$	–	–	–	–	[19]
Hold time $t_{htr}$	0	–	–	–	–	–	–	–	[18]
Receiver									
Setup time $t_{sr}$	–	–	–	–	$0.2 \times T_{tr}$	–	–	–	[20]
Hold time $t_{hr}$	–	–	–	–	$0.2 \times T_{tr}$	–	–	–	[20]

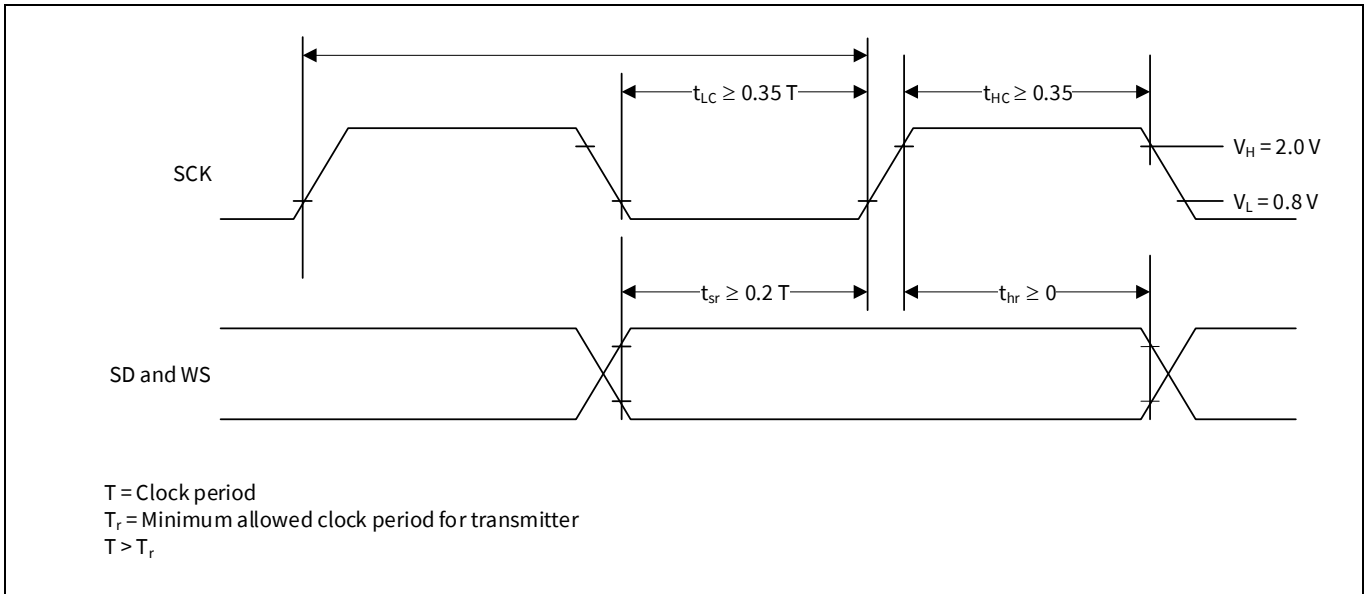
**Notes**

17. The system clock period  $T$  must be greater than  $T_{tr}$  and  $T_r$  because both the transmitter and receiver have to be able to handle the data transfer rate.
18. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason,  $t_{HC}$  and  $t_{LC}$  are specified with respect to  $T$ .
19. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than  $0.35T_r$ , any clock that meets the requirements can be used.
20. Because the delay ( $t_{dtr}$ ) and the maximum transmitter speed (defined by  $T_{tr}$ ) are related, a fast transmitter driven by a slow clock edge can result in  $t_{dtr}$  not exceeding  $t_{RC}$  which means  $t_{htr}$  becomes zero or negative. Therefore, the transmitter has to guarantee that  $t_{htr}$  is greater than or equal to zero, so long as the clock rise-time  $t_{RC}$  is not more than  $t_{RCmax}$ , where  $t_{RCmax}$  is not less than  $0.15T_{tr}$ .
21. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and  $T$ , always giving the receiver sufficient setup time.
22. The data setup and hold time must not be less than the specified receiver setup and hold time.

Specifications



**Figure 15 I<sup>2</sup>S transmitter timing**



**Figure 16 I<sup>2</sup>S receiver timing**



Packaging diagrams

## 12 Packaging diagrams

### 12.1 62-pin FBGA package

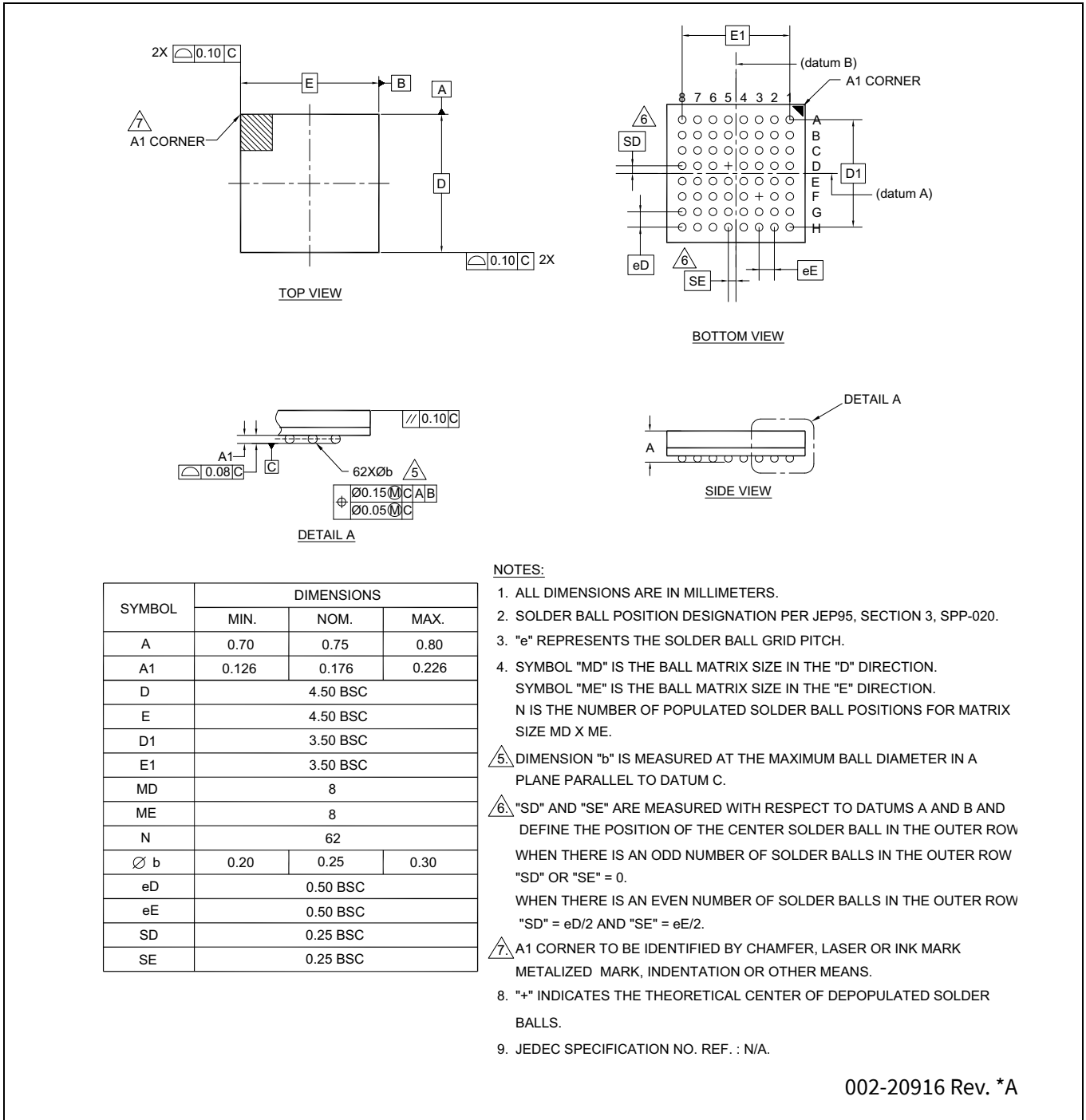


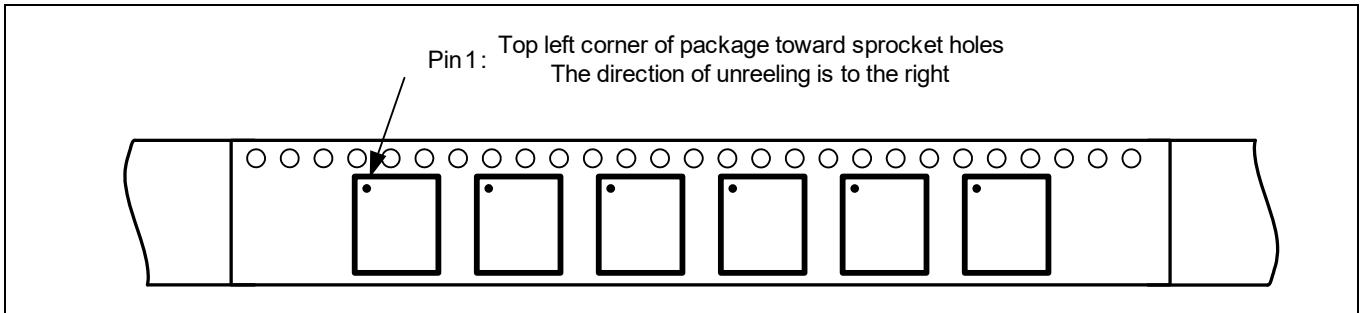
Figure 17 62-ball FBGA (4.5 × 4.5 × 0.8 mm) WDA062/BU62A package outline (PG-VFBGA-62), 002-20916

**12.2 Tape reel and packaging specifications**

**Table 30 CYW20819 62-pin FBGA tape reel specifications**

Parameter	Value
Quantity per reel	5500 parts
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	12 mm
Pocket pitch	8 mm
Sprocket hole pitch	4 mm

The top-left corner of the CYW20819 package is situated near the sprocket holes, as shown in [Figure 18](#).



**Figure 18 Pin 1 orientation**

---

Ordering information

## **13            Ordering information**

**Table 31        Ordering information**

<b>Part number</b>	<b>Package</b>	<b>Ambient operating temperature</b>
CYW20819A1KFBG	4.5 mm × 4.5 mm 62-ball FBGA	-30°C to 85°C

## 14 Acronyms

**Table 32 Acronyms**

<b>Term</b>	<b>Description</b>
ACL	asynchronous connection-less
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
BBC	Bluetooth® baseband core
BDR	basic data rate
BLE	Bluetooth® low energy
BR	basic data rate
CMOS	complementary metal oxide semiconductor
CRC	cyclic redundancy check
ECDSA	elliptic curve digital signature algorithm
ED	erroneous data
EDR	enhanced data rate
EIR	extended inquiry response
ePDS	extended power down sleep
eSCO	extended synchronous connection-oriented
EPR	encryption pause resume
FEC	forward error correction
FPU	floating point unit
GAP	generic access profile
GATT	generic attribute profile
GCI	global coexistence interface
GFSK	Gaussian Frequency Shift Keying
GPIO	general-purpose I/O
HCI	host control interface
HEC	header error control
HID	human-interface device
I2C	inter-integrated circuit
I2S	inter-IC sound bus
IF	intermediate frequency
JTAG	joint test action group
L2CAP	logical link control and adaptation protocol
LC	link control
LCU	link control unit
LDO	low drop out
LE	low energy
LED	light emitting diode

## Acronyms

**Table 32**      **Acronyms** *(continued)*

<b>Term</b>	<b>Description</b>
LHL	lean high land
LMAC	lower MAC
LO	local oscillator
LPO	low power oscillator
LSTO	link supervision time out
MOSI	master out slave in
OEM	original equipment manufacturer
OTP	one-time programmable
OCF	on chip flash
OTA	over-the-air
PA	power amplifier
PBF	packet boundary flag
PCM	pulse code modulation
PDM	pulse density modulation
PDS	power down sleep
PLL	phase locked loop
PMU	power management unit
POR	power-on reset
PWM	pulse width modulation
QFN	quad flat no-lead
QoS	quality of service
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read-only memory
RSSI	receiver signal strength indicator
RTC	real time clock
RX/TX	receive/transmit
SCO	synchronous connection-oriented
SDS	shut down sleep
SECI	serial enhanced coexistence interface
SPI	serial peripheral interface
SSP	secure simple pairing
SSR	sniff subrating
SWD	serial wire debug
TRNG	true random number generator
TSSI	transmit signal strength indicator



---

Acronyms

**Table 32**      **Acronyms** *(continued)*

<b>Term</b>	<b>Description</b>
UART	universal asynchronous receiver/transmitter
WDT	watchdog timer



Revision history

**Revision history**

<b>Document revision</b>	<b>Date</b>	<b>Description of changes</b>
*K	2024-05-08	Release to web.

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**Email:**

[erratum@infineon.com](mailto:erratum@infineon.com)

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