AIROC™ Bluetooth® Low Energy 5.4 MCU

General description

The Infineon AIROC™ CYW20829 is a high-performance, ultra-low-power and "Secure" MCU + Bluetooth® LE platform, purpose-built for IoT applications. It combines a high-performance microcontroller with Bluetooth® LE (5.4) connectivity, high-performance analog-to-digital conversion audio input, I^2S/PCM, CAN, LIN for automotive use cases and other standard communication and timing peripherals. CYW20829 employs high level of integration to minimize external components, reducing the device footprint and costs associated with implementing Bluetooth® Low Energy solutions. AIROC™ CYW20829 is the optimal solution for wireless input devices, remotes, keyboards, joysticks, Bluetooth® Mesh, automotive, asset tracking, and Bluetooth® LE IoT applications that need 10 dBm RF output power such as lighting and home automation.

Features

- **32-bit application core subsystem**
  - 48/96-MHz Arm® Cortex®-M33 CPU with single-cycle multiply and memory protection unit (MPU)
  - ARMv8-M architecture
  - CMOS 40-nm process
  - User-selectable core logic operation at either 1.1 V or 1.0 V
  - Active CPU current slope with 1.1 V core operation
    - Cortex®-M33: 40 µA/MHz
  - Active CPU current slope with 1.0 V core operation
    - Cortex®-M33: 22 µA/MHz
  - Datawire (DMA) controller with 16 channels
  - 32-KB cache for greater XIP performance with lower power
- **Memory subsystem**
  - 256-KB SRAM with power and data retention control
  - OTP eFuse array for security provisioning
- **Bluetooth® Low Energy subsystem**
  - 48-MHz Arm® Cortex®-M33 CPU with 2.4 GHz RF transceiver with 50 Ω antenna drive
  - Digital PHY
  - Link layer engine supporting master and slave modes
  - Programmable TX power: up to 10 dBm
  - RX sensitivity:
    - LE-1 Mbps: -98 dBm
    - LE-2 Mbps: -95 dBm
    - Coded PHY 500 kbps (LE-LR): –101 dBm
    - Coded PHY 125 kbps (LE-LR): –106 dBm
  - 5.2 mA TX (0 dBm), 17.2 mA TX (10 dBm), and 5.6 mA RX (LE 1 Mbps) current with 3.0 V supply and using internal buck converter
  - Link layer engine supports up to 16 connections simultaneously, four are peripheral
  - Angle of Arrival (AoA) and Angle of Departure (AoD)[1]

---

[1] For the end user AoA/AoD solutions like RTLS, Direction Finding, and so on, customers and partners will be required to build or license various system components to realize the final solution.

Features

- **Low-power 1.7 V to 3.6 V operation**
  - Six power modes for fine-grained power management
  - Deep Sleep mode current of 4.5 µA with 64 KB SRAM retention
  - On-chip DC-DC buck converter
- **Flexible clocking options**
  - 8-MHz internal main oscillator (IMO) with ±2% accuracy
  - Ultra-low-power 32 kHz internal low-speed oscillator (ILO)
  - Two oscillators: High-frequency (24 MHz) for radio PLL and low-frequency (32 kHz watch crystal) for LPO
  - 48-MHz low power IHO (internal oscillator)
  - Frequency-locked loop (FLL) for multiplying IMO frequency
  - Integer and fractional peripheral clock dividers
- **Quad SPI (QSPI)/serial memory interface (SMIF)**
  - eXecute-In-Place (XIP) from external quad SPI flash
  - On-the-fly encryption and decryption
  - Support for DDR
  - Supports single, dual, and quad interfaces with throughput up to 384 Mbps
- **Serial communication**
  - Three run-time configurable Serial Communication Blocks (SCBs)
    - First SCB: Configurable as SPI or I^{2}C
    - Second SCB: Configurable as SPI or UART
    - Third SCB: Configurable as I^{2}C or UART
    - Only 2 instances of specific buses (SPI/I2C/UART) are possible among 3 SCBs
- **Audio subsystem**
  - Two pulse density modulation (PDM) channels and one I^{2}S channel with time division multiplexed (TDM) mode
- **Timing and pulse-width modulation**
  - Seven 16-bit and two 32-bit Timer/Counter Pulse-Width Modulator (TCPWM) blocks, for MCU. Multiple PWMs needed for color LEDs
  - PWM supports center-aligned, edge, and pseudo-random modes
- **ADC and MIC**
  - 12b sigma-delta switched cap ADC for audio and DC measurements
- **Up to 32 programmable GPIOs**
  - One I/O port (8 I/Os) enables Boolean operations on GPIO pins; available during system Deep Sleep
  - Programmable drive modes, strengths, and slew rates
  - Two overvoltage-tolerant (OVT) pins
  - Up to six, used for SMIF
- **Security built into platform architecture**
  - ROM-based root of trust via uninterruptible "Secure Boot"
  - Step-wise authentication of execution images
  - Secure execution of code in execute-only mode for protected routines
  - All debug and test ingress paths can be disabled
  - Up to four protection contexts (One available for customer code)

- - Secure debug support via authenticated debug token
  - Encrypted image support for external SMIF memory
- **Cryptography hardware**
  - Hardware Acceleration for symmetric cryptographic methods and hash functions
  - True Random Number Generation (TRNG) function
- **Packages**
  - 56-lead 6 mm x 6 mm

Eclipse IDE for Modustoolbox™ software

Modustoolbox™ software is Infineon's comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code repositories on GitHub. This includes:

- Board support packages (BSPs) aligned with Infineon kits
- Low-level resources, including a hardware abstraction layer (HAL) and peripheral driver library (PDL)
- Middleware enabling industry-leading features such as Bluetooth® Low Energy, and mesh networks
- An extensive set of thoroughly tested code example applications

Note: *The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Infineon MCUs and SoCs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires fine-grained control.*

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a Project Creator, a Library Manager, a BSP Assistant, peripheral and library configurators, as well as the optional Eclipse IDE for the ModusToolbox™, as Figure 1 shows. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software.

Eclipse IDE for Modustoolbox™ software
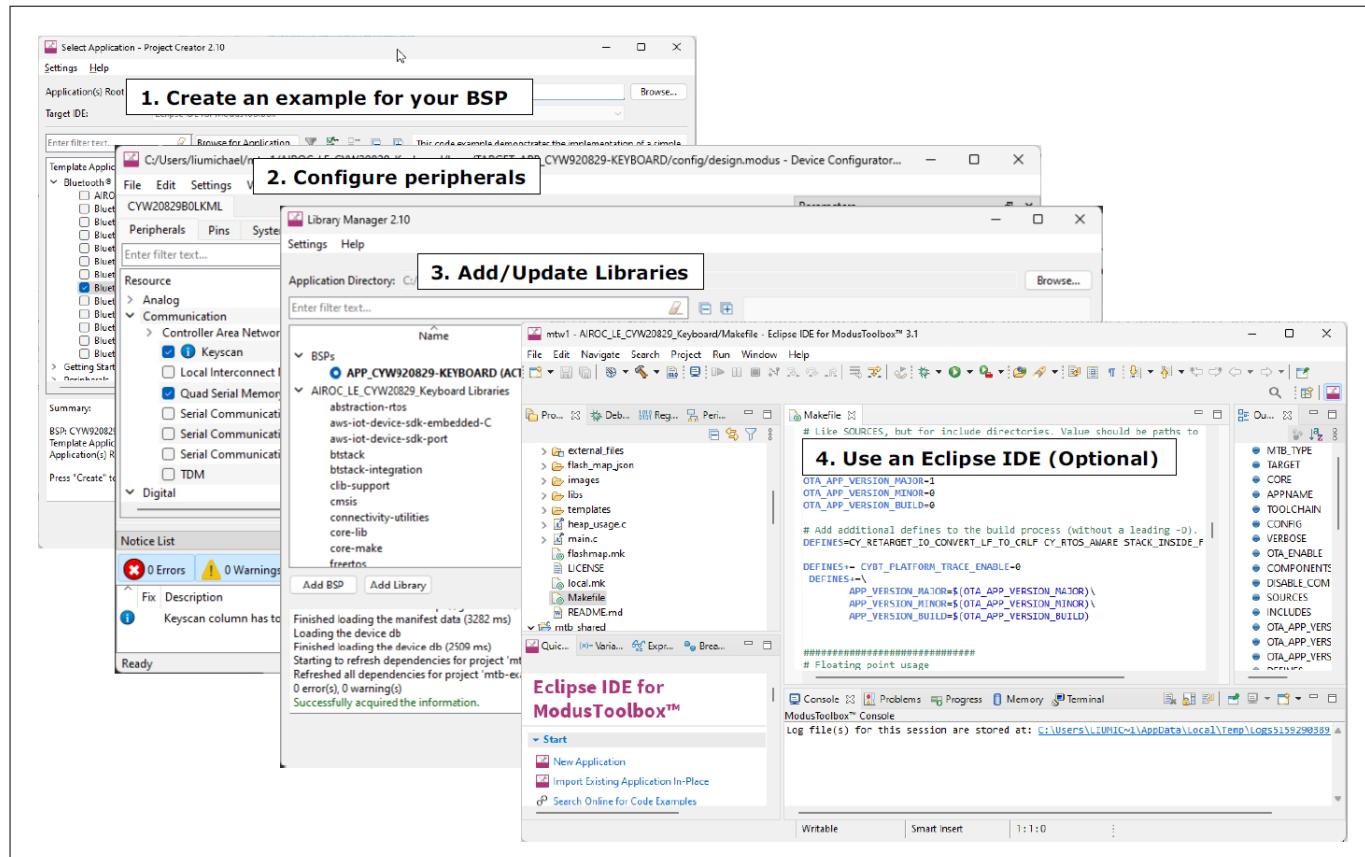
Figure 1 **ModusToolbox™ software tools**

Table of contents

1   Block diagram

Figure 2 shows the major subsystems and a simplified view of their interconnections. The color coding shows the lowest power mode where a block is still functional. For example, the SRAM is functional down to DS-RAM mode. It should also be noted that six SMIF IOs are in addition to the 32 GPIOs listed in Figure 2.
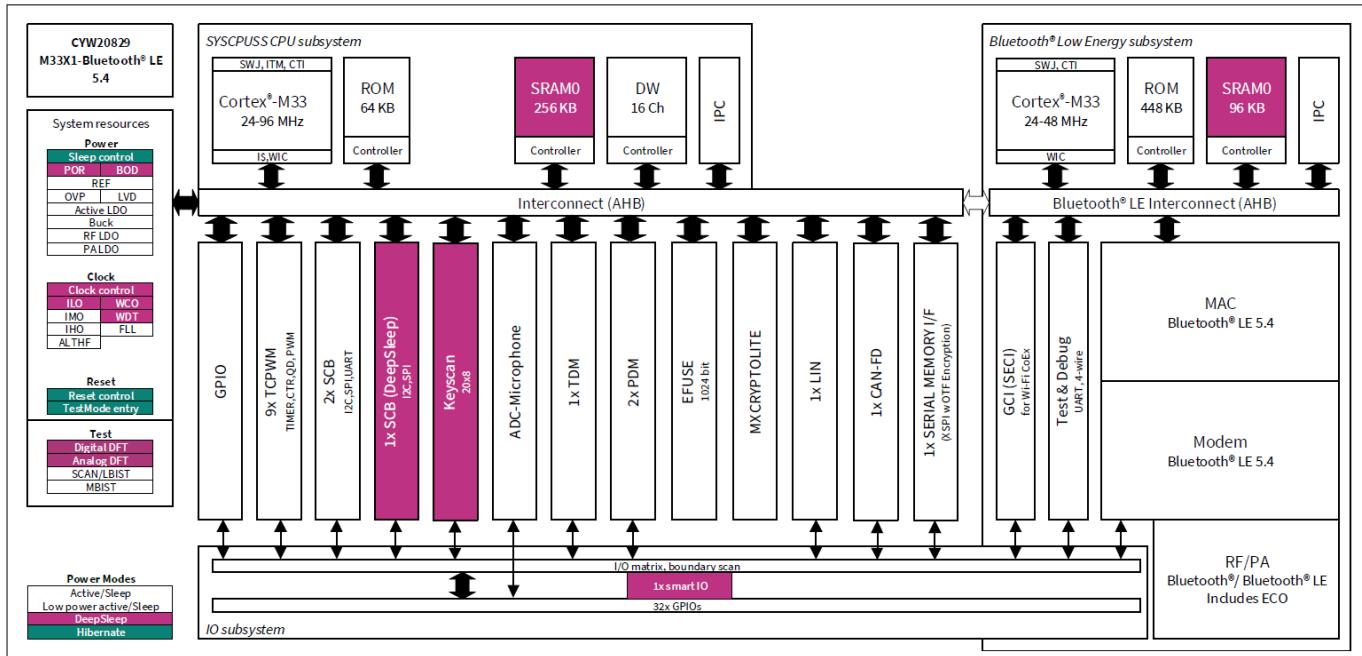
Figure 2   Functional block diagram

AIROC™ CYW20829 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. All device interfaces can be permanently disabled (device security) for applications concerned about attacks due to a maliciously reprogrammed device. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is settable by the user.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The Eclipse IDE for ModusToolbox™ and Integrated Development Environment (IDE) provide fully integrated programming and debug support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, CYW20829 provides a very high level of security.

2 Functional description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in Figure 2. For more detailed information, refer to the following documentation:

- **Board support package (BSP) documentation**

BSPs are available on GitHub. They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example here. This search link finds all currently available BSPs on the Infineon GitHub site.

- **Hardware abstraction layer(HAL) API reference manual**

The Infineon HAL provides a high-level interface to configure and use hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The HAL API Reference provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.

2.1 CPU and memory subsystem

AIROC™ CYW20829 has multiple bus masters, as Figure 2 shows. They are: CPU, datawire, QSPI, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm® AMBA high-performance bus (AHB) arbitration. An interprocessor communication block (IPC) provides communication between the CPU and the Bluetooth® LE sub-system.

2.1.1 CPU

The Cortex®-M33 has single-cycle multiply and a memory protection unit (MPU). It can run at up to 96 MHz in LP mode and 48 MHz in ULP mode. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

Cortex®-M33 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the Armv8-M architecture reference manual).

The main MCU also implements device-level security, safety, and protection features. Cortex®-M33 provides a secure, interruptible boot function. This guarantees that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

The CPU has the following power draw, at V_{DDD} = 3.0 V and using the internal buck regulator.

Table 1   **Active current slope at V_{DDD} = 3.0 V using the internal buck regulator**

System power mode		
CPU	ULP	LP
	22 µA/MHz	40 µA/MHz

The CPU can be selectively placed in Sleep and Deep Sleep power modes as defined by Arm®. The CPU also implements a Deep Sleep RAM (DS-RAM) mode in which almost all the circuits except RAM are powered OFF. Data in RAM is retained to maintain state. Upon exit, the CPU goes through a reset but can use the data in RAM to skip software initialization.

The CPU also has nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

CYW20829 has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the "host") communicates with the DAP through the device serial wire

debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in the CPU.

CPU debug and trace features are as follows:

- Six hardware breakpoints and four watchpoints, serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin

2.1.2　Interrupts

The CPU has interrupt request lines (IRQ), with the interrupt source 'n' directly connected to IRQn.

Each interrupt supports eight configurable priority levels. One system interrupt can be mapped to the CPU non-maskable interrupts (NMI). Multiple interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC.

2.1.3　Datawire

Datawire is a light weight DMA controller with 16 channels, which support CPU-independent accesses to memory and peripherals. The descriptors for the channels are in SRAM and the number of descriptors is limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination.

2.1.4　Cryptography accelerator (Cryptolite)

A combination of HW and SW is able to support several cryptographic functions. Specifically it supports the following functions:

- Encryption/decryption
  - AES-128 hardware accelerator with following supported modes:
    - Electronic Code Book (ECB)
    - Cipher Block Chaining (CBC)
    - Cipher Feedback (CFB)
    - Output Feedback (OFB)
    - Counter (CTR)
- Hashing
  - Secure Hash Algorithm (SHA-256) hardware accelerator
- Message Authentication Functions (MAC)
  - Hashed Message Authentication Code (HMAC) acceleration using SHA-256 hardware
- True Random Number Generator (TRNG)
- Vector unit hardware accelerator
  - Digital Signature Verification using RSA
  - Digital Signature Verification using ECDSA

2.1.5　Protection units

CYW20829 has multiple types of protection to control erroneous or unauthorized access to memory and peripheral registers.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secure/non-secure, and protection context.

Protection units are configured at "Secure Boot" to control access privileges and rights for bus masters and peripherals. Up to eight protection contexts ("Secure Boot" is in protection context 0) allow access privileges for memory and system resources to be set by the "Secure Boot" process per protection context by bus master and code privilege level. Multiple protection contexts are available.

2.1.6   AES-128

AES-128 component to accelerate block cipher functionality. This functionality supports forward encryption of a single 128 bit block with a 128 bit key. SHA-256 component to accelerate hash functionality. This component supports message schedule calculation for a 512-bit message chunk and processing of a 512-bit message chunk.

2.1.7   Vector unit (VU)

VU component to accelerate asymmetric key cryptography (for example, RSA and ECC). This component supports large integer multiplication, addition, and so on. TRNG component based on a set of ring oscillators.

The TRNG includes a HW health monitor.

2.1.8   Controller area network flexible data-rate (CAN FD)

CYW20829 supports the CAN FD controller that supports one CAN FD channel. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard; an ISO 16845:2015 certificate is available. It also implements the time-triggered CAN (TTCAN) protocol specified in ISO 11898-4 (TTCAN protocol levels 1 and 2) completely in hardware. All functions concerning the handling of messages are implemented by the RX and TX handlers. The RX handler manages message acceptance filtering, transfer of received messages from the CAN core to a message RAM, and provides receive-message status. The TX handler is responsible for the transfer of transmit messages from the message RAM to the CAN core, and provides transmit-message status.

2.1.9   Local interconnect network (LIN)

CYW20829 contains a LIN channel. Each channel supports transmission/reception of data following the LIN protocol according to ISO standard 17987. Each LIN channel connects to an external transceiver through a 3-pin interface (including an enable function) and supports master and slave functionality. Each block also supports classic and enhanced checksum, along with break detection during message reception and wake-up signaling. Break detection, sync field, checksum calculations, and error interrupts are handled in hardware.

2.1.10   Real time clock (RTC)

- Year/Month/Date, Day-of-week, Hour: Minute: Second fields
- 12 and 24 hour formats
- Automatic leap-year correction

2.1.11   Memory

CYW20829 contains the SRAM, ROM, and eFuse memory blocks.

- **SRAM**: CYW20829 has 256-KB of SRAM. Power control and retention granularity is 64-KB blocks allowing the user to control the amount of memory retained in Deep Sleep. Memory is not retained in Hibernate mode.

2 Functional description

- **ROM**: The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code (ROM Boot) for several system functions. The ROM contains, primarily device initialization and security. ROM code is executed, in protection context 0.
- **eFuse**: A one-time programmable (OTP) eFuse array consists of 1024 bits, which are reserved for system use such as Die ID, Device ID, initial trim settings, device life cycle, and security settings. Some of the bits are available for storing security key information and hash values and can be programmed by the user for device security.

Each fuse is individually programmed; once programmed (or "blown"), its state cannot be changed. Blowing a fuse transitions it from the default state of '0' to '1'. To program an eFuse, VDDIO1 must be at 2.5 V ±5%.

Because blowing an eFuse is an irreversible process, programming is recommended only in mass production under controlled factory conditions by Infineon provided provisioning tools.

2.1.12   Boot code

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Device trim setting (calibration)
- Setting the device protection units
- Setting device access restrictions for secure life cycle states
- Configures the Debug Access Port
- In secure life cycle supports secure debug via authenticated debug token
- Configures the SMIF for external flash access
- In secure life cycle validates first user code in external flash by checking its digital signature. Supports OTF decryption of encrypted images in external flash
- Copies the application bootstrap from the external flash to SRAM and jumps to the ROM. It cannot be changed and acts as the Root of Trust in a secure system

It should also be noted that the ROM code sets the system clock to 48 MHz IHO source.

2.1.13   Memory map

The 32-bit (4 GB) address space is divided into the regions shown in Table 3. Note that code can be executed from the Code, and Internal RAM or External flash.

Table 2   Address map

Address range	Name	Use
0x0000 0000 – 0x1FFF FFFF	Code	Program code region. It includes the exception vector table, which starts at address 0
0x2000 0000 – 0x3FFF FFFF	SRAM	Data region
0x4000 0000 – 0x5FFF FFFF	Peripheral	All peripheral registers. Code cannot be executed from this region. Bit-band in this region is not supported
0x6000 0000 – 0x8FFF FFFF	External NVM	SMIF/Quad SPI, (see the QSPI interface serial memory interface (SMIF). Code can be executed from this region
0xA000 0000 – 0xDFFF FFFF	External Device	Not used
0xE000 0000 – 0xE00F FFFF	Private Peripheral Bus	Provides access to peripheral registers within the CPU core
0xE010 0A000 – 0xFFFF FFFF	Device	Device-specific system registers

2 Functional description

The device memory map is shown in Table 3.

Table 3   **Internal memory address map**

Address range	Memory type	Size
0x0000 0000 – 0x0001 0000	ROM	64 KB
0x2000 0000 - 0x 2004 0000	SRAM	Up to 256 KB

3 System resources

3.1 Power system

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brownout detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The V_{DDD} supply (1.7 V to 3.6 V) powers an on-chip buck regulator which offers a selectable (1.0 V or 1.16 V) core operating voltage (VCCD). The selection lets users choose between two system power modes:

• System Low Power (LP) operates VCCD at 1.1 V and offers high performance, with no restrictions on device configuration

• System Ultra Low Power (ULP) operates VCCD at 1.0 V for exceptional low power, but imposes limitations on clock speeds

The Bluetooth® radio requires 1.1 V for operation. Bluetooth® system may override user core voltage selection when the radio is turned on. System voltage will return to the user selected value automatically once Bluetooth® radio activity is completed. Refer to Power supply considerations for more details.

3.1.1 Power modes

CYW20829 can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the relevant application note,

Power modes supported by CYW20829, in the order of decreasing power consumption, are:

• System Low-power (LP) - All peripherals and CPU power modes are available at maximum speed

• System Ultra Low-power (ULP) - All peripherals and CPU power modes are available, but with limited speed

• CPU Active - CPU is executing code in system LP or ULP mode

• CPU Sleep - CPU code execution is halted in system LP or ULP mode

• CPU Deep Sleep - CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode

• System Deep Sleep - only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode

• System Hibernate - Device and I/O states are frozen and the device resets on wakeup. Multiple sources available to wake up from this mode, including RTC, P0.5 and P1.4

• Deep Sleep RAM - only RAM and IO states are retained. All system activity except for select low power peripherals ceases until system exits from this state. The CPU resets upon exit but can skip software initialization since RAM is retained

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). System LP, ULP, Deep Sleep, Deep Sleep RAM and Hibernate modes are additional low-power modes supported by the CYW20829.

3.1.2 CYW20829 clock system

CYW20829 clock system consists of a combination of oscillators, external clock, and frequency-locked loop. Specifically, the following:

• Internal main oscillator (IMO)

3 System resources

- Internal low-speed oscillator (ILO)
- Watch crystal oscillator (WCO)
- System 24 MHz crystal oscillator
- External clock input
- One frequency-locked loop (FLL)
- Internal high-speed oscillator (IHO)

Clocks may be buffered and brought out to a pin on a smart I/O port.

Table 4 shows the mapping of port and associated clock group mapped to peripherals.

Table 4   Mapping of clock groups to peripherals

PCLK group	Root clock (clk_hf)	Peripherals	Frequency		Description
			LP (1.1 V Typ)	ULP (1.0 V Typ)	
0	clk_hf0	CPU Trace	24 MHz	24 MHz	-
1	clk_hf1	SCB	96 MHz	48 MHz	Async peripherals: Strobe signals are driven through dividers; Interface clock is generated inside the peripheral with the main group clock
		TCPWM			
		LIN			
		CANFD			
		SMARTIO			
2	clk_hf0	SMIF	96 MHz	48 MHz	Direct connection pass through from clk_hf. This clock is not used for interface clock, rather it is used for the MMIO clocks of SMIF, BTSS and CRYPTO. BTSS uses this clock for Master and Slave AHB/MMIO transactions, and SMIF also uses this clock for FAST/SLOW clocks
		BTSS			
		CRYPTO			
3	clk_hf1	PDM	96 MHz	48 MHz	Uses PERI ACLK with default div by 2 option, required interface frequencies are obtained by further division inside the peripheral
		TDM			
4	clk_hf2	BTSS	48 MHz	48 MHz	RPU clock for BTSS
5	clk_hf3	ADCMIC	24 MHz	24 MHz	Direct connection for ADCMIC, main source of clk_hf3 is clk_althf which is the BTSS ECO clock
6	clk_hf1	SMIF	96 MHz	48 MHz	Direct connection for SMIF and SMARTIO peripherals. This clock is an interface clocks for these peripherals

3.1.3   Internal main oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed during testing to achieve the specified accuracy.

The IMO default frequency is 8 MHz and tolerance is ±2%.

3 System resources

3.1.4   Internal low-speed oscillator (ILO)

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes.

3.1.5   Precision internal low-speed oscillator (PILO)

The PILO is a precision low-power oscillator running at 32 kHz. It is factory calibrated to meet Bluetooth® Low Energy requirements. Like the ILO, it can operate in all power modes.
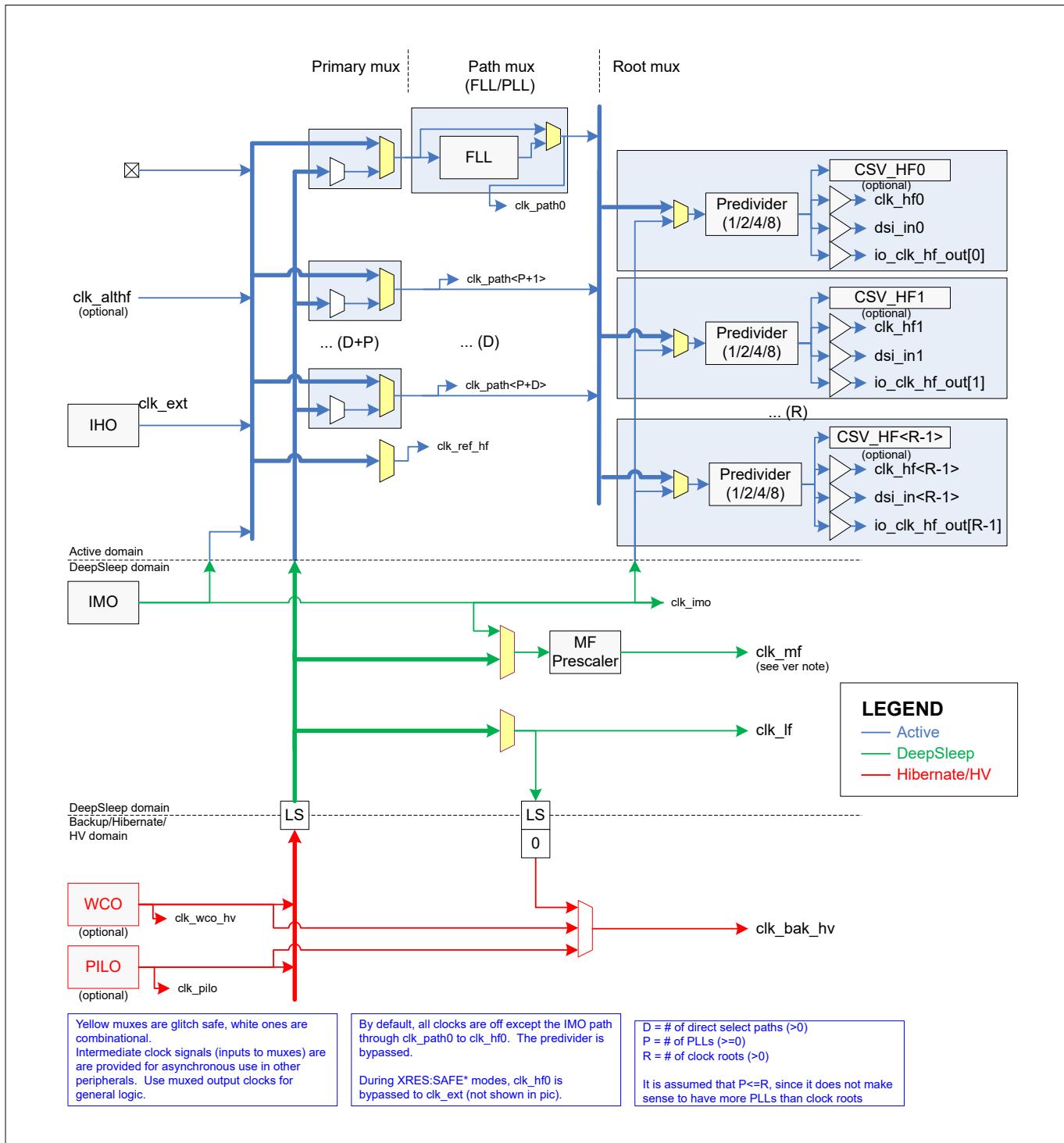
Figure 3   CYW20829 clocking diagram with corresponding oscillators

Note: *Using PILO as the ILO clock source will result in longer boot time.*

3.1.6   External crystal oscillators (ECO)

Figure 4 shows all of the external crystal oscillator circuits for CYW20829. The component values shown are typical; check the ECO specifications for the crystal values, and the crystal datasheet for the load capacitor values. The ECO and WCO require balanced external load capacitors. For more information, see the HW design guidelines. Note that its performance is affected by GPIO switching noise.
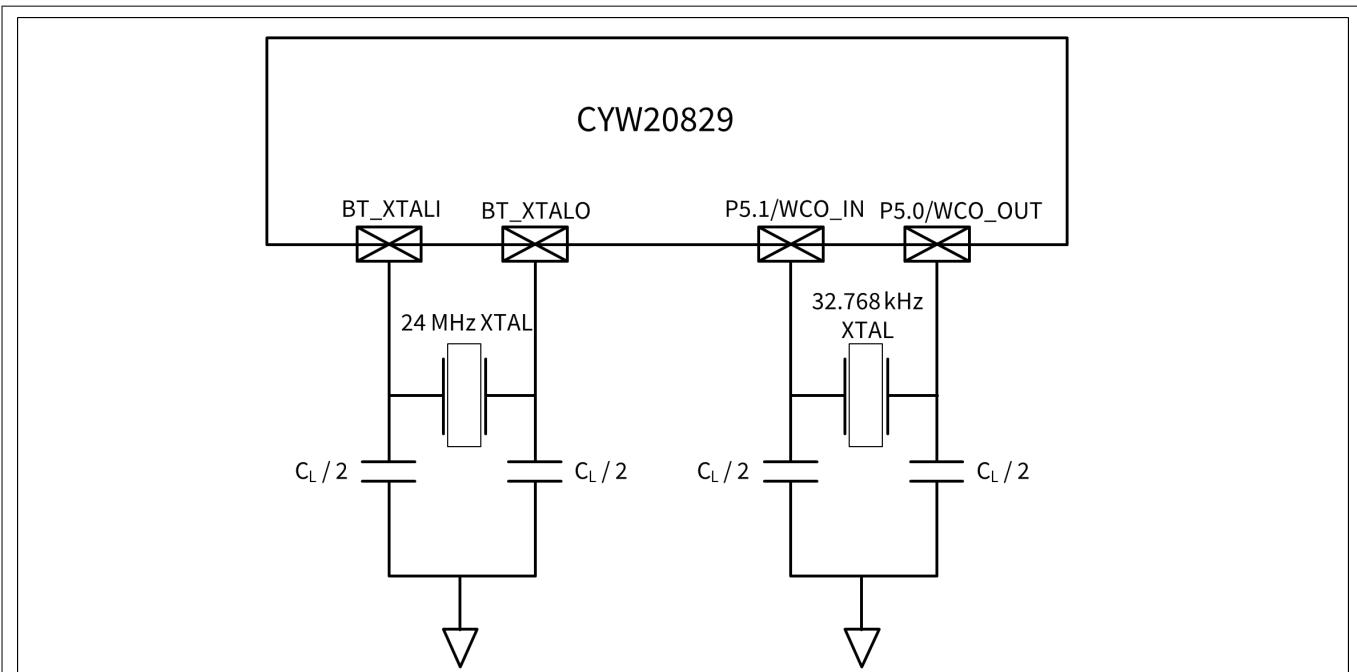
Figure 4   External oscillator

Figure 4   External oscillator

3.1.7   Watchdog timers (WDT, MCWDT)

CYW20829 has one WDT and two multi-counter WDTs (MCWDTs). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can do interrupt/wakeup generation in system LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can do periodic interrupt/wakeup generation in system LP/ULP and Deep Sleep power modes.

3.1.8   Clock dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are one or more:

•   8-bit clock dividers

•   16-bit integer clock dividers

•   16.5-bit fractional clock dividers

•   24.5-bit fractional clock divider

3.1.9 Trigger routing

CYW20829 contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called "one-to-one triggers", which connect a specific source to a destination. The user can enable or disable the route.

3.1.10 Reset

CYW20829 can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DDD} and generate a reset if V_{DDD} falls below the minimum required logic operating voltage
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active LOW. It can be connected either to a pull-up resistor to V_{DDD}, or to an active drive circuit, as Figure 5 shows. If a pull-up resistor is used, select its value to minimize current draw when the pin is pulled LOW; 10 kΩ is typical
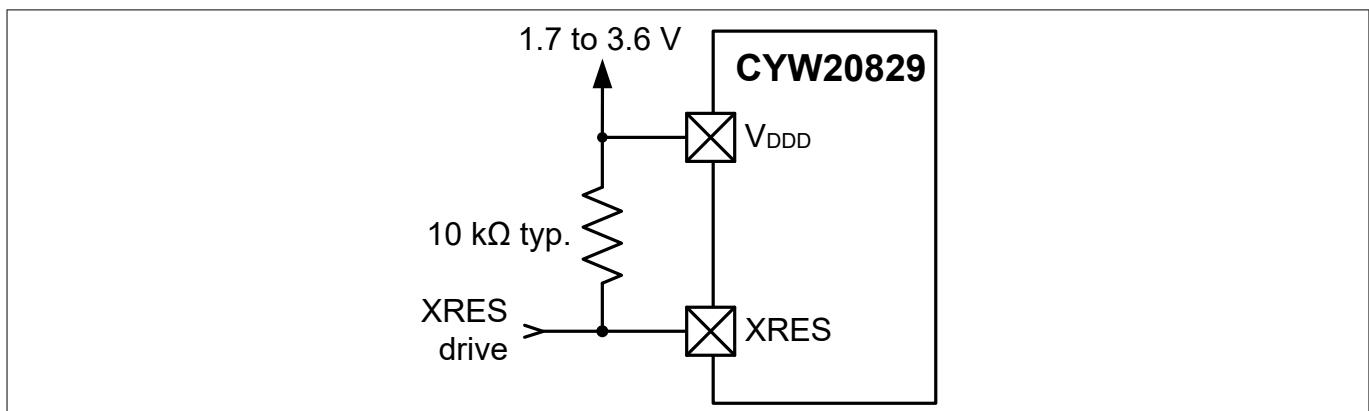
Figure 5   **XRES connection diagram**

- Watchdog Timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period
- Software-initiated reset to reset the device on demand using firmware
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code
- Hibernate wakeup reset to bring the device out of the system Hibernate low-power mode

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

3.2 Bluetooth® LE radio and subsystem

CYW20829 incorporates a Bluetooth® 5.4 LE subsystem (BLESS) that contains the physical layer (PHY) and link layer (LL) engines with an embedded security engine. The Bluetooth® LE SS supports all Bluetooth® LE 5.4 features including LE 2 Mbps, LE Long Range, LE Advertising Extensions, LE Isochronous Channels, Periodic Advertising with Responses (PAwR), Encrypted Advertising Data, LE GATT Security Levels Characteristic and Advertising Coding Selection. Infineon also provides extensive driver library and middleware support for Bluetooth® LE; see Eclipse IDE for Modustoolbox™ software.

The physical layer consists of the digital PHY and the RF transceiver that transmits and receives Gaussian frequency shift keying (GFSK) packets at 1 or 2 Mbps over a 2.4 GHz ISM band, The device also supports Bluetooth® LE long range, both 500 and 125 kbps speeds.

The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50 Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it through the antenna.

3.3 Programmable analog-to-digital converter (ADC)

3.3.1 Sigma delta ADC

The ADC block is a single switched-cap Σ-Δ ADC core for audio and DC measurement. It operates at the 12-MHz clock rate and has 32 DC input channels, including eight GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC.

One of three internal references may be used for the ADC reference voltage: VDDA, VDDA/2, and an analog reference (AREF). AREF is nominally 1.2 V, trimmed to ±1%.

3.4 Programmable digital

- System Deep Sleep operation
- Asynchronous or synchronous (clocked) operation
- Can be synchronous or asynchronous

3.5 Fixed-function digital

3.5.1 Timer/counter/pulse-width modulator (TCPWM) block

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes
- Clock pre-scaling (division by 1, 2, 4,....64, 128)
- Double buffering of compare/capture and period values• Underflow, overflow, and capture/compare output signals

- Supports interrupt on:
    - Terminal count - Depends on the mode; typically occurs on overflow or underflow
    - Capture/compare - The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Two 32-bit TCPWMs
- Seven 16-bit TCPWMs

3.5.2 Serial communication blocks (SCB)

- This product line has three SCBs:
    - First SCB: Configurable as SPI or I^{2}C
    - Second SCB: Configurable as SPI or UART
    - Third SCB: Configurable as I^{2}C or UART
- One SCB (SCB #0) can operate in system Deep Sleep mode with an external clock; this SCB can be either SPI slave or I^{2}C slave
- **I^{2}C mode:** The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI2C, which creates a mailbox address range and effectively reduces I^{2}C communication to reading from and writing to an array in the memory. The SCB supports a 256-byte FIFO for receive and transmit

The I^{2}C peripheral is compatible with I^{2}C standard-mode, Fast Mode, and Fast Mode Plus devices. The I^{2}C bus I/O is implemented with GPIO in open-drain modes.

- **UART mode:** This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO 7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated
- **SPI mode:** The SPI mode supports full SPI, Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and Microwire (half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with a 4-MHz clock

3.5.3 QSPI interface serial memory interface (SMIF)

A serial memory interface is provided, running at up to 48 MHz. It supports single, dual and quad SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute-in-Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers

In XIP mode, the external memory is mapped into the CYW20829 internal address space, enabling code execution directly from the external memory. To improve performance, a 32 KB cache is included. XIP mode also supports AES-128 based on-the-fly encryption and decryption, enabling secure storage and access of code and data in the external memory.

3.6 GPIO

CYW20829 has up to 32 GPIOs, which implement:

- • Eight drive strength modes:
  - Analog input mode (input and output buffers disabled) on some IOs
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
  - Hold mode for latching previous state (used for retaining the I/O state in system Hibernate and deep sleep mode)
  - Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to eight pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 4 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than V_{DDD}. OVT pins are commonly used with I^2C, to allow powering the chip OFF while maintaining a physical connection to an operating I^2C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see Electrical specifications.

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

In order to get the best performance, the following frequency and drive mode constraints may be applied. The values (refer to Table 5) represent drive strengths.

Table 5 **DRIVE_SEL values**

Ports	Maximum frequency	Drive strength for V_{DDD} < 2.7 V	Drive strength for V_{DDD} > 2.7 V
Ports 0, 1	8 MHz	Up to 4 mA	Up to 8 mA
Ports 2 to 5	16 MHz; 24 MHz for SPI	Up to 4 mA	Up to 8 mA

3.7 Special-function peripherals

3.7.1 Audio subsystem

This subsystem consists of the following hardware blocks:

- One inter-IC sound (I^2S) interface
- Two pulse-density modulation (PDM) to pulse-code modulation (PCM) decoder channels

The I^2S interface implements two independent hardware FIFO buffers - TX and RX, which can operate in master or slave mode. The following features are supported:

3 System resources

- Multiple data formats - I^{2}S, left-justified, Time Division Multiplexed (TDM) mode A, and TDM mode B
- Programmable channel/word lengths - 8/16/18/20/24/32 bits
- Internal/external clock operation. Up to 192 ksps
- Interrupt mask events - trigger, not empty, full, overflow, underflow, watchdog
- Configurable FIFO trigger level with datawire support

The I^{2}S interface is commonly used to connect with audio codecs, simple DACs, and digital microphones. The PDM-to-PCM decoder implements a single hardware Rx FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length - 16/18/20/24 bits
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksps
- Programmable high-pass filter gain
- Interrupt mask events - not empty, overflow, trigger, underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM data line.

4 Pinouts

Table 6   **Packages and pin information**

Pin name	Pin number	I/O	Power domain	Description
	56-lead			
Microphone				
MIC_P	54	I	V_{DDA}	Microphone positive input
MIC_N	55			Microphone negative input
MIC_BIAS	53	O		Microphone bias supply
Onboard switching regulator and LDOs				
V_{DDQ}	15	I	-	External supply to PMU analog
V_{CC_BUCK}	17		-	External supply to switching regulator
LX_BUCK	16	O	-	Switching regulator output
V_{CCD}	18		-	Digital LDO output
V_{CCI}	19	I	-	RF and digital LDO input
Baseband supply				
V_{DDIO_0}	42	I	V_{DDIO_0}	Supply for GPIO ports
V_{DDIO_1}	52		V_{DDIO_1}	Supply for GPIO ports and eFuse programming. See Table 9 for eFuse programming requirements.
V_{DDIO_A}	7		V_{DDIO_A}	Supply for analog GPIO ports
V_{DDA}	56		V_{DDA}	Analog power supply voltage
RF power supply				
V_{CCRF}	20	O	-	RFLDO output
V_{DDD}	22	I	-	PALDO and sub-system resources supply
V_{CCPA_0}	21	O	-	PALDO output
BT_VCOVDD	28	I	BT_VCOVDD	VCO supply
BT_LNAVDD	26		BT_LNAVDD	LNA supply
BT_IFVDD	27		BT_IFVDD	IFPLL power supply
BT_PLLVDD	29		BT_PLLVDD	RFPLL and crystal oscillator supply
BT_PAVDD	24		BT_PAVDD	Internal PA supply
Radio I/O				
BT_RF	25	I/O	BT_RF	RF antenna port
Crystal				
BT_XTALI	30	I	BT_PLLVDD	Crystal oscillator input. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent.

(table continues...)

4 Pinouts

Table 6 **(continued) Packages and pin information**

Pin name	Pin number 56-lead	I/O	Power domain	Description
BT_XTALO	31	O		Crystal oscillator output
GPIO				
P0.0	32	I/O	V_{DDIO}	General input and output port. See Table 7 for alternate functions. P0.5 and P1.4 can be used as the wake source for hibernate mode
P0.1	33			
P0.2	34			
P0.3	35			
P0.4	36			
P0.5	37			
P1.0	38			
P1.1	39			
P1.2	40			
P1.3	41			
P1.4	43			
P1.5	44			
P1.6	45			
P2.0	46			
P2.1	47			
P2.2	48			
P2.3	49			
P2.4	50			
P2.5	51			
P3.0	1			
P3.1	2			
P3.2	3			
P3.3	4			
P3.4	5			
P3.5	6			
P3.6	8			
P3.7	9			
P4.0	13			
P4.1	14			
P5.0/WCO_OUT	10			

(table continues…)

4 Pinouts

Table 6 **(continued) Packages and pin information**

Pin name	Pin number	I/O	Power domain	Description
	56-lead			
P5.1/WCO_IN	11			
P5.2	12			
XRES	23	I		Active-low system reset without internal pull-up resistor
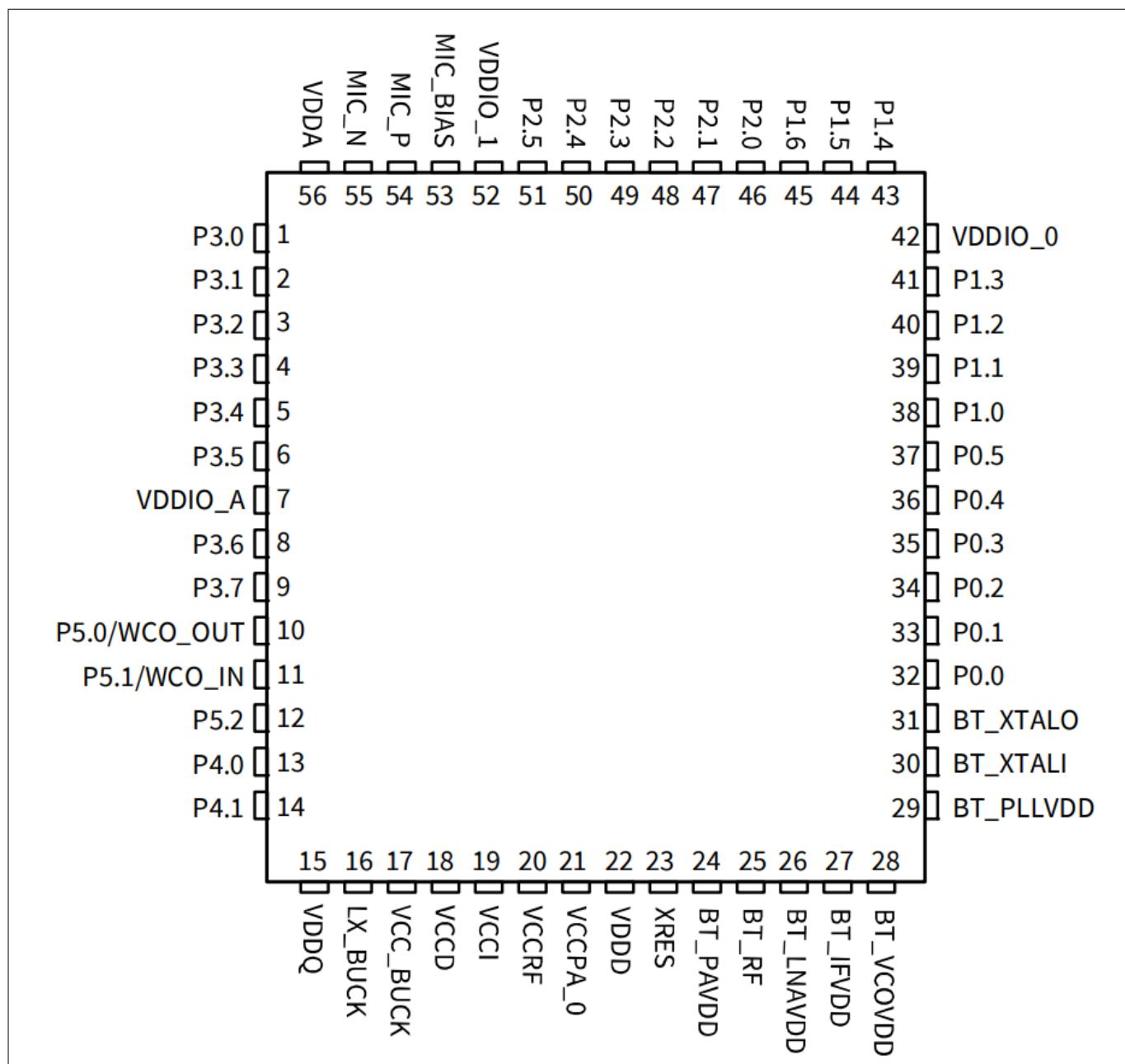
Figure 6 **Device pinout for 56-lead package**

Each port pin has multiple alternate functions. These are defined in Table 7.

4 Pinouts

Table 7   **Multiple alternate functions**[1]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P0.0	-	tcpwm[0].line_compl[0]:3	tcpwm[0].line_compl[262]:0	-	-	-	-	-	pdm.pdm_clk[1]:0	-	-	tdm.tdm_tx_mck[0]:0	tdm.tdm_rx_mck[0]:0	-	smif.spihb_select1	keyscan.ks_col[2]	-	-	scb[0].spi_select1:0	-
P0.1	-	tcpwm[0].line[1]:3	tcpwm[0].line[256]:1	-	-	-	-	-	pdm.pdm_data[1]:0	-	-	tdm.tdm_tx_sck[0]:0	-	-	-	keyscan.ks_col[3]	-	-	scb[0].spi_select2:0	-
P0.2	-	tcpwm[0].line_compl[1]:3	tcpwm[0].line_compl[256]:1	-	-	-	-	-	-	peri.tr_io_input[4]:0	-	tdm.tdm_tx_fsync[0]:0	-	-	-	keyscan.ks_col[11]	scb[0].i2c_scl:0	-	scb[0].spi_mosi:0	-
P0.3	-	tcpwm[0].line[0]:4	tcpwm[0].line[257]:1	-	-	-	-	scb[1].spi_select3:0	-	-	-	tdm.tdm_tx_sd[0]:0	-	-	-	keyscan.ks_col[12]	scb[0].i2c_sda:0	-	scb[0].spi_miso:0	-

(table continues…)

4 Pinouts

Table 7 (continued) Multiple alternate functions[1]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P0.4	-	tcpwm[0].line_compl[0]:4	tcpwm[0].line_compl[257]:1	srss.ext_clk:0	cpuss.trace_data[3]:1	-	-	scb[1].spi_select2:0	-	peri.tr_io_input[0]:0		tdm.tdm_rx_sck[0]:0	-	-	-	keyscan.ks_row[0]	-	-	scb[0].spi_clk:0	-
P0.5	-	tcpwm[0].line[1]:4	tcpwm[0].line[258]:1		cpuss.trace_data[2]:1	-	-	scb[1].spi_select1:0	-	peri.tr_io_input[1]:0		tdm.tdm_rx_fsync[0]:0	-	-	smif.spihb_select1	keyscan.ks_row[1]	-	-	scb[0].spi_select0:0	-
P1.0	-	tcpwm[0].line_compl[1]:4	tcpwm[0].line_compl[258]:1	-	cpuss.trace_data[1]:1	scb[1].uart_cts:0	-	scb[1].spi_select0:0	-	-	peri.tr_io_output[0]:0	tdm.tdm_rx_sd[0]:0	-	-	-	keyscan.ks_row[2]	-	cpuss.swj_swo_tdo	-	-
P1.1	-	tcpwm[0].line[0]:5	tcpwm[0].line[259]:1	-	cpuss.trace_data[0]:1	scb[1].uart_rts:0	-	scb[1].spi_clk:0	-	-	peri.tr_io_output[1]:0	-	-	-	-	keyscan.ks_row[3]	-	cpuss.swj_swdoe_tdi	-	-

(table continues...)

4 Pinouts

Table 7 **(continued) Multiple alternate functions[1]**

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P1.2	-	tcpwm[0].line_compl[0]:5	tcpwm[0].line_compl[259]:1	-	cpuss.trace_clock:1	scb[11].uart_rx:0	scb[2].i2c_scl:1	scb[1].spi_mosi:0	-	peri.tr_io_input[2]:0	-	-	-	-	-	keyscan.ks_row[4]	-	cpuss.swj_swdio_tms	-	-
P1.3	-	tcpwm[0].line[1]:5	tcpwm[0].line[260]:1	-	-	scb[11].uart_tx:0	scb[2].i2c_sda:1	scb[1].spi_miso:0		peri.tr_io_input[3]:0	-	-	-	-	-	keyscan.ks_row[5]	-	cpuss.clk_swj_swclk_tclk	-	-
P1.4	-	tcpwm[0].line_compl[1]:5	tcpwm[0].line_compl[260]:1	-	-	-	-	-	-	-	lin[0].lin_en[1]:0	-	-	-	-	keyscan.ks_col[4]	-	-	-	-
P1.5	-	tcpwm[0].line[0]:6	tcpwm[0].line[261]:1	-	-	-	-	-	-	-	lin[0].lin_rx[1]:0	-	-	-	-	keyscan.ks_col[5]	-	-	-	-

(table continues...)

4 Pinouts

Table 7 **(continued) Multiple alternate functions[1)]**

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P1.6	-	tcpwm[0].line_compl[0]:6	tcpwm[0].line_compl[261]:1	-	-	-	-	-	-	-	lin[0].lin_tx[1]:0	-	-	-	-	keyscan.ks_col[6]	srss.cal_wave	-	-	-
P2.0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	smif.spihb_select0	-	-	-	-	-
P2.1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	smif.spihb_data3	-	-	-	-	-
P2.2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	smif.spihb_data2	-	-	-	-	-
P2.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	smif.spihb_data1	-	-	-	-	-

(table continues…)

4 Pinouts

Table 7   **(continued) Multiple alternate functions**[1]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P2.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	smif.spihb_data0	-	-	-	-	-
P2.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	smif.spihb_clk	-	-	-	-	-
P3.0	adcmic.gpio_adc_in[0]	tcpwm[0].line[0]:0	tcpwm[0].line[256]:0	-	cpuss.trace_data[3]:0	scb[2].uart_cts:0	-	scb[1].spi_select0:1	-	-	-	-	-	btss.uart_cts:0	-	keyscan.ks_col[13]	-	-	-	-
P3.1	adcmic.gpio_adc_in[1]	tcpwm[0].line_compl[0]:0	tcpwm[0].line_ompl[256]:0	-	cpuss.trace_data[2]:0	scb[2].uart_rts:0	-	scb[1].spi_clk:1	-	-	lin[0].lin_en[0]:0	-	-	btss.uart_rts:0	-	keyscan.ks_col[14]	-	cpuss.rst_swj_trstn	-	-

(table continues...)

4 Pinouts

Table 7 **(continued) Multiple alternate functions**[1]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P3.2	adcmic.gpio_adc_in[2]	tcpwm[0].line[1]:0	tcpwm[0].line[257]:0	-	cpuss.trace_data[1]:0	scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[1].spi_mosi:1	pdm.pdm_clk[0]:0	peri.tr_io_input[6]:0	lin[0].lin_rx[0]:0	canfd[0].ttcan_rx[0]	adcmic.clk_pdm:0	btss.uart_rxd:0	-	keyscan.ks_col[15]	-	-	-	-
P3.3	adcmic.gpio_adc_in[3]	tcpwm[0].line_compl[1]:0	tcpwm[0].line_ompl[257]:0	-	cpuss.trace_data[0]:0	scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[1].spi_miso:1	pdm.pdm_data[0]:0	peri.tr_io_input[7]:0	lin[0].lin_tx[0]:0	canfd[0].ttcan_tx[0]	adcmic.pdm_data:0	btss.uart_txd:0	-	keyscan.ks_col[16]	-	-	-	-
P3.4	adcmic.gpio_adc_in[4]	tcpwm[0].line[0]:1	tcpwm[0].line[258]:0	-	cpuss.trace_clock:0	-	-	scb[1].spi_select3:1	-	-	-	-	-	-	-	keyscan.ks_col[7]	-	-	-	-
P3.5	adcmic.gpio_adc_in[5]	tcpwm[0].line_compl[0]:1	tcpwm[0].line_ompl[258]:0	-	-	-	-	scb[1].spi_select2:1	-	-	-	-	-	-	-	keyscan.ks_col[8]	-	-	-	-

(table continues...)

4 Pinouts

Table 7 **(continued) Multiple alternate functions**[1]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P3.6	adc mic.gpio_adc_in[6]	tcpwm[0].line[1]:1	tcpwm[0].line[259]:0	-	-	-	-	scb[1].spi_select1:1	-	-	-	-	-	-	-	keyscan.ks_col[9]	-	-	-	-
P3.7	adc mic.gpio_adc_in[7]	tcpwm[0].line_compl[1]:1	tcpwm[0].line_ompl[259]:0	-	-	-	-	-	-	-	-	-	-	-	-	keyscan.ks_col[10]	-	-	-	-
P4.0	-	tcpwm[0].line_compl[1]:2	tcpwm[0].line_ompl[261]:0	-	-	-	-	-	-	-	-	-	-	-	-	keyscan.ks_row[6]	scb[0].i2c_scl:1	-	scb[0].spi_mosi:1	-
P4.1	-	tcpwm[0].line[0]:3	tcpwm[0].line[262]:0	-	-	-	-	-	-	-	-	-	-	-	-	keyscan.ks_row[7]	scb[0].i2c_sda:1	-	scb[0].spi_miso:1	-

(table continues...)

4 Pinouts

Table 7 **(continued) Multiple alternate functions**[1]

Port/Pin	Analog	ACT #0	ACT #1	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #11	ACT #12	ACT #13	ACT #14	ACT #15	DS #2	DS #3	DS #5	DS #6	DS #7
P5.0 / WCO _OUT	-	tcpwm[0].line[0]:2	tcpwm[0].line[260]:0	srss.ext_clk:1	-	scb[2].uart_cts:1	-	scb[1].spi_select0:2	pdm.pdm_clk[0]:1	-	-	canfd[0].ttcan_rx[0]	adcmic.clk_pdm:1	btss.uart_cts:1	-	keyscan.ks_col[17]	-	-	-	-
P5.1 / WCO _IN	-	tcpwm[0].line_compl[0]:2	tcpwm[0].line_ompl[260]:0	-	-	-	-	-	pdm.pdm_data[0]:1	-	-	canfd[0].ttcan_tx[0]	adcmic.pdm_data:1	-	-	keyscan.ks_col[0]	-	-	-	-
P5.2	-	tcpwm[0].line[1]:2	tcpwm[0].line[261]:0	-	-	-	-	-	-	-	-	-	-	-	-	keyscan.ks_col[1]	-	-	-	-

1) The notation for a signal is of the form IPName[x].signal_name[u]:y.

IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.

For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize utilization of on-chip resources.

5   Power supply considerations

Figure 7 shows the typical connections for power pins for all supported packages. In the QFN packages, all internal grounds are routed to the metal pad (EPAD) in the package. This pad must be grounded on the PCB. Figure 7 shows 10 dBm PA configuration. For 0 dBm, connect BT_PAVDD to V_{CCRF}.
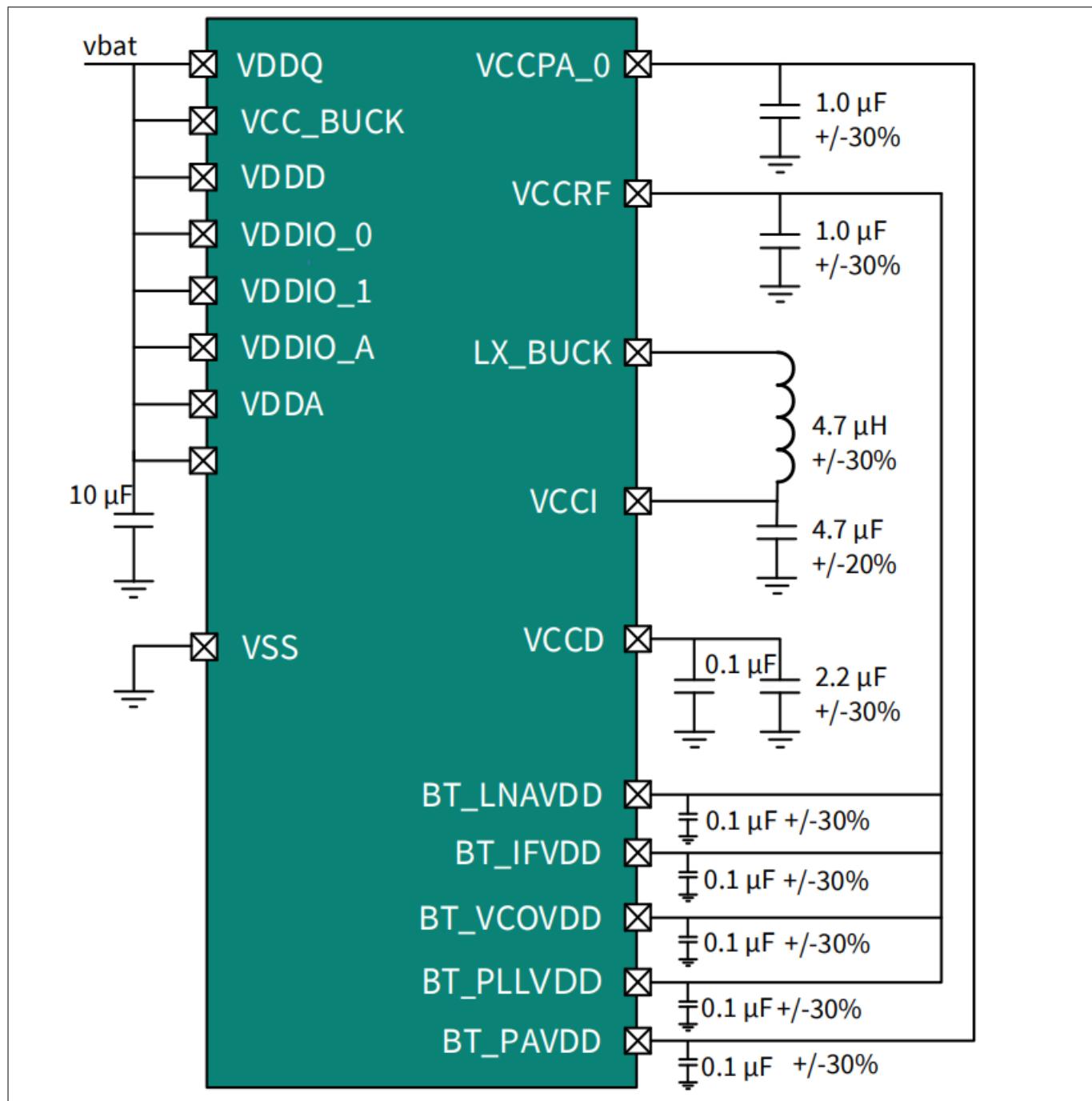
Figure 7   CYW20829 power topology

6 Electrical specifications

All specifications are valid for -40°C < T_A < 85°C and for 1.71 V to 3.6 V except where noted.

6.1 Absolute maximum ratings

Table 8 **Absolute maximum ratings[1]**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	−0.5	-	4	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	−0.5		1.2		Absolute maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	−0.5		V_{DD} + 0.5		
SID4	I_{GPIO_ABS}	Current per GPIO	−25		25	mA	
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	−0.5		0.5		
SID3A	ESD_HBM	Electrostatic discharge human body model	2200		–	V	
SID4A	ESD_CDM	Electrostatic discharge charged device model	500				
SID5A	LU	Pin current for latchup-free operation	−100		100	mA	
SIDWA8	$V_{undershoot}$	Maximum undershoot voltage for I/O			−0.5	V	Duration not to exceed 25% of the SIDWA9 V duty cycle
SIDWA9	$V_{overshoot}$	Maximum overshoot voltage for I/O			V_{DDIO} + 0.5		
SIDWA10	T_j	Maximum junction temperature			125	°C	–

1) Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Operating conditions

Table 9 **Power supply range, CPU current, and transition time specifications[1]**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC specifications							
SID6	V_{DDD}	Internal regulator	1.7	-	3.6	V	-

(table continues...)

6 Electrical specifications

Table 9 (continued) Power supply range, CPU current, and transition time specifications[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID7	V_{DDA}	Analog power supply voltage. Shorted to VDDIOA on PCB					Internally unregulated supply
SID7M	V_{DDM}	Microphone supply voltage					
SID7R	V_{DDRF}	RF LDO input. Connect to output of internal buck	-	1.16	-	-	-
SID7C	V_{DDC}	Digital LDO input. Connect to output of internal buck					
SID7P	V_{DDD}	PA LDO input	2.7	-	3.6	V	For TX10 mode, BT_PAVDD connected to VCCPA. The minimum supply voltage is 2.7 V
SID7B	V_{DDIO_0}	GPIO supply for ports	1.7		3.6		-
SID7E	V_{DDIO_1}	Supply when programming eFuse	2.38	2.5	2.62		eFuse programming voltage
SID7A	V_{DDIO_A}	GPIO supply for analog ports. Short to V_{DDA} on PCB	1.7	-	3.6		-
SID8	V_{CCD} (LP)	Output voltage (for core logic bypass)	-	1.1	-	V	High speed mode
SID9	V_{CCD} (ULP)	Output voltage (for core logic bypass)		1.0			ULP mode. Valid for −20 to 85°C
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	μF	X5R ceramic or better. Value for 0.8 to 1.2 V
SID11	C_{EXC}	Power supply decoupling capacitor	-	10	-		X5R ceramic or better
SID12	V_{CCRF}	Output voltage (for radio)		1.1		V	-
SID13	V_{CCPA}	Output voltage (for PA)		2.5			-
SID14	V_{CCM}	Output voltage (for MIC)		2.5			-
SID523	V_{DDQ}	External supply to PMU analog	1.7	-	3.6		-
SID524	V_{CC_BUCK}	External supply to switching regulator					-
SID525	BT_PAV$_{DD}$	Internal PA supply	1		2.75		-
SID526	BT_RF	RF power supply			1.2		-
SID527	BT_LNAV$_{DD}$	LNA supply					-

(table continues...)

6 Electrical specifications

Table 9 **(continued) Power supply range, CPU current, and transition time specifications**[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID528	BT_IFV$_{DD}$	IFPLL power supply					-
SID529	BT_VCOV$_{DD}$	VCO supply					-
CPU currents and transition times Cortex® M33 Active mode							
Execute with cache enabled							
SIDC2	I$_{DD4}$	Execute from cache; CM33 Active 96 MHz. FLL. Dhrystone	-	4.8	5.8	mA	V$_{DDD}$ = 3.0 V, Buck ON, Max at 60°C
				7.4	8.4		V$_{DDD}$ = 1.8 V, Buck ON, Max at 60°C
SIDC3	I$_{DD5}$	Execute from cache; CM33 Active 48 MHz. IHO. Dhrystone	-	2.4	3.4	mA	V$_{DDD}$ = 3.0 V, Buck ON, Max at 60°C
				3.7	4.1		V$_{DDD}$ = 1.8 V, Buck ON, Max at 60°C
SIDC4	I$_{DD6}$	Execute from cache; CM33 Active 8 MHz. IHO. Dhrystone		0.9	1.5		V$_{DDD}$ = 3.0 V, Buck ON, Max at 60°C
				1.27	1.75		V$_{DDD}$ = 1.8 V, Buck ON, Max at 60°C
SIDS1	IDD11	CM33 Sleep 96 MHz with FLL		1.5	2.2		V$_{DDD}$ = 3.0 V, Buck ON, Max at 60°C
				2.2	2.7		VDDD = 1.8 V, Buck ON, Max at 60°C
SIDS2	I$_{DD12}$	CM33 Sleep 48 MHz with IHO		1.2	1.9		V$_{DDD}$ = 3.0 V, Buck ON, Max at 60°C
				1.7	2.2		V$_{DDD}$ = 1.8 V, Buck ON, Max at 60°C
SIDS3	I$_{DD13}$	CM33 Sleep 8 MHz with IHO		0.7	1.3		V$_{DDD}$ = 3.0 V, Buck ON, Max at 60°C
				0.96	1.5		V$_{DDD}$ = 1.8 V, Buck ON, Max at 60°C
Deep Sleep mode							
SIDDS1_B	I$_{DD33A\_B}$	With internal Buck enabled and 64K SRAM retention	-	5.7		µA	At 25°C (with typical Silicon)
SIDDS2_B	I$_{DD33B\_B}$	With internal Buck enabled and 128K SRAM retention		6.2			At 25°C (with typical Silicon)
SIDDS5_B	I$_{DD33E\_B}$	With internal Buck enabled and 256K SRAM retention		7.5			At 25°C (with typical Silicon)
SIDDS3_B	I$_{DD33C\_B}$	With internal Buck enabled and 64K SRAM retention DS-RAM		4.5			At 25°C (with typical Silicon)

(table continues...)

---

6 Electrical specifications

Table 9 (continued) Power supply range, CPU current, and transition time specifications[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDDS4_B	IDD33D_B	With internal Buck enabled and 128K SRAM retention DS-RAM		5			At 25°C (with typical Silicon)
SIDDS6_B	I_{DD33F_B}	With internal Buck enabled and 256K SRAM retention DS-RAM		6	-		At 25°C (with typical Silicon)
Hibernate mode							
SIDHIB1	I_{DD34}	V_{DDD} = 1.8 V	-	300	-	nA	No clocks running
SIDHIB2	I_{DD34A}	V_{DDD} = 3.0 V	-	500			
SIDHIB3	I_{DD35}	V_{DDD} = 1.8 V	-	800			WCO is running
SIDHIB4	I_{DD35A}	V_{DDD} = 3.0 V	-	1000			
Power mode transition times							
SID13A	T_{DS_ACT}	Deep Sleep to Active transition time. Guaranteed by design	-	45	60	µs	DS to Active with 1.0 V operation, with upper inrush current limit
SID13B	T_{DS_ACTLP}	Deep Sleep to Active LP transition time. Guaranteed by design		20	35		DS to Active LP with 0.9 V operation
SID13C	T_{DSR_ACT}	Deep Sleep-RAM to Active transition time. Guaranteed by design		-	800		DS to Active with 1.0 V operation, with upper inrush current limit
SID13D	T_{DSR_ACTLP}	Deep Sleep-RAM to Active LP transition time. Guaranteed by Design		-	800		DS-RAM to Active LP with 0.9 V operation
SID14	T_{HIB_ACT}	Hibernate to Active transition time		2000	-		Hibernate to Active with 1.0 V operation, with upper inrush current limit
SID14A	T_{HIB_ACTLP}	Hibernate to Active LP transition time		2000			Hibernate to Active with 0.9 V operation, with upper inrush current limit

1) Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

---

6 Electrical specifications

6.2.1 XRES

Table 10 **XRES DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID17	T_{XRES_IDD}	IDD when XRES asserted	-	300	-	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$			800			V_{DDD} = 3.3 V
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DD}	-		V	CMOS input
SID78	V_{IL}	Input voltage low threshold	-		0.3 × V_{DD}		
SID80	C_{IN}	Input capacitance		3		pF	-
SID81	$V_{HYSXRES}$	Input voltage hysteresis		100		mV	
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}		-	100	µA	

Table 11 **XRES AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	-	1000	-	µs	Normal mode, 96 MHz M33, upper inrush current
SID16	T_{XRES_PW}	XRES pulse width	5	-			-

6.2.2 GPIO

Table 12 **GPIO DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	-	-	V	CMOS input
SID57A	I_{IHS}	Input current when Pad > V_{DDIO} for O_{VT} inputs	-		10	µA	Per I²C spec
SID58	V_{IL}	Input voltage LOW threshold			0.3 × V_{DD}	V	CMOS input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}		-		-
SID242	V_{IL}		-		0.3 × V_{DD}		
SID243	V_{IH}	LVTTL input, V_{DD} > 2.7 V	2.0		-		
SID244	V_{IL}		-		0.8		
SID59	V_{OH}	Output voltage high level	V_{DD} – 0.5		-		I_{OH} = 8 mA

(table continues…)

6 Electrical specifications

Table 12 (continued) GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID62A	V_{OL}	Output voltage low level	-		0.4		I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	-
SID64	$R_{PULLDOWN}$	Pull-down resistor					
SID65	I_{IL}	Input leakage current (absolute value)	-	-	2	nA	25°C, V_{DD} = 3.0 V
SID66	C_{IN}	Input capacitance			5	pF	-
SID67	V_{HYSTTL}	Input hysteresis LVTTL V_{DD} > 2.7 V	100	0	-	mV	
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	-			
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	-		100	µA	
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current			200	mA	

Table 13 GPIO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode. 10% to 90% of V_{DD}	-	3.5	-	ns	C_{LOAD} = 15 pF, 8 mA drive strength, V_{DDIO} > 2.7 V
SID70A	T_{RISEF_1}			5.5			C_{LOAD} = 15pF, V_{DDIO} < 2.7 V, maximum slew and drive strength
SID71	T_{FALLF}	Fall time in Fast Strong mode. 10% to 90% of V_{DD}		3.5			C_{LOAD} = 15 pF, 8 mA drive strength, V_{DDIO} > 2.7 V
SID71A	T_{FALLF_1}			5.5			C_{LOAD} = 15pF, V_{DDIO} < 2.7 V, maximal slew and drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong mode. 10% to 90% of V_{DD}	52	-	142		C_{LOAD} = 15 pF, 8 mA drive strength, $V_{DD} \leq$ 2.7 V
SID72A	T_{RISES_2}		48		102		C_{LOAD} = 15 pF, 8 mA drive strength, 2.7 V < $V_{DD} \leq$ 3.6
SID73	T_{FALLS_1}	Fall time in Slow Strong mode. 10% to 90% of V_{DD}	44		211		C_{LOAD} = 15 pF, 8 mA drive strength, $V_{DD} \leq$ 2.7 V

(table continues...)

6 Electrical specifications

Table 13   (continued) GPIO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID74	$F_{GPIOUT1}$	GPIO Fout; Fast Strong mode	-		100	MHz	90/10%, 15 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode			1.5		
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode			100		
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode			1.3		
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq$ V_{DD} $\leq$ 3.6 V			100		90/10% V_{IO}

6.3   Analog peripherals

Table 14   Internal reference specification

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93R	V_{REFBG}	-	1.188	1.2	1.212	V	-

6.3.1   AUD ADC

Table 15   MIC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
MIC specifications							
DM.4	-	Audio/Mic supply - Mic_avdd	1.8	-	3.3	V	-
DM.5		Current consumption	-	1.5	-	mA	25°C, Mic_avdd = 3 V, excludes MIC bias loading current
DM.6		Power down current		0.1		µA	25°C, Mic_avdd = 3 V
DM.21		MIC PGA gain range	0	-	42	dB	-
DM.22		MIC PGA gain step	-	1	-		
DM.23		MIC PGA gain error		±1			
DM.24		PGA input referred noise		-	4	µV	@ 42 dB PGA gain A-weighted

(table continues…)

6 Electrical specifications

Table 15 **(continued) MIC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DM.25		Passband gain flatness			-	dB	PGA + ADC, 100-4 kHz
DM.26		MIC bias output voltage - Micvdd * 0.75 * 1.12		2.52		V	Micvdd = 3
DM.27		MIC bias loading current		-	3	mA	-
DM.28		MIC bias noise				µV	Referred to PGA input, 20-8 kHz, A-weighted
DM.29		MIC bias PSRR			-	dB	1 kHz

Table 16 **ADC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DM.2	-	Analog supply voltage - V_{DDA}	1.7	-	3.6	V	-
DM.5		Active current consumption - V_{DDC}	-	2	-	mA	25°C
DM.5a		Active current consumption - V_{DDA}		0.5			25°C, V_{DDA} = 3 V
DM.6		Power down current - V_{DDA}		0.1		µA	25°C - ADC disabled with device in Active mode
DM.6a		Power down current - V_{DDC}		1			
DM.8		Absolute error - Includes gain error, offset and distortion		-	5	%	-
DM.10		ENOB - Audio application		12	-	Bit	
DM.11		ENOB - Static application		11			
DM.12		ADC input full scale - Audio application		1.6		Vpp	
DM.13		ADC input full scale - Static application	0	-	V_{DDA}		
DM.14		Conversion rate - Audio application	16	48	-	kHz	
DM.15		Conversion rate - Static application	50	100	-		
DM.16		Signal bandwidth - Audio application	20	-	8000	Hz	

(table continues...)

6 Electrical specifications

Table 16   **(continued) ADC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DM.17		Signal bandwidth - Static application	-	DC	-		
DM.18		Startup time - Audio application		10		ms	
DM.19		Startup time - Static application		20		µs	
DM.30		ADC SNR	78	-		dB	0 dB PGA gain, A-weighted
DM.31		ADC THD+N	74				−3 dB FS input, 0 dB PGA gain
DM.33		GPIO source impedance	-		1k	W	10 µs measurement time

6.4 Digital peripherals

Table 17   **Timer/counter/PWM (TCPWM) specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	-	-	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz			180		
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz			270		
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz			540		
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency			100	MHz	Fc max = Fcpu Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width for all trigger events	2/Fc		-	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected

(table continues...)

6 Electrical specifications

Table 17 **(continued) Timer/counter/PWM (TCPWM) specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	1.5/Fc				Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5 A	TC_{RES}	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM.5 B	PWM_{RES}	PWM resolution					Minimum pulse width of PWM output
SID.TCPWM.5 C	Q_{RES}	Quadrature inputs resolution	2/Fc				Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar

Table 18 **Serial communication block (SCB) specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
I^{2}C DC specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	-	-	30	µA	-
SID150	I_{I2C2}	Block current consumption at 400 kHz			80		
SID151	I_{I2C3}	Block current consumption at 1 Mbps			180		
SID152	I_{I2C4}	I^{2}C enabled in Deep Sleep mode			1.7		At 60°C
I^{2}C AC specifications							
SID153	F_{I2C1}	Bit rate	-	-	1	Mbps	-
UART DC specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	-	-	30	µA	-

(table continues...)

6 Electrical specifications

Table 18   (continued) Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID161	I_{UART2}	Block current consumption at 1000 kbps			180		
UART AC specifications							
SID162A	F_{UART1}	Bit rate	-	-	3	Mbps	ULP mode
SID162B	F_{UART2}				8		LP mode
SPI DC specifications							
SID163	I_{SPI1}	Block current consumption at 1 Mbps	-	-	220	µA	-
SID164	I_{SPI2}	Block current consumption at 4 Mbps			340		
SID165	I_{SPI3}	Block current consumption at 8 Mbps			360		
SID165A	I_{SP14}	Block current consumption at 25 Mbps			800		
SPI AC specifications for LP mode (1.1 V) unless noted otherwise							
SID166	F_{SPI}	SPI operating frequency Master and externally clocked Slave	-	-	24	MHz	-
SID166B	F_{SPI_EXT}	SPI operating frequency Master (Fscb is SPI clock)			Fscb/4		Fscb max is 96 MHz in LP mode, 24 MHz in ULP mode
SID166A	F_{SPI_IC}	SPI Slave internally clocked			24		-
SPI Master mode AC specifications for LP mode (1.1 V) unless noted otherwise							
SID167	T_{DMO}	MOSI valid after SClock driving edge	-	12	12	ns	20 ns max. for ULP (0.9 V) mode
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	-	-		Full clock, late MISO sampling
SID169	T_{HMO}	MOSI data hold time	0		5		Referred to Slave capturing edge
SID169C	T_{DHI}	SPI Master: MISO hold time after SCLK capturing edge	0	-	-		-
SID169A	$T_{SSELMSCK1}$	SSEL valid to first SCK valid edge	18	21	21		Referred to Master clock edge
SPI Slave mode AC specifications for LP mode (1.1 V) unless noted otherwise							
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	5	-	-	ns	-
SID170A	SPI_FREQ	For LP mode	48			MHz	

(table continues...)

6 Electrical specifications

Table 18 (continued) Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext. Clk. mode	-		20	ns	35 ns max. for ULP (1.0 V) mode
SID171	T_{DSO}	MISO valid after Sclock driving edge in Internally Clk. Mode			TDSO_EXT + 3*Tscb		Tscb is Serial Communication Block clock period
SID171B	T_{DSO}	MISO valid after Sclock driving edge in Internally Clk. Mode with median filter enabled			TDSO_EXT + 4*Tscb		Tscb is Serial Communication Block clock period
SID172	T_{HSO}	Previous MISO data hold time	5.5		-		-
SID172C	T_{HIS}	SPI MOSI hold from SCLK					

6.5 Audio subsystem

Table 19 Audio subsystem specifications[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PDM specifications							
SID400P	Fmax_clk_sys	Clock frequency for clk_sys	-	96	-	MHz	PVT18 ss, 0.90 V, −40°C, scl40 library, minimum parameters
SID401	Fmax_clk_if_srss	Clock frequency for audio clock reference clk_if_srss		48			PVT18 ss, 0.90 V, −40°C, scl40 library, minimum parameters
SID402	Idyn_act_typ	Typical dynamic current when cell is active. See the DC spec table for related static current spec, if applicable		-	110	µA/MHz	PVT16 tt, 1.1 V, 25°C, scl40 library, typical parameters clk_audio: 49.152 MHz clk_sys: 50 MHz
SID403	Idyn_act_max	Maximum dynamic active current. See the DC spec table for related static current spec, if applicable			132		PVT20 ff, 1.21 V, 150°C, scl40 library, maximum parameters clk_audio: 49.152 MHz clk_sys: 50 MHz

(table continues...)

6 Electrical specifications

Table 19 **(continued) Audio subsystem specifications**[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID403A	Idyn_slp_typ	Typical dynamic current when cell is idle. See the DC spec table for related static current spec, if applicable			80		PVT16 tt, 1.1 V, 25°C, scl40 library, typical parameters, clocks toggling clk_audio: 49.152 MHz clk_sys: 50 MHz
SID403B	T_SETUP	Receiver setup			10	ns	PVT18 ss, 0.90 V, −40°C, scl40 library, minimum parameters
SID403C	PDM_HOLD	Data input hold time to PDM_CLK edge	10		-		PVT18 ss, 0.90 V, −40°C, scl40 library, minimum parameters
SID404A	CPDM	Load	-		-	pF	-
SID404	PDM_OUT	Audio sample rate	8	10	48	ksps	
SID405	PDM_WL	Word length	16	-	24	bits	
SID412	PDM_ST	Startup time	-	48	-		WS (Word Select) cycles

I²S specifications. The same for LP and ULP modes unless stated otherwise.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID413	I2S_WORD	Length of I²S word	8	-			
SID414B	I2S_BCK_F	Bit Clock frequency in LP mode	-				
SID414BU	I2S_BCK_F_U	Bit Clock frequency in ULP mode					
SID414BP	I2S_BCK_P	Bit Clock period		1/ I2S_BCK_F			
SID414BP U	I2S_BCK_P_U	Bit Clock period in ULP mode		1/ I2S_BCK_F_U			
SID414	I2S_WS_FREQ	Word clock frequency in LP mode		-			
SID414M	I2S_WS_FREQ_U	Word clock frequency in ULP mode					
SID435L	I2S_BCK_TL	Bit clock low period in LP Mode	0.35*I2S_BCK_P				

(table continues...)

6 Electrical specifications

Table 19   (continued) Audio subsystem specifications[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID415IL	I2S_MCKI_TL	Master clock IN low period in LP (or) ULP mode	0.45*tM CLK				
SID415IH	I2S_MCKI_TH	Master clock IN high period in LP (or) ULP Mode					
SID415OL	I2S_MCKO_TL	Master clock Out low period in LP (or) ULP mode	0.35*tM CLK	0.45*tMCLK to 0.4*tMC LK			
SID415OH	I2S_MCKO_TH	Master clock Out high period in LP (or) ULP mode		0.45*tMCLK to 0.4*tMC LK			
SID416	TDM_OUTPUT_L OAD_MAX	Capacitive load	10	-			
I²S Slave mode							
SID430	I2S_S_TS_WS	WS Setup time before the first edge following the driving edge of Bit Clock for LP Mode	0.2 * I2S_BC K_P	-		ns	-
SID430U	I2S_S_TS_WS _U	WS Setup time before the first edge following the driving edge of bit clock for ULP mode	0.2 * I2S_BC K_P_U				
SID430A	I2S_S_TH_WS	WS Hold time after the first edge following the driving edge of bit clock, LP or ULP mode	0				
SID432	I2S_S_SDO	SDO Propagation delay from driving edge of bit clock for LP mode	0.3 * I2S_BC K_P		0.2 * I2S_B CK_P		
SID432U	I2S_S_SDO_U	SDO Propagation delay from driving edge of bit clock for ULP mode	0.3 * I2S_BC K_P_U		0.2 * I2S_B CK_P _U		
I²S Master mode							
SID437	I2S_M_WS	WS propagation delay from driving edge of bit clock for LP mode	0	-	0.2 * I2S_B CK_P	ns	-

(table continues...)

6 Electrical specifications

Table 19   **(continued) Audio subsystem specifications[1]**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID437_U	I2S_M_WS_U	WS propagation delay from driving edge of bit clock for ULP mode			0.2 * I2S_B CK_P _U		
SID438	I2S_M_SDO	SDO Propagation delay from driving edge of bit clock for LP mode			0.2 * I2S_B CK_P		
SID438U	I2S_M_SDO_ U	SDO Propagation delay from driving edge of bit clock for ULP mode			0.2 * I2S_B CK_P _U		Associated clock edge depends on selected polarity

1)   TMCLK_SOC is the internal I2S master clock period.

6.6   System resources

6.6.1   Power-on reset

Table 20   **Power-on reset (POR) with brownout detect (BOD) DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Precise POR (PPOR)							
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes. V_{DDD}	1.54	-	-	V	BOD Reset guaranteed for V_{DDD} levels below 1.54 V
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep. V_{DDD}	1.54				-
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	-		100	mV/μs	Active mode

Table 21   **POR with BOD AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in system Deep Sleep mode	-	-	10	mV/μs	BOD operation guaranteed

6.6.2   Voltage monitors

Table 22   **Voltage monitors DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID195	V_{HVDI1}	-	1.38	1.43	1.47	V	-

(table continues…)

6 Electrical specifications

Table 22 **(continued) Voltage monitors DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID196	V_{HVDI2}		1.57	1.63	1.68		
SID197	V_{HVDI3}		1.76	1.83	1.89		
SID198	V_{HVDI4}		1.95	2.03	2.10		
SID199	V_{HVDI5}		2.05	2.13	2.2		
SID200	V_{HVDI6}		2.15	2.23	2.3		
SID201	V_{HVDI7}		2.24	2.33	2.41		
SID202	V_{HVDI8}		2.34	2.43	2.51		
SID203	V_{HVDI9}		2.44	2.53	2.61		
SID204	V_{HVDI10}		2.53	2.63	2.72		
SID205	V_{HVDI11}		2.63	2.73	2.82		
SID206	V_{HVDI12}		2.73	2.83	2.92		
SID207	V_{HVDI13}		2.82	2.93	3.03		
SID208	V_{HVDI14}		2.92	3.03	3.13		
SID209	V_{HVDI15}		3.02	3.13	3.23		
SID211	LVI_IDD	Block current	-	5	15	µA	

Table 23 **Voltage monitors AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	-	-	170	nS	-

6.6.3 SWD and trace interface

Table 24 **SWD and trace specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID214	F_SWDCLK2	1.7V ≤ V_{DDD} ≤ 3.6V	-	-	25	MHz	LP mode; V_{CCD} = 1.1 V
SID214L	F_SWDCLK2L				12		ULP mode; V_{CCD} = 1.0 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T		-	ns	For both LP and ULP modes
SID216	T_SWDI_HOLD						
SID217	T_SWDO_VALID		-		0.5 * T		-
SID217A	T_SWDO_HOLD		1		-		

(table continues...)

6 Electrical specifications

Table 24 **(continued) SWD and trace specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID214T	F_TRCLK_LP1	With trace data setup/hold times of 2/1 ns respectively	-		48	MHz	LP mode, V_{DD} = 1.1 V
SID215T	F_TRCLK_LP2	With trace data setup/hold times of 3/2 ns respectively			48		
SID216T	F_TRCLK_ULP				24		ULP mode, V_{DD} = 1.0 V

6.6.4 Internal main oscillator

Table 25 **IMO DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	-	9	15	µA	-

Table 26 **IMO AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	FIMOTOL1	Frequency variation centered on 8 MHz	-	-	±2	%	-
SID227	T_{JITR}	Cycle-to-cycle and period jitter	-		-	µs	

6.6.5 Internal low-speed oscillator

Table 27 **ILO DC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	-	9	15	µA	-

Table 28 **ILO AC specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO startup time	-	-	7	µs	Startup time to 80% of final frequency
			-	-	35	µs	Startup time to 95% of final frequency
SID236	$T_{LIODUTY}$	ILO duty cycle					-
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency					± 10% variations

6 Electrical specifications

6.6.6 FLL

Table 29   Frequency locked loop (FLL) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID450	FLL_RANGE	Input frequency range	0.040	-	96.00	MHz	Upper limit is for External input
SID451	FLL_OUT_DIV 2	Output frequency range. V_{CCD} = 1.1 V	24.00				Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV 2	Output frequency range. V_{CCD} = 0.9 V			48.00		
SID452	FLL_DUTY_DI V2	Divided-by-2 output; High or Low	47.00		53.00	%	-
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on deep sleep wakeup	-		11.00	µs	With IMO input, less than 10°C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz.
SID455	FLL_JITTER	Period jitter (1 sigma at 100 MHz)			18.00	ps	-
SID456	FLL_CURREN T	CCO + logic current			5.50	µA/MH z	

6.6.7 Crystal oscillator

Table 30   ECO specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
MHz ECO DC specifications							
SID316	I_{DD_MHZ}	Block operating current with Cload up to 18 pF	-	1200	-	µA	Type 24 MHz
MHz ECO AC specifications							
SID317	F_MHz	Crystal frequency range	-	24	-	MHz	-
kHz ECO DC specifications							
SID318	IDD_kHz	Block operating current with 32-kHz crystal	-	0.38	1	µA	-
SID321E	ESR32K	Equivalent series resistance		80	-	kΩ	
SID322E	PD32K	Drive level		-	0.5	µW	
kHz ECO AC specifications							
SID319	F_kHz	32-kHz trimmed frequency	-	32.8	-	kHz	-
SID320	Ton_kHz	Startup time		-	1000	ms	
SID320E	F_{TOL32K}	Frequency tolerance		50	250	ppm	

6.6.8 Clock source switching time

Table 31 **Clock source switching time specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID262	TCLK$_{SWITCH}$	Clock switching from one CLK_HF to another CLK_HF in clock periods[1]	-	-	4 clk1 + 3 clk2	periods	-

1) As an example, if the clk_path[1] source is changed from the IMO to the FLL (see Figure 3) then clk1 is the IMO and clk2 is the FLL.

6.6.9 QSPI

Table 32 **QSPI specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SMIF QSPI specifications. All specs with 15-pF load							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	-	-	48	MHz	LP mode (1.1 V)
SID390QU	Fsmifclocku	SMIF QSPI output clock frequency			24		ULP mode (1.0 V)
SID397Q	Idd_qspi	Block current in LP mode (1.0 V)			1900	µA	LP mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (0.9 V)			590		ULP mode (1.0 V)
SID399A	SDR_TCSH0	CS# active hold to CK	4		-	ns	-
SID399B	SDR_TOUT_SETUP_LF	Output setup time of DQ[3:0] to CK high	5.1				
SID399C	SDR_TOUT_HOLD_LF	Output hold time of DQ[3:0] to CK high					
SID399D	SDR_TIN_V	CK low to DQ[3:0] input valid time	-		6.7		
SID399E	SDR_TIN_HO	CK low to DQ[3:0] input hold time	1		-		

6.6.10 Smart I/O

Table 33 **Smart I/O specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID420	SMIO_BYP	Smart I/O Bypass delay	-	-	2	ns	-
SID421	SMIO_LUT	Smart I/O LUT prop delay					

6 Electrical specifications

6.6.11 JTAG boundary scan

Table 34 **JTAG boundary scan**

Spec ID#		Parameter	Min	Typ	Max	Unit	Desctiption
JTAG boundary scan parameters							
SID460	TCKLOW	TCK LOW minimum	34	-	-	ns	-
SID461	TCKHIGH	TCK HIGH	10				
SID462	TCK_TDO	TDO clock-to-out (max) from falling TCK	-		22		
SID463	TSU_TCK	TDI, TMS Setup time before rising TCK	12		-		
SID464	TCk_THD	TDI, TMS Hold time after rising TCK	10				
SID465	TCK_TDOV	TCK to TDO data valid (High-Z to active)	22				
SID466	TCK_TDOZ	TCK to TDO data valid (Active to High-Z)					
JTAG boundary scan parameters for 1.1 V (LP) mode operation							
SID468	TCKLOW	TCK low	52	-		ns	-
SID469	TCKHIGH	TCK high	10				
SID469A	TCKPERIOD	CLK_JTAG_PERIOD, 30 pF load	-	62			
SID470	TCK_TDO	TCK falling edge to output valid		-	40		
SID471	TSU_TCK	Input valid to TCK rising edge	12				
SID472	TCk_THD	Input hold time to TCK rising edge	10				
SID473	TCK_TDOV	TCK falling edge to output valid (High-Z to active)	40				
JTAG boundary scan p for 1.0 V (ULP) mode operation							
SID468A	TCKLOW	TCK low	102	-	-	ns	-
SID469A	TCKHIGH	TCK high	20				
SID470A	TCK_TDO	TCK falling edge to output valid	-		80		
SID471A	TSU_TCK	Input valid to TCK rising edge	22		-		
SID472A	TCk_THD	Input hold time to TCK rising edge	20	-	-	ns	-

(table continues...)

6 Electrical specifications

Table 34 **(continued) JTAG boundary scan**

Spec ID#	Parameter		Min	Typ	Max	Unit	Desctiption
SID473A	TCK_TDOV	TCK falling edge to output valid (High-Z to active)	80				
SID474A	TCK_TDOZ	TCK fallingedgetooutput valid (Active to high-Z)					

6.7 Bluetooth® LE

Table 35 **Bluetooth® LE subsystem specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
RF receiver specifications (1 Mbps)							
SID317R[1]	RXS, IDLE	RX sensitivity with ideal transmitter	-	-98	-	dBm	Across RF operating frequency range
SID318R[2]				-96.5			
SID319R	PRXMAX	Maximum received signal strength at < 30.8% PER		-5			RF-PHY specification (RCV-LE/CA/06/C)
SID320R	CI1	Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX		9	21	dB	RF-PHY specification (RCV-LE/CA/03/C)
SID321R	CI2	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 1 MHz		-3	15		
SID322R	CI3	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz		-45	-17		
SID323R	CI4	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 3 MHz		-49	-27		
SID324R	CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at image frequency (FIMAGE)		-31	-9		

(table continues...)

6 Electrical specifications

Table 35   (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID325R	CI6	Adjacent channel interference Wanted Signal at −67dBm and Interferer at image frequency (FIMAGE ± 1 MHz)		-35	-15		
RF receiver specifications (2 Mbps)							
SID326[1]	RXS, IDLE	RX sensitivity with ideal transmitter	-	-95	-	dBm	Across RF operating frequency range
SID327[2]				-93.5			
SID328R	PRXMAX	Maximum received signal strength at < 30.8% PER		-5			RF-PHY specification (RCV-LE/CA/06/C)
SID329R	CI1	Co-channel interference, Wanted Signal at −67 dBm and Interferer at FRX		7	21	dB	RF-PHY specification (RCV-LE/CA/03/C)
SID330	CI2	Adjacent channel interference Wanted Signal at −67 dBm and Interferer at FRX ± 2 MHz		-2	15		
SID331	CI3	Adjacent channel interference Wanted Signal at −67 dBm and Interferer at FRX ± 4 MHz		-42	-15		
SID332	CI4	Adjacent channel interference Wanted Signal at −67 dBm and Interferer at ≥ FRX ± 6 MHz		-42	-27		
SID333	CI5	Adjacent channel interference Wanted Signal at −67 dBm and Interferer at Image frequency (FIMAGE)		-29	-9		
SID334	CI6	Adjacent channel interference Wanted Signal at −67 dBm and Interferer at Image frequency (FIMAGE ± 2 MHz)		-40	-15		
RF receiver specification S2 (500 kbps)							

(table continues...)

6 Electrical specifications

Table 35 **(continued) Bluetooth® LE subsystem specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID501	RXS, IDLE	RX sensitivity with Ideal Transmitter, Standard Mod Index Rx	.	-101	-	dBm	Across RF operating frequency range
SID506	CI1	Co-channel interference, Wanted Signal at –72 dBm and Interferer at FRX	-	3	17	dB	RF-PHY specification (RCV-LE/CA/28/C)
SID507	CI2	Adjacent channel interference Wanted Signal at –72 dBm and Interferer at FRX ± 1 MHz		-11	11		
SID508	CI3	Adjacent channel interference Wanted Signal at –72 dBm and Interferer at FRX ± 2 MHz		-50	-21		
SID509	CI4	Adjacent channel interference Wanted Signal at –72 dBm and Interferer at FRX ± 3 MHz		-53	-31		
SID510	CI5	Adjacent channel interference Wanted Signal at –72 dBm and Interferer at image frequency (FIMAGE)		-37	-13		
SID511	CI6	Adjacent channel interference Wanted Signal at –72 dBm and Interferer at image frequency (FIMAGE ± 1 MHz)		-42	-19		
RF Receiver specification S8 (125 kbps)							
SID512	RXS, IDLE	RX sensitivity with Ideal Transmitter [2]	-	-106	-	dBm	Across RF operating frequency range
SID517	CI1	Co-channel interference, Wanted Signal at –79 dBm and Interferer at FRX		6	12	dB	RF-PHY specification (RCV-LE/CA/29/C)
SID518	CI2	Adjacent channel interference Wanted Signal at –79 dBm and Interferer at FRX ± 1 MHz		-18	6	-	

(table continues...)

6 Electrical specifications

Table 35   (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID519	CI3	Adjacent channel interference Wanted Signal at −79 dBm and Interferer at FRX ± 2 MHz		-52	-26		
SID520	CI4	Adjacent channel interference Wanted Signal at −79 dBm and Interferer at FRX ± 3 MHz		-51	36		
SID521	CI5	Adjacent channel interference Wanted Signal at −79 dBm and Interferer at Image frequency (FIMAGE)		-40	-18		
SID522	CI6	Adjacent channel interference Wanted Signal at −79 dBm and Interferer at Image frequency (FIMAGE ± 1 MHz)		-47	-24		
RF Receiver specification (1 and 2 Mbps)							
SID338	OBB1	Out of Band Blocking Wanted Signal at −67 dBm and Interferer at F = 30 −2000 MHz	-30	TBD	-	dBm	RF-PHY specification (RCV-LE/CA/04/C)
SID339	OBB2	Out of Band Blocking Wanted Signal at −67 dBm and Interferer at F = 2003 - 2399 MHz	-35	TBD	-	dBm	RF-PHY specification (RCV-LE/CA/04/C)
SID340	OBB3	Out of Band Blocking, Wanted Signal at −67 dBm and Interferer at F = 2484 - 2997 MHz					
SID341	OBB4	Out of Band Blocking Wanted Signal at -67 dBm and Interferer at F = 3000 - 12750 MHz	-30				RF-PHY specification (RCV-LE/CA/04/C)
SID342	IMD	Intermodulation Performance Wanted Signal at −64 dBm and 1 Mbps Bluetooth® LE, 3rd, 4th and 5th offset channel	-50	-			RF-PHY specification (RCV-LE/CA/05/C)

(table continues...)

6 Electrical specifications

Table 35 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID343	RXSE1	Receiver Spurious emission 30 MHz to 1.0 GHz	-		-57		100 kHz measurement bandwidth ETSI EN300 328 V2.1.1
SID344	RXSE2	Receiver Spurious emission 1.0 GHz to 12.75 GHz			-53		1 MHz measurement bandwidth ETSI EN300 328 V2.1.1
RF Transmitter specifications							
SID345	TXP, ACC	RF power accuracy	-2	-	2	dB	-
SID346	TX0	Power range	-	23	-		–24 dBm to 0 dBm
	TX10			33			–24 dBm to 10 dBm
SID347	TXP, 0 dBm	Output power, 0 dB power setting		0		dBm	For TX10 mode, BT_PAVDD connected to VCCPA. The minimum supply voltage VDDPA is 2.7 V
SID348	SID348	Output power, 10 dBm power setting		10			
SID349	TXP, MIN	Output power, minimum power setting		-20			
SID350	F2Max	Average frequency deviation for 10101010 pattern	185	-		kHz	RF-PHY specification (TRM-LE/CA/05/C)
SID350R	F2Max_2M	Average frequency deviation for 10101010 pattern for 2 Mbps	370				
SID350LR	F1Max_S8	Average frequency deviation for 10101010 pattern for 125 bps	185				RF-PHY specification (TRM-LE/CA/13/C)
SID351	F1AVG	Average frequency deviation for 11110000 pattern	225	250	275		RF-PHY specification (TRM-LE/CA/05/C)
SID351R	F1AVG_2M	Average frequency deviation for 11110000 pattern for 2 Mbps	450	500	550		RF-PHY specification (TRM-LE/CA/05/C)
SID351R	F1AVG_S8	Average frequency deviation for 11110000 pattern for 125 kbps	225	250	275		RF-PHY specification (TRM-LE/CA/13/C)
SID352	EO	Eye opening = ΔF2AVG/ΔF1AVG	0.8	-	-	-	RF-PHY specification (TRM-LE/CA/05/C)

(table continues...)

6 Electrical specifications

Table 35 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID353	FTX,ACC	Frequency accuracy	-150		150	kHz	RF-PHY specification (TRM-LE/CA/06/C)
SID354	FTX,MAXDR	Maximum frequency drift	-50		50		RF-PHY specification (TRM-LE/CA/06/C)
SID355	FTX, INITDR	Initial frequency drift	-20		20		RF-PHY specification (TRM-LE/CA/06/C)
SID355LR	FTX, INITDR, S8		-19.2		19.2		RF-PHY specification (TRM-LE/CA/14/C)
SID356	FTX, DR	Maximum drift rate	-20		20	kHz/ 50 µs	RF-PHY specification (TRM-LE/CA/06/C)
	FTX, DR, S8		-19.2		19.2		RF-PHY specification (TRM-LE/CA/14/C)
SID357	IBSE1	In Band Spurious Emission at 2 MHz offset (1 Mbps) In Band Spurious Emission at 4 MHz offset (2 Mbps)	-		-20	dBm	RF-PHY specification (TRM-LE/CA/03/C)
SID358	IBSE2	In Band Spurious Emission at > 3 MHz offset (1 Mbps) In Band Spurious Emission at > 6 MHz offset (2 Mbps)			-30		
SID359	TXSE1	Transmitter Spurious Emissions (Averaging), < 1.0 GHz	-	-	-55.5		FCC-15.247
SID360	TXSE2	Transmitter Spurious Emissions (Averaging), > 1.0 GHz			-41.5		

RF Current specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID361	IRX1_wb	Receive current (LE 1 Mbps)	-	5.6	-	mA	Measured with VCC_BUCK = 3.0 V. In all cases, VCCI = 1.16 V and VCCRF = 1.1 V. For
SID362	ITX1_0dBm	TX current at 0 dBm setting (LE 1 Mbps)		5.2			

(table continues...)

6 Electrical specifications

Table 35   **(continued) Bluetooth® LE subsystem specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID365R	ITX1_10dBm	TX current at 10 dBm setting (LE 1 Mbps)		17.2			TX0, BT_PAVDD = VCCRF. For TX10, BT_PAVDD = VCCPA = 2.5 V
General RF specifications							
SID373	FREQ	RF operating frequency	2400	-	2482	MHz	-
SID374	CHBW	Channel spacing	-	2	-		
SID375	DR1	On-air data rate (1 Mbps)		1000		kbps	
SID376	DR2	On-air data rate (2 Mbps)		2000			
RSSI specifications							
SID379	RSSI, ACC	RSSI accuracy	-4	-	4	dB	−95 dBm to −20 dBm measurement range
SID381	RSSI, PER	RSSI sample period	-	6	-	µs	–
System-level Bluetooth® LE specifications							
SID433R	Adv_Pwr	Advertising power, 1.28 s advertising interval, 31 bytes, TX 0 dBm	-	44.5	-	µW	Connectible advertising, VBAT = 3.0 V
SID434R	Conn_Pwr_300	Connection power, 300 ms connection interval, 0 bytes, TX 0 dBm		64.6			VBAT = 3.0 V
SID435R	Conn_Pwr_1S	Connection power, 1000 ms connection interval, 0 bytes, TX 0 dBm		29.5			

1)   Coherent demodulator enabled with stable modulation index.
2)   Coherent demodulator enabled with standard modulation index.

7   Ordering information

Table 36 lists the CYW20829 part numbers and features.

Table 36   Ordering part numbers

Product	Package	Ambient operating temperature
CYW20829B0LKML[1]	6 × 6 × 0.9 mm 56-lead	−40°C to 85°C

1)   T and R device with "T"

8 Packaging

This product line is offered in 56-lead package.

Table 37 **Package dimensions**

Spec ID#	Package	Description	Package drawing number
PKG_2	56-lead	56-lead, 6 × 6 × 0.9 mm height with 0.35-mm pitch	002-31757

Table 38 **Package characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
TA	Operating ambient	-	−40	25	85	°C
TJ	Operating junction			-	100	
TJA	Package θ JA (56-lead)		-	13.8	-	°C/watt
TJC	Package θ JC (56-lead)			4.8		

Table 39 **Solder reflow peak temperature**

Package	Maximum peak temperature	Maximum time at peak temperature
56-lead	260°C	30 s

Table 40 **Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2**

Package	MSL
56-lead	MSL-3

8 Packaging

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e	0.35 BSC		
N	56		
ND	14		
L	0.30	0.40	0.50
b	0.11	0.16	0.21
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
D	6.00 BSC		
E	6.00 BSC		
A	-	-	0.90
A1	0.00	-	0.05
A3	0.203 REF		
R	0.20 TYP		
K	0.30 MIN		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-31757 Rev. **

Figure 8   56-lead QFN 6.0 x 6.0 x 0.9 mm LT56F 4.60 x 4.60 mm E-Pad (SAWN), Package outline (PG-VQFN-56)

9 Acronyms

Table 41 **Acronyms used in this document**

Acronym	Description
3DES	triple DES (data encryption standard)
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BOD	brown-out detect
BTSS	Bluetooth® sub system
CAD	computer aided design
CBC	cipher block chaining
CFB	cipher feedback
CCO	current controlled oscillator
CM0+	Cortex®-M0+, an Arm® CPU
CM4	Cortex®-M4, an Arm® CPU
CMOS	complementary metal-oxide-semiconductor, a process technology for IC fabrication
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSD	CAPSENSE™ sigma-delta
CTR	Counter
DAC	digital-to-analog converter, see also IDAC, VDAC
DAP	debug access port
DES	data encryption standard
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DSI	digital system interconnect
ECB	electronic code book
ECC	elliptic curve cryptography
ECDSA	elliptic curve digital signature algorithm
ECO	external crystal oscillator
EMI	electromagnetic interference
ESD	electrostatic discharge

(table continues...)

9 Acronyms

Table 41 (continued) Acronyms used in this document

Acronym	Description
FIFO	first-in, first-out
FLL	frequency locked loop
FS	full-speed
GND	Ground
GPIO	general-purpose input/output
HMAC	hash-based message authentication code
HSIOM	high-speed I/O matrix
I/O	input/output, see also GPIO, DIO, SIO, USBIO
I^{2}C, or IIC	Inter-Integrated Circuit, a communications protocol
I^{2}S	inter-IC sound
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
IoT	internet of things
IPC	inter-processor communication
IRQ	interrupt request
JTAG	Joint Test Action Group
LIN	Local Interconnect Network, a communications protocol
LP	low power
LS	low-speed
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MCWDT	multi-counter watchdog timer
MISO	master-in slave-out
MMIO	memory-mapped input output
MOSI	master-out slave-in
MPU	memory protection unit

(table continues...)

9 Acronyms

Table 41   (continued) Acronyms used in this document

Acronym	Description
MSL	moisture sensitivity level
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
OFB	output feedback
OTP	one-time programmable
OVT	overvoltage tolerant
PCB	printed circuit board
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
PLL	phase-locked loop
POR	power-on reset
PRNG	pseudo random number generator
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QD	quadrature decoder
QSPI	quad serial peripheral interface
RAM	random-access memory
RISC	reduced-instruction-set computing
ROM	read-only memory
RTC	real-time clock
RX	receive
SAR	successive approximation register
SARMUX	SAR ADC multiplexer bus
SCB	serial communication block
SHA	secure hash algorithm
SMIF	serial media interface
SNR	signal-to-noise ration
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SROM	supervisory read-only memory
SWD	serial wire debug, a test protocol
SWJ	serial wire JTAG

(table continues…)

9 Acronyms

Table 41	(continued) Acronyms used in this document
Acronym	**Description**
SWO	single wire output
SWV	serial-wire viewer
TCPWM	timer, counter, pulse-width modulator
TDM	time division multiplexed
TRNG	true random number generator
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
ULP	ultra-low power
WCO	watch crystal oscillator
WDT	watchdog timer
WIC	wakeup interrupt controller
XIP	execute-in-place
XRES	external reset input pin

10 Document conventions

10.1 Units of measure

Table 42   **Units of measure**

Symbol	Unit of measure
°C	degrees celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSb	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	picofarad
ppm	parts per million

(table continues…)

10   Document conventions

Table 42   (continued) Units of measure

Symbol	Unit of measure
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document version	Date of release	Description of changes
*H	2024-04-09	Updated the doc status to Final.
		Updated Bluetooth® Low Energy subsystem and added a footnote.
		Updated the part number: CYW20829B0LKMLTXUMA1/ CYW20829B0LKMLXQLA1 to "CYW20829B0LKML" in the Table 36.
		Added IFX code Packaging information in Figure 8.
*I	2024-04-19	Updated template; no content update.

Trademarks

The Bluetooth® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc., and any use of such marks by Infineon is under license.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.